Quadrature Switched/Floated Capacitor Power Amplifier With Reconfigurable Self-Coupling Canceling Transformer for Deep Back-Off Efficiency Enhancement

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***Abstract*— This article presents a quadrature switched/floated capacitor power amplifier (SFCPA) with deep back-off efficiency enhancement. The SFCPA is introduced to decrease the dynamic power consumption at power back-off (PBO), which could improve the system efficiency (SE). The reconfigurable self-coupling canceling transformer (RSCCT) with enhanced tuning range of turn ratio is used to achieve impedance boosting for further improved efficiency at deep PBO. Based on the proposed SFCPA, a watt-level quadrature digital power amplifier (DPA) with IQ cell sharing, hybrid Doherty, and impedance boosting is proposed for deep PBO efficiency enhancement. Implemented in 40-nm CMOS, the proposed DPA with 1.2-/2.4-V supply achieves 30.3-dBm saturated output power (P_{out}) with 36.6%/32.9%/29.1%/23.7%/18.6%/13.2% SE for 0-/3-/6-/9-/12-/15-dB PBOs at 2.4 GHz. For 60-MHz 256-QAM modulation signal, it delivers 23.32-dBm average output power (P_{avg}) with an error vector magnitude (EVM) of −31.9 dB and an average drain efficiency (DE) of 30.7%. For 40-MHz 1024-QAM signal, it shows 20.44-dBm P_{avg} with an EVM of −35.9 dB and an average DE of 22.6%.**

***Index Terms*— CMOS, Doherty, IQ cell sharing, power amplifier, reconfigurable self-coupling canceling transformer (RSCCT), switched/floated capacitor power amplifier (SFCPA).**

I. Introduction

THE modern wireless communication systems in portable devices require transmitters (TXs) with watt-level output power (P_{out}) for higher signal-to-noise ratio. Meanwhile, to save battery life, lower power consumption is required. CMOS digital power amplifiers (DPAs) exhibit merits of high peak efficiency and low cost. However, the modulation signal with large peak-to-average-power ratios (PAPRs) in wireless communication leads to efficiency degradation of conventional DPAs. Thus, high efficiency, especially at power back-off (PBO) for enhanced average efficiency, is demanded in PAs.

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To increase the efficiency of PA at PBOs, various techniques are developed, such as envelop tracking (ET) [1], [2], outphasing [3]–[7], Doherty [8]–[13], load modulation [14], [15], and Class-G [16], [17]. To further improve the PA efficiency at deep PBO, the multi-way combined Doherty PA with switched transformer [18], Class-G Doherty [19]–[21], subharmonic switching (SHS) [22]–[24], and hybrid Doherty with impedance boosting [25] are developed. The multi-way combined PA with switched transformer introduces various efficiency peaks due to the load modulation [18], which suffers from relatively large circuit size and limited passive efficiency. Class-G Doherty PAs [19]–[21] show competitive efficiency at deep PBOs. However, supply switching is needed, which would lead to linearity degradation due to mode switching [19]. To mitigate the degradation from supply switching, the Class-G voltage-mode Doherty is proposed with extra hardware overhead [20], [21]. The SHS PAs [22]–[24] can enhance the PA efficiency at deep PBO by using subharmonic component of carrier frequency, which sacrifices the circuit size due to multiple power combined ways. The technique of hybrid Doherty and impedance boosting [25] increases the PA efficiency at deep PBO with less power-combining ways and dc power supplies. However, the degraded passive efficiency limits the PA efficiency at deep PBO.

The polar TXs [26], [27] are proposed with high peak efficiency. However, the polar TXs require a complex coordinate rotation digital computer (CORDIC) and phase modulator (PM). Besides, the phase control and amplitude control should be synchronized, which could affect bit error rate and error vector magnitude (EVM) performance. Compared to polar TXs, quadrature TXs [28]–[35] show advantages of simpler architecture and higher data rate. Meanwhile, the technique of I/Q cell sharing can increase the peak efficiency of quadrature TX [31]. Recently, the quadrature PAs with PBO efficiency enhancement are reported with competitive performances [25], [30]–[35]. However, it is still challenging to increase the efficiency at deep PBOs for quadrature PAs.

In this article, a watt-level quadrature switched/floated capacitor power amplifier (SFCPA) with reconfigurable self-coupling canceling transformer (RSCCT) for deep PBO efficiency enhancement is presented [36]. Compared with

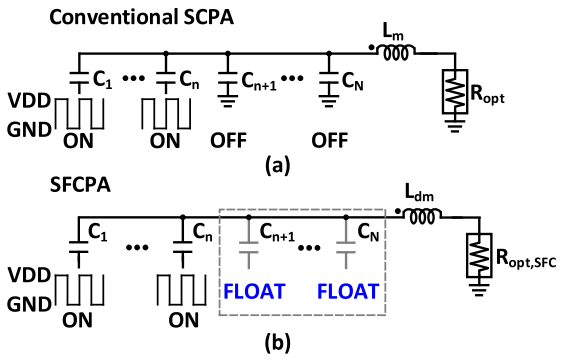


Fig. 1. (a) Conventional SCPA. (b) Proposed SFCPA.

conventional switched capacitor power amplifier (SCPA), the proposed SFCPA decreases the undesired dynamic power consumption required to charge and discharge the capacitor array at PBOs, which leads to the enhanced PA efficiency. The RSCCT is introduced with enhanced tuning range of turn ratio, which achieves the impedance boosting to further improve the PA efficiency. The proposed quadrature SFCPA achieves six efficiency peaks at 0-/3-/6-/9-/12-/15-dB PBOs without supply switching. This article is organized as follows. Section II discusses the principles of SFCPA and operation of efficiency enhancement based on SFCPA. Section III introduces the architecture of the proposed watt-level quadrature SFCPA, where the theory and implementation of the proposed RSCCT are investigated. Section IV shows the measurement results and comparisons with state of the arts. Finally, the conclusion is given in Section V.

II. Principle and Operation

A. Switched/Floated Capacitor Power Amplifier

The conventional SCPA with good AM–AM linearity is shown in Fig. 1(a). The total number of unit capacitor is N. The capacitance of C_i $(i = 1, \ldots, N)$ is C. The n unit capacitors are switched by square waveform. The other unit cells are switched OFF and connected to the ground. The dynamic power P_{SC} required to charge and discharge the capacitor array leads to efficiency degradation at PBO [37].

To solve this problem, the SFCPA is proposed in this article. The schematic of the SFCPA is shown in Fig. 1(b). The capacitance of C_i $(i = 1, \ldots, N)$ is C. Similar to SCPA, the bottom plates of switched-ON capacitors are switched between VDD and GND. However, the bottom plates of unused capacitors are floated and not connected to GND. Then, the dynamic power consumption P_{SFC}, which is needed to charge and discharge the capacitor array, is decreased. Therefore, the PBO efficiency of SFCPA could be enhanced compared to conventional SCPA.

The schematic and equivalent circuit of SFCPA are shown in Fig. 2. The source resistance of each unit cell (i.e., ON-resistance of switch) is set to be R_s. The total equivalent source resistance is R_s/n, where n is the number of switched-ON unit cells. The inductor L_{dm} is used to achieve the output impedance matching. Then, the output power of the proposed SFCPA can be calculated by the following equation:

$$P_{out,SFC} = \frac{2VDD^2}{\pi^2} \times \frac{R_{opt,SFC}}{(R_{opt,SFC} + R_s/n)^2} \tag{1}$$

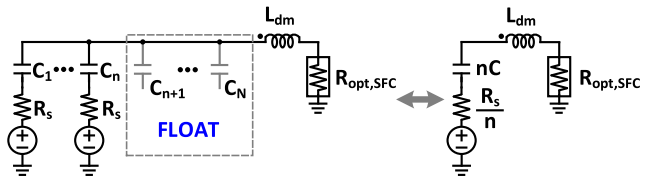


Fig. 2. Schematic and its equivalent circuit of SFCPA.

where $L_{dm} = 1/(4\pi^2 f^2 \times nC)$ is used for non-reflective output matching and f is the operation frequency. The dynamic power consumption P_{SFC} required to charge and discharge capacitor array can be expressed as

$$P_{SFC} = C_{in} \times VDD^2 \times f \tag{2}$$

where C_{in} is the input capacitance driven through the selected switches [37]. Once the unused unit capacitor is floated, C_{in} could be regarded as 0, which makes $P_{SFC} = 0$. The power dissipation on the source resistor is

$$P_{Rs,SFC} = \frac{2VDD^2}{\pi^2} \times \frac{R_s/n}{(R_{opt,SFC} + R_s/n)^2}. \tag{3}$$

Then, the drain efficiency (DE) of the proposed SFCPA can be calculated as

$$DE_{SFC} = \frac{P_{out,SFC}}{P_{out,SFC} + P_{SFC} + P_{Rs,SFC}} = \frac{\frac{R_{opt,SFC}}{R_s/n}}{\frac{R_{opt,SFC}}{R_s/n} + 1} (n = 1, \ldots, N). \tag{4}$$

When the following relationship is defined:

$$t = \frac{R_{opt,SFC}}{R_s/n}. \tag{5}$$

Equation (4) can be further expressed as

$$DE_{SFC} = \frac{t}{t+1}. \tag{6}$$

It can be seen that the DE of SFCPA is only related to the coefficient t. To obtain the maximal DE in the whole PBO range, the coefficient t should maintain constant. Also, t should be much larger than 1 for higher DE of SFCPA.

The typical DE of conventional SCPA and proposed SFCPA is calculated and compared in Fig. 3. The detailed derivation to obtain the DE of SCPA is shown in the Appendix. t is 5 for both SFCPA and SCPA in the calculation. As shown in Fig. 3, the proposed SFCPA shows the same peak DE with SCPA at 0-dB PBO. The proposed SFCPA maintains maximal DE in the whole PBO range. In contrast, the DE of SCPA is significantly decreased at PBO due to the dynamic power P_{SC}. Moreover, the DE of SCPA is limited by finite Q_{loaded} of on-chip matching network. Typically, Q_{loaded} is limited to 2–3 for fully integrated CMOS implementation [37].

However, in practical implementation, the floated unit cell of SFCPA introduces the parasitic capacitor, which would lead to efficiency degradation. The diagram of SFCPA considering the parasitic capacitor of floated unit cell is shown in Fig. 4. The capacitance of unit capacitor is C. The parasitic capacitance of

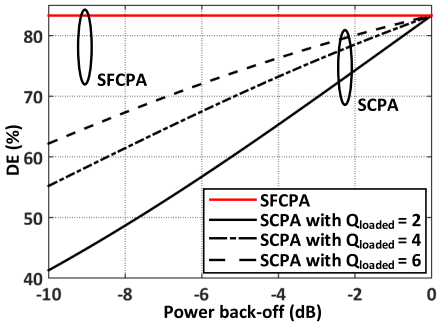


Fig. 3. Calculated typical DE of the proposed SFCPA and conventional SCPA with various loaded quality factors ($t = 5$).

each floated unit cell is C_{par}. The ratio of C_{par} to C is assumed to be r. Then, the following equation can be obtained:

$$r = \frac{C_{\text{par}}}{C}. \tag{7}$$

The number of switched-ON unit capacitor is n ($n = 1, \ldots, N$). Also, $N - n$ unit capacitors are floated, which introduces the total parasitic capacitance of $(N-n)C_{\text{par}}$. Then, the output power can be calculated as

$$P'_{\text{out,SFC}} = \frac{2n^2\text{VDD}^2}{\pi^2[n + (N-n)r]^2} \times \frac{R_{\text{opt,SFC}}}{(R_{\text{opt,SFC}} + R_s/n)^2}. \tag{8}$$

The dynamic power P_{SFC} needed to charge and discharge the capacitor array is computed as

$$P'_{\text{SFC}} = \frac{n(N-n)r}{[n + (N-n)r]^2} \times \frac{2\text{VDD}^2}{\pi R_{\text{opt,SFC}} Q_{\text{loaded}}}. \tag{9}$$

The power dissipation on the source resistor is

$$P'_{R_s,\text{SFC}} = \frac{2n^2\text{VDD}^2}{\pi^2[n + (N-n)r]^2} \times \frac{R_s/n}{(R_{\text{opt,SFC}} + R_s/n)^2}. \tag{10}$$

Then, the DE of the SFCPA considering parasitic capacitor can be expressed as

$$\begin{aligned}\text{DE}'_{\text{SFC}} &= \frac{4nR'^2_{\text{opt,SFC}}}{4nR'^2_{\text{opt,SFC}} + A + 4nR'_{\text{opt,SFC}}R_s/n} \\ &= \frac{4n\left(\frac{R'_{\text{opt,SFC}}}{R_s/n}\right)^2}{4n\left(\frac{R'_{\text{opt,SFC}}}{R_s/n}\right)^2 + B + 4n\frac{R'_{\text{opt,SFC}}}{R_s/n}} \\ &= \frac{4nt^2}{4nt^2 + \frac{\pi r(N-n)(t+1)^2}{Q_{\text{loaded}}} + 4nt}\end{aligned} \tag{11}$$

where

$$A = \frac{\pi r(N-n)\left(R'_{\text{opt,SFC}} + R_s/n\right)^2}{Q_{\text{loaded}}} \tag{12}$$

$$B = \frac{\pi r(N-n)\left(\frac{R'_{\text{opt,SFC}}}{R_s/n} + 1\right)^2}{Q_{\text{loaded}}} \tag{13}$$

$$t = \frac{R'_{\text{opt,SFC}}}{R_s/n}. \tag{14}$$

Q_{loaded} is the loaded quality factor of the network. The typical DE of SFCPA considering C_{par} is calculated with $Q_{\text{loaded}} = 6$ and $t = 5$, as shown in Fig. 5. Various values of r are concluded. In practical circuits, r is usually less than 0.4. It is notable that the parasitic capacitor C_{par} of floated unit cell leads to the efficiency degradation of SFCPA at PBO. Therefore, C_{par} should be limited in circuit design for higher PBO efficiency. Besides, the typical DE of SCPA with $Q_{\text{loaded}} = 6$ and $t = 5$ is calculated and shown in Fig. 5, which is still lower than the DE of SFCPA with $r = 0.4$.

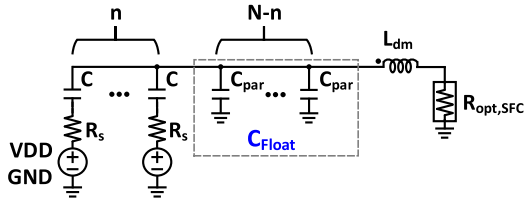


Fig. 4. Schematic of SFCPA considering the parasitic capacitor C_{par} of floated unit cell.

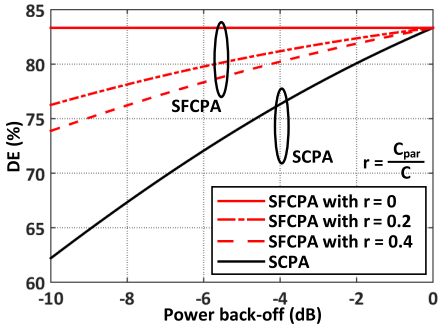


Fig. 5. Calculated DE of SCPA and SFCPA at PBO ($Q_{\text{loaded}} = 6$ and $t = 5$).

B. Deep PBO Efficiency Enhancement Based on SFCPA

Based on the SFCPA, the proposed quadrature DPA with hybrid Doherty and impedance boosting is proposed for efficiency enhancement at deep PBO. The corresponding operation is shown in Fig. 6. Two operation modes (modes I and II) and eight typical states (A, B, C, D, E, F, G, and H) are adopted. Two conditions (i.e., states A, B, C, and D with I input code $=$ Q input code and states E, F, G, and H with I input code or Q input code $= 0$) are discussed. The capacitance of each unit capacitor is C. Also, the total number of unit cells is N for main and auxiliary PAs. The RSCCT is used to convert different load impedances of PA to output load. The corresponding trajectories of load impedances for main and auxiliary PAs are compared in Fig. 7. The DE at PBO is shown in Fig. 8. The condition of $I = Q$ means that the combined I/Q vectors show the same magnitude, which delivers output voltage at the phases of 45°, 135°, 225°, and 315° in the complex domain. The condition of I or $Q = 0$ means that the I or Q vector is disabled, which delivers output voltage only at the phases of 0°, 90°, 180°, and 270° in the complex domain. Then, the proposed SFCPA could introduce six efficiency peaks at 0-/3-/6-/9-/12-/15-dB PBOs.

The detailed operation is clearly explained as follows. From 0- to 6-dB PBO range with $I = Q$, the proposed SFCPA operates in mode I. No unit cell is floated in mode I. At state A, the load impedances for main and auxiliary PAs are R_{opt}. All unit cells of main and auxiliary PAs are switched ON to deliver the maximal P_{out}. The equivalent total source

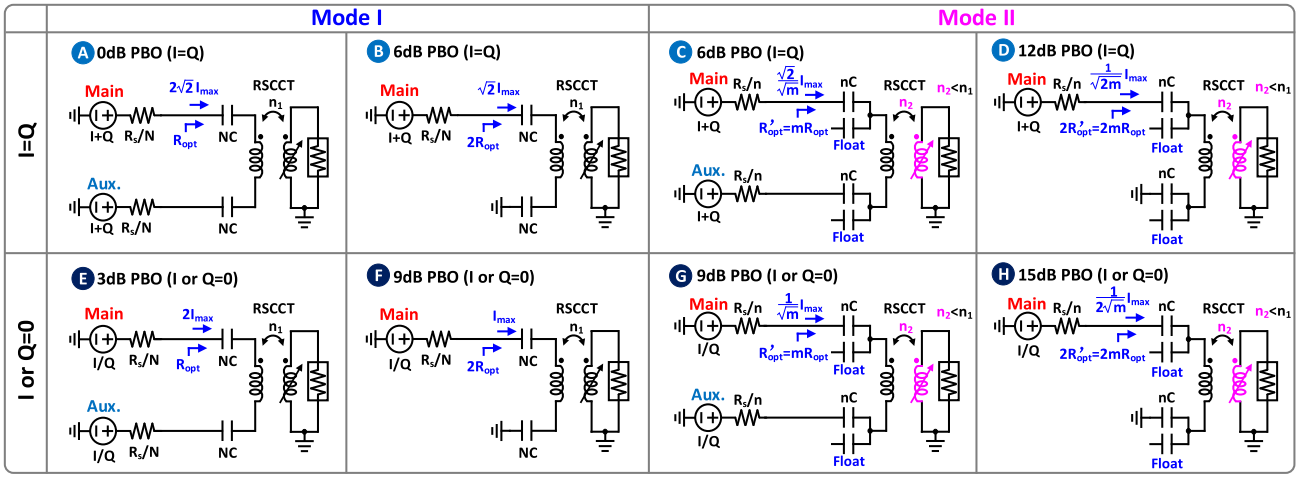


Fig. 6. Operation of the proposed SFCPA with hybrid Doherty and impedance boosting.

impedance is R_s/N. From state A to B, the auxiliary PA is turned off gradually. The switched-OFF unit cells are connected to GND. It leads to good AM–AM distortion due to the similar operation with SCPA. Thus, the output voltage is nearly linear with amplitude control code. The load impedance $Z_{\rm LM}$ of main PA is increased to $2R_{\rm opt}$ due to the Doherty operation at state B, which introduces the efficiency enhancement at 6-dB PBO. Meanwhile, the load impedance $Z_{\rm LA}$ of auxiliary PA is decreased to 0. From 6-dB to lower PBO level, the proposed SFCPA operates in mode II. The number of switched-ON unit cells is n, which is not changed during mode II. At state C, both main and auxiliary PAs are partially ON. The n unit cells are floated. Also, the equivalent total source impedance is R_s/n. An $N-n$ number of unused capacitors are floated to decrease $P_{\rm SFC}$ with enhanced efficiency at 6-dB PBO. Meanwhile, the passive load impedances of main and auxiliary PAs are reconfigured to be $R'_{\rm opt}$ by the RSCCT. The ratio of $R'_{\rm opt}$ to $R_{\rm opt}$ is defined as

$$m = \frac{R'_{\rm opt}}{R_{\rm opt}}. \tag{15}$$

Then, $R'_{\rm opt}$ is equal to $mR_{\rm opt}$. The output current for main and auxiliary PAs are $(2/m)^{1/2}I_{\max}$ at state C. With increased load impedance of $R'_{\rm opt} = mR_{\rm opt}$, the impedance turn ratio n_2 of the matching network in mode II is decreased compared to the turn ratio n_1 in mode I. In addition, as discussed in Section II-A, the coefficient t is required to be unchanged for states A and C. At state A, t can be calculated as

$$t = \frac{R_{\rm opt}}{R_s/N}. \tag{16}$$

At state C, t can be computed as

$$t = \frac{R'_{\rm opt}}{R_s/n} = \frac{mR_{\rm opt}}{R_s/n}. \tag{17}$$

Then, the following relationship can be derived based on (16) and (17).

$$m = \frac{N}{n}. \tag{18}$$

To avoid the amplitude discontinuity at mode switching, the output power of states B and C

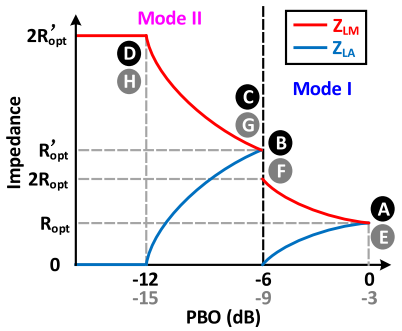


Fig. 7. Trajectories of load impedances for main and auxillary PAs.

should be the same. Then, the following equations can be obtained:

$$P_{{\rm out},B} = \frac{4{\rm VDD}^2 R_{\rm opt}}{\pi^2(2R_{\rm opt}+R_s/N)^2} = \frac{4{\rm VDD}^2 t}{\pi^2(2t+1)^2}R_s/N. \tag{19}$$

$$P_{{\rm out},C} = \frac{4{\rm VDD}^2 R'_{\rm opt}}{\pi^2(R'_{\rm opt}+R_s/n)^2} = \frac{4{\rm VDD}^2 t}{\pi^2(t+1)^2}R_s/n. \tag{20}$$

Then, the ratio m can be determined by the following equation based on (18)–(20) when $P_{{\rm out},B} = P_{{\rm out},C}$:

$$m = \frac{N}{n} = \left(\frac{2t+1}{t+1}\right)^2. \tag{21}$$

When t is much larger than 1, m is close to 4. Then, at state C, a quarter of main and auxillary PA unit cells are switched ON with load impedance of $4R_{\rm opt}$. Also, other unit cells are floated. From state C to D, the number of floated capacitors in main and auxiliary PAs remains unchanged. Meanwhile, the switching unit cells in auxiliary PA are switched OFF gradually, which leads to limited AM–AM distortion due to the similar operation with SCPA. At state D, the proposed SFCPA introduces the efficiency peak at 12-dB PBO. The load impedance of main PA is $2R'_{\rm opt}$ due to the Doherty operation. Note that no unit cell is floated in mode I. Meanwhile, the number of floated unit cells is n in mode II, which is not changed. The operations of states E and H (I or $Q=0$) are similar to states A–D ($I=Q$). The detailed information of eight states (i.e., A, B, C, D, E, F, G, and H) is summarized in Table I.

TABLE I
DETAILED OPERATION STATES OF THE PROPOSED SFCPA

Mode	State	PBO (dB)	Main PA					Aux. PA				
			Output Current	Load Impedance	Number of unit cell			Output Current	Load Impedance	Number of unit cell		
					ON	OFF	FLOAT			ON	OFF	FLOAT
I	A	0	$2\sqrt{2}I_{max}$	R_{opt}	N	0	0	$2\sqrt{2}I_{max}$	R_{opt}	N	0	0
I	B	-6	$\sqrt{2}I_{max}$	$2R_{opt}$	N	0	0	0	0	0	N	0
II	C	-6	$\sqrt{2/m}I_{max}$	mR_{opt}	n	0	N-n	$\sqrt{2/m}I_{max}$	mR_{opt}	n	0	N-n
II	D	-12	$I_{max}/\sqrt{2m}$	2mR_{opt}	n	0	N-n	0	0	0	n	N-n
I	E	-3	$2I_{max}$	R_{opt}	N	0	0	$2I_{max}$	R_{opt}	N	0	0
I	F	-9	I_{max}	$2R_{opt}$	N	0	0	F2	0	0	N	0
II	G	-9	$I_{max}/\sqrt{m}$	mR_{opt}	n	0	N-n	$I_{max}/\sqrt{m}$	mR_{opt}	n	0	N-n
II	H	-15	$I_{max}/(2\sqrt{m})$	2mR_{opt}	n	0	N-n	0	0	0	n	N-n

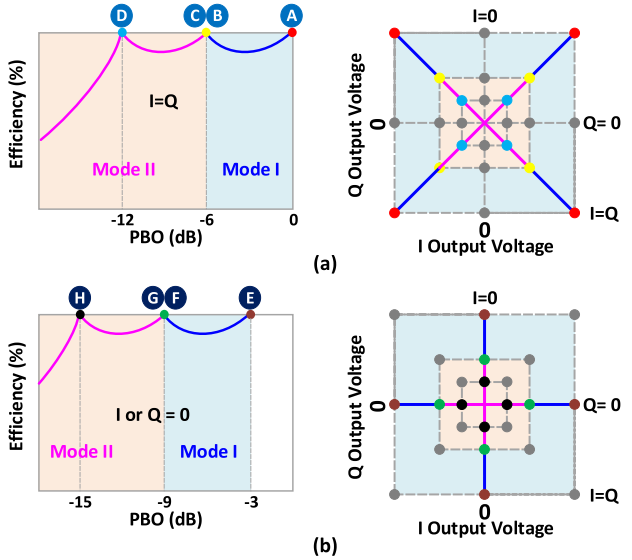


Fig. 8. DE of the proposed SFCPA. (a) I input code = Q input code. (b) I input code or Q input code = 0.

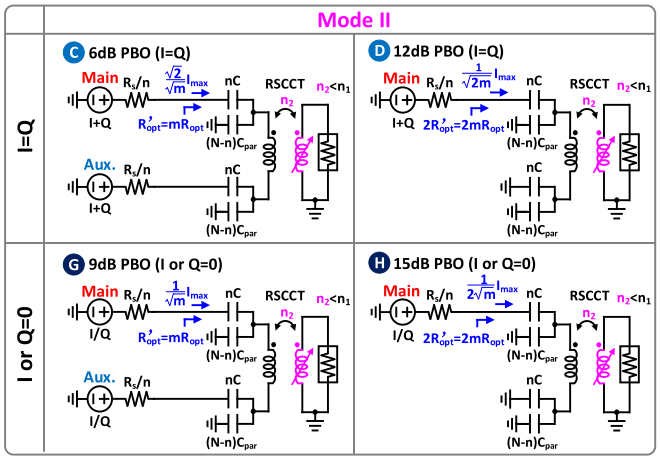


Fig. 9. Operation of the proposed SFCPA in mode II considering the parasitic capacitor of floated unit cell.

However, in practical operation, the effect of parasitic capacitor C_{par} of floated unit cell on PBO efficiency should be considered. The parasitic capacitance of each floated unit cell is assumed to be $C_{\text{par}} = rC$. Note that (16) and (17) are still required when C_{par} is included. In operation mode I, no unit cell is floated. Thus, the corresponding operation is similar to the aforementioned operation of mode I ignoring C_{par}. The detailed operation for mode II considering C_{par} of floated unit cell is shown in Fig. 9. The number of switched-ON unit cell is n for main and auxillary PAs. Meanwhile, the $N - n$ floated unit cells introduce the total parasitic capacitance of $(N - n)C_{\text{par}}$. To avoid the amplitude discontinuity at mode switch, the output power of states B and C should be the same. Based on (16), (17), and (22), the output power of states B and C can be calculated by

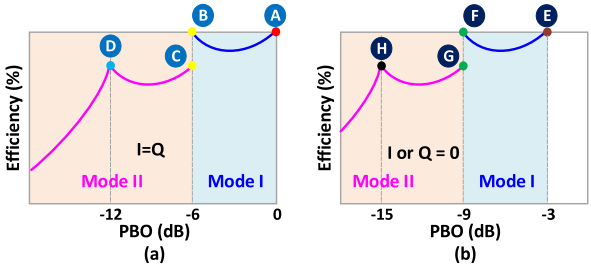


Fig. 10. DE of the proposed SFCPA at PBO considering parasitic capacitor of floated unit cell. (a) I input code = Q input code. (b) I input code or Q input code = 0.

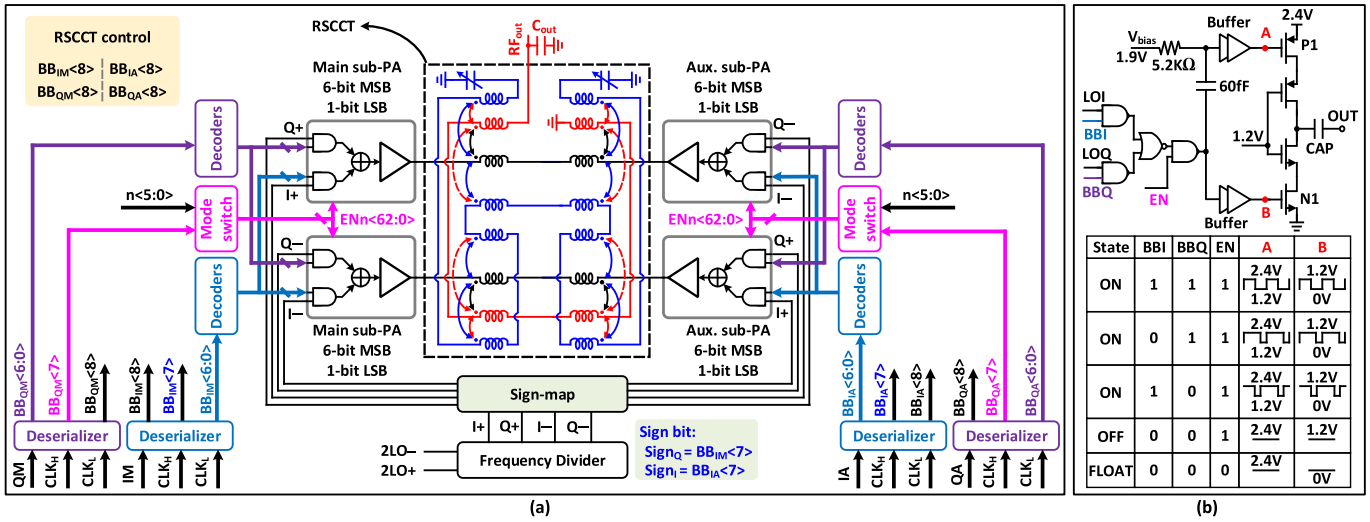
$$P'_{\text{out},B} = \frac{4\text{VDD}^2 R_{\text{opt}}}{\pi^2(2R_{\text{opt}} + R_s/N)^2} = \frac{4\text{VDD}^2 t}{\pi^2(2t+1)^2} R_s/N \quad (22)$$

$$\begin{aligned} P'_{\text{out},C} &= \frac{n^2}{[n+(N-n)r]^2} \times \frac{4\text{VDD}^2}{\pi^2 R'_{\text{opt}}} \\ &= \frac{n^2}{[n+(N-n)r]^2} \times \frac{4\text{VDD}^2}{\pi^2 m R_{\text{opt}}} \\ &= \frac{n^2}{[n+(N-n)r]^2} \times \frac{4\text{VDD}^2 t}{\pi^2(t+1)^2} R_s/n. \end{aligned} \quad (23)$$

The number of switched-ON unit cell at state C (or state G) can be determined when $P'_{\text{out},B} = P'_{\text{out},C}$ is required. Then, the following relationship can be derived:

$$m[1+(m-1)r]^2 = \left(\frac{2t+1}{t+1}\right)^2. \quad (24)$$

Therefore, when $r = C_{\text{par}}/C$ and $t = N \times R'_{\text{opt}}/R_s$ are known, the variable m can be determined. Meanwhile, the number of switched-ON unit cells at state C (or state G) is $n = N/m$. The DE of SFCPA considering C_{par} is shown in Fig. 10. The parasitic capacitor caused by floated unit cell leads to the efficiency degradation in mode II. Moreover, in practical implementation, PBO efficiency at states B, D, F, and H would be degraded by nonideal elements, such as switch loss and passive loss [18], which are not discussed in this article.



State	BBI	BBQ	EN	A	B
ON	1	1	1	2.4V 1.2V	1.2V 0V
ON	0	1	1	2.4V 1.2V	1.2V 0V
ON	1	0	1	2.4V 1.2V	1.2V 0V
OFF	0	0	1	2.4V	1.2V
FLOAT	0	0	0	2.4V	0V

Fig. 11. (a) Block diagram of the proposed SFCPA. (b) Schematic and detailed operation of SFCPA unit cell.

III. Circuit Implementation

A. Architecture

The block diagram of the proposed quadrature IQ cell shared SFCPA with hybrid Doherty, impedance boosting, and RSCCT is shown in Fig. 11(a). The SFCPA is introduced to decrease the dynamic power consumption, which benefits for PBO efficiency enhancement. Meanwhile, the hybrid Doherty and impedance boosting is used to further improve the PA efficiency at PBO. The technique of hybrid Doherty and impedance boosting utilizes the reconfigurable matching network with controllable impedance turn ratio to boost the load impedance of PA at PBO, which leads to efficiency enhancement. Besides, the IQ cell sharing technique is also employed to improve the efficiency of quadrature PA.

The main and auxiliary PAs are composed of four identical differential IQ cell shared sub-PA arrays. Each sub-PA consists of 6-bit MSB controlled by thermometer codes and 1-bit LSB unit cells controlled by binary codes. The switched/floated capacitor structure is utilized to implement the unit cell of sub-PA array. The unit cells can be switched among three operation states (i.e., ON, OFF, and FLOAT). The output matching is composed of the 4-to-1 RSCCT with switched capacitor C_t and output capacitor C_{out}. The turn ratio of RSCCT can be controlled to achieve impedance boosting, which further improves the PA efficiency at PBO.

The quadrature LOs with 25% duty cycle are generated by a quadrature frequency divider. The quadrant of output signal is selected by the sign-map circuit controlled by sign bits (i.e., Sign_Q and Sign_I). Four 1:9 deserializers are used to convert the serial BB signals (i.e., QM, IM, IA, and QA) to parallel 9-bit BB signals (i.e., BB_{QM}, BB_{IM}, BB_{IA}, and BB_{QA}). Among the parallel 9-bit BB signals, 7-bit BB signals are converted to 6-bit thermometer codes and 1-bit binary codes by decoders, which controls the MSB and LSB unit cells of each sub-PA, respectively. The mode switch circuit is mainly composed of decoder and other logic control circuits. $\text{BB}_{\text{QM}}\langle 7\rangle$ and $\text{BB}_{\text{QA}}\langle 7\rangle$ are used as the enable signals of mode switch circuit of main and auxillary PAs, respectively. Note that $\text{BB}_{\text{QM}}\langle 7\rangle = \text{BB}_{\text{QA}}\langle 7\rangle$ in this work. $n\langle 5{:}0\rangle$ is the 6-bit binary code, which represents the number of floated unit cells. The ENn is enable signal of mode switch in each unit cell. When the enable signals (i.e., $\text{BB}_{\text{QM}}\ \langle 7\rangle$ and $\text{BB}_{\text{QA}}\langle 7\rangle$) are active, the mode switch circuit converts the binary code $n\langle 5{:}0\rangle$ into thermometer code $\text{ENn}\langle 62{:}0\rangle$, which controls the 6-bit MSB unit cells. Note that $n\langle 5:0\rangle$ can be finely adjusted to compensate for the PVT effect. Other BB signals are used to control the quadrant (i.e., Sign_Q and Sign_I) and RSCCT.

B. Switched/Floated Capacitor Unit Cell

The schematic of the unit cell based on SFCPA is shown in Fig. 11(b). The cascode inverter structure with 2VDD supply (i.e., 2.4 V) is used in the SFCPA unit cell to deliver higher output power. The dimensions of NMOS and PMOS are 54 μm/40 nm and 108 μm/40 nm, respectively. The ac-coupled capacitor is 60 fF. The voltage of V_{bias} is 1.9 V. Also, its resistor is 5.2 kΩ. LOI and LOQ are quadrature LOs with 25% duty cycle. BBI and BBQ are BB control signals for in-phase and quad-phase, respectively. EN is the enable signal of "FLOAT" state. CAP is 300 fF for 6-bit MSB. The CAP is 150 fF for 1-bit LSB. The detailed operation of the SFCPA unit cell is shown in Fig. 12. In ON state, the EN is 1. The capacitor CAP is switched between 2VDD and GND by the square waveform with 50% duty cycle when BBI = BBQ = 1. When BBI or BBQ = 1, the capacitor CAP is switched between 2VDD and GND by the square waveform with 75% duty cycle. In the OFF state, BBI and BBQ are 0 and EN is 1. At present, NMOS N1 is switched ON and PMOS P1 is switched OFF, which makes the CAP connected to GND. In the "FLOAT" state, BBI, BBQ, and EN are 0. CAP is floated with both NMOS N1 and PMOS P1 switched OFF.

However, in practical implementation, the parasitic capacitors of transistors, which leads to efficiency degradation, should be considered. The schematic of SFCPA unit cell considering parasitic capacitor of in "FLOAT" state is shown in Fig. 12. When the unit cell is floated, the parasitic capacitors of transistors and CAP can be regarded as the single capacitor C_{par}. The equivalent parasitic capacitance of C_{par} is about 95 fF for MSB unit cell seen by the output port. The source

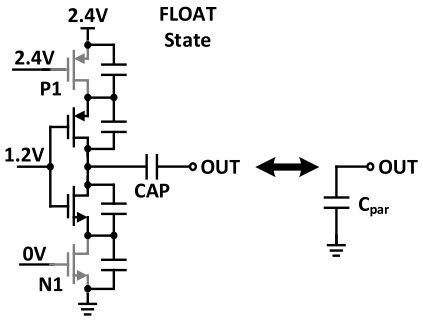


Fig. 12. Parasitic capacitors of floated SFCPA unit cell.

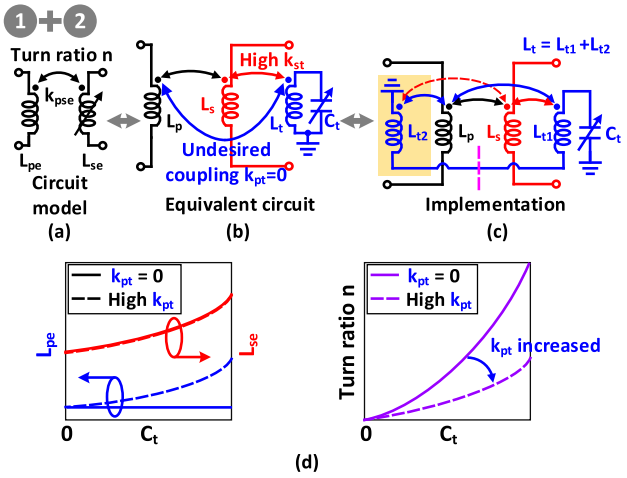


Fig. 13. (a) Circuit model, (b) equivalent circuit, and (c) implementation of the RSCCT. (d) Effect of coupling coefficient k_{pt} on equivalent inductances and turn ratio n.

resistance R_s/N ($N = 63$ for 6-bit MSB) is about 0.317 Ω. The load impedance R_{opt} at 0 dB PBO is designed to be 2.46 Ω for watt-level output power. Thus, the coefficient t is about 6.275 according to (16). The variable m is about 2 according to (24), which means that the load impedances of main and auxillary PAs are $2R_{opt}$ at state C or G. Then, the number n is calculated to be about $0.5N$. Nearly, half of the unit cells are set to be switched ON. Also, nearly, half of the unit cells are floated at state C (or state G), which delivers the same output power with state B (or state F).

C. Reconfigurable Output Matching Network

To achieve the operation of the proposed SFCPA with hybrid Doherty and impedance boosting, the output matching network based on RSCCT is introduced. The RSCCT is proposed with enhanced tuning range of turn ratio, which could convert different load impedance to output 50 Ω.

1) Reconfigurable Self-Coupling Canceling Transformer: The circuit model of RSCCT is shown in Fig. 13(a). To increase the turn ratio n of transformer, the equivalent secondary inductance L_{se} is finely increased, while the equivalent primary inductance L_{pe} needs to be unchanged. The equivalent circuit of RSCCT is shown in Fig. 13(b). The extra inductor L_t and tunable capacitor C_t are introduced in the transformer. The equivalent secondary inductance L_{se} is determined by C_t and L_t EM coupled to L_s with coupling coefficient k_{st} [25]. Meanwhile, the equivalent primary inductance L_{pe} is also affected by L_t and C_t due to the unwanted coupling between L_t and L_p with coupling factor k_{pt}. The effect of undesired coupling k_{pt} on turn ratio n is shown in Fig. 13(d). L_{se} can be adjusted in a large range, which implies a controllable turn ratio n. However, the undesired coupling k_{pt} leads to increased L_{pe} with increasing C_t, which limits the tuning range of turn ratio n. The tuning range of n would be further limited with increased k_{pt}.

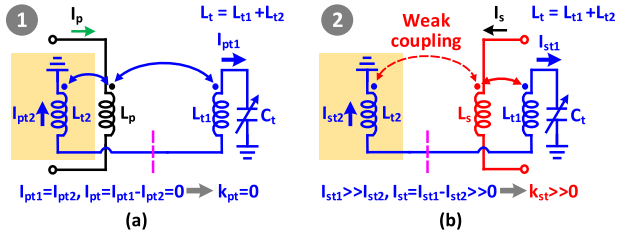


Fig. 14. Operation of the proposed RSCCT. (a) Case 1. (b) Case 2.

To solve this problem, the self-coupling canceling transformer is introduced. The detailed circuit implementation is shown in Fig. 13(c). The inductor L_t is composed of two inductors L_{t1} and L_{t2} with opposite induced current. To clearly explain the complex coupling relationships of the RSCCT, two cases are discussed individually, as shown in Fig. 14(a) and (b), respectively. The induced current of L_{t1} and L_{t2} is I_{pt1} and I_{pt2}, respectively. In case 1, the secondary inductor L_s is not shown. L_p is coupled identically with both L_{t1} and L_{t2}, which induces equivalent current I_{pt1} and I_{pt2} with equal magnitude and opposite sign. Due to the intrinsically canceling of I_{pt1} and I_{pt2}, the total current I_{pt} of L_t is zero, which means that unwanted coupling (i.e., k_{pt}) between L_p and L_t is canceled. Meanwhile, in case 2, the primary inductor L_p is not shown. L_s shows strong coupling with L_{t1} and weak coupling with L_{t2}. Then, the induced current I_{st2} can be ignored compared with I_{st1}. Thus, a relatively large total current I_{st} of L_t is obtained, which implies a high coupling factor of k_{st} between L_s and L_t.

The simplified configuration of the proposed RSCCT is shown in Fig. 15(a). The corresponding lumped model circuit of the RSCCT is shown in Fig. 16. The top thick metal layers are used to implement the transformer for higher quality factor Q. For better understanding, L_p and L_s are expressed in black and red, respectively. L_{t1} and L_{t2} are represented in blue. The tunable capacitor C_t is connected with L_{t1}. The typical inductances of L_p, L_s, L_{t1}, and L_{t2} are 184, 176, 205, and 70 pH, respectively. The coupling coefficient of k_{ps} between L_p and L_s is 0.83. The configurations for cases 1 and 2 are shown in Fig. 15(b) and (c), respectively. In case 1, the configuration of L_s is not shown. The inductor L_p is located between L_{t1} and L_{t2}. L_p is coupled to L_{t1} and L_{t2} with similar coupling factor, which generates currents I_{pt1} and I_{pt2} with similar magnitude and opposite sign. The total current I_{pt} of L_t is decreased due to intrinsically canceling of I_{pt1} and I_{pt2}. Then, the unwanted coupling k_{pt} is suppressed. In case 2, L_p is not shown. L_{t1} is located between the two parallel coils of L_s. L_s with parallel coils is coupled to L_{t1} with enhanced coupling. Meanwhile, L_{t2} is located far from L_s, which leads to a relatively weak coupling. Thus, large total

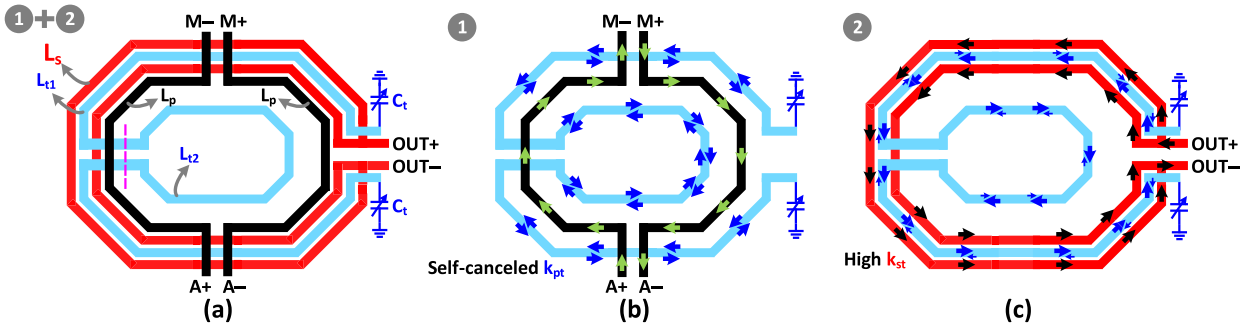


Fig. 15. (a) Configuration of the RSCCT. Corresponding configurations for (b) case 1 and (b) case 2 of the RSCCT.

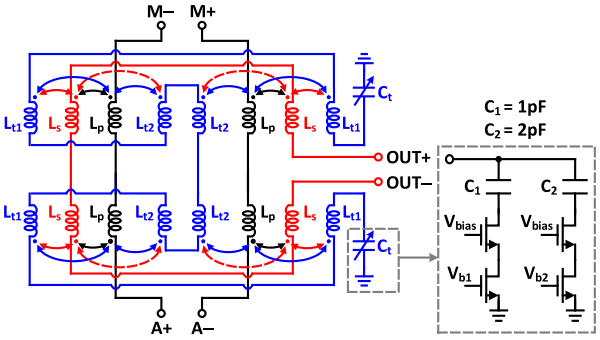


Fig. 16. Lumped model circuit of the RSCCT.

current of L_t is obtained, which means a strong coupling with factor of k_{st} between L_s and L_t.

The EM-simulated results of the RSCCT are shown in Fig. 17. As shown in Fig. 17(a), k_{pt} is less than 0.3, while k_{st} is larger than 0.5. k_{st}/k_{pt} with/without inductor L_{t2} is compared in Fig. 17(b). k_{st}/k_{pt} is significantly increased by L_{t2}. As shown in Fig. 17(c), when C_t is tuning within 3.5 pF, L_{se} is significantly increased from 176 to 218 pH with nearly constant L_{pe} from 184 to 188 pH. The effect of C_t on equivalent quality factors of primary and secondary inductors is shown in Fig. 17(d). Q_{pe} for primary inductor has shown a little degradation. Meanwhile, Q_{se} of secondary inductor drops from 14.9 to about 7.1. The equivalent coupling coefficients k_{pse} and n/k_{pse} are shown in Fig. 17(e) and (f), respectively. k_{pse} is slightly effected by C_t. n/k_{pse} is significantly increased with increasing C_t. As shown in Fig. 16, a 2-bit switched capacitor is used to implement C_t. The switched capacitors C_1 and C_2 are 1 and 2 pF, respectively. For better reliability of the switches, the cascode structure is adopted here.

2) Output Matching Network Based on RSCCT: Based on the RSCCT, the output matching network is shown in Fig. 18. The differential output signals of main and auxiliary PAs are combined and converted to single-ended output. A capacitor C_{out} is located at single-ended output for optimized matching. The load impedances Z_{LM} and Z_{LA} for main and auxiliary PAs are set to be $R_{opt} = 2.46\ \Omega$ at states A and E. Following the previous theoretical analysis, Z_{LM} and Z_{LA} should be reconfigured to be $2R_{opt}$ at states C and G by the proposed RSCCT. The simulated Z_{LM} across C_t at 2.4 GHz is shown in Fig. 19(a). The imaginary part of Z_{LM} should be finely compensated to be 0 by optimizing the matching network. Then, C_t is set to be 3 pF to achieve $2R_{opt}$ at states C and G.

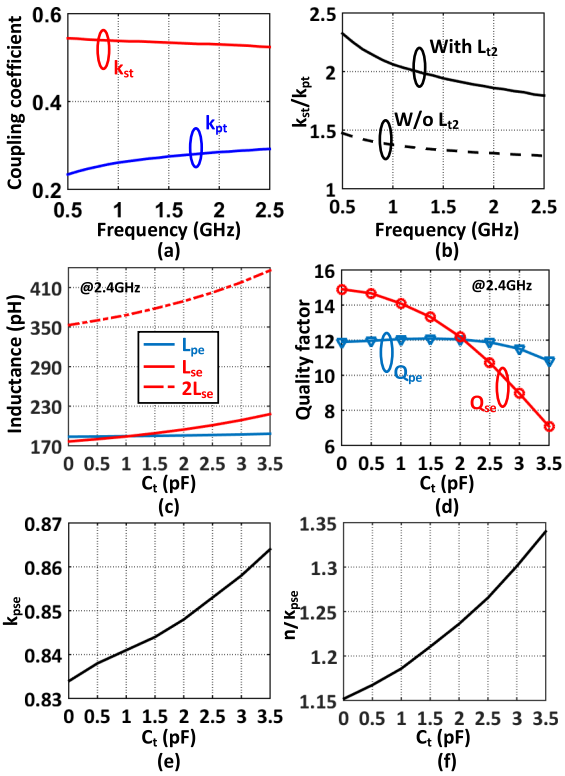


Fig. 17. EM-simulated results of the RSCCT. (a) k_{pt} and k_{st} across frequency. (b) Ratio of k_{st}/k_{pt} with and without inductor L_{t2} across frequency. (c) L_{pe} and L_{se} across C_t. (d) Equivalent quality factors Q_{pe} and Q_{se} across C_t. (e) Equivalent coupling coefficient k_{pse} across C_t. (f) Ratio of n/k_{pse} across C_t.

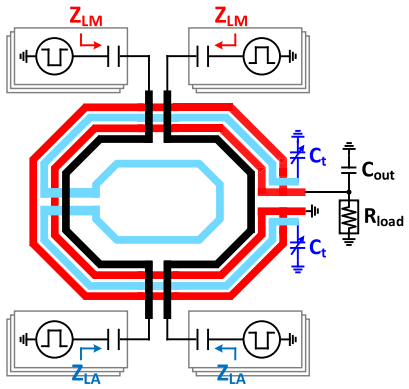


Fig. 18. Output matching network based on RSCCT.

The simulated output power across n/N at state C is shown in Fig. 19(b). To achieve the same output power with state B (i.e., 6-dB PBO) at state C, nearly, half of the unit cells should

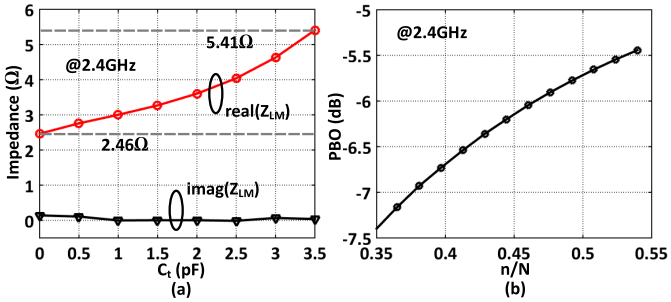


Fig. 19. (a) Simulated Z_{LM} across C_t. (b) Simulated output power of state C at 2.4 GHz across n/N. n unit cells are switched ON, while $N-n$ unit cells are floated.

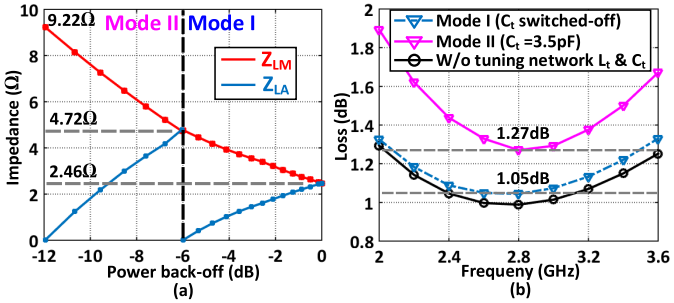


Fig. 20. (a) Simulated Z_{LM} and Z_{LA} versus PBO level at 2.4 GHz. (b) Simulated power loss of the output matching network based on RSCCT with/without tuning network.

be switched ON, which verifies the mechanism mentioned above. Then, the simulated load impedances Z_{LM} and Z_{LA} versus PBO level at 2.4 GHz are shown in Fig. 20(a). Due to the Doherty operation, from 0- to 6-dB PBO, Z_{LM} is increased from 2.46 to 4.72 Ω. Also, Z_{LA} is decreased from 2.46 Ω to 0. At state C, Z_{LM} and Z_{LA} are reconfigured to be about 4.72 Ω. From 6- to 12-dB PBO, Z_{LM} is increased, while Z_{LA} is decreased to 0. Based on the proposed reconfigurable output matching network with RSCCT, the desired operation can be obtained. The simulated power losses of the output matching network are shown in Fig. 20(b). Three conditions of matching networks (i.e., mode I, mode II, and without extra tuning network Lt and Ct) are compared. The proposed output matching network based on RSCCT features the minimal power loss of 1.05 and 1.27 dB at 2.8 GHz for modes I and II, respectively. The power loss is less than 1.9 dB from 2.1 to 3.6 GHz for modes I and II. The external tuning network with L_t and C_t in mode II introduces about 0.27 dB extra power loss at 2.8 GHz comparing to the fixed network without L_t and C_t.

IV. Fabrication and Measurement

The proposed quadrature SFCPA with RSCCT is fabricated in a 40-nm CMOS technology, which occupies 2 mm × 1.1 mm, including all I/O pads with 1.2-/2.4-V supply, as shown in Fig. 21. The chip core size is only 1.3 mm × 0.6 mm. The measurement setup is shown in Fig. 22. A signal generator is used to generate the 2LO signal. A wideband balun converts the 2LO signal to differential, which feeds the proposed SFCPA through the GSSG probe. Four serial baseband signals (i.e., IA, QA, IM, and QM) are generated by the arbitrary waveform generator (AWG) and converted to four

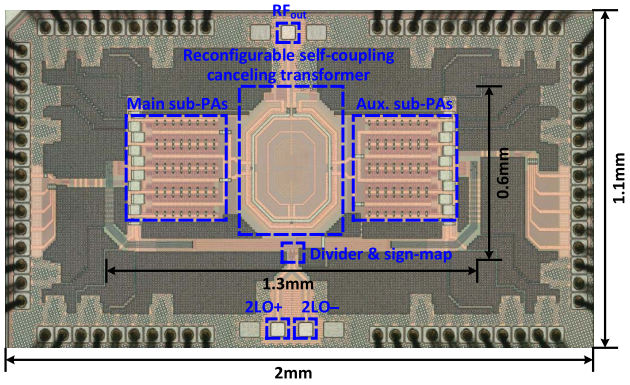


Fig. 21. Die micrograph.

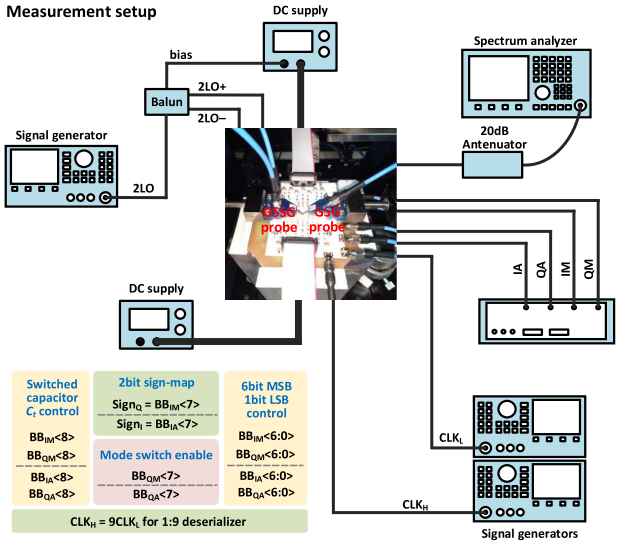


Fig. 22. Measurement setup.

9-bit parallel signals (i.e., $BB_{\mathrm{IA}}\langle 8{:}0\rangle$, $BB_{\mathrm{QA}}\langle 8{:}0\rangle$, $BB_{\mathrm{IM}}\langle 8{:}0\rangle$, and $BB_{\mathrm{QM}}\langle 8{:}0\rangle$) by four on-chip deserializers. Two sampling clocks (i.e., CLK_H and CLK_L with $\mathrm{CLK}_H = 9\mathrm{CLK}_L$) are introduced by two extra signal generators. The frequency of the CLKH should be nine times of CLKL. The CLKH and CLKL are sinusoidal waveforms with 1.1-V peak-to-peak voltage and 0.55-V dc biasing. Besides, the output signal of the proposed SFCPA is attenuated by a 20-dB attenuator and measured by the spectrum analyzer.

The measured saturated output power, DE, and system efficiency (SE) versus frequency are shown in Fig. 23. The proposed SFCPA features a peak P_{sat} of 30.3 dBm with a DE of 41.3% and an SE of 36.5% at 2.4 GHz. The 3-dB operational bandwidth is about 2.15–3.35 GHz. The power dissipation of core circuits, driving circuits, quadrature frequency divider, and all the logic blocks is considered in the SE calculation. For CW measurement at 2.4 GHz, the power consumptions of the PA arrays, quadrature frequency divider, and digital circuits (including decoders, deserializers, and buffers) at peak P_{sat} are about 2593, 1, and 335 mW, respectively.

The measured DE and SE of the proposed SFCPA with two typical conditions versus output power at 2.4 GHz are shown in Fig. 24. The proposed SFCPA achieves DE of 41.3%, 37.5%, 36.1%, 30.9%, 26.2%, and 20.2% at 0-, 3-, 6-, 9-, 12-, and 15-dB PBOs. Meanwhile, it exhibits SE of 36.5%,

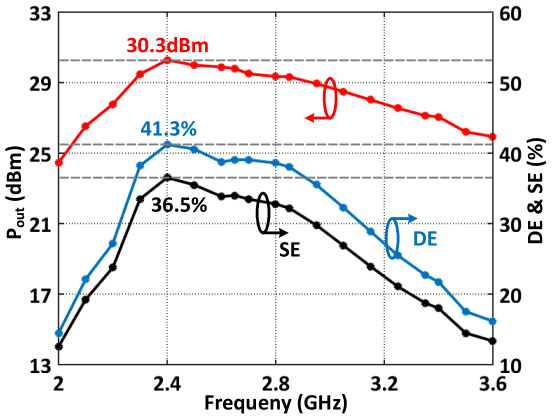


Fig. 23. Measured saturated output power and peak efficiency.

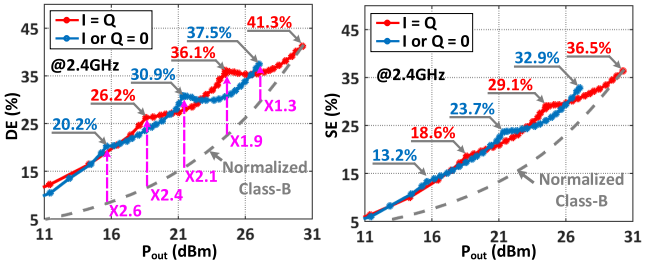


Fig. 24. Measured DE and SE versus P_{out} at 2.4 GHz.

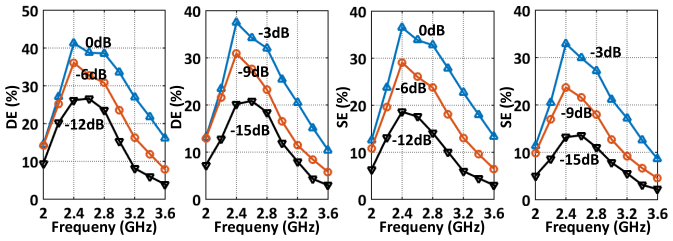


Fig. 25. Measured DE and SE at various PBO levels over the frequency.

32.9%, 29.1%, 23.7%, 18.6%, and 13.2% for 0-, 3-, 6-, 9-, 12-, and 15-dB PBOs. The measured DE and SE at various PBO levels over the frequency are shown in Fig. 25. The measured typical AM–AM/AM–PM distortions of condition $I = Q$ and condition Q code $= 0$ at 2.4 GHz are shown in Fig. 26(a) and (b), respectively. At state C, nearly, half of the main and auxiliary PAs are switched ON to deliver the same output amplitude with state B, while other capacitor unit cells are floated at state C. Then, the proposed SFCPA introduces a little amplitude discontinuity at mode switching. Besides, the proposed SFCPA shows a little AM–AM distortion in each operation mode due to the similar operation with SCPA.

The proposed SFCPA introduces about 9.5° and 9.3° phase discontinuity at the mode switching for condition $I = Q$ and $Q = 0$, respectively. However, it exhibits a little AM–PM distortion in each operation mode. Since the condition $I = Q$ and $I/Q = 0$ adopt the same output matching, the AM–AM and AM–PM distortions of $I = Q$ are similar to $I/Q = 0$.

Based on the static AM–AM and AM–PM distortions, a 2-D digital predistortion (DPD) is adopted to further minimize the AM–AM and AM–PM distortions. The amplitude digital control signals for QAM signal are pulse-shaped and filtered by using a square-root raised cosine filter. The reconfigurable

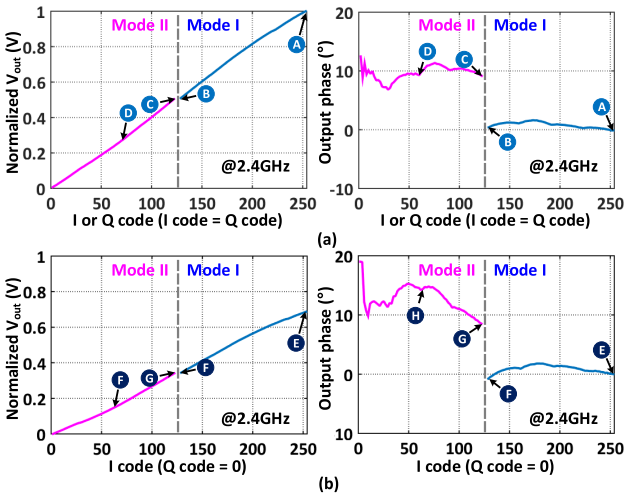


Fig. 26. Measured typical AM–AM and AM–PM distortions of (a) condition I code $= Q$ code and (b) condition Q code $= 0$.

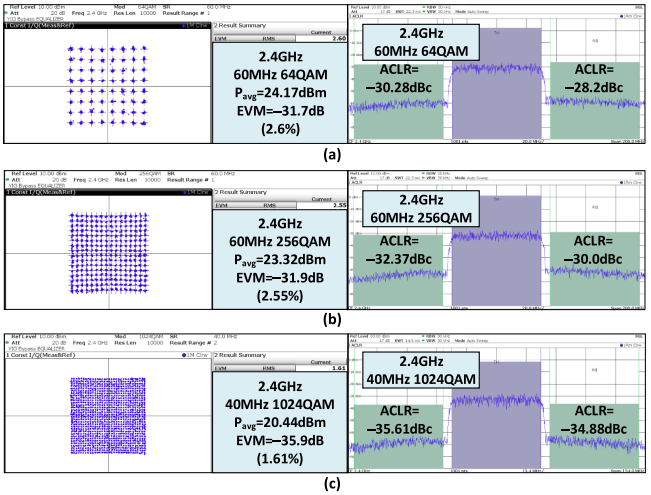


Fig. 27. Measured output spectrum and constellation of (a) 60-MHz 64-QAM, (b) 60-MHz 256-QAM, and (c) 40-MHz 1024-QAM signals.

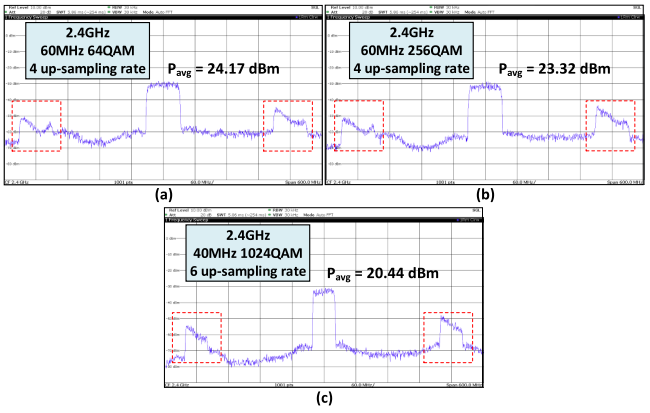


Fig. 28. Measured OOB spectrum of (a) 60-MHz 64-QAM, (b) 60-MHz 256-QAM, and (c) 40-MHz 1024-QAM signals.

output matching network should be synchronously switched to mode I or II according to the up-sampled BB signals. Then, the 60-MHz 64-QAM, 60-MHz 256-QAM, and 40-MHz 1024-QAM modulation signals at 2.4 GHz are measured and shown in Fig. 27. The measured 60-MHz 64-QAM signal

TABLE II
COMPARISON WITH STATE-OF-THE-ART QUADRATURE DIGITAL PAS

	This work		JSSC2017 [31]	ISSCC2017 [32]	ISSCC2020 [34]	JSSC2021 [35]	JSSC2021 [25]
Architecture	**Quadrature SFCPA with hybrid Doherty and impedance boosting**		IQ sharing	IQ sharing SCPA	IQ sharing with complex-domain load modulation	Quadrature Class-G Doherty	IQ hybrid Doherty and impedance boosting
Technology	**40nm CMOS**		28nm CMOS	28nm CMOS	55nm CMOS	65nm CMOS	40nm CMOS
Supply (V)	**1.2/2.4**		1.1	1.1	1.2/2.4	1.25/2.55	1.1
Supply switching	**NO**		NO	NO	NO	YES	NO
Matching	**1 transformer**		Off-chip	1 transformer	1 transformer	2 transformer	1 transformer
Frequency (GHz)	**2.4**		0.8	2.5	0.85	2.2	2.8
Peak P_{out} (dBm)	**30.3**		13.9	28.6	29.3	27.8	24.2
η peaks	**6**		2	8	3	7	6
η peaks at PBOs (dB)	**0/3/6/9/12/15**		0/3	0/2.5/3/5.5/6/9/12/15	0/3/6	0/2.5/3/5.5/6/12/15	0/3/6/9/12/15
Peak η (%)	**41.3 (DE)**	**36.5 (SE)**	40.4 (PAE)	35 (PAE)	43.1 (PAE)	32.1 (SE)	38.5 (DE)
η @ 3dB PBO (%)	**37.5 (DE)**	**32.9 (SE)**	>33 (PAE)*	30* (PAE)	35* (PAE)	28* (SE)	39.3 (DE)
η @ 6dB PBO (%)	**36.1 (DE)**	**29.1 (SE)**	N/A	24* (PAE)	32* (PAE)	24* (SE)	29.6 (DE)
η @ 9dB PBO (%)	**30.9 (DE)**	**23.7 (SE)**	N/A	N/A	N/A	12* (SE)	29.5 (DE)
η @ 12dB PBO (%)	**26.2 (DE)**	**18.6 (SE)**	N/A	13.9 (PAE)	N/A	14* (SE)	18.4 (DE)
η @ 15dB PBO (%)	**20.2 (DE)**	**13.2 (SE)**	N/A	N/A	N/A	5* (SE)	14.9 (DE)
Modulation	**60MHz 256QAM#**	**40MHz 1024QAM#**	LTE 10MHz 16-QAM	LTE 5-10MHz	LTE 10MHz 64QAM	20MHz 1024QAM	10MHz 256QAM
P_{avg} (dBm)	**23.32**	**20.44**	6.97	20.7	23.6	21.0	16.2
Average η (%)	**30.7 (DE)**	**22.6 (DE)**	29.1 (PAE)	14.6 (PAE)	24.4 (PAE)	18.4 (SE)	24.6 (DE)
EVM (dB)	**–31.9**	**–35.9**	–29.9	–29.9	–25.6	–43	–32.3
Chip size (mm^2)	**2.2 (0.78**)**		1.09	1**	1.196**	3	2.1 (0.83**)

*Estimated from figures **Core size #Limited by measurement setup

shows the average output power (P_{avg}) of 24.17 dBm with an average DE of 31.2%, an EVM of −31.7 dB, and an ACLR ⩽ −28.2 dBc. For 60-MHz 256-QAM signal, it features P_{avg} of 23.32 dBm with an average DE of 30.7%, an EVM of −31.9 dB, and an ACLR ⩽ −30 dBc. Besides, the 40-MHz 1024-QAM signal is also supported by the proposed SFCPA, which exhibits P_{avg} of 20.44 dBm with an average DE of 22.6%, an EVM of −35.9 dB, and an ACLR ⩽ −34.88 dBc. The out-of-band (OOB) spectra of 60-MHz 64-QAM, 60-MHz 256-QAM, and 40-MHz 1024-QAM signals are shown in Fig. 28(a)–(c), respectively. The spectrum image is mainly caused by the digitized and time-sampled interpolations of the signal envelope [38]. The proposed DPA adopts the power digital-to-analog converters (DACs) based on zero-order hold (ZOH) interpolations, which introduces spectral images at integer multiples of the sampling frequency [39]. The maximal sampling frequency is only 240 MHz, which limits the OOB spectrum, including the spectral image suppression and OOB spectrum noise floor. The larger sampling frequency would move the replicas to higher offset, which enhances the OOB spectrum performance. Note that the jump-based discontinuity caused by mode switch increases the duration and amplitude of the glitch, which leads to performance degradation of EVM, ACLR, and OOB noise. To enhance the performance of EVM, ACLR, and OOB noise, higher BB sampling frequency and higher resolution of power-DAC should be used. Besides, the jump-based discontinuity should be avoided and limited at mode switch by circuit optimization.

Fig. 29(a) shows the measured EVM and ACLR of 256-QAM and 1024-QAM modulation signals versus symbol rate. The modulation signals transmit the maximal P_{avg} without PBO. With constant maximal 240-MHz sampling frequency, the modulation signal with higher symbol shows lower up-sampling rate. The lower up-sampling rate leads to EVM degradation, especially for higher order QAM signal. It can be seen that the EVM of 1024-QAM signal increases more sharply with increased symbol rate comparing to the 256-QAM signal, as shown in Fig. 11. Thus, the EVM of 10-MHz 1024-QAM signal (i.e., −38.71 dB) is much

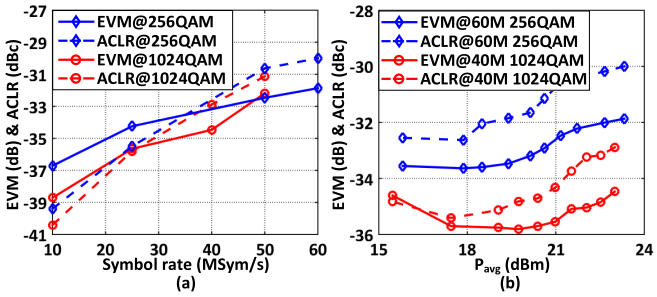


Fig. 29. (a) Measured EVM and ACLR of modulation signals versus symbol rate. (b) Measured EVM and ACLR of modulation signals versus average output power P_{avg}.

lower than that of 10-MHz 256-QAM signal (i.e., −36.71), while the EVM of 50-MHz 1024-QAM is higher than that of 50-MHz 256-QAM. The measured EVM and ACLR of modulation signals versus P_{avg} are shown in Fig. 29(b). The EVM and ACLR of 256-QAM and 1024-QAM modulation signals could be further improved at proper PBO level. The comparison with previous state-of-the-art quadrature DPAs is shown in Table II. The proposed quadrature SFCPA exhibits watt-level P_{out} of 30.3 dBm with an SE of 36.5%. Moreover, without supply switching, the PA efficiency is effectively improved at 0-/3-/6-/9-/12-/15-dB PBO, which leads to higher average efficiency. Besides, the proposed SFCPA could support the complex modulation signals, such as 256- and 1024-QAM signals.

V. CONCLUSION

In this article, a quadrature SFCPA is presented with RSCCT for deep PBO efficiency enhancement. The SFCPA, which decreases the dynamic power consumption required to charge and discharge capacitor array, introduces efficiency enhancement at PBO. The RSCCT is proposed with enhanced tuning range of turn ratio, which achieves the boosted PA load impedance. Then, based on hybrid Doherty and impedance boosting, the proposed SFCPA introduces multiple efficiency peaks without supply switching. The proposed SFCPA fabricated in 40-nm CMOS technology shows the merits of high

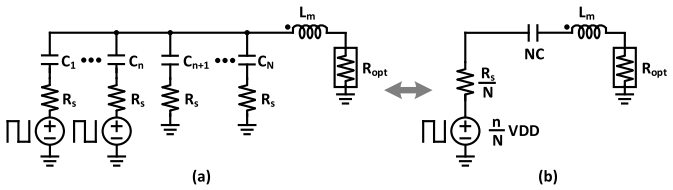


Fig. 30. (a) Circuit of SCPA considering the switch resistor R_s and (b) its Thévenin equivalent circuit.

peak and average efficiency, watt-level output power, low cost, and high integration level, which are attractive for wireless communication applications.

APPENDIX

The equivalent circuit of SCPA considering the switch resistance R_s is shown in Fig. 30. The output power of the SCPA can be calculated as

$$P_{\text{out,SC}} = \frac{2\text{VDD}^2}{\pi^2}\left(\frac{n}{N}\right)^2 \frac{R_{\text{opt}}}{(R_{\text{opt}} + R_s/N)^2}. \tag{25}$$

The dynamic power P_{SC} to charge and discharge the capacitor array is

$$P_{\text{SC}} = \frac{n(N-n)}{2\pi N^2 Q_{\text{loaded}} R_{\text{opt}}}\text{VDD}^2. \tag{26}$$

The power dissipation $P_{\text{RS,SC}}$ on the switch resistor can be calculated by

$$P_{R_s,\text{SC}} = \frac{2\text{VDD}^2}{\pi^2}\left(\frac{n}{N}\right)^2 \frac{R_s/N}{(R_{\text{opt}} + R_s/N)^2}. \tag{27}$$

The load impedance R_{opt} is defined to be

$$R_{\text{opt}} = t\frac{R_s}{N}. \tag{28}$$

where t is a coefficient. Then, the DE of the SCPA is expressed by

$$\begin{aligned}\text{DE}_{\text{SC}} &= \frac{P_{\text{out,SC}}}{P_{\text{out,SC}} + P_{\text{SC}} + P_{\text{Rs,SC}}} \\ &= \frac{4n^2 R_{\text{opt}}^2}{4n^2 R_{\text{opt}}^2 + \frac{\pi n(N-n)(R_{\text{opt}}+R_s/N)^2}{Q_{\text{loaded}}} + 4n^2 R_{\text{opt}} R_s/N} \\ &= \frac{4n^2 t^2}{4n^2 t^2 + \frac{\pi n(N-n)(t+1)^2}{Q_{\text{loaded}}} + 4n^2 t}.\end{aligned} \tag{29}$$

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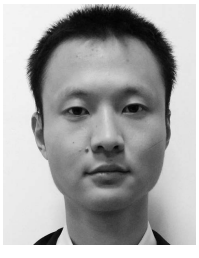

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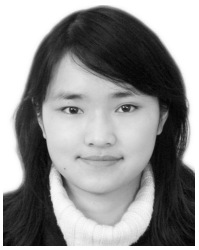

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