A Low Phase Noise and High FoM Distributed-Swing-Boosting Multi-Core Oscillator Using Harmonic-Impedance-Expanding Technique

Yiyang Shu, *Member, IEEE*, Huizhen Jenny Qian, *Member, IEEE*, Xiang Gao, *Senior Member, IEEE*, and Xun Luo, *Senior Member, IEEE*

***Abstract*— In this article, a distributed-swing-boosting and harmonic-impedance-expanding multi-core oscillator is proposed to achieve low phase noise and high figure-of-merit (FoM), simultaneously. First, a distributed-coupling multi-core topology is introduced to reduce the chip area with no mode ambiguity. Then, the distributed-swing-boosting and harmonic-impedance-expanding structure is developed to boost the gate swing and square-like waveform of V_{DS}. The common-mode (CM) resonances around the second harmonic and the differential-mode (DM) resonances around the third harmonic are utilized to suppress the flicker noise up-conversion and achieve harmonic shaping. Meanwhile, the dual-resonance response expands the high-impedance frequency ranges around the harmonics, and thus, the effect of harmonic shaping can be obtained over a wide frequency range. Fabricated in a 40-nm CMOS process, the oscillator measured exhibits low phase noise and high FoM simultaneously with a compact chip size. The minimum phase noise is −138.9 dBc/Hz at the 1-MHz offset, corresponding to an FoM of 195.1 dBc/Hz. The $1/f^3$ phase noise corner is 100–130 kHz over the 26.6% tuning range.**

***Index Terms*— Distributed coupling, figure-of-merit (FoM), flicker noise, harmonic impedance expanding, multi-core, oscillator, phase noise.**

I. Introduction

THE rapid development of high-speed communication and radar systems has stringent requirements on the spectral purity of RF oscillators. Meanwhile, to maximize the battery lifetime, the phase noise normalized to power consumption is of great concern. Therefore, the oscillator with low phase noise as well as high figure-of-merit (FoM) is one of the critical challenges in the wireless system. Based on Lesson's phase noise equation [1], the expression of FoM that normalizes the phase noise to power and frequency can be calculated as

$$\text{FoM} = 10\log_{10}\left(\frac{2\eta Q^2}{10^3 kTF}\right) \tag{1}$$

where k is Boltzmann's constant, T is the absolute temperature, η is the power efficiency, F is the device effective noise factor, and Q is the tank's quality factor. Thus, high power efficiency, high quality factor, and low effective noise factor are preferred to obtain the high FoM. On the other hand, the aggravated flicker noise in scaled CMOS technologies may worsen the close-in phase noise [2], [3]. Thus, the suppression of flicker noise up-conversion is also important for good phase noise performance.

Common-mode (CM) tail-filtering technique is introduced to achieve the state-of-the-art FoM [4]. However, the extra tail inductor increases the chip size and needs extra tuning mechanism to support a wide operation band. Recently, to reduce the noise sensitivity of the LC oscillator with single tank, various harmonic-shaping techniques [5]–[14] are reported. By setting the differential-mode (DM) [5], [6] and CM [7], [8] resonances at specific harmonic frequencies, the rms value of impulse sensitive function (ISF) is reduced, while flicker noise up-conversion due to the Groszkowski effect [15] can be suppressed. Then, the FoM is effectively

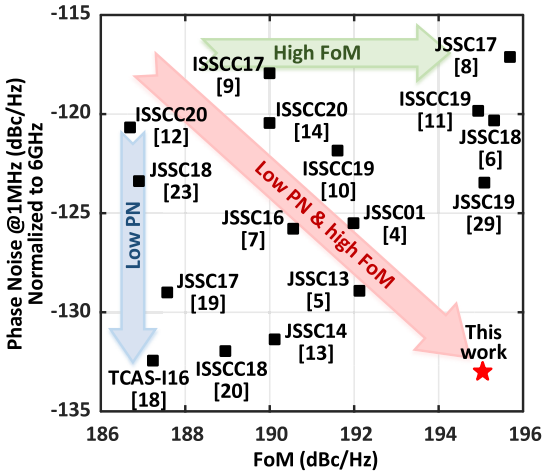

Fig. 1. Normalized phase noise and FoM of state-of-the-art oscillators.

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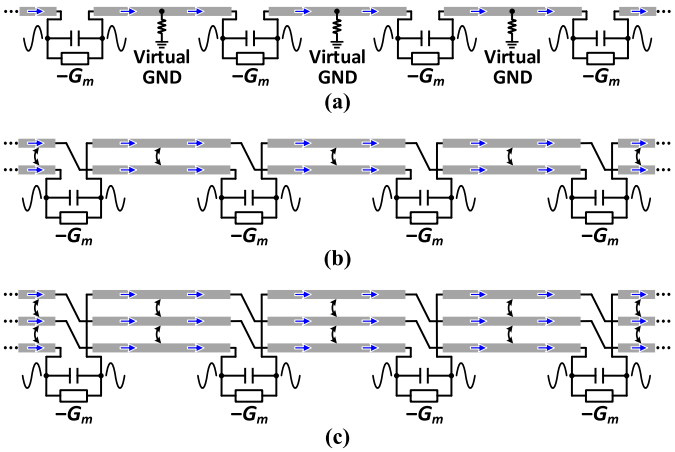
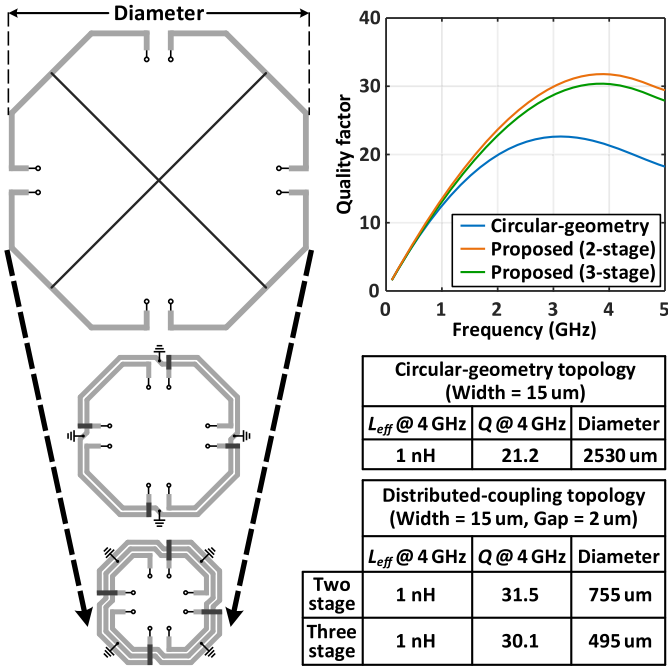


Fig. 2. Unfolded types of (a) circular-geometry oscillator, (b) two-stage distributed-coupling topology, and (c) three-stage distributed-coupling topology.



Circular-geometry topology (Width = 15 um)		
L_{eff} @ 4 GHz	Q @ 4 GHz	Diameter
1 nH	21.2	2530 um

	Distributed-coupling topology (Width = 15 um, Gap = 2 um)		
	L_{eff} @ 4 GHz	Q @ 4 GHz	Diameter
Two stage	1 nH	31.5	755 um
Three stage	1 nH	30.1	495 um

Fig. 3. Layout and quality factor of the circular-geometry oscillator and proposed distributed-coupling topology.

improved. However, to meet the strict ratios between fundamental frequency and harmonic resonances, the robustness of the harmonic-shaping effect with the tuning of frequency is limited. On the other hand, with the scaling down of advanced technology, the reduced power supply limits the maximum power taken by a single-core resonate tank. Thus, most of the harmonic-shaping oscillators are suitable for low-power situation and hardly meet the requirement of ultra-low phase noise. To break the limitation of single-core oscillator, the low-phase-noise oscillators have evolved from the single-core to multi-core type [16]–[21]. Occupying N (or more) times of chip size, it is possible for N-core oscillator to burn N times higher power and decrease the phase noise by $10\log(N)$ dB. The circular-geometry oscillator is a compact topology of multi-core oscillator [22], [23]. By merging the resonators together, the chip size can be reduced. Nevertheless, it needs high-resistance center taps to avoid unwanted modes. For NMOS or PMOS active core, the center taps cannot be used to supply the power. Thus, this topology is only suitable for CMOS type, which leads to a limited voltage swing. Due to the challenge of chip area and multi-core coupling, the FoM of published multi-core oscillators is worse than the state-of-the-art single-core oscillators. Therefore, as surveyed in Fig. 1, it is not easy for existing oscillators to obtain low phase noise and high FoM simultaneously.

To overcome the limitation of conventional multi-core oscillator, this article proposes a distributed-swing-boosting and harmonic-impedance-expanding quad-core oscillator [24], which can achieve low phase noise, high FoM, and compact chip size simultaneously. A distributed-coupling multi-core topology is introduced to reduce the chip size and determine the current direction of each core without resistor in center taps. Thus, the NMOS-only or PMOS-only couple pair can be adopted. Based on the distributed-coupling multi-core topology, the distributed-swing-boosting oscillator is developed. The gate swing is boosted by the three-stage coupling, while the harmonic-shaped waveforms of drain and source are both obtained to form a boosted V_{DS}. The CM resonance around the second harmonic and the DM resonances around the third harmonic are utilized to suppress the flicker noise up-conversion and reduce the ISF. Moreover, the dual-resonance response expands the high-impedance frequency ranges around the harmonics. Thus, the robustness of the performance with the tuning of frequency is improved. Fabricated in a 40-nm CMOS technology, the proposed oscillator achieves a 26.6% tuning range from 3.09 to 4.04 GHz. The minimum phase noise is -138.9 dBc/Hz at the 1-MHz offset, corresponding to an FoM of 195.1 dBc/Hz. The $1/f^3$ phase noise corner is 100–130 kHz. Although operating at lower frequency, the chip size of the proposed oscillator is still much smaller than other published quad-core oscillators.

This article is organized as follows. In Section II, the distributed-coupling multi-core topology is discussed. Section III demonstrates the principles of harmonic-impedance-expanding technique and the design of distributed-boosting harmonic-impedance-expanding multi-core oscillator. The optimization and phase noise analysis are also provided in this section. In Section IV, the measurements of the oscillator are provided and compared. Finally, a conclusion is given in Section V.

II. Distributed-Coupling Multi-Core Topology

The unfolded type of the circular-geometry oscillator is shown in Fig. 2(a). Adjacent active cores are connected by the inductor. The high-resistance traces are used to avoid latching and mode ambiguity. Then, the currents in each inductor flow in the same direction. For the proposed distributed-coupling multi-core topology, the non-adjacent cores are connected by the multi-segment inductors. Fig. 2(b) and (c) shows the two-stage and three-stage types of the distributed-coupling

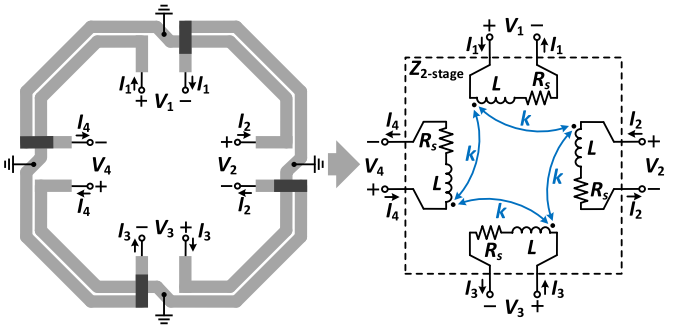


Fig. 4. Four-port passive and simplified equivalent model of the two-stage distributed-coupling topology.

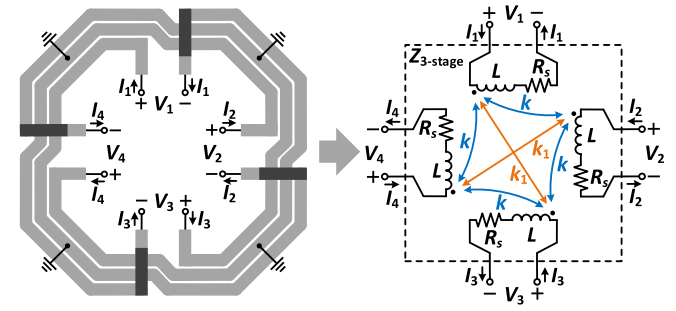


Fig. 5. Four-port passive and simplified equivalent model of the three-stage distributed-coupling topology.

topology. Each inductor can be regarded as two or three segments. Each segment couples the previous or next inductor. The inductors in the multi-core chain are distributed-coupled together to ensure the same current direction in each inductor. Therefore, the high-resistance traces in center taps can be replaced by power supply or ground to support the NMOS-only or PMOS-only active core.

At single-GHz frequency, due to the large area penalty, multi-core oscillator is rarely adopted, especially for core number ≥ 4. To reduce the phase noise, one can try to lower the inductance by shrinking the diameter of inductor. However, for a much smaller inductance, the quality factor starts dropping dramatically as series resistance losses start to dominate [18]. Moreover, the small diameters increase coupling between the traces and reduce the coil's inductance per unit length. This destructive coupling is also harmful to the quality factor [23]. On the other hand, with the decreasing of inductance, the capacitance must increase to keep the same oscillation frequency. The interconnections in the capacitor array will become more significant and lower the tank's quality factor [25]. For the circular-geometry oscillator operating at single-GHz, the long routing of inductor introduces considerable parasitic capacitance, which leads to a low self-resonance of the inductor and thus may limit the quality factor at the desired frequency. In the proposed distributed-coupling topology, the inductance in a specific area becomes double for two-stage type or triple for three-stage type. Meanwhile, the couplings among the coils can increase the magnetic flux seen from each inductor without introducing resistive loss, which benefits the quality factor [26]. Moreover, compared to the multi-coil single-core inductor, the increased inner diameter of the proposed topology can reduce the mutual coupling between traces carrying out-of-phase current. Then, the quality factor can be higher. Fig. 3 compares the quad-core layouts of the circular-geometry oscillator [i.e., Fig. 3 (top left)] and the proposed distributed-coupling topologies [i.e., two-stage type in Fig. 3 (middle left) and three-stage type in Fig. 3 (bottom left)]. In order to compare the quality factors of different topologies, the four-port passives can be equivalent to four paralleled single inductors with the same effective inductance L_{eff}. To obtain the effective inductance of 1 nH and optimized quality factor at 4 GHz, the trace width is chosen as 15 μm, while the diameters of the three quad-core layouts are 2530, 755, and 495 μm. The proposed topology obtains a remarkable reduction of chip size. Meanwhile, the optimized quality factor at 4 GHz of the proposed topology is increased by about 50%, which is benefitted for better phase noise performance and FoM. As a result, the proposed topology can balance the inductance, quality factor, and capacitor banks for low phase noise and compact chip area.

The effective inductance and quality factor in Fig. 3 are obtained when the voltage and current in each core follow the desired condition in Fig. 2. However, for an N-core oscillator, it is possible to exist N modes with different phase relationships of each core [23]. To quantitatively discuss the possible oscillation modes of the proposed distributed-coupling multi-core topology, the passive of quad-core distributed-coupling topology is studied. The four-port passive can be modeled as a 4×4 Z-matrix as follows:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \tag{2}$$

where I_{1-4} and V_{1-4} are the currents and voltages seen from each port. Figs. 4 and 5 show the four-port passive and simplified equivalent models of the two- and three-stage topologies, respectively. L and R_s are the inductance and parasitic resistance seen from each port without the couplings, respectively. It is notable that, without using the high-resistance trace, the parasitics of center taps are small enough compared to the passive. Thus, this part is not considered in the simplified model but included in the EM simulation of the whole passive as presented later. For the two-stage topology shown in Fig. 4, k is the equivalent coupling factor between adjacent inductors. Then, the Z-matrix of the two-stage passive is expressed as follows:

$$Z_{2-\text{stage}} = \begin{bmatrix} R_s + j\omega L & j\omega kL & 0 & j\omega kL \\ j\omega kL & R_s + j\omega L & j\omega kL & 0 \\ 0 & j\omega kL & R_s + j\omega L & j\omega kL \\ j\omega kL & 0 & j\omega kL & R_s + j\omega L \end{bmatrix}. \tag{3}$$

Since the load connected to each port is identical and the resonator is central symmetric, the excitation conditions should be set to meet the symmetry. Then, the effective impedances seen from each port can be calculated as $Z_{\text{eff}} = V_n/I_n$ (i.e., $n = 1,2,3,4$) by determining the phase relationship as follows:

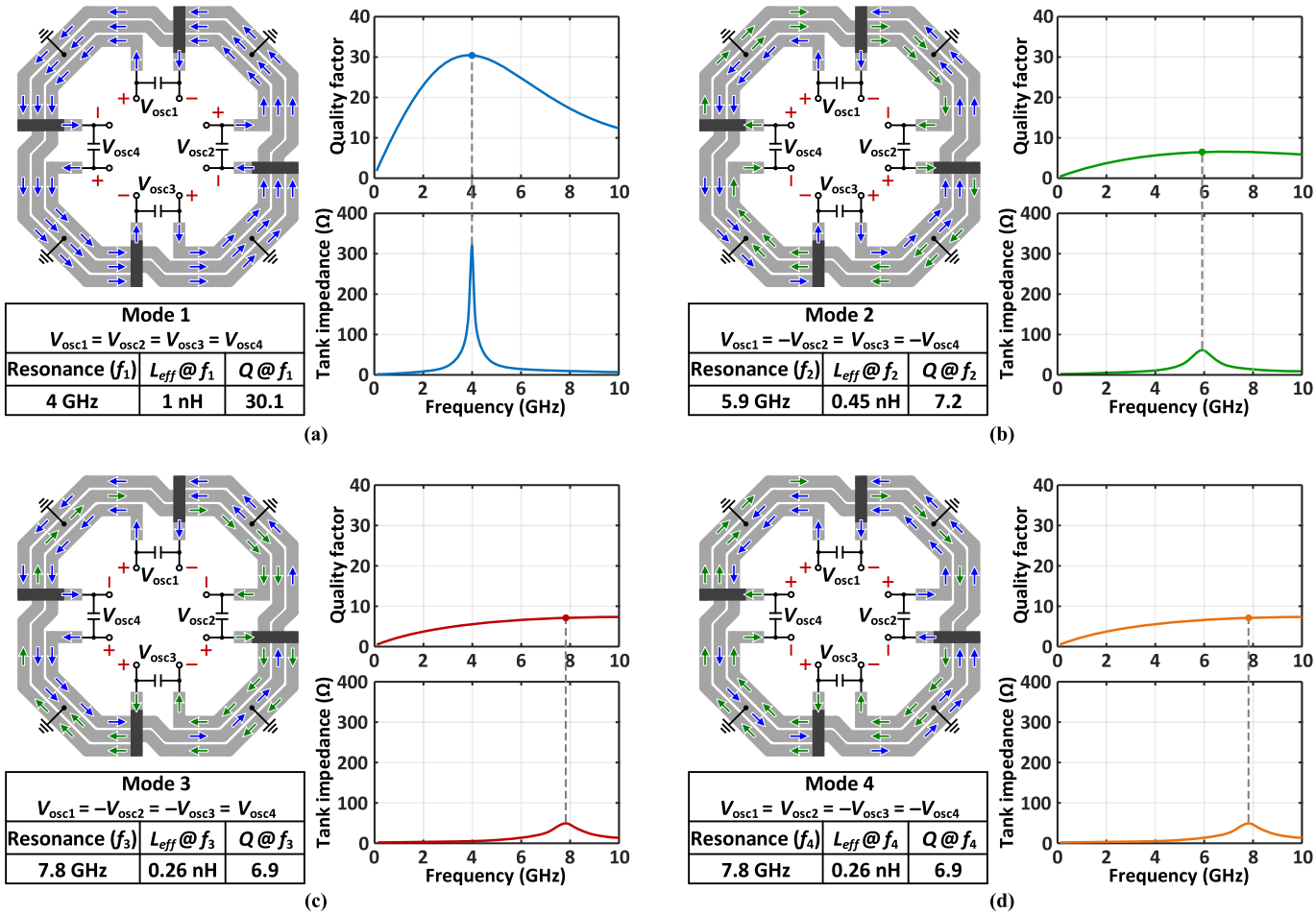


Fig. 6. Currents, inductor's effective quality factors, and tank impedances of (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

1) mode1: $V_1 = V_2 = V_3 = V_4$; 2) mode 2: $V_1 = -V_2 = V_3 = -V_4$; 3) mode 3: $V_1 = -V_2 = -V_3 = V_4$; and 4) mode 4: $V_1 = V_2 = -V_3 = -V_4$. The effective impedances in each mode are given as

$$Z_{2-\text{stage,mode1}} = R_s + j\omega L(1+2k) \tag{4}$$

$$Z_{2-\text{stage,mode2}} = R_s + j\omega L(1-2k) \tag{5}$$

$$Z_{2-\text{stage,mode3}} = Z_{2-\text{stage,mode4}} = R_s + j\omega L. \tag{6}$$

For the three-stage topology shown in Fig. 5, there are couplings between any two inductors. The equivalent coupling factor between opposite inductors is k_1. The Z-matrix of the three-stage passive is expressed as follows:

$$Z_{3-\text{stage}} = \begin{bmatrix} R_s + j\omega L & j\omega kL & j\omega k_1 L & j\omega kL \\ j\omega kL & R_s + j\omega L & j\omega kL & j\omega k_1 L \\ j\omega k_1 L & j\omega kL & R_s + j\omega L & j\omega kL \\ j\omega kL & j\omega k_1 L & j\omega kL & R_s + j\omega L \end{bmatrix}. \tag{7}$$

The effective impedances in each mode are calculated as

$$Z_{3-\text{stage,mode1}} = R_s + j\omega L(1+2k+k_1) \tag{8}$$

$$Z_{3-\text{stage,mode2}} = R_s + j\omega L(1-2k+k_1) \tag{9}$$

$$Z_{3-\text{stage,mode3}} = Z_{3-\text{stage,mode4}} = R_s + j\omega L(1-k_1). \tag{10}$$

For both two- and three-stage topologies, mode 1 has the largest effective inductance, while the resistances of all the modes are identical. The effective quality factor is calculated as $\omega L_{\text{eff}}/R_{\text{eff}}$. Considering the expression of resonance frequency, the quality factor at the resonance frequency is expressed as $(L_{\text{eff}}/C)^{1/2}/R_{\text{eff}}$. Assuming that the capacitances in different modes are constant, the quality factor is proportional to $(L_{\text{eff}})^{1/2}/R_{\text{eff}}$. For the two-stage topology, the quality factor of mode 1 is $((1+2k)/(1-2k))^{1/2}$ times the quality factor of mode 2 and $(1+2k)^{1/2}$ times the quality factor of modes 3 and 4. For the three-stage topology, the quality factor of mode 1 is $((1+2k+k_1)/(1-2k+k_1))^{1/2}$ times the quality factor of mode 2 and $((1+2k+k_1)/(1-k_1))^{1/2}$ times the quality factor of modes 3 and 4. Therefore, for both topologies, the quality factor of mode 1 is higher than other modes.

Based on the mode analysis of the four-port passive, the four-port resonator can be used to discuss the resonances corresponding to each oscillation mode. Consider a four-port resonator formed by the distributed-coupled passive with each port connected by a capacitor. The resonances can be obtained by the tank impedance seen from each port. Taking the three-stage topology as an example, the EM simulation of the passive considering the center taps is used to verify the concept. Fig. 6 shows the inductor's effective quality factors and tank impedances of each mode. $V_{\text{osc1}-4}$ are the voltages of each oscillator core. In mode 1, all the currents flow in a counterclockwise direction, and the superposition of magnetic field leads to a high effective inductance and high quality

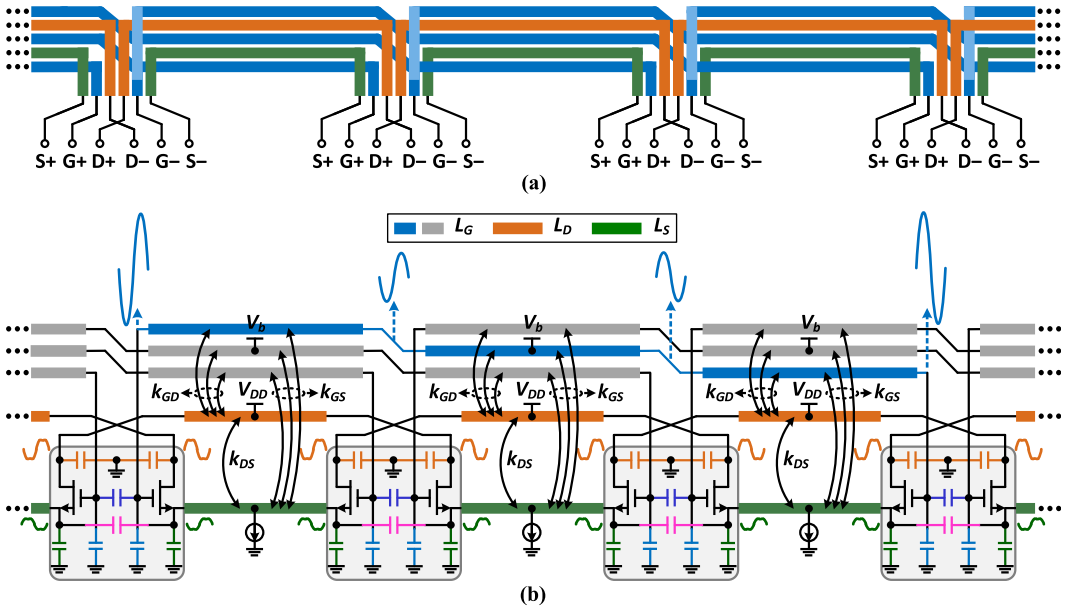


Fig. 7. Diagrams of (a) distributed-swing-boosting transformer and (b) distributed-swing-boosting and harmonic-impedance-expanding oscillator chain.

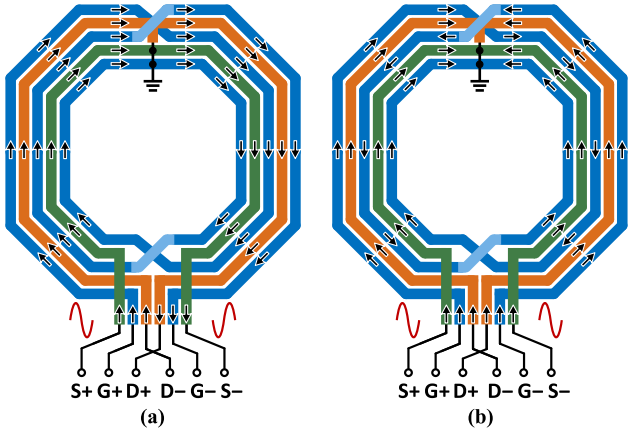


Fig. 8. Single-core equivalent transformer excited in (a) DM and (b) CM input signal.

factor of 30.1 at the resonance of 4 GHz. In modes 2, 3, and 4, the magnetic fields generated by counterclockwise-flowing currents and clockwise-flowing currents (i.e., shown in blue and green respectively) cancel each other out. As a result, the quality factor in mode 2 is only 7.2 at the resonance of 5.9 GHz, while the quality factors in modes 3 and 4 are 6.9 at the resonance of 7.8 GHz. As expected, there is only one mode (i.e., mode 1) that has the high quality factor of the passive, which is higher than four times the quality factors of unwanted modes. By properly choosing the transconductance of the couple pairs, the unwanted modes at higher frequencies cannot be excited. Then, the mode ambiguity or concurrent oscillation can be avoided.

III. Distributed-Swing-Boosting and Harmonic-Impedance-Expanding Quad-Core Oscillator

The distributed-coupling multi-core topology has been discussed to achieve high quality factor with a compact chip size. However, the topology of oscillator is still based on conventional class-B type, which is not suitable for reducing the effective noise factor. Therefore, the distributed-swing-boosting and harmonic-impedance-expanding technique is developed. Fig. 7(a) shows the diagrams of distributed-swing-boosting transformer. The inductors connected to drains and sources (i.e., in green and orange, respectively) are nested in the three-stage distributed-coupling inductors connected to gates. The distributed-swing-boosting and harmonic-impedance-expanding oscillator chain using the proposed transformer is shown in Fig. 7(b). To clarify the effect of distributed-swing-boosting, only one of the distributed-coupling inductors is highlighted in blue. It is notable that each gate inductor couples three drain inductors and source inductors. Thus, the voltage swing at the gate can be boosted by the distributed three-stage coupling. Due to the anti-phase connection between drain and source, the voltage swing of V_{DS} is also boosted. With the multi-order resonator, the CM and DM resonances around harmonics can be utilized to suppress the flicker noise up-conversion and achieve the harmonic shaping of voltage waveform. Thus, the rms value of ISF is reduced within a period, and then, the FoM of oscillator can be improved. Since the voltage waveforms of gate and drain are both utilized, the harmonics of V_{DS} are formed by the harmonics of both V_D and V_S. Moreover, compared with published harmonic-shaping techniques, the high-impedance ranges around the harmonic frequencies are expanded. The phase of CM and DM responses fluctuate around 0° within an expanded frequency range. Therefore, the robustness of the performance with the tuning of frequency is improved.

A. Harmonic-Impedance-Expanding Technique

The DM and CM harmonic-shaping effects have been achieved simultaneously by the class-$F_{2,3}$ oscillator [7], which introduces the sharp magnitude response and monotonous phase response around the second and third harmonics. Thus, the harmonic-shaping effect is very sensitive to the ratio

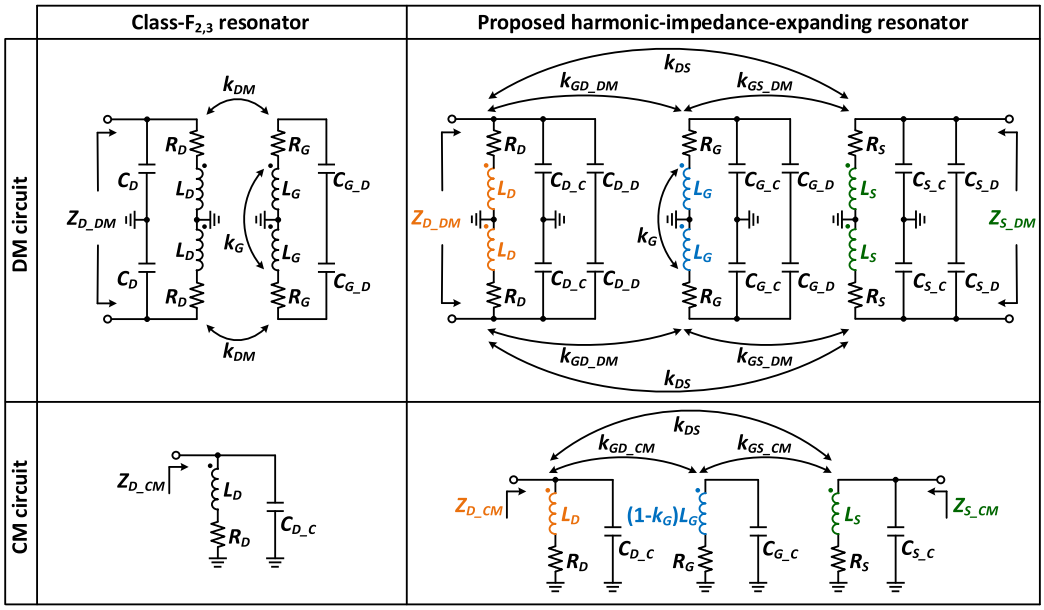


Fig. 9. Circuit models of the class-$F_{2,3}$ resonator and the proposed harmonic-impedance-expanding resonator in DM and CM.

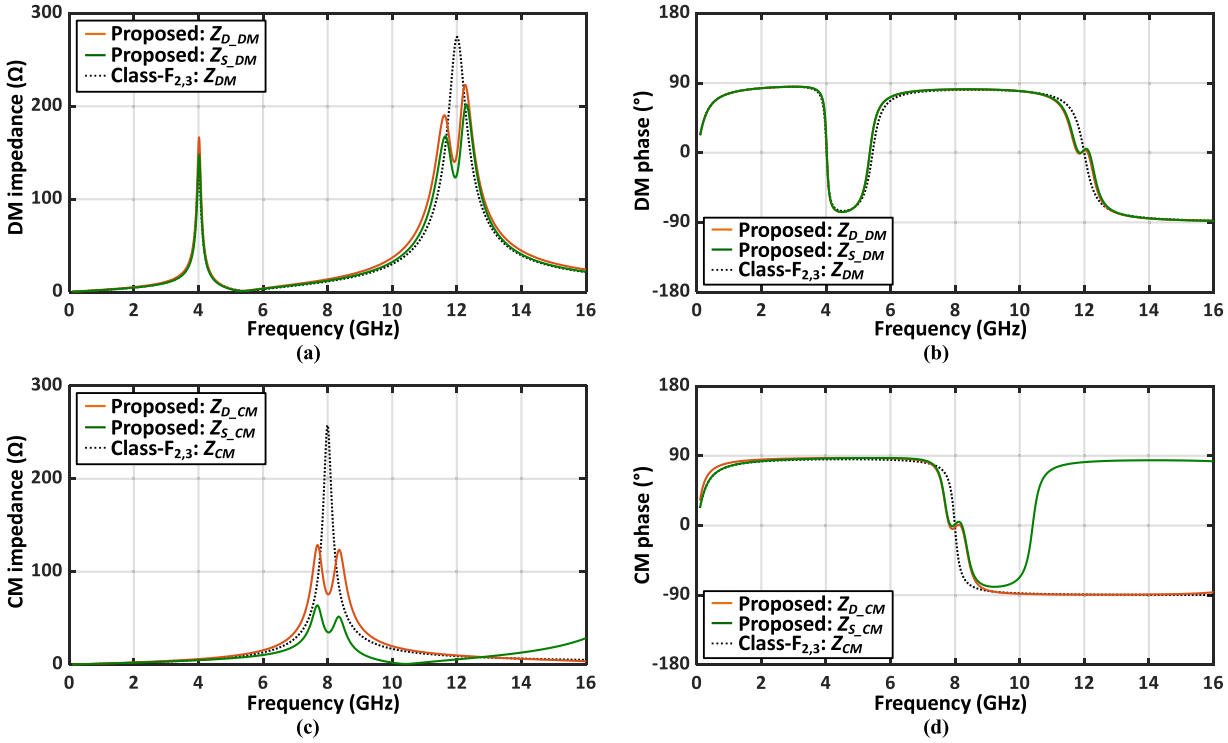


Fig. 10. (a) DM impedance, (b) DM phase response, (c) CM impedance, and (d) CM phase response of the class-$F_{2,3}$ and proposed resonators.

of resonances. Since the oscillation frequency is tuned by both the primary and secondary capacitors, it is not easy to meet the strict requirement of resonances' ratio during the operation frequency, which will lead to the fluctuation of phase noise with the tuning of frequency. To overcome this challenge, one solution is to reduce the quality factors at the resonances. Then, the sensitivity of this method to the ratio of resonances can be reduced. However, the low quality factor also leads to low impedances at harmonic frequencies and thus reduces the effect of harmonic shaping and FoM of the oscillator.

In the proposed harmonic-impedance-expanding technique, multiple resonances are introduced around the harmonic frequencies. The distributed-swing-boosting transformer for the multi-core topology can be equivalent to multiple single-core transformers combined together. Although the single-core type has lower quality factor as discussed in Section II, it is helpful for the analysis of resonances due to the low complexity.

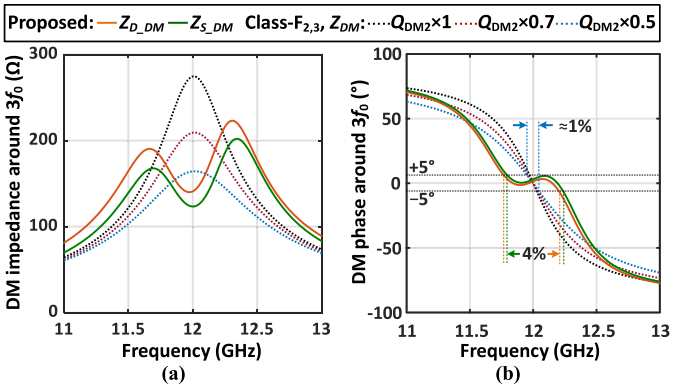


Fig. 11. Simulated DM (a) impedances and (b) phase responses around third harmonic.

Fig. 8 shows the equivalent transformer excited in DM and CM input signal. In DM excitation, the currents in the three types of inductors are in the same direction. The induced currents add constructively, which leads to the strong couplings of k_{GS} and k_{GD} (i.e., larger than 0.7). The coupling between L_D and L_S is also introduced. In CM excitation, the currents in L_D and L_S are still in the same direction. However, the directions of currents in the three winds of L_G are different. Differing from the class-$F_{2,3}$ type, where the induced currents in the two winds of L_G are almost canceled by each other, the currents in the three winds of L_G cannot be fully canceled in the proposed transformer. Thus, there are still weak CM couplings of k_{GS} and k_{GD}. Fig. 9 compares the circuit models of the class-$F_{2,3}$ resonator and the proposed harmonic-impedance-expanding resonator in DM and CM. For the class-$F_{2,3}$ resonator, the primary winding of the transformer connects a pair of single-ended capacitors, whereas the secondary winding connects the differential capacitors. In CM, due to the negligible coupling between the two windings, the secondary winding is equivalent to be removed. In the proposed resonator, all the windings of the transformer have single-ended capacitors and differential capacitors. Z_D and Z_S are the input impedances seen from the drain and source. In both modes, the couplings between the three windings are non-negligible. $k_{\mathrm{GD\_DM}}$, $k_{\mathrm{GD\_CM}}$, $k_{\mathrm{GS\_DM}}$, and $k_{\mathrm{GS\_CM}}$ are used to describe the different coupling of k_{GD} and k_{GS} in DM and CM, respectively. The self-coupling of L_G leads to a high inductance in DM and low inductance in CM. The expressions of each impedance are given in the Appendix.

Fig. 10 shows the impedances and phase responses of the class-$F_{2,3}$ resonator and the proposed harmonic-impedance-expanding resonator in DM and CM. For both types of resonators, the fundamental DM resonances are set at 4 GHz. To simplify the comparison, the quality factors of all the inductors are set to 16 at 4 GHz. In DM, due to the increased order of the resonator, two resonances are obtained around the third harmonic to expand the high-impedance frequency range. The flattened phase response with a small ripple is obtained to satisfy the phase condition of harmonic shaping around 0° over a wider frequency range. In CM, due to the non-negligible L_G, the high-order resonator is still obtained. Two resonances are obtained around the second harmonic.

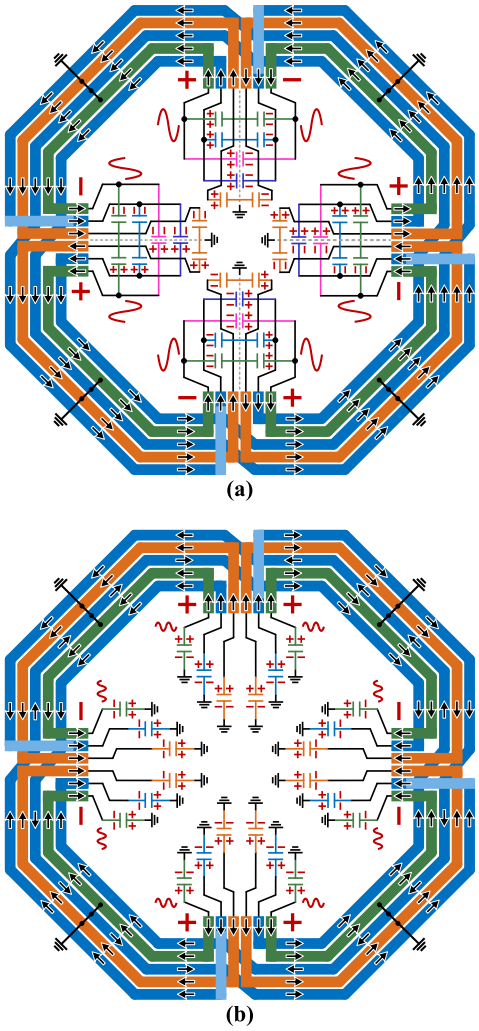


Fig. 12. Quad-core distributed-swing-boosting harmonic-impedance-expanding resonator in (a) DM and (b) CM.

The CM phase response around 0° is expanded to satisfy the requirement of reducing the flicker noise up-conversion. In the proposed architecture, the harmonic-shaping effect is mainly introduced by the DM third harmonic. Due to the coupling between L_D and L_S, although the high-impedance range is expanded, the peak of the impedance is reduced. In order to make a comparison considering both of the harmonic-shaping effect and effective high-impedance frequency range, the class-$F_{2,3}$ resonator with different quality factors at the second DM resonance (i.e., Q_{DM2}) is set as the reference. Fig. 11 compares the simulated DM impedances and phase responses around the third harmonic. For the conventional type, once halving Q_{DM2}, the peak impedance is reduced to lower than the proposed type. The frequency range of phase response smaller than ±5° is only about 1%. For the proposed type, the frequency range of both $\angle Z_{D\_\mathrm{DM}}$ and $\angle Z_{S\_\mathrm{DM}}$ smaller than ±5° is 4%, which is four times the frequency range of conventional type. Accordingly, the proposed harmonic-impedance-expanding resonator can keep the impedance around the third harmonic at a high level and effectively extend the frequency range of near-zero phase response.

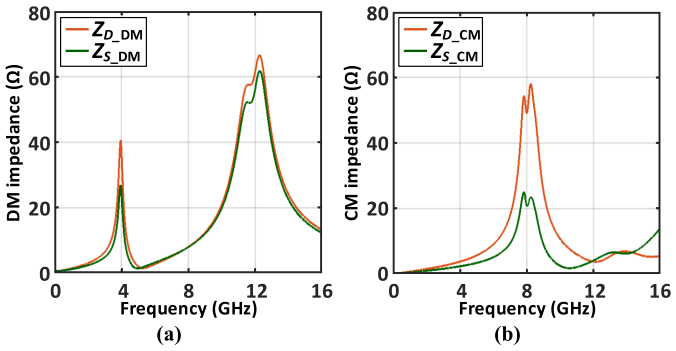


Fig. 13. Simulated (a) DM and (b) CM impedances of quad-core harmonic-impedance-expanding resonator.

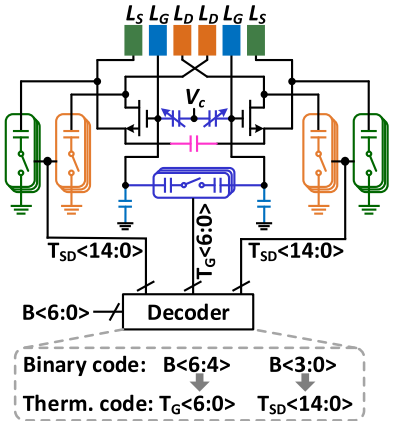


Fig. 14. Circuit implementation of the proposed oscillator.

B. Quad-Core Harmonic-Impedance-Expanding Resonator

Based on the analysis of single-core resonator, the quad-core harmonic-impedance-expanding resonator is proposed. Fig. 12(a) and (b) shows the quad-core harmonic-impedance-expanding resonator in DM and CM, respectively. In DM excitation, both the single-ended and differential capacitors can be seen from the port, as shown in Fig. 12(a). The adjacent cores are in the same phase. The currents in the three kinds of inductors are in the same direction. In CM excitation, only the single-ended capacitors are effective, as shown in Fig. 12(b). In this mode, to keep the symmetry of currents seen from each port, the phase in each core is in-phase, while the adjacent cores are out-of-phase. It is notable that, considering the harmonic currents of practical devices, the second harmonic current cannot keep out-of-phase. Then, the CM currents of adjacent cores will be canceled by each other and lead to the deviation between simulation and analysis. By adjusting the values of single-ended capacitors, the CM response can be calibrated. The simulated impedances in DM and CM based on the EM simulation of the transformer's layout are shown in Fig. 13. The simulated inductances of L_G, L_D, and L_S are 1080, 210, and 180 pH, respectively. The corresponding quality factors at 4 GHz are 25, 12, and 11, respectively. The frequency responses of the quad-core resonator still match the analysis of single-core type.

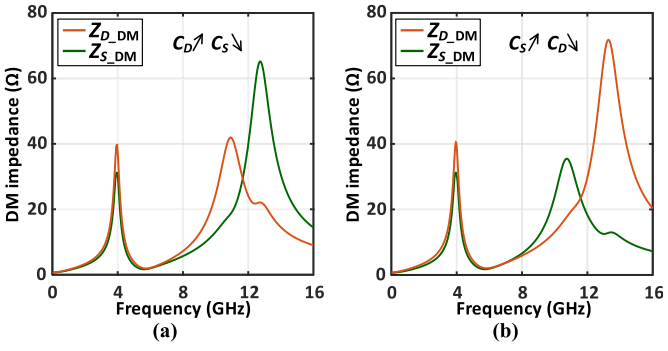


Fig. 15. Simulated DM impedances for (a) large C_D small C_S and (b) large C_S small C_D.

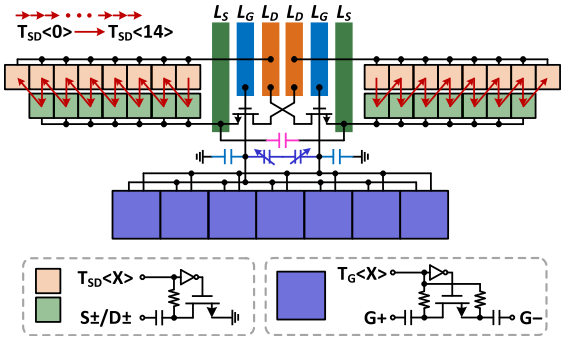


Fig. 16. Frequency tuning and layout plan of the capacitor banks.

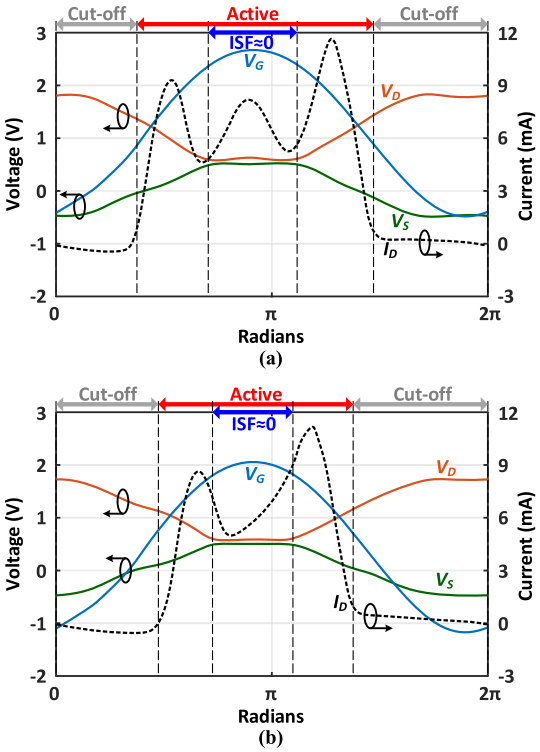


Fig. 17. Simulated voltage and current when V_b is (a) 1 and (b) 0.5.

C. Circuit Design

The circuit implementation of the proposed oscillator is shown in Fig. 14. The core transistors are 25× (5/0.27 μm) thick-oxide devices that withstand the large swing without breakdown and reliability issue. Seven differential switch

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ARTS

	This work	JSSC'17 [8]	TCAS-I'16 [18]	JSSC'16 [7]	JSSC'17 [19]	ISSCC'18 [6]	ISSCC'18 [20]	JSSC'19 [31]	ISSCC'20 [14]**
Technology	**40nm CMOS**	28nm CMOS	65nm CMOS	40nm CMOS	55nm BiCMOS	65nm CMOS	130nm BiCMOS	130nm CMOS	40nm CMOS
Supply voltage (V)	**1.1**	0.7	2.15	1	1.2	0.6	3	1.2	0.5
Freq. range (GHz)	**3.09 to 4.04**	4.7 to 5.4	4.07 to 4.91	5.4 to 7	17.4 to 20.3	3.49 to 4.51	13 to 15	2.05 to 2.47	4.1 to 5
Tuning range	**26.6%**	13.8%	18.6%	25%	15.3%	25.5%	14.3%	18.6%	19.8%
PN@1MHz (dBc/Hz)	**–132.18 to –138.92**	–119	–136*	–126.7	–118.5	–122.8	–124	–130	-123.1
PN@1MHz (dBc/Hz) Normalized to 6 GHz	**–128.7 to –133.2**	–116.9	–132.5	–125.8	–129	–120	–131.9	–122.3	-120.6
$1/f^3$ corner (kHz)	**100 to 130**	160 to 300*	130 to 300	60 to 130	800*	100 to 300	40*	32 to 60	130
Power (mW)	**20.9 to 23.1**	0.5	126.8	12	43.2	1.2	72	2.6	4.3
FoM (dBc/Hz)	**191.1 to 195.1**	195.5	187.2	191.4	188.7	195.6	189	195.2	190
FoM_T (dBc/Hz)	**199.6 to 203.6**	198.3	192.6	197.4	192.4	203.7	192.1	200.6	195.9
VCO core	**Quad-core**	Single-core	Dual-core	Single-core	Quad-core	Single-core	Quad-core	Single-core	Single-core
Core size (mm^2)	**0.36**	0.18	0.37	0.13	0.52	0.22	1	0.36	0.14

*Estimated from figures ** Data at 300K (27°C)

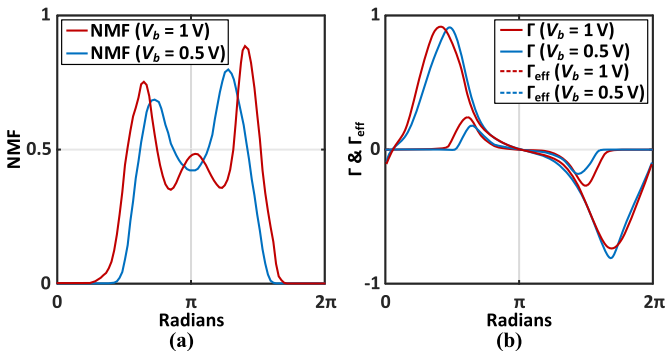


Fig. 18. Simulated (a) NMF and (b) ISF and effective ISF.

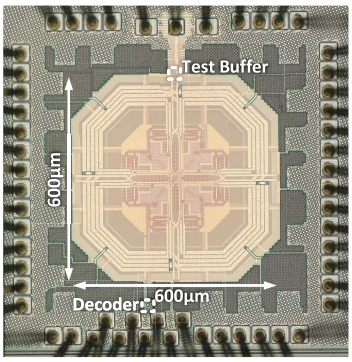


Fig. 20. Chip micrograph.

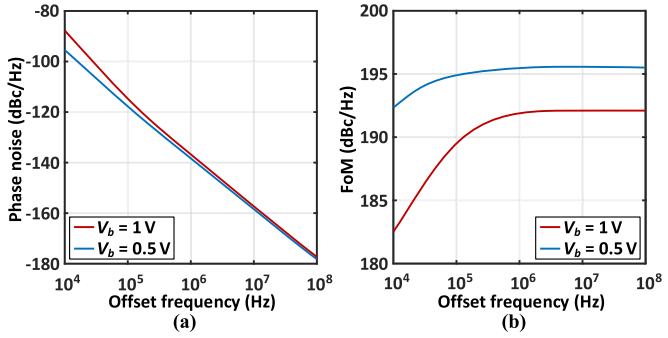


Fig. 19. Simulated (a) phase noise and (b) FoM.

capacitors (controlled by 7-bit thermometer code, $T_G\langle 6{:}0\rangle$) achieve the coarse frequency tuning. The middle frequency tuning is achieved by eight pairs of single-ended switch capacitors connected to the drain and seven pairs of single-ended switch capacitors connected to the source. The drain and source switch capacitors are controlled by a unified 15-bit thermometer code $T_{SD}\langle 14{:}0\rangle$. Then, continuous frequency tuning is achieved by the varactors connected to the gate. Since the quad-core distributed-coupling transformer is large enough compared to the single-core type, the active devices and capacitor banks are placed inside the transformer to reduce the chip size. The distance between the inside elements and the transformer is larger than 60 μm to minimize the influence on the quality factor. The supply, bias, and tail current are drawn from the center taps of the transformer and connected to the outside. For the CM operation of single-ended capacitors, there is a small amount of current that needs to return. Therefore, eight strips of mesh ground with 20-μm width are used to support the current flowing to the outside of the passive. Then, the current returns to the supply through the on-chip decoupling capacitor. It is notable that the two resonances around the third harmonic are determined by the drain capacitor and source capacitor. When the drain capacitor and source capacitor are not tuned together, the resonances around the harmonic will separate, as shown in Fig. 15. Then, the condition of harmonic-impedance expanding is hard to satisfy. To overcome this challenge, the frequency tuning

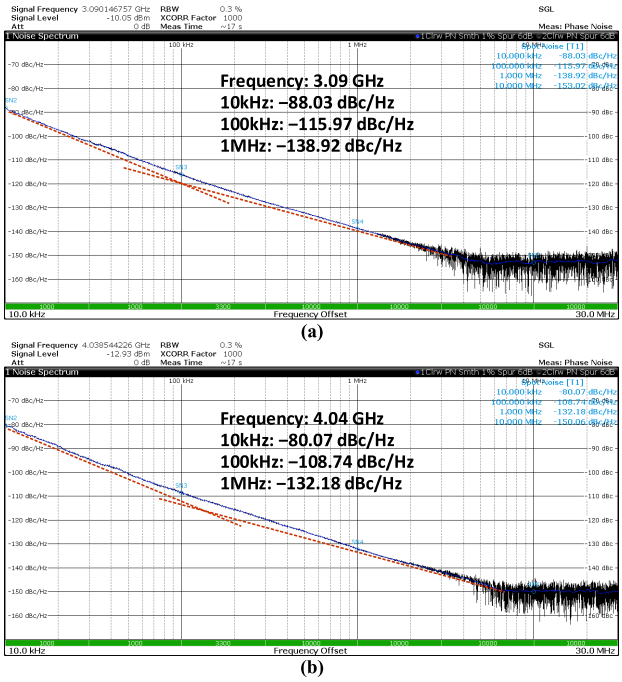


Fig. 21. Measured phase noise at (a) 3.09 and (b) 4.04 GHz.

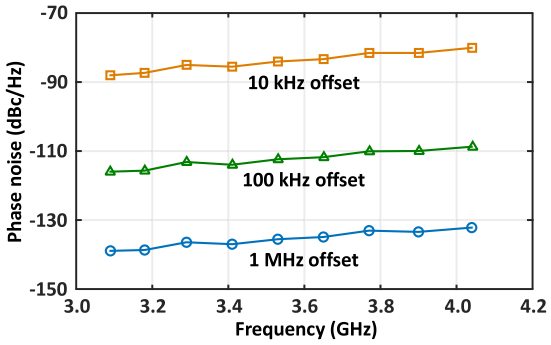


Fig. 22. Measured phase noise with the change of frequency.

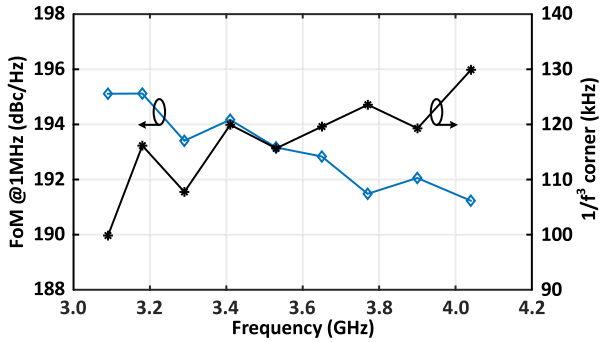


Fig. 23. Measured 1-MHz FoM and $1/f^3$ corner.

and layout plan of the capacitor banks is shown in Fig. 16. With increasing control code T_{SD}, the two banks of drain and source capacitors are turned off in sequence to ensure the resonances around harmonic moving simultaneously along with the fundamental frequency.

D. Phase Noise

As proved in other harmonic-shaping oscillators, the harmonic-shaped square-like waveform can improve the phase noise performance and FoM. In the proposed oscillator, the harmonic shaping leads to a flat span of V_{DS} around 0 V, where the phase of the waveform is insensitive to the injected noise and leads to the ISF close to zero. Then, the time proportion when the noise current of MOSFET contributes to the phase noise is decreased within a period. Note that V_S is in-phase with V_G and out-of-phase with V_D. This will lead to more time when the MOSFET is turned on. To further improve the phase noise performance, the bias of the oscillator is optimized under the startup condition. Fig. 17(a) and (b) shows the simulated voltage and current when bias voltage (i.e., V_b) is 1 and 0.5, respectively. With V_b reduced from 1 to 0.5, the conduction angle of the MOSFET is obviously reduced [27], [28], while the startup condition within the operation frequency is satisfied. Then, the time when the MOSFET is turned on is compressed, while the time for near-zero ISF is slightly reduced. It is notable that, due to the unavoidable imbalance of the layout, there is still a slight asymmetry of the waveform's rise and fall, which will lead to the flicker noise up-conversion. The reduced conduction angle can also alleviate this problem by decreasing the effective part of the asymmetric waveform. To further investigate the effective noise factor of the MOSFET, the effective ISF is simulated, which is defined as $\Gamma_{\mathrm{eff}}(\omega_0 t) = \Gamma(\omega_0 t) \cdot \alpha(\omega_0 t)$. Here, $\Gamma(\omega_0 t)$ and $\alpha(\omega_0 t)$ are the functions of ISF and noise modulation function (NMF), respectively. The simulated NMF, ISF, and effective ISF are shown in Fig. 18, where the ISF is obtained using the perturbation projection vector method [29], [30]. For the low-bias condition, with the narrowed NMF, the rms value of effective ISF is reduced within a period. The symmetry of effective ISF is improved, which means a lower dc value of effective ISF and suppressed flicker noise up-conversion. Fig. 19(a) shows the simulated phase noise under different biases, which exhibits an obvious reduction in the $1/f^3$ region. Meanwhile, with the reduced power consumption, FoM is improved in both $1/f^3$ and $1/f^2$ regions, as shown in Fig. 19(b).

IV. Fabrication and Measurements

The proposed multi-core oscillator is designed and fabricated with a 40-nm CMOS technology. Fig. 20 shows the micrograph of the chip. The core size is 600 μm $\times$ 600 μm. A resistive loaded buffer connects one side of the drain inductor to the output, while dummy buffers are used to balance the parasitics of each side. The current consumption of the oscillator is 19–21 mA under a supply voltage of 1.1 V. The frequency and phase noise are measured by R&S FSW43 and FSWP50, respectively. The results exhibit a continuous 26.6% tuning range from 3.09 to 4.04 GHz. The measured K_{VCO} is 13–28 MHz/V. Fig. 21 shows the measured phase noise. At 3.09 and 4.04 GHz, the 100-kHz offset phase noises are −115.97 and −108.74 dBc/Hz, while the 1-MHz offset phase noises are −138.92 and −132.18 dBc/Hz, respectively. The phase noise at 10-MHz offset is limited

by the test buffer's noise floor. The measured phase noise at different frequency settings is shown in Fig. 22. The FoM at 1-MHz offset is between 191.1 and 195.1 dBc/Hz, as shown in Fig. 23. The estimated $1/f^3$ phase noise corner is 100–130 kHz.

The measured results are summarized and compared with the state of the arts in Table I. The proposed oscillator exhibits obvious advantages in the phase noise performance and FoM. The normalized phase noise is lower than other multi-core oscillators, while the FoM is comparable to state-of-the-art single-core oscillators. Thus, high performance and low power consumption are both ensured. Although operating at lower frequency, the chip size of the proposed oscillator is much smaller than other published quad-core oscillators [19], [20]. Compared with dual-core oscillator [18], it still has an advantage on chip size.

V. Conclusion

A distributed-swing-boosting and harmonic-impedance-expanding multi-core oscillator is proposed in this article. The distributed-coupling multi-core topology is investigated to reduce the chip size and determine the current direction of each core without resistor in center taps. Thus, the NMOS-only or PMOS-only couple pair can be adopted. Based on the distributed-coupling multi-core topology, the harmonic-impedance-expanding technique is developed, where the CM resonance around the second harmonic and the DM resonances around the third harmonic are utilized to suppress the flicker noise up-conversion and reduce the ISF. Moreover, the dual-resonance response expands the high-impedance frequency ranges around the harmonics. Thus, the robustness of the performance with the tuning of frequency is improved. Fabricated in a 40-nm CMOS technology, the proposed oscillator achieves low phase noise and high FoM simultaneously. The chip size of the quad-core oscillator is compact even compared to dual-core oscillator.

Appendix

The expressions of Z_{D_DM}, Z_{S_DM}, Z_{D_CM}, and Z_{S_CM} in Fig. 9 are calculated as (11)–(14), where $M_{\mathrm{GD}\_D} = k_{\mathrm{GD\_DM}}(L_G L_D)^{1/2}$, $M_{\mathrm{GS}\_D} = k_{\mathrm{GS\_DM}}(L_G L_S)^{1/2}$, $M_{\mathrm{DS}} = k_{\mathrm{DS}}(L_D L_S)^{1/2}$, $M_{\mathrm{GD}\_C} = k_{\mathrm{GD\_CM}}(L_G L_D)^{1/2}$, and $M_{\mathrm{GS}\_C} = k_{\mathrm{GS\_CM}}(L_G L_S)^{1/2}$. Meanwhile, for simplicity, the stand-alone peak impedances in (11)–(14), as shown at the bottom of the page, are expressed as

$$Z_{\mathrm{LC}\_D\_D} = R_D + sL_D + 1/s\big(C_{D\_C} + C_{D\_D}\big) \tag{15}$$

$$Z_{\mathrm{LC}\_S\_D} = R_S + sL_S + 1/s\big(C_{S\_C} + C_{S\_D}\big) \tag{16}$$

$$Z_{\mathrm{LC}\_G\_D} = R_G + sL_G(1+k_G) + 1/s\big(C_{G\_C} + C_{G\_D}\big) \tag{17}$$

$$Z_{LC\_D\_C} = R_D + sL_D + 1/sC_{D\_C} \tag{18}$$

$$Z_{\mathrm{LC}\_S\_C} = R_S + sL_S + 1/sC_{S\_C} \tag{19}$$

$$Z_{\mathrm{LC}\_G\_C} = R_G + sL_G(1-k_G) + 1/sC_{G\_C}. \tag{20}$$

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$$Z_{D\_\mathrm{DM}} = \frac{\frac{2}{s(C_{D\_C}+C_{D\_D})}\big[(sL_D+R_D)\big(s^2M_{\mathrm{GS}\_D}^2 - Z_{\mathrm{LC}\_G\_D}Z_{\mathrm{LC}\_S\_D}\big) + s^2\big(M_{\mathrm{GD}\_D}^2 Z_{LC\_S\_D} + M_{DS}^2 Z_{LC\_G\_D} - 2sM_{\mathrm{GD}\_D}M_{\mathrm{GD}\_D}M_{\mathrm{DS}}\big)\big]}{s^2\big[M_{\mathrm{GS}\_D}^2 Z_{\mathrm{LC}\_D\_D} + M_{\mathrm{GD}\_D}^2 Z_{\mathrm{LC}\_S\_D} + M_{\mathrm{DS}}^2 Z_{\mathrm{LC}\_S\_D} - 2sM_{\mathrm{GD}\_D}M_{\mathrm{GD}\_D}M_{\mathrm{DS}}\big] - Z_{\mathrm{LC}\_D\_D}Z_{\mathrm{LC}\_S\_D}Z_{\mathrm{LC}\_G\_D}} \tag{11}$$

$$Z_{S\_\mathrm{DM}} = \frac{\frac{2}{s(C_{S\_C}+C_{S\_D})}\big[(sL_S+R_S)\big(s^2M_{\mathrm{GD}\_D}^2 - Z_{\mathrm{LC}\_G\_D}Z_{\mathrm{LC}\_D\_D}\big) + s^2\big(M_{\mathrm{GS}\_D}^2 Z_{LC\_D\_D} + M_{\mathrm{DS}}^2 Z_{LC\_G\_D} - 2sM_{\mathrm{GD}\_D}M_{\mathrm{GD}\_D}M_{\mathrm{DS}}\big)\big]}{s^2\big[M_{\mathrm{GS}\_D}^2 Z_{\mathrm{LC}\_D\_D} + M_{\mathrm{GD}\_D}^2 Z_{\mathrm{LC}\_S\_D} + M_{\mathrm{DS}}^2 Z_{\mathrm{LC}\_S\_D} - 2sM_{\mathrm{GD}\_D}M_{\mathrm{GD}\_D}M_{\mathrm{DS}}\big] - Z_{\mathrm{LC}\_D\_D}Z_{\mathrm{LC}\_S\_D}Z_{\mathrm{LC}\_G\_D}} \tag{12}$$

$$Z_{D\_\mathrm{CM}} = \frac{\frac{1}{sC_{D\_C}}\big[(sL_D+R_D)\big(s^2M_{\mathrm{GS}\_C}^2 - Z_{\mathrm{LC}\_G\_C}Z_{\mathrm{LC}\_S\_C}\big) + s^2\big(M_{\mathrm{GD}\_C}^2 Z_{LC\_S\_C} + M_{\mathrm{DS}}^2 Z_{LC\_G\_C} - 2sM_{\mathrm{GD}\_C}M_{\mathrm{GD}\_C}M_{\mathrm{DS}}\big)\big]}{s^2\big[M_{\mathrm{GS}\_C}^2 Z_{\mathrm{LC}\_D\_C} + M_{\mathrm{GD}\_C}^2 Z_{\mathrm{LC}\_S\_C} + M_{\mathrm{DS}}^2 Z_{\mathrm{LC}\_S\_C} - 2sM_{\mathrm{GD}\_C}M_{\mathrm{GD}\_C}M_{\mathrm{DS}}\big] - Z_{\mathrm{LC}\_D\_C}Z_{\mathrm{LC}\_S\_C}Z_{\mathrm{LC}\_G\_C}} \tag{13}$$

$$Z_{S\_\mathrm{CM}} = \frac{\frac{1}{sC_{S\_C}}\big[(sL_S+R_S)\big(s^2M_{\mathrm{GD}\_C}^2 - Z_{\mathrm{LC}\_G\_C}Z_{\mathrm{LC}\_D\_C}\big) + s^2\big(M_{\mathrm{GS}\_C}^2 Z_{LC\_D\_C} + M_{\mathrm{DS}}^2 Z_{LC\_G\_C} - 2sM_{\mathrm{GD}\_C}M_{\mathrm{GD}\_C}M_{\mathrm{DS}}\big)\big]}{s^2\big[M_{\mathrm{GS}\_C}^2 Z_{\mathrm{LC}\_D\_C} + M_{\mathrm{GD}\_C}^2 Z_{\mathrm{LC}\_S\_C} + M_{\mathrm{DS}}^2 Z_{\mathrm{LC}\_S\_C} - 2sM_{\mathrm{GD}\_C}M_{\mathrm{GD}\_C}M_{\mathrm{DS}}\big] - Z_{\mathrm{LC}\_D\_C}Z_{\mathrm{LC}\_S\_C}Z_{\mathrm{LC}\_G\_C}} \tag{14}$$

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