A 32-kHz-Reference 2.4-GHz Fractional-*N* Oversampling PLL With 200-kHz Loop Bandwidth

Junjun Qiu, *Graduate Student Member, IEEE*, Zheng Sun, *Member, IEEE*, Bangan Liu, *Member, IEEE*, Wenqian Wang, *Student Member, IEEE*, Dingxin Xu, *Graduate Student Member, IEEE*, Hans Herdian, *Member, IEEE*, Hongye Huang, *Member, IEEE*, Yuncheng Zhang, *Graduate Student Member, IEEE*, Yun Wang, *Member, IEEE*, Jian Pang, *Member, IEEE*, Hanli Liu, *Member, IEEE*, Masaya Miyahara, *Member, IEEE*, Atsushi Shirane, *Member, IEEE*, and Kenichi Okada, *Senior Member, IEEE*

***Abstract*— In this article, a mixed–signal, 32-kHz reference-based 2.4-GHz fractional-*N* over-sampling phase-locked loop (OSPLL) is proposed. Different from the conventional 1× sampling PLL, which only uses zero-crossing timing information of the reference signal, the proposed OSPLL fully utilizes both the voltage and timing domain information of the reference signal and realizes oversampling ratio (OSR) times phase detection (PD) in one reference cycle. The proposed OSPLL employs the digital-to-analog converter (DAC) to construct the reference-like feedback signal in the voltage domain and utilizes the digital-to-time converter (DTC) to improve PD resolution in the time domain. The adaptive lookup table (LuT)-based calibration is proposed to generate the correct information for DAC and DTC control. A clocked passive comparator works as a bang-bang phase detector (BBPD) for the PLL control and LuTs' construction. The co-design of low-noise analog circuits and digital calibrations enables good jitter and spur performance. The proposed OSPLL is fabricated in 65-nm CMOS technology, with the core area of 0.58 mm^2, and the power consumption is 4.97 mW with a 1-V power supply. It achieves 5.79-ps root-mean-square (rms) jitter in fractional-*N* modes with the loop-bandwidth (BW_{loop}) of 200 kHz, corresponding to the figures of merit (FoMs) of −217.8 dB. The measured fractional spur is less than −36 dBc, and the reference spur is −78 dBc, respectively.**

***Index Terms*— 32 kHz, bang-bang phase detector (BBPD), BW_{loop}, comparator (CMP), constant-slope digital-to-time converter (DTC), digital-to-analog converter (DAC), fractional-*N*, frequency synthesizer, inductor–capacitor (LC) oscillator (DCO), jitter, mixed analog-digital circuit, over-sampling phase-locked loop (OSPLL), phase noise, reference construction.**

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Junjun Qiu, Zheng Sun, Wenqian Wang, Dingxin Xu, Hans Herdian, Hongye Huang, Yuncheng Zhang, Yun Wang, Jian Pang, Atsushi Shirane, and Kenichi Okada are with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo 152-8550, Japan (e-mail: qiu@ssc.pe.titech.ac.jp).

Bangan Liu is with Qualcomm Inc., San Diego, CA 92121 USA.

Hanli Liu is with Broadcom Inc., San Jose, CA 95134 USA.

Masaya Miyahara is with High Energy Accelerator Research Organization, Ibaraki 305-0801, Japan.

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I. Introduction

THE low-jitter phase-locked loop (PLL) is necessarily applied in the analog-to-digital converter (ADC), baseband circuit, and high-frequency transceiver. There are many types of research about PLL in analog, digital, and mixed-signal ways. Analog PLL [1], [2], usually implemented with charge pump architecture, is free of quantization noise while sensitive to the PVT variations. Digital PLL [3], [4] is more attractive recently for its high PVT immunity and design portability. However, the inherent limitation caused by the gate delay barriers the further improvement of the phase noise. This calls for the demand of the mixed-signal PLL [5], [6] design with the advantage of both analog PLL and digital PLL for a better jitter performance and environment noise immunity. For a given PLL structure, the optimal BW_{loop} is essential to balance the in-band and out-of-band phase noise contributions and minimize the jitter [7], [8]. However, in the actual case, the reference frequency (f_{REF}) limits the achievable BW_{loop}. The jitter contribution of PLL's output can be divided into the in-band part and the out-of-band part. The in-band phase noise mainly contributes from the quantization noise and thermal noise of PD, while the digital-controlled-oscillator (DCO) noise largely dominates the out-of-band phase noise. With the scaled CMOS technology, the in-band phase noise can be suppressed to be lower than −100 dBc/Hz. The corresponding optimal BW_{loop} can be several MHz. This is derived with the assumption that the oscillator holds less than −100-dBc/Hz phase noise at 1-MHz offset and less than 2.5-mW power consumption, which is the regular design in the literature [9], while, on the other hand, the stability constraint of PLL restricts the achievable BW_{loop}. This limitation makes it difficult to realize a low-jitter frequency synthesizer with a low f_{REF} source [2]. Thus, a high f_{REF} source is more popular than a lower one [10]–[12] in ultra-low-jitter PLL applications.

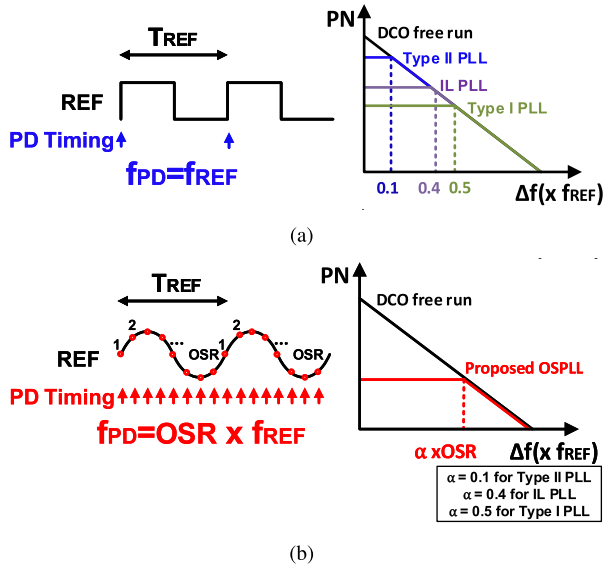

Fig. 1. Principle comparison between (a) conventional PLL and (b) proposed oversampling PLL.

However, the cost of the high f_{REF} source is much higher than the latter. This may create a barrier to the mass adoption of wireless devices. Under this circumstance, it poses a demand to seek a method to break the BW_{loop} limitation caused by f_{REF} to realize good jitter performance even with a low f_{REF}.

Among the low f_{REF} sources, the 32-kHz clock is most commonly implemented in Internet-of-Things (IoT) devices as a real-time clock (RTC). Due to its low frequency, the power consumption itself can be negligible [13]. If the radio frequency (RF) transmission can be realized with a 32-kHz reference, the IoT devices will only need a 32-kHz reference source, instead of multi-reference sources [14]. With the target IoT application of 2.4 GHz with the 32-kHz reference, the comparison of conventional PLL architectures is firstly considered and discussed in the following.

The different achievable BW_{loop} with a different PLL architecture is shown in Fig. 1(a). As the most popular PLL architecture in the literature, the type II PLL can force the phase error near zero and achieve a wide acquisition range. As aforementioned, its BW_{loop} can be limited to be less than 3 kHz with 32-kHz reference. This narrow bandwidth will lead the DCO phase noise to deteriorate the output jitter performance [15]. The type I PLL [11], [16] or the injection lock PLL [17], [18], which can realize 40% or 50% f_{REF} BW_{loop} in theory, face the same problem of limited BW_{loop}. The frequency multiplier, such as a doubler [4] or a quadrupler [19], can be adopted to improve the f_{REF}. However, a higher time multiplier is difficult to implement due to the complex calibration required to correct the reference duty cycle [6]. To further improve the frequency of PD operation, the cascaded PLL [20] proves efficient to boost the low f_{REF} to a higher one and use the latter for the final clock generation. However, the final noise performance is still influenced by the first-stage PLL. To get a good jitter performance, the phase noise of first-stage's DCO needs to be carefully suppressed, which suffers from the tradeoff with the power consumption.

For the above conventional PLLs, the reason that caused the limitation of the achievable BW_{loop} is typically related to the frequency of PD and the gain of PLL blocks. The latter is proportional to PD's voltage-to-phase gain, DCO's frequency-to-voltage gain, the loop filter's gain, and inversely proportional to the division ratio from f_{OUT} to f_{REF}. Among those block gain settings, the PD's gain is sensitive to other blocks' noise and usually dominates the performance of achievable BW_{loop} for a given PD frequency. Clock rising edge timing comparison by the digital bang-bang phase detector (BBPD) [10], [21] or multi-bit TDC [22], [23] attracts attention in the literature for their simple implementation and good jitter performance, as illustrated in the left-hand side of Fig. 1(a). To further improve the PD gain, the sampling mixed-signal PDs are in introduced by Wu *et al.* [6], Sharma and Krishnaswamy [16], Gao *et al.* [24], Liao and Dai [25], and Liao *et al.* [26]. These works either use the feedback clock to sample the slope-controlled reference signal or utilize the reference clock to sample the slope-controlled feedback signal. However, the PD frequency is limited to be equal to f_{REF}, which basically constraints the achievable BW_{loop}.

With the concerns mentioned above, an over-sampling PD is needed, which directly samples the reference signal (waveform) for oversampling ratio (OSR) times in one reference cycle, as shown on the right-hand side of Fig. 1(b). In this manner, the achievable BW_{loop} can be extended to OSR time wider than conventional PLLs. With the assistance of a low-noise PD design, the wider BW_{loop} effectively suppresses the out-of-band phase noise and improves overall jitter performance. To realize over-sampled PD, Seol *et al.* [27], [28] employ OSR comparators (CMPs) as the multi-phase PDs operating at f_{REF}. However, the fixed division ratio makes it difficult for the fractional-N operation.

To solve the above issues, a 32-kHz reference, 2.4-GHz fractional-N over-sampling PLL (OSPLL) is presented in this article, with achieving 200-kHz BW_{loop}. The new oversampling PD is proposed with one CMP needed. The compensation method in both voltage and time domains is realized by a digital-to-analog converter (DAC) and a digital-to-time converter (DTC), respectively. The robust lookup table (LuT)-based calibration is practical to construct the reference information and improve the jitter performance. The proposed architecture applies to the fractional-N operation.

The following of this article is organized as follows. In Section II, the proposed OSPLL operation is described, as well as the noise analysis and design considerations. The detailed architecture of the proposed OSPLL and building blocks are presented in Section III. The measurement results are shown in Section IV. Finally, conclusions are drawn in Section V.

II. Proposed OSPLL

A. OSPLL General Architecture

Before discussing the proposed OSPLL architecture, the possible ways to realize over-sampled phase detection (PD) are considered. The basic idea of the OSPLL is to utilize the voltage information of reference to represent the timing.

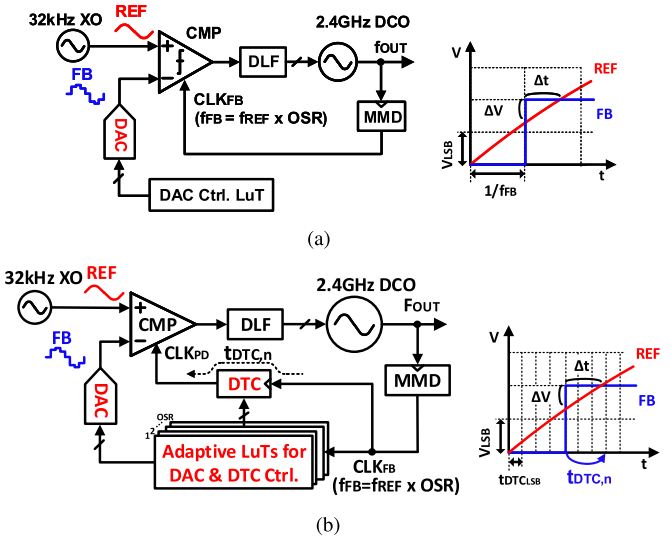

Fig. 2. Possible way for OSPLL realization (a) only voltage domain compensation and (b) proposed OSPLL with voltage, time domain compensation, and adaptive calibration.

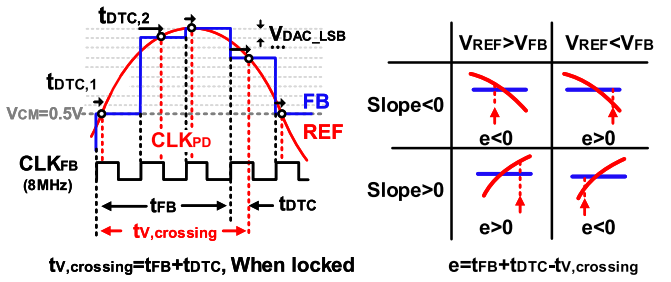

Fig. 3. Proposed oversampling PD operation.

One possible way is to digitalize the reference by a high-resolution continuous-time ADC first. In that case, the PD can be conducted in the all-digital domain. However, the reference signal will be polluted by the quantization noise in this digitalization process, and the high power cost of ADC will disadvantage the design. The reference signal is directly connected to the PD in the analog domain in this design to reduce the introduced reference-path noise, as shown in Fig. 2(a). By comparing the voltage difference between reference and feedback signal at $\mathrm{CLK_{FB}}$, which is generated by the multi-modulus divider (MMD), the time error information can be read out to control the PLL operation. However, the resolution of DAC will constraint the achievable PD accuracy. After loop settling, the toggles of $\mathrm{CLK_{FB}}$ between two LSBs of a 10-bit DAC will lead to a larger than 9-ns time error based on (1), which will deteriorate the output jitter performance

$$\Delta t \approx \frac{\Delta V}{SS_{\mathrm{REF}}} \tag{1}$$

$$SS_{\mathrm{REF}} = 2\pi f_{\mathrm{REF}} A_{\mathrm{REF}} \cos(2\pi f_{\mathrm{REF}} t) \tag{2}$$

where ΔV is quantization error and Δt is the corresponding time error, as shown in Fig. 2(a). SS_{REF} is the reference slope at sampling timing t, and A_{REF} is the reference amplitude.

To compensate for the time error caused by the DAC's resolution and further improve the PD resolution, a time-domain compensation realized by DTC can be adopted, as shown in Fig. 2(b). Since DTC resolution can be designed much higher than the DAC-related time step, the quantization limitation caused by DAC is broken.

On the other hand, the control for DAC and DTC is impossible to preset correctly for the nonlinear propagation that reference may go through in the actual environment. Any wrong set of DAC or DTC control will lead to spur and degrades the output phase noise. To solve this issue, the adaptive LuT-based calibration circuits are included. They construct the control information based on the CMP's output e(t) and calibrate the final DAC and DTC controls to be uncorrelated with the e(t) with the LMS algorithm.

Finally, the general architecture of the proposed OSPLL is shown in Fig. 2(b). When the phase is locked, the voltages of reference and feedback signal are equal at $\mathrm{CLK_{PD}}$, and the following equations are satisfied:

$$V_{\mathrm{REF}} = V_{\mathrm{FB}} \tag{3}$$

$$V_{\mathrm{REF}} = A_{\mathrm{REF}} \sin(2\pi f_{\mathrm{REF}} t_{\mathrm{V,crossing}}) + n_{\mathrm{REF}} \tag{4}$$

$$V_{\mathrm{FB}} = A_{\mathrm{FB}} \sin[2\pi f_{\mathrm{FB}}(t_{\mathrm{FB}} + t_{\mathrm{DTC}})] + n_{\mathrm{FB}} \tag{5}$$

where V_{REF} and V_{FB} are the voltages of reference and feedback signal, respectively. A_{FB} is the amplitude of the feedback. f_{FB} represents the frequency of the feedback signal. $t_{\mathrm{V,crossing}}$ is the timing of the reference and feedback voltage crossing, and t_{FB} is the timing information of $\mathrm{CLK_{FB}}$, which is synchronous with f_{OUT}. t_{DTC} is the delay generated by DTC. n_{REF} and n_{FB} means the voltage noise of the reference and feedback, respectively. With A_{REF} approximately equal to A_{FB}, the timing relationship between $t_{\mathrm{V,crossing}}$ and $t_{\mathrm{FB}} + t_{\mathrm{DTC}}$ can be obtained by the voltage domain comparison. As shown in the following equation, the voltage difference is the product of phase error and the slope of reference when the frequency is locked. Depending on the slope of the reference, the phase error of the same voltage error is opposite polarity, as illustrated in Fig. 3:

$$V_{\mathrm{REF}} - V_{\mathrm{FB}} \approx A_{\mathrm{REF}} \phi_e \cos\left(2\pi f_{\mathrm{REF}} t_{\mathrm{V,crossing}} + \frac{\phi_e}{2}\right) \tag{6}$$

$$\phi_e = 2\pi f_{\mathrm{REF}} t_{\mathrm{V,crossing}} - 2\pi (t_{\mathrm{FB}} + t_{\mathrm{DTC}}) \tag{7}$$

where ϕ_{e} represents the phase error the main PLL targets to cancel. V_{FB} goes through a phase-to-voltage conversion by LuTs and, finally, translates into analog domain by a 10-bit RDAC. Depending on the sampling point m, which is an integer distributed from 1 to OSR, the voltage information can be selected from the corresponding address LuT banks. Since the voltage crossing phase is not the integer division of 2π in both integer mode or fractional mode, $\phi_{\mathrm{DTC,m}}$ always exists and varies with m to compensate for this fractional phase. The voltage difference of V_{REF} and V_{FB} is quantized to the 1-bit signal e(t), which converts the CMP as a BBPD in OSPLL. In the fractional mode, the fractional delay is included in the t_{DTC}. Except for the fractional delay generation circuit, the building blocks of fractional mode are the same as the integer one.

B. System Noise Analysis of the Proposed OSPLL

To optimize the jitter performance of the proposed architecture, the noise analysis of the whole loop is needed.

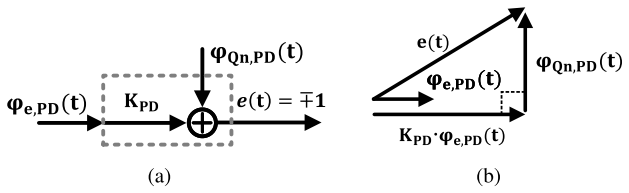

Fig. 4. (a) Linearized model of BBPD. (b) Signal space model of BBPD.

The simplified phase domain model is shown in Fig. 5. ϕ_{REF}, $\phi_{\mathrm{Qn,PD}}$, and ϕ_{VCO} represent the phase domain noise from reference, BBPD's quantization, and voltage-controlled oscillator (VCO). $V_{\mathrm{n,PD}}$ is defined as the voltage domain input-referred noise of the PD, which mainly includes the thermal noise, flicker noise, and nonlinearity effect added in the CMP process before quantization. $\phi_{\mathrm{Vn,PD}}$ is the corresponding noise in the phase domain caused by $V_{\mathrm{n,PD}}$. ϕ_{e} is the phase noise input to the PD before $\phi_{\mathrm{Vn,PD}}$ superimposed. $\phi_{\mathrm{e,PD}}$ represents the phase noise input to the PD. K_{PD} is the phase-to-voltage gain of the BBPD. α and β define the proportional and integral parameters implemented in the digital loop filter (DLF). γ is the integral parameter implemented in the DTC construction loop. ϕ_{DTC} represents the phase noise introduced by the DTC calibration loop. ϕ_{FB} defines the feedback phase noise after MMD. The weight function will be introduced in the afterward paragraphs. K_{VCO} is the voltage-to-frequency gain of the VCO, and N is the division ratio of MMD.

In the conventional PD, $\phi_{\mathrm{Vn,PD}}$ can be regarded to zero for the square wave sharp voltage conversion, while, for the proposed OSPLL, it cannot be ignored for the slow slope of 32 kHz. The introduced $\phi_{\mathrm{Vn,PD}}$ needs to be carefully designed in case of in-band phase noise pollution.

BBPD, a typical nonlinear time-invariant block, can be linearized, as shown in Fig. 4(a). The gain of BBPD, K_{PD}, is defined as the ratio of the cross correlation of output and input to the autocorrelation of the input itself [8], [29], as shown in the following equation:

$$K_{\mathrm{PD}} = \frac{E[\phi_{\mathrm{e,PD}}(t)e(t)]}{E[{\phi_{\mathrm{e,PD}}}^2(t)]} = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\phi_{\mathrm{e,PD}}}} \tag{8}$$

where $\sigma_{\phi_{\mathrm{e,PD}}}$ represents the standard derivation of $\phi_{\mathrm{e,PD}}$. The K_{PD} definition can be easily understood from the signal space, as shown in Fig. 4(b). When the added quantization noise $\phi_{\mathrm{Qn,PD}}$ is orthogonal to the product of K_{PD} and $\phi_{\mathrm{e,PD}}(t)$, K_{PD} can be gotten. To clarify K_{PD}, the jitter of PD input needs to be defined. Fundamentally, the jitter contribution of $\phi_{\mathrm{e,PD}}$ comes from reference noise, PD voltage noise, PD quantization noise, and VCO noise, while, unlike the conventional low reference PLLs, where the VCO noise dominates $\phi_{\mathrm{e,PD}}$ for the narrow $\mathrm{BW_{loop}}$, $\phi_{\mathrm{e,PD}}$ of the proposed OSPLL is mainly dominated by the noise of reference and PD voltage noise. Since ϕ_{REF} and $\phi_{\mathrm{Vn,PD}}$ go through a high pass filter to generate the noise input to PD [8], $\phi_{\mathrm{e,PD}}$ contains almost all noise from ϕ_{REF} and $\phi_{\mathrm{Vn,PD}}$. $\phi_{\mathrm{e,PD}}$ can be expressed as

$$\sigma^2_{\phi_{\mathrm{e,PD}}} \approx \sigma^2_{\phi_{\mathrm{REF}}} + \sigma^2_{\phi_{\mathrm{Vn,PD}}}. \tag{9}$$

To calculate $\sigma^2_{\phi_{\mathrm{Vn,PD}}}$, the probability density function transfer from voltage to phase can be calculated by

$$\begin{aligned} p(\phi_{\mathrm{Vn,PD}}) &= \frac{p(V_{\mathrm{n,PD}})}{d\phi_{\mathrm{Vn,PD}}/dV_{\mathrm{n,PD}}} \\ &= \frac{SS_{\mathrm{REF}}}{2\sqrt{2}\pi^{\frac{3}{2}}\sigma_{\mathrm{Vn,PD}} f_{\mathrm{FB}}} \exp\left(-\frac{\phi^2_{\mathrm{Vn,PD}}(t) SS^2_{\mathrm{REF}}}{8(\pi f_{\mathrm{FB}}\sigma_{\mathrm{Vn,PD}})^2}\right) \end{aligned} \tag{10}$$

where $p(\cdot)$ is the probability function. Equation (9) can be further derived to

$$\begin{aligned} \sigma^2_{\phi_{\mathrm{e,PD}}} &\approx \sigma^2_{\phi_{\mathrm{REF}}} + \frac{(2\pi f_{\mathrm{FB}}\sigma_{V_{\mathrm{n,PD}}})^2}{SS^2_{\mathrm{REF}}} \\ &= \sigma^2_{\phi_{\mathrm{REF}}} + \frac{\mathrm{OSR}^2}{[A_{\mathrm{REF}} cos(2\pi f_{\mathrm{REF}} t)]^2}\sigma^2_{V_{\mathrm{n,PD}}}. \end{aligned} \tag{11}$$

Depending on the size relationship of $\sigma^2_{\phi_{\mathrm{REF}}}$ and $\sigma^2_{\phi_{\mathrm{Vn,PD}}}$, $\sigma^2_{\phi_{\mathrm{e,PD}}}$ characteristic changes. If $\sigma_{\phi_{\mathrm{REF}}}$ is larger than $\sigma_{\phi_{\mathrm{Vn,PD}}}$ at reference zero-crossing, the decrease in SS_{REF} will amplify $\sigma_{\phi_{\mathrm{Vn,PD}}}$. When the two get equal, from (11), it can be derived that $(\sigma_{\phi_{\mathrm{REF}}}/\sigma_{\mathrm{Vn,PD}}) = (\mathrm{OSR}/(A_{\mathrm{REF}}|\cos(2\pi\, \mathrm{f_{REF}t})|))$. When this equation satisfies at $|\cos(2\pi\, \mathrm{f_{REF}t})|$ less than 0.2, which means $(\sigma_{\phi_{\mathrm{REF}}}/\sigma_{\mathrm{Vn,PD}}) > (5\mathrm{OSR}/A_{\mathrm{REF}})$, the jitter contribution of $\phi_{\mathrm{e,PD}}$ can be viewed as dominated by the reference phase noise over 80% of a sine reference. K_{PD} can be regarded as time-invariant over sampling points. On the other hand, if $\sigma_{\phi_{\mathrm{REF}}}$ is much smaller than $\sigma_{\mathrm{Vn,PD}}$, $\phi_{\mathrm{e,PD}}$ is largely influenced by slope, as well as K_{PD}, which means that K_{PD} is a time-variant parameter. Regardless of either situation, $\phi_{\mathrm{Vn,PD}}$ becomes significantly large when the reference slope is near zero, corresponding to the sine peak region. This influences the output phase noise power shake with the frequency of twice of f_{REF}. The phase noise power becomes extremely large at the reference's zero slope region. This needs to be eliminated for overall phase noise suppression. In the design, the (1/cos) effect is bounded to control the loop, which is realized by freezing e(t) (set as zero) at sine reference peak region to control the DLF.

The output phase without weight function can be derived as follows:

$$\phi_{\mathrm{OUT}} = \frac{(\phi_{\mathrm{Vn,PD}} + \phi_{\mathrm{REF}})NXT}{1+XT} + \frac{\phi_{\mathrm{Qn,PD}}NXT}{K_{\mathrm{PD}}(1+XT)} + \frac{\phi_{\mathrm{n,VCO}}}{1+XT} \tag{12}$$

$$T = K_{\mathrm{PD}}\left(\alpha + \frac{\beta f_{\mathrm{FB}}}{2\pi f}\right)\frac{K_{\mathrm{VCO}}}{2\pi f}\frac{1}{N} \tag{13}$$

$$X = 1 - K_{\mathrm{PD}}\frac{\gamma f_{\mathrm{REF}}}{2\pi f} \tag{14}$$

where T is the open-loop transfer function of the proposed OSPLL and X is the transfer function of DTC control loop. $\mathrm{BW_{loop}}$ of DTC construction is set much narrower than the main PLL since the operation frequency of the construction loop is f_{REF} rather than f_{PD}. Furthermore, the integral parameter of the low-pass filter (LPF), γ, is set small for the accuracy guarantee. With this characteristic, the effect of DTC construction loop on the output jitter can be neglected, which means X approaching to 1.

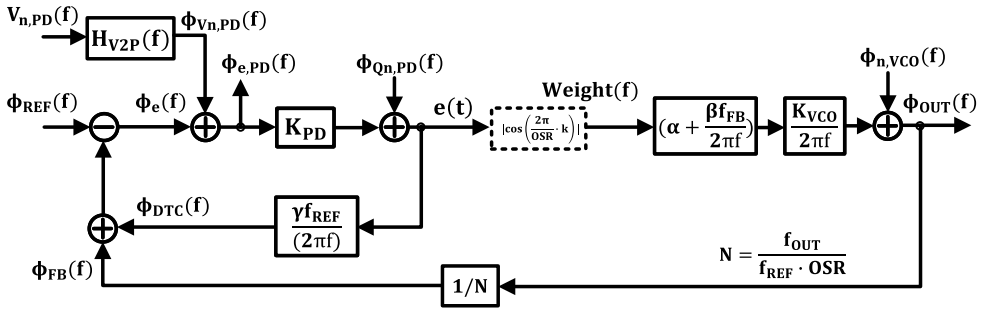

Fig. 5. Linearized periodical switched OSPLL model in the phase domain.

From the analysis, $H_{\mathrm{V2P}}(f)$ proves to be a periodic time varying system. The model of $H_{\mathrm{V2P}}(f)$ in Fig. 5 behaves in the periodically switched way. The frequency transfer from $V_{\mathrm{n,PD}}(f)$ to $\phi_{\mathrm{Vn,PD}}(f)$ can be derived based on the theories about time-variant periodical switched system in [30]–[32]. Since the discrete operation is conducted by the sampling operation, the z transform is used here

$$\phi_{\mathrm{Vn,PD}}(z) = \sum_{m=1}^{\mathrm{OSR}} \phi_{\mathrm{Vn,PD,m}}(z) \tag{15}$$

$$\phi_{\mathrm{Vn,PD,m}}(z) = \frac{1}{\mathrm{OSR}} \sum_{k=1}^{\mathrm{OSR}} W^{-mk} V_{\mathrm{n,PD}}(zW^{-m}) H_{\mathrm{V2P,k}}(z) \tag{16}$$

$$H_{\mathrm{V2P,k}}(z) = \frac{\mathrm{OSR}}{A_{\mathrm{REF}} \cos(\frac{2\pi k}{\mathrm{OSR}})} \tag{17}$$

where $z = e^{j2\pi f/f_{\mathrm{FB}}}$ and $W^{-k} = e^{j(2\pi k/\mathrm{OSR})} (j = \sqrt{-1})$. $H_{\mathrm{V2P,k}}$ represents the transfer function at $\mathrm{k_{th}}$ sampling point from voltage to phase domain. $V_{\mathrm{n,PD}}(f)$ can be modeled as wideband white noise of comparator sampling noise variance sampled at f_{FB}. The equations above shows the nonlinearity effect on the $\phi_{\mathrm{Vn,PD}}$ spectrum. With the same voltage domain noise, the slower slope leads to a larger $\phi_{\mathrm{Vn,PD}}$, and the overall noise spectrum of $\phi_{\mathrm{Vn,PD}}$ will be increased.

To compensate for this noise effect caused by $V_{\mathrm{n,PD}}$, a slope-based weight function is applied. For a sine reference, the weight function $|\cos(2\pi\,\mathrm{m/OSR})|$ is multiplied to e(t) at m_{th} sampling point, as shown in the dot block in Fig. 5. The overall TF with the weight function adopted can be derived based on the similar equations of $\phi_{\mathrm{Vn,PD}}$ derivation. Since the input and output terminals are all in analog domain, the conversion from z transform to the Fourier transform is applied. The ϕ_{OUT} spectrum can be derived as follows when the cosine weight function is applied:

$$\phi_{\mathrm{OUT}}(f) = \sum_{m=-\infty}^{\infty} [H_{m,LPF}(f)\phi_{\mathrm{LPF}}(f - mf_{\mathrm{REF}}) + H_{m,HPF}(f)\phi_{\mathrm{HPF}}(f - mf_{\mathrm{REF}})] \tag{18}$$

$$\phi_{\mathrm{LPF}}(f) = \phi_{\mathrm{REF}}(f) + \phi_{\mathrm{Vn,PD}}(f) + \frac{\phi_{\mathrm{Qn,PD}}(f)}{K_{\mathrm{PD}}} \tag{19}$$

$$\phi_{\mathrm{HPF}}(f) = \phi_{\mathrm{n,VCO}}(f) \tag{20}$$

$$H_{m,LPF}(f) = \frac{1 - e^{\frac{j2\pi f}{f_{\mathrm{FB}}}}}{\frac{j2\pi f}{f_{\mathrm{REF}}}} \sum_{k=1}^{\mathrm{OSR}} W^{-km} N \frac{T_{\mathrm{k}}(f)}{1 + T_{\mathrm{k}}(f)} \tag{21}$$

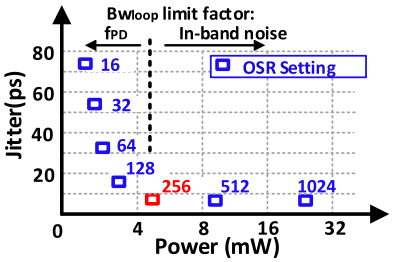

Fig. 6. Simulated jitter and power tradeoff over different OSR settings.

$$H_{m,HPF}(f) = \frac{1 - e^{\frac{j2\pi f}{f_{\mathrm{FB}}}}}{\frac{j2\pi f}{f_{\mathrm{REF}}}} \sum_{k=1}^{\mathrm{OSR}} W^{-km} \frac{1}{1 + T_{\mathrm{k}}(f)} \tag{22}$$

$$T_{\mathrm{k}}(f) = \left|\cos\left(\frac{2\pi k}{\mathrm{OSR}}\right)\right| K_{\mathrm{PD}} \left(\alpha + \frac{\beta f_{\mathrm{FB}}}{2\pi f}\right) \frac{K_{\mathrm{VCO}}}{2\pi f} \frac{1}{N} \tag{23}$$

where $H_{\mathrm{m,LPF}}$ represents the LPF effect of PLL on ϕ_{LPF}, which mainly includes the noise from reference and PD. $H_{\mathrm{m,HPF}}$ represents the high-pass filter effect of PLL on ϕ_{HPF}, which includes the noise from VCO. T_{k} is open loop transfer function of PLL corresponding to the $\mathrm{k_{th}}$ sampling point. The application of weight function can effectively suppress the (1/cos) leaded noise on $\phi_{\mathrm{Vn,PD}}$. This can also effectively suppress the spur level at f_{REF} and its multiplied frequency with the suppressed in-band phase noise. From the above equations, for the given f_{REF}, f_{OUT}, and the external noise sources, the basic parameter influencing the whole loop performance is the value of OSR, which is defined by the ratio of f_{FB} to f_{REF}. A larger OSR is effectively to reduce the division ratio and enlarge $\mathrm{BW_{loop}}$, so as to suppress the in-band jitter contribution from VCO, while this is realized by the cost of high operation frequency of the loop, which usually consumes a lot of power. Meanwhile, the LuT size for DAC and DTC control will increase exponentially. The OSR setting suffers from the tradeoff between jitter performance, power consumption, and area occupation. The tradeoff between power and jitter performance is shown in Fig. 6. In this simulation, the phase noise settings about the reference and VCO are −145 and −92 dBc/Hz at a 100-kHz offset, respectively. With different noise settings, the optimal OSR setting may change. Based on the tradeoff simulation, the OSR of 256 is chosen. For the OSR less than 256, the achievable $\mathrm{BW_{loop}}$ is limited by the frequency of PD. Further increase in the OSR larger than

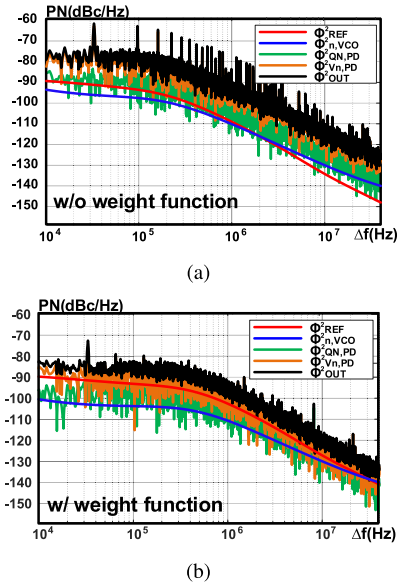

Fig. 7. Output phase noise contribution (a) without weight function and (b) with weight function.

256 leads to more power with negligible jitter improvement, which is limited by the in-band jitter contribution. This in-band phase noise includes ϕ_{REF}, $\phi_{\mathrm{Vn,PD}}$, and $\phi_{\mathrm{Qn,PD}}$. $\phi_{\mathrm{Qn,PD}}$ is suppressed by K_{PD}. Therefore, mainly ϕ_{REF} and $\phi_{\mathrm{Vn,PD}}$ contribute to the in-band phase noise. This can be seen from the simulation in Fig. 7. The phase noise contribution with and without weight function is also simulated, as illustrated in Fig. 7. Consisted with the theoretical calculation, the weight function is effective to improve the overall jitter performance and suppress the f_{REF} spurs.

III. Circuit Implementation

The overall architecture of the proposed OSPLL is shown in Fig. 8. Three loops are implemented in the proposed OSPLL: coarse PLL, main PLL, and calibration loop. To eliminate the false frequency locking and shorten the fine PLL convergence time, the coarse PLL is implemented. The reference and feedback signals are buffered from sine wave to square wave for frequency detection. A dead-zone included phase-frequency detector is implemented in the coarse PLL. The generated pulse is counted at f_{OUT}, which corresponds to the PD resolution of around 400 ps. The coarse PLL can automatically turn off the energy-consuming counter and loop filter to reduce the system power consumption.

The main PLL compares the sine reference and feedback signal by a low-noise rail-to-rail passive CMP. The generated 1-bit output e(t) multiplies the weight function in the digital domain and goes through a DLF to control the fine bank of VCO. The feedback signal is generated by a 10-bit RDAC and controlled by an LuT-based calibration loop, which operates at 8-MHz $\mathrm{CLK_{FB}}$. DTC control is generated by the LuT-based calibration circuit, which operates in the background to follow the reference changes in the environment closely. The implemented LuT has OSR address corresponding to OSR sampling points. As shown in Fig. 8, The LuT address is calculated by a counter-based phase accumulator, ranging from 1 to OSR. The LuTs for DAC and DTC control are implemented with the feedback loop, which adaptively constructs the LuT bank value with $e(t)$ control. The weight function can be controlled from SPI and can be selected ON or OFF to compensate for the nonlinear effect of reference. At the n_{th} sampling point, the n_{th} LuT banks' values are output, and the generated e(t) influences the next n_{th} address LuT banks values. To cover a long-range delay, the cascaded DTC is adopted for 0.6-ps resolution and 107.3-ns range. The FCW is input from SPI. First, it goes through a first-order DSM to calculate the integer part of FCW to control the MMD. For the fractional-N operation, the left fractional part of FCW ($\mathrm{FCW_{frac}}$) is calculated by subtracting the output of DSM from its input. $\sum Q_{\mathrm{N}}$ accumulates $\mathrm{FCW_{frac}}$ to generate the control for DTC. Before controlling DTC, the LMS-gain-based calibration works to calibrate the gain mismatch between the DCO period and DTC full-scale delay. The multiplication output $C_{\mathrm{DTC_{frac}}}$ is added with $C_{\mathrm{DTC_{fine}}}$ to control the fine DTC. A low-noise inductor–capacitor (LC)-VCO is implemented with 20-kHz/unit cap gain for limit cycle elimination.

A. Comparator-Based Phase Detector

A low-noise CMP is needed to realize a high PD resolution. In this work, a chopper-type CMP [33] is adopted for its simple design and efficient noise suppression. The operation of the proposed CMP is shown in Fig. 9. The architecture of the on-chip oscillator circuit can be referred to [14]. The crystal outside the chip is EPSON FC-135R. The 10-bit RDAC is used to generate the FB signal, as shown in Fig. 9.

The operation of the CMP is composed of three steps, as illustrated in Fig. 10. The first step is the pre-charge step. In this step, $\mathrm{SW_{XO}}$ and $\mathrm{SW_{INV}}$ turn on, and the voltage of node A charges to V_{REF}. The auto-zero of the inverter fixed the voltage at node B to be the inverter threshold voltage V_{th}. After the settling time for the pre-charge, the sampling is conducted. $\mathrm{SW_{INV}}$ turns off at the rising edge timing of $\mathrm{CLK_{PD}}$, which is output by DTC. After the sampling, the charge of the capacitor keeps stable as $V_{\mathrm{REF@clk_{PD}}} - V_{\mathrm{th}}$. To avoid the signal-dependent charge injection effect of $\mathrm{SW_{XO}}$, $\mathrm{SW_{XO}}$ turns off slightly after the $\mathrm{SW_{INV}}$. The third step is the comparison step. In this step, $\mathrm{SW_{DAC}}$ turns on, and the voltage of node A charges to V_{FB}. With the capacitor charge conservation characteristic, the voltage at node B will settle to the voltage of the value of

$$V_{\mathrm{B}} = V_{\mathrm{FB}} - V_{\mathrm{REF@CLK_{PD}}} + V_{\mathrm{th}}. \tag{24}$$

This voltage is sampled at the rising edge of $\mathrm{CLK_{LF}}$, which is the delayed clock of $\mathrm{CLK_{PD}}$. The delay τ_{D} influences the loop delay and needs to be controlled to be less than one PD period. The inverters amplifies the voltage difference between V_{FB} and $V_{\mathrm{REF@CLK_{PD}}}$ to generate the polarity e(t). In this implementation, the complementary switch is used in SW_{XO} and $\mathrm{SW_{DAC}}$ to reduce the charge injection effect. A 2-pF metal–insulator–metal (MIM) capacitor is adopted for its linear property and thermal noise reduction ability. The flicker noise is reduced by increasing the inverter area, with a 24-dB dc gain of the inverter at near V_{th} bias. The separate LuT

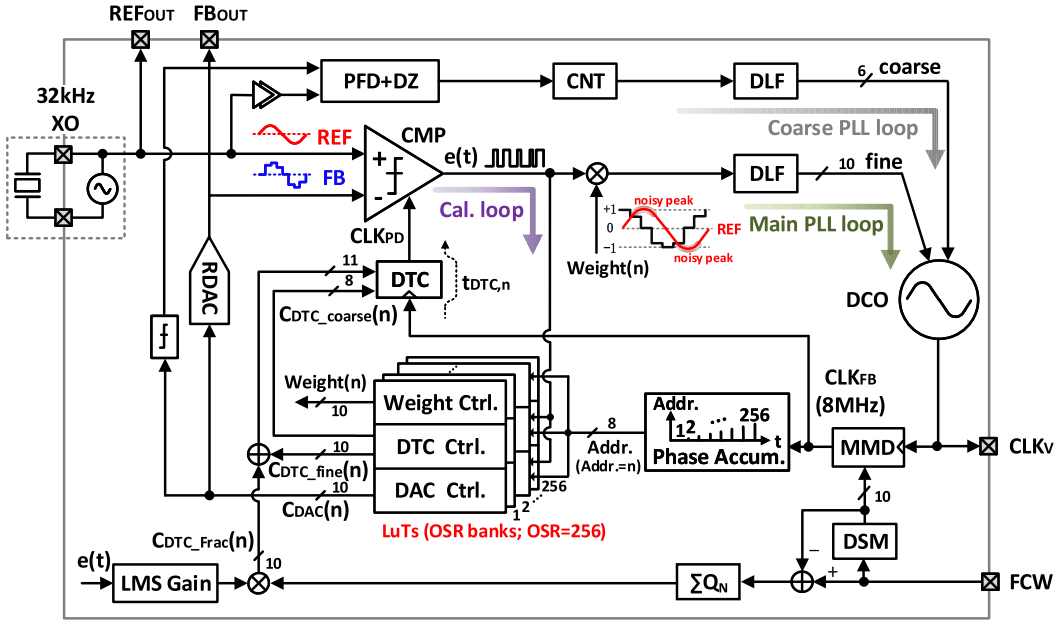

Fig. 8. Overall architecture of the proposed OSPLL.

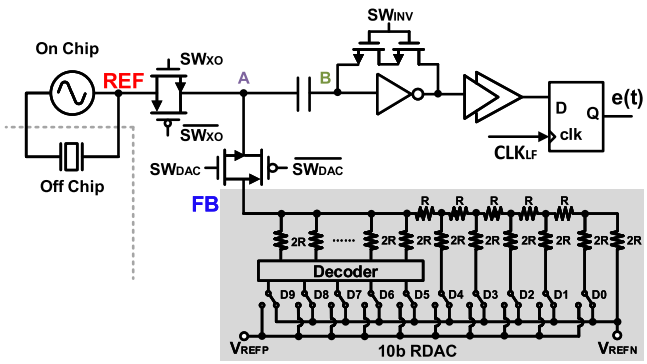

Fig. 9. Detail circuit of rail-to-rail low-noise CMP and 10-bit RDAC.

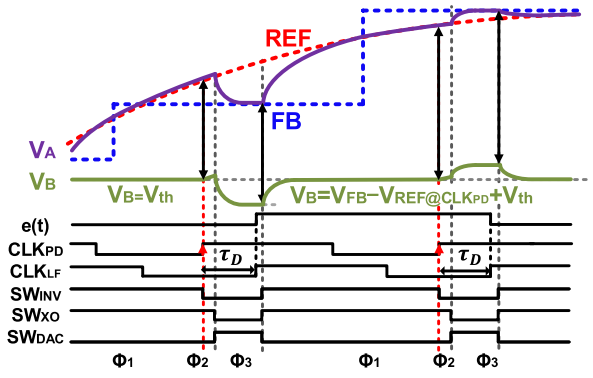

Fig. 10. Operation flow of CMP.

bank is built for each sampling address, and the static offset for each address can be eliminated by calibration. Hence, the signal amplitude-dependent noise can be canceled, with only random noise consideration left. The sampling circuit

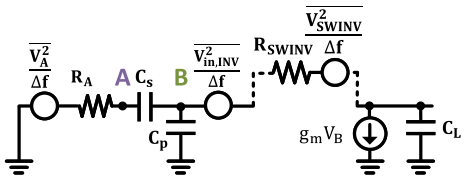

Fig. 11. Equivalent small-signal circuit noise model of CMP.

is a dynamic circuit whose noise characteristic changes at different steps. The equivalent circuit models of the proposed CMP are drawn in Fig. 11. The final output noise is the combination of these two states [34]. R_A represents the equivalent resistance seen from A node, and $(\overline{V_A^2}/\Delta f)$ is the power spectrum density (PSD) of R_A. R_{SWINV} represents the resistance of the SW_{INV}, and the corresponding PSD is $(\overline{V_{SWINV}^2}/\Delta f)$. $(\overline{V_A^2}/\Delta f)$ is the PSD of the inverter, and g_m is the transconductance of the inverter. The integrated noise of node B at the pre-charge and comparison stages can be calculated based on the following equations:

$$\overline{V_{B,p}^2} \approx \frac{KTC_s}{(C_p+C_L)(C_s+C_p+C_L)} + \frac{KT}{C_s+C_p} \quad (25)$$

$$\overline{V_{B,c}^2} \approx \frac{KTC_s}{C_p(C_s+C_p)} + \frac{KT}{g_m C_L} \quad (26)$$

$$\overline{V_{B,total}^2} = \overline{V_{B,p}^2} + \overline{V_{B,c}^2} \quad (27)$$

where C_s and C_p represent the sampling capacitor and parasitic capacitor at node B, respectively. C_L is the load capacitor. K is Boltzmann's constant, and T is the absolute temperature. $\overline{V_{B,p}^2}$ and $\overline{V_{B,c}^2}$ are the integrated noise powers of node B at the pre-charge step and the comparison step, respectively. In the pre-charge step, the thermal power spectral density is lower than the CMP step while with a wider noise bandwidth.

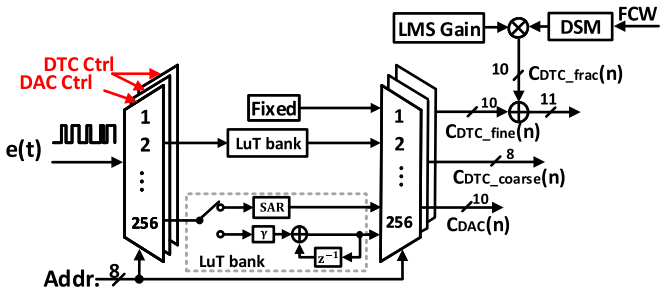

Fig. 12. LuT architecture for DAC and DTC control.

The integrated noise power at the pre-charge step is relatively smaller than the CMP step. The total noise $V_{\mathrm{B,total}}$ is defined as the input-referred voltage noise of PD process, which is equivalent to the definition of $V_{\mathrm{n,PD}}$ in Section II. This noise is simulated by Pnoise simulation, and the integral root-mean-square (rms) voltage noise of $V^2_{\mathrm{B,total}}$ is around 40 μV.

B. Adaptive Lookup Table Construction

Three LuTs are used for DAC, coarse DTC, and fine DTC control construction, as shown in Fig. 12. Unlike the existing LuT construction methods in [35] and [36], which usually needs more than hundreds of reference cycles to construct the LuT, the LuT construction proposed in this work is based on the combination of successive approximation (SAR) logic and the LPF process. The SAR logic is implemented based on the binary search method, and the LPF process is based on the digital accumulator. During the LuT construction, the SAR logic is first turned on, which quickly constructs the LuT bank from MSB to LSB with bit-length's reference cycle. After the LSB is set, the switch automatically connects to the LPF path and turns on the LPF, which corrects the LuT bank value with a slower speed while higher resolution.

The tunable internal parameter γ in LPF guarantees the accuracy of the final control value, while the SAR logic speeds up the construction process. The construction behavior simulations are shown in Fig. 13; compared with the conventional LuT construction method, the proposed one can shorten the convergence time by more than 100 times.

The construction process of three LuTs is done by order of resolution. After the fine PLL is locked, the DAC construction starts. Since the time error is much smaller than 9 ns when fine PLL is locked, this is enough to converge C_{DAC} to the final LSB. In the process of C_{DAC} construction, $C_{\mathrm{DTC\_coarse}}$, and $C_{\mathrm{DTC\_fine}}$ for all sampling addresses are set the same, as shown in Fig. 14(a). With the default C_{DAC} set as the common-mode voltage (V_{cm}), e(t) stretches C_{DAC} to fit reference voltage. To eliminate the phase noise degradation due to the DAC control code toggling, the DAC control construction is set to be foreground one. Since the DAC control construction is done by the adaptive feedback loop, the DAC INL effect will be automatically considered. This means that the correct voltage value is not important in this process, while the voltage crossing point matters.

After the C_{DAC} convergency, the register holds its value, and DTC control construction starts. The DTC delay is used to compensate for the time caused by DAC's voltage quantization, as shown in Fig. 14(b). The DTC construction is a background calibration, which is also conducted with the same architecture of Fig. 12. Since the DTC construction is settled when the corresponding address LuT bank value is near a dc value, this means that the corresponding address CMP output is dominated by the random noise only regardless of the static offset. Thus, this adaptive feedback construction automatically eliminates the static offset effect from CMP. With the DTC construction, the phase error ϕ_{e} dramatically decreases, as illustrated in Fig. 15.

With the consideration of fractional-N operation, the LMS gain calibration circuit is implemented. The LMS gain calibration is only needed when the $\mathrm{FCW_{frac}}$ dominator is larger than OSR, and it is done before DTC construction. When the $\mathrm{FCW_{frac}}$ dominator is smaller than OSR, LuT construction can built the delay information for each address. This is because, in the implementation, the denominator of $\mathrm{FCW_{frac}}$ is set as the 2^N, where N bit-length of $\mathrm{FCW_{frac}}$. When this 2^N is smaller than OSR, the fractional control $C_{\mathrm{DTC_{frac}}}$ for every sampling point is fixed, and this value can be constructed by the automatic LuT calibration. This delay can be automatically considered in $C_{\mathrm{DTC_{fine}}}$ construction, which means that the $C_{\mathrm{DTC_{frac}}}$ generation can be turned off. When 2^N is larger than OSR, the fractional delay for every sampling point is changing, which means that additional delay controlled by $C_{\mathrm{DTC\_frac}}$ is needed.

C. DTC Implementation

To compensate for the long-range time error caused by DAC voltage quantization while guaranteeing the resolution of PD, the cascaded DTC is implemented, as illustrated in Fig. 16(a). An 8-bit coarse DTC is implemented based on the DCO clock resolution, which achieves a 106-ns delay range. The fine DTC is implemented with the constant slope one. The fine DTC realizes different delays by charging a different V_{X} to V_{th} (threshold voltage of inverter) with the same charge speed based on the $C_{\mathrm{DAC\_fine}}$. The constant slope DTC performs better in integral nonlinearity (INL) than the variable slope DTC. The architecture of the fine DTC and the post-layout simulated INL is shown in Fig. 16(b). It realizes 0.6 ps with INL of less than 2 LSB. This makes DTC leaded quantization noise less than -120 dBc/Hz, which is negligible in the in-band noise contribution.

D. DCO Implementation

A robust low-phase-noise CMOS LC-VCO is implemented in this work [37], as shown in Fig. 17. The 4-bit coarse bank is governed by the frequency tuning word from SPI, with a 50-MHz/LSB frequency resolution. The 6-bit switch capacitor-based medium-bank is controlled by the coarse PLL, with a frequency resolution of 1.25 MHz/LSB. To make sure that the fine PLL finally works in the random noise regime other than the limit cycle [38], the white noise introduced to the PLL loop should be larger than the quantization noise

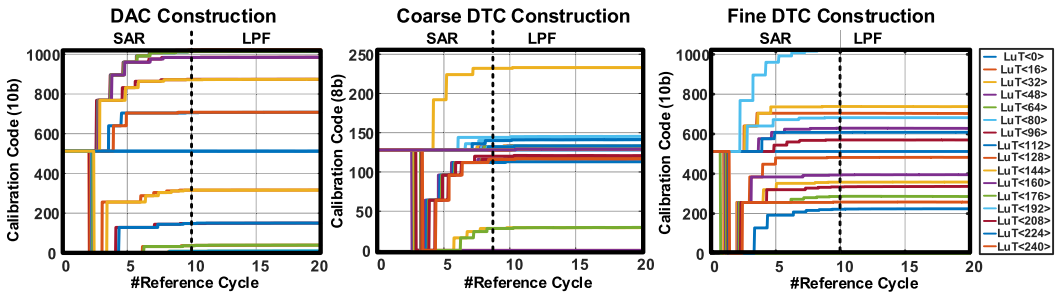

Fig. 13. Simulation results of LuTs' construction.

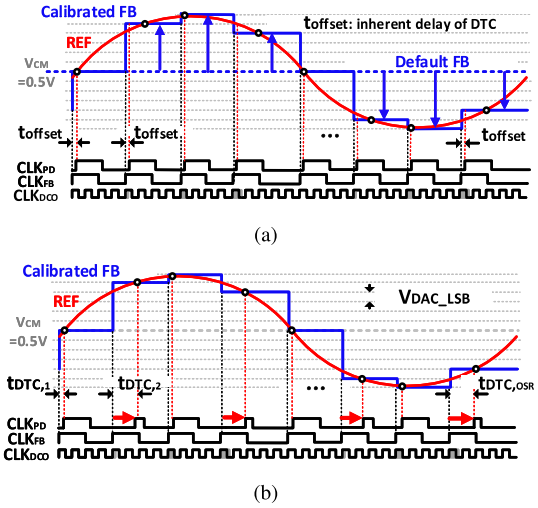

Fig. 14. Adaptive LuT construction of (a) DAC control and (b) DTC control.

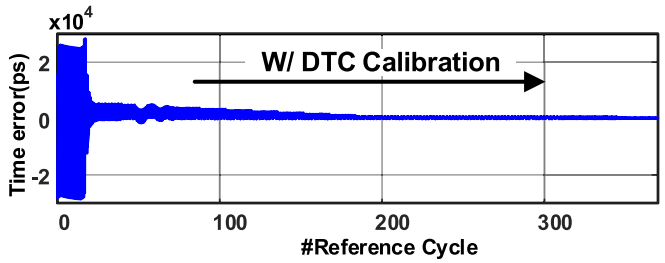

Fig. 15. Simulated time error with DTC calibration.

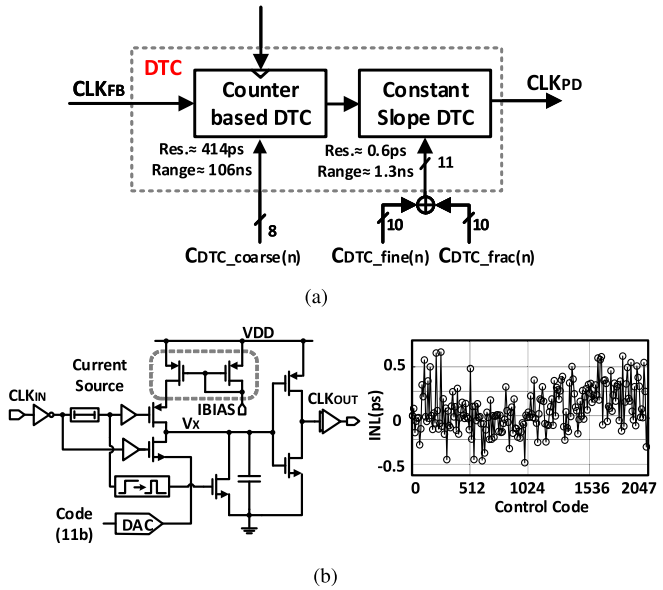

Fig. 16. DTC architecture of (a) overall cascaded DTC and (b) constant slope fine DTC and post-layout simulated INL performance.

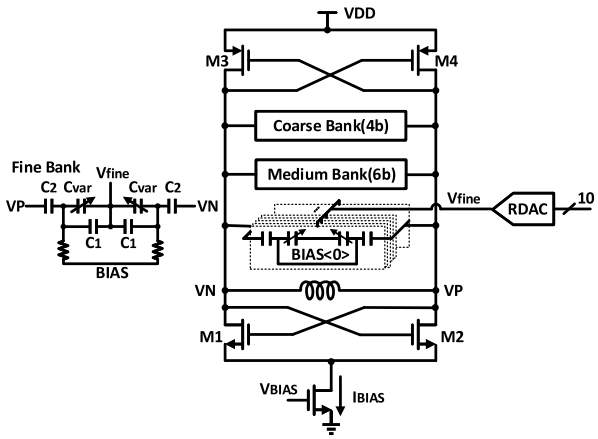

Fig. 17. LC-oscillator with fine resolution of a 20-kHz/unit cap.

introduced by DCO. The white noise in the proposed OSPLL mainly includes phase noise from a reference signal and $V_{\mathrm{n,PD}}$, which can be expressed as (9). The noise relationship and the quantization noise introduced by DCO can be represented as

$$\sigma_{\phi_{\mathrm{QN,DCO}}} \leq \sqrt{\sigma_{\phi_{\mathrm{REF}}}^2 + \sigma_{\phi_{\mathrm{Vn,PD}}}^2} \tag{28}$$

$$\sigma_{\phi_{\mathrm{QN,DCO}}} = \frac{(1+D)}{\sqrt{3}} \cdot N\alpha K_{\mathrm{T}} \cdot 2\pi f_{\mathrm{FB}} \tag{29}$$

where $\sigma_{\phi_{\mathrm{QN,DCO}}}$ represents the standard derivation of the quantization noise of DCO in the phase domain. D is the loop delay, and K_{T} is the DCO resolution in the time domain. In the OSPLL design, D is set as 1, the loop filter proportional gain α is 2, and the division ratio N is 288. With the above requirement, the resolution of DCO is designed with K_{T} of 4 fs/LSB, corresponding to the frequency resolution of 20 kHz/LSB. This high resolution is realized by the 10-bit fine bank, as shown in Fig. 17. The parallel capacitor C_1 is implemented to further reduce the fine resolution of the

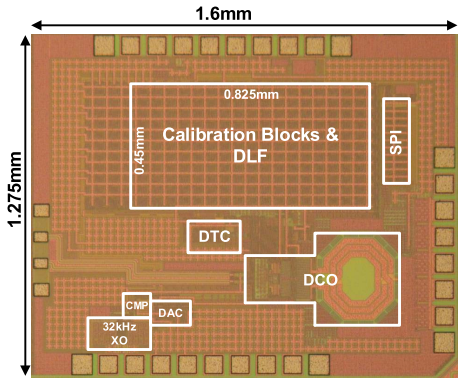

Fig. 18. Die photograph.

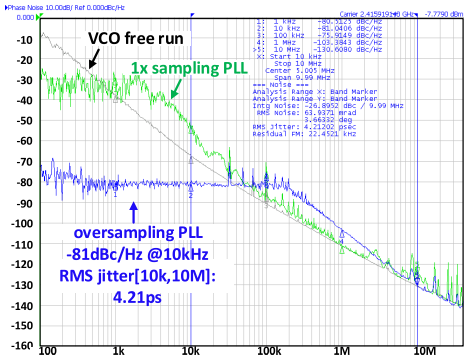

Fig. 19. Measured phase noise performance at integer-N mode, FCW = 288.

TABLE I
POWER CONSUMPTION AND AREA OCCUPATION OF EACH BLOCK

	Power (mW)	Active Area (mm^2)
DCO	1.1	0.151
DAC	0.62	0.011
DTC	0.08	0.015
CMP	0.2	0.005
XO	0.007	0.023
Digital Core	2.96(2.93*)	0.371
Total	**4.97(4.93*)**	**0.576**

* integer mode

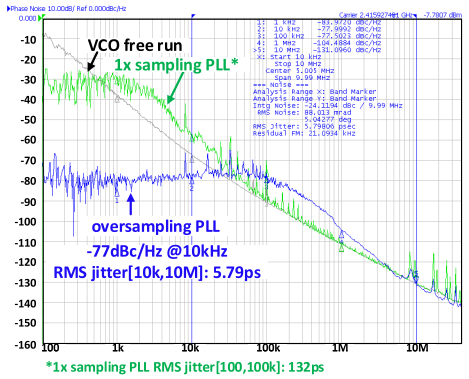

Fig. 20. Measured phase noise at fractional-N mode, FCW = 288.001.

varactor, while the series capacitor C_2 keeps the capacitance of each cell constant. Different bias tunings generated from the resistor ladder are adopted for different fine caps, which improves the linearity performance of the fine bank. A 4-bit input first-order delta–sigma modulator (DSM) is adopted in the digital domain to control 1 LSB of the fine bank, which further improves the f_{OUT} channel conversion resolution to be around 1 kHz/LSB.

IV. MEASUREMENT RESULTS

The proposed OSPLL is fabricated in the 65-nm CMOS technology. Except for DCO, DTC, CMP MMD, PFD, RDAC, and XO, the other blocks in Fig. 8 are synthesized with the non-modified standard cell library. The high digital intensive design increases the noise immunity. Fig. 18 shows the die photo of the proposed OSPLL. The core area of the proposed OSPLL is 0.58 mm^2, and the power consumption is 4.97 mW at the near-integer fractional-N mode. Decoupling capacitors are adopted for supply noise filtering. The detailed power and area occupation of each block is shown in Table. I. The table shows that the digital core occupies the most power and area, which can be reduced with the scaled technology. The LuT-based calibration circuit occupies more than 80% power of the digital core. Compared with the integer mode, the power consumption of fraction mode is 30μW more, which is contributed from LMS gain calibration mainly. The phase noise is measured by the signal source analyzer (Keysight E5052B), and the spectrum is measured by the spectrum analyzer (Anritsu MS2830A). The reference is provided by an arbitrary waveform generator (Keysight M8190A).

Fig. 19 shows the measured phase noise performance in integer-N mode. The VCO free-run phase noise is shown in the gray line, which indicates the −110-dBc/Hz phase noise at 1-MHz offset. The in-band phase noise at the integer mode is measured with −81 dBc/Hz at 10-kHz offset. The rms jitter integrated from 10 kHz to 10 MHz is 4.21 ps at the integer-N mode. Compared with the conventional 1× sampling PLL, the loop bandwidth is efficiently extended by around 100 times, and the jitter performance is improved from 100 ps to less than 10 ps. Fig. 20 shows the measured phase noise performance at near-integer (8-kHz offset) fractional-N mode. It shows that the integrated jitter is 5.79 ps, and the corresponding in-band phase noise is −77 dBc/Hz at 10-kHz offset. The related BW_{loop} is around 200 kHz. The phase noise of OSPLL is larger than 1× PLL at the out-of-band part. This is mainly influenced by the in-band phase noise, which is mainly dominated by the reference noise and Vn, PD noise. Since the in-band phase noise is filtered with a 20-dB decrease per decade frequency at the out-of-band, the noise suppression at near OSPLL BW_{loop} frequency is more severe in the 1× PLL case. The measured spectrum at near-integer (8-kHz offset) fractional-N mode is shown in Figs. 21 and 22. The reference spur can be suppressed to be as low as −78 dBc due to the calibration circuits. The measured fractional spur performance is shown in Fig. 23. The fractional spur at 8-kHz offset is measured with −40 dBc, which is mainly restricted by the fine DTC INL performance.

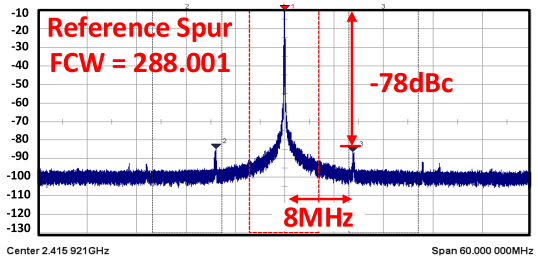

Fig. 21. Measured reference spurs at the near integer mode.

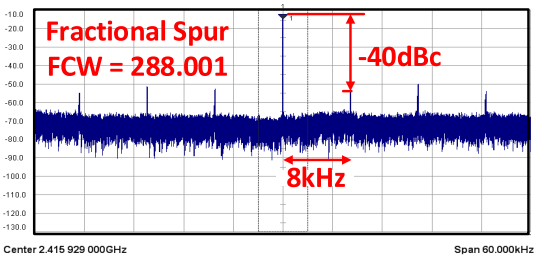

Fig. 22. Measured fractional spurs at the near integer mode.

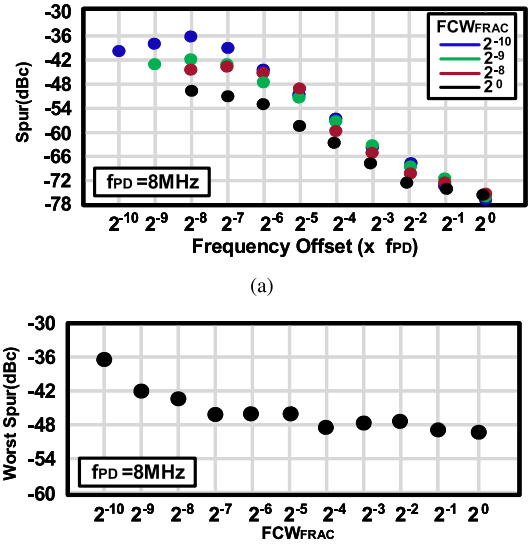

Fig. 23. Measured (a) spurs at different frequency offsets with different FCW_{frac}'s and (b) worst spurs at different FCW_{frac}'s.

The worst fractional spur is measured at 32 kHz with −36-dBc performance. This high spur level is resulted from the adopted calibration method and DTC INL performance both. The dither-based calibration method can be adopted to suppress this spur level. Considering the nonlinear propagation of the reference signal, the sawtooth reference is tested in the measurement, With the calibration, the reference information can be constructed, as shown in Fig. 24. The corresponding reference spur can be suppressed by 12 dB after calibration.

Comparisons with other works [2], [4], [16], [20], [24], [27], [39] are summarized in Table II. The proposed fractional-*N* OSPLL breaks the 1/10 f_{REF} BW_{loop} limitation over

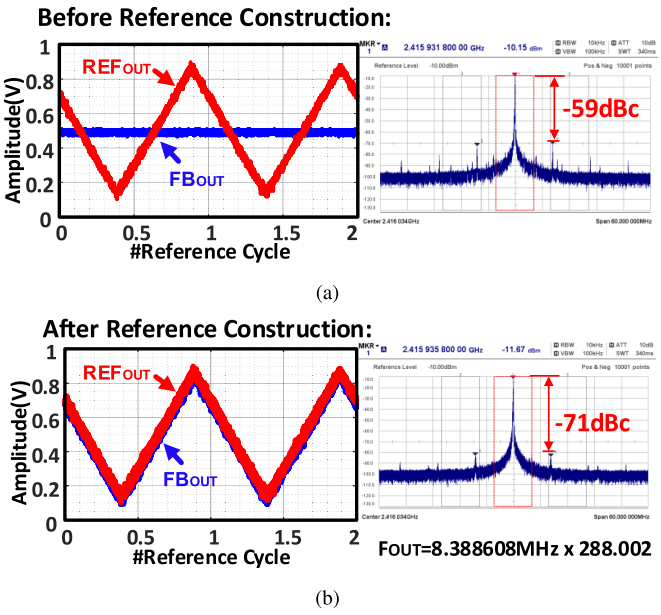

Fig. 24. Measured performance of sawtooth reference construction (a) before construction and (b) after construction.

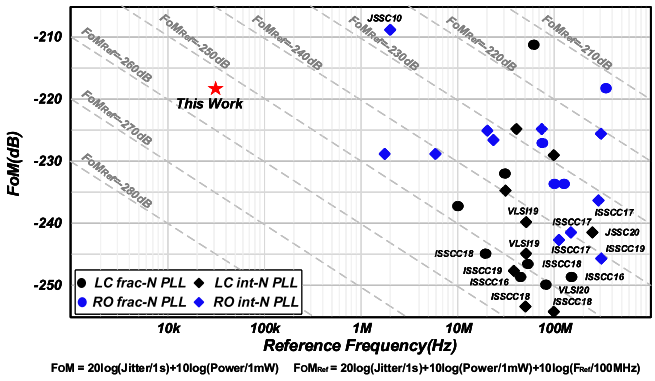

Fig. 25. Comparison chart with state-of-the-art works.

six times and achieves better jitter performance compared with the conventional 32-kHz f_{REF}-based PLL. The reference frequency limits the jitter improvement in the real design. For a low-jitter frequency synthesizer design, higher frequency reference are easier to achieve better figure of merit (FoM), which is unfair for the low frequency synthesizer. For this reason, the reference normalized FoM is assisted to do the comparison with other works [40]. The definition of FoM and FoM_{REF} is shown as follows:

$$\mathrm{FoM} = 20\log\left(\frac{\mathrm{Jitter}}{1\ \mathrm{s}}\right) + 10\log\left(\frac{\mathrm{Power}}{1\ \mathrm{mW}}\right) \tag{30}$$

$$\mathrm{FoM_{REF}} = 20\log\left(\frac{\mathrm{Jitter}}{1\ \mathrm{s}}\right) + 10\log\left(\frac{\mathrm{Power}}{1\ \mathrm{mW}}\right) + 10\log\left(\frac{\mathrm{f_{REF}}}{100\ \mathrm{MHz}}\right). \tag{31}$$

The extended comparison with the state-of-the-art PLLs is shown in Fig. 25. The gap at low reference frequency exists and poses more challenges for low-jitter realization.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART PLLS

	JSSC'15 [2]	VLSI'20 [27]	JSSC'19 [16]	JSSC'12 [20]	ISSCC'16 [24]	ISSCC'18 [4]	VLSI'20 [39]	**This Work**
	Integer-*N*			**Fractional-*N***				
Technology	28 nm FDSOI	28 nm CMOS	65 nm CMOS	130 nm CMOS	28 nm CMOS	65 nm CMOS	130 nm CMOS	65 nm CMOS
f_{OUT} [GHz]	0.96	2.0	2.05 to 2.55	2.55 to 3	2.7 to 4.33	2.0 to 2.8	2.99 to 3.5	2.0 to 2.8
f_{REF} [MHz]	0.032768	50	50	50	40	26	80	**0.032768**
BW_{loop} [MHz]	0.002*	50*	2*	5*	2*	1*	3*	**0.2**
BW_{loop}/f_{REF}	0.0625	1	0.04	0.1	0.05	0.0385	0.0375	**6.25**
OSR	1	40	1	1	1	2	1	**256**
Jitter [ps] Integ.Freq(Hz)	523 (2 k to 20 k)	0.508 (10 k to 100 M)	0.11 (10 k to 100 M)	0.255 (100 to 40 M)	0.16 (10 k to 10 M)	0.53 (10 k to 10 M)	0.11 (10 k to 40 M)	5.79 (10 k to 10 M)
Architecture	CP+DP-LF	Multi-RSPD	RSPD	Cascaded PLL	ADC+DTC	TDC+DTC	DAC+ADC	**DAC+DTC assisted OSPLL**
Core Area [mm^2]	0.15	0.07	0.3	0.5	0.3	0.23	0.27	0.576
Power [mW]	0.486	3.6	3.7	14.2	8.2	0.98	9.2	4.97
Ref. Spur [dBc]	-65	-80	-67	-87	-78	-72	-79	-78
Frac. Spur [dBc]	–	–	–	-53.9	-54	-56	-56	-36
FoM [dB]	-188.7	-240.3	-253	-240.3	-246.8	-246	-250.3	-217.8
FoM_{REF} [dB]	-223.5	-243.3	-256	-243.3	-250.8	-251.4	-251.2	**-252.6**

* estimated from figures

With the lower jitter low-frequency reference and wider achievable BW_{loop}, the gap can be filled.

V. CONCLUSION

A 32-kHz reference 2.4-GHz fractional-*N* OSPLL is proposed in this article. The proposed OSPLL constructs a reference-like feedback signal for the over-sampled PD. The voltage difference between the reference and the feedback is compared at the rising edge of CLK_{PD}, which is generated by CLK_{FB} plus the DTC delay. A clocked passive circuitry-based CMP is designed with low-noise properties and work as the BBPD. Adaptive LuTs are implemented for the DAC and DTC control construction. This effectively improves system robustness to the environment variation and avoids the static offset of the CMP. Cascaded DTC is implemented in this work for the long-range and high-resolution delay. Fine resolution bank DCO is adopted to avoid the limit cycle problem. The OSPLL achieves 5.79-ps rms jitter and −36.0-dBc worst fractional spur with 4.97-mW power consumption in the fractional-*N* mode, corresponding to −217.8-dB FoM.

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Junjun Qiu (Graduate Student Member, IEEE) received the B.Sc. degree in electrical and electronic engineering from the East China University of Science and Technology, Shanghai, China, in 2016, and the M.E. degree in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2018, where she is currently pursuing the Ph.D. degree in electrical and electronic engineering.

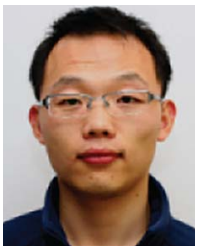
She has been focusing on fully synthesizable digital baseband circuit design for sub-GHz wireless transceiver systems. Her current research interests include high-performance phase-locked loop design and mixed-signal wireless communication system design for Bluetooth low energy.

Ms. Qiu was a recipient of the IEEE SSCS Student Travel Grant Award in 2020.

Zheng Sun (Member, IEEE) was born in Yancheng, China, in 1993. He received the B.S. degree in information engineering from Southeast University, Nanjing, China, in 2014, the M.S. degree in information, production, and systems engineering from Waseda University, Fukuoka, Japan, in 2015, and the Ph.D. degree in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2021.

From April 2021 to July 2021, he was a Post-Doctoral Researcher with Tokyo Institute of Technology. He is currently with Apple Inc., Tokyo, working on wireless connectivity. He was involved in low-power transceivers for the Internet of Things, mixed-signal circuits, and low-power digital phase-locked loop (PLL) designs. His research interests include transceivers for Bluetooth low energy, low-power/high-performance LC-voltage-controlled oscillator (VCO) for ISM/5G applications, and ultra-low-jitter PLLs for 5G cellular and harmonic suppression techniques for the power amplifier.

Dr. Sun also serves as a Reviewer for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the *Microelectronics Journal* (Elsevier), and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.



Bangan Liu (Member, IEEE) received B.Eng. degree from Northwestern Polytechnical University, Xi'an, China, in 2011, the M.S. degree from the University of Science and Technology of China, Hefei, China, in 2014, and the Ph.D. degree from Tokyo Institute of Technology, Tokyo, Japan, in 2019.

He was an Intern with the Apple Japan Design Center, Tokyo, in 2019. He is currently with Qualcomm Inc., San Diego, CA, USA, where he develops high-performance 5G cellular radio frequency integrated circuits (RFICs). His research interests include frequency synthesizers, digital-intensive/digitally assisted mixed-signal systems, and RF/mm-Wave circuits.

Dr. Liu also serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, and the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.

Wenqian Wang (Student Member, IEEE) was born in Xuancheng, China. He received the B.Eng. degree from the School of Microelectronics, Xidian University, Xi'an, China, in 2019. He is currently pursuing the master's degree with Tokyo Institute of Technology, Tokyo, Japan.

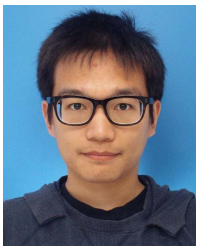
His current research interests include analog and mixed-signal circuits, as well as frequency synthesizers.

Dingxin Xu (Graduate Student Member, IEEE) received the B.Eng. degree from the Southern University of Science and Technology, Shenzhen, China, in 2018, and the M.Eng. degree from Tokyo Institute of Technology, Tokyo, Japan, in 2020, where he is currently pursuing the Ph.D. degree in electronic engineering.

His current research interests include mixed-signal circuit and frequency synthesizer design.

Hans Herdian (Member, IEEE) was born in Bekasi, Indonesia. He received the B.Sc. degree from Bandung Institute of Technology, Bandung, Indonesia, in 2016, and the M.S. degree from Tokyo Institute of Technology, Tokyo, Japan, in 2018, where he is currently pursuing the Ph.D. degree.

His research interests include passive components characterization and performance enhancement on the CMOS process for mm-Wave applications.



Hongye Huang (Member, IEEE) was born in Guilin, China, in 1994. He received the B.E. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2016, and the M.E. degree from Tokyo Institute of Technology, Tokyo, Japan, in 2018, where he is currently pursuing the Ph.D. degree.

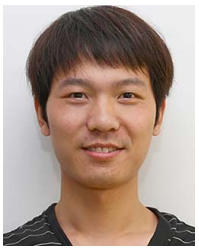
His current research interests include mixed-signal integrated circuits and frequency synthesizers.

Mr. Huang is a scholarship recipient of the Watanuki International Scholarship Foundation in fiscal years 2020 and 2021.

Yuncheng Zhang (Graduate Student Member, IEEE) received the B.S. and M.E. degrees in electrical engineering from the University of Science and Technology of China (USTC), Hefei, China, in 2013 and 2016, respectively. He is currently pursuing the Ph.D. degree with Tokyo Institute of Technology, Tokyo, Japan.

His research interests include power-efficient wireless transceivers, all-digital phase-locked loops, and analog-to-digital converters.

Mr. Zhang was a recipient of the IEEE SSCS Student Travel Grant Award in 2019 and the Best Design Award at the IEEE/ACM ASP-DAC University Design Contest in 2021.



Yun Wang (Member, IEEE) received the B.S. and M.S. degrees from the University of Electronic Science and Technology of China, Chengdu, China, in 2011 and 2014, respectively, and the Ph.D. degree in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2019.

He was an Intern with Pohang University of Science and Technology, Pohang, South Korea, in 2013, and Device Technology Laboratories, NTT Corporation, Atsugi, Japan, in 2016. He is currently a Post-Doctoral Researcher with Tokyo Institute of Technology. His research interests include CMOS radio frequency (RF)/millimeter-wave wireless systems, 5G phased-array mobile systems, and satellite communication.

Dr. Wang was a recipient of the IEICE Best Paper Award in 2018, the Best Student Paper Award (First Place) at the 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), and the Seiichi Tejima Research Award in 2021. He also serves as a reviewer for IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, and the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.

Jian Pang (Member, IEEE) received the bachelor's and master's degrees from Southeast University, Nanjing, China, in 2012 and 2014, respectively, and the Ph.D. degree from the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, in 2019.

From 2019 to 2020, he was a Post-Doctoral Researcher with Tokyo Institute of Technology, where he is currently a Special Appointed Assistant Professor, focusing on 5G millimeter-wave systems. His current research interests include high-data-rate area-efficient millimeter-wave transceivers, power-efficient power amplifiers for 5G mobile systems, MIMO, and mixed-signal systems.

Dr. Pang was a recipient of the IEEE SSCS Student Travel Grant Award in 2016, the IEEE SSCS Predoctoral Achievement Award for 2018–2019, and the Seiichi Tejima International Student Research Award in 2020. He also serves as a Reviewer for IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I & II, and IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS.

Hanli Liu (Member, IEEE) received the B.S. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2013, and the M.E. degree in physical electronics and the Ph.D. degree in physical electronics with a focus on low-power transceivers for Internet-of-Things and low-power low-jitter frequency synthesizers from Tokyo Institute of Technology, Tokyo, Japan, in 2015 and 2018, respectively.

He was an Intern with the Mixed-Signal IC Group, Toshiba Cooperate Research and Development Center, Kawasaki, Japan, in 2017, where he was involved in studying digital phase-locked loop (PLL) architectures. He was with Samsung Semiconductor Inc., San Jose, CA, USA, where he was involved in the high-speed SerDes for 5G and high-performance PLL design. He is currently with Broadcom Inc., San Jose, where he is involved in the low-power mixed-signal design, such as digital-PLL and analog-to-digital converters (ADCs). His research interests include ultra-low-power wireless transceivers for Bluetooth low-energy applications, low-power low-jitter digital PLLs, and ultra-low-jitter PLLs for 5G cellular.

Dr. Liu was a recipient of the Japanese Government (MEXT) Scholarship, the SSCS Predoctoral Achievement Award for 2017–2018, and the Chinese Government Award for Outstanding Self-Financed (non-government sponsored) Students Abroad in 2019. He also serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SOLID-STATE CIRCUITS LETTERS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.

Masaya Miyahara (Member, IEEE) received the B.E. degree in mechanical and electrical engineering from Kisarazu National College of Technology, Kisarazu, Japan, in 2004, and the M.E. and Ph.D. degrees from the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, in 2006 and 2009, respectively.

From 2009 to 2017, he was with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, where he has been an Assistant Professor since 2009. He is currently an Associate Professor with the Institute of Particle and Nuclear Studies, High Energy Accelerator Research Organization, Ibaraki, Japan. His research interests are mixed-signal circuits and sensor read-out large-scale integration (LSI) for particle and nuclear physics experiments.

Dr. Miyahara is also a member of the IEEE Solid-State Circuits Society and The Institute of Electronics, Information and Communication Engineers (IEICE). He is/was a member of the Technical Program Committees of IEEE Asian Solid-State Circuits Conference (A-SSCC) and an Associate Editor of *IEICE Transactions on Electronics*.

Atsushi Shirane (Member, IEEE) received the B.E. degree in electrical and electronic engineering and the M.E. and Ph.D. degrees in electronics and applied physics from Tokyo Institute of Technology, Tokyo, Japan, in 2010, 2012, and 2015, respectively.

From 2015 to 2017, he was with Toshiba Corporation, Kawasaki, Japan, where he developed an 802.11ax Wireless LAN RF transceiver. From 2017 to 2018, he was with Nidec Corporation, Kawasaki, where he researched intelligent motors with wireless communication. He is currently an Assistant Professor with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology. His current research interests include RF CMOS transceiver for Internet of Things (IoT), 5G, and satellite communication.

Dr. Shirane was a member of the IEEE Solid-State Circuits Society and the Institute of Electronics, Information and Communication Engineers (IEICE).

Kenichi Okada (Senior Member, IEEE) received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively.

From 2000 to 2003, he was a Research Fellow of the Japan Society for the Promotion of Science at Kyoto University. In 2003, he joined Tokyo Institute of Technology, Tokyo, Japan, as an Assistant Professor, where he is currently a Professor of electrical and electronic engineering. He has authored or coauthored more than 400 journal articles and conference papers. His current research interests include millimeter-wave CMOS wireless transceivers for 20/28/39/60/77/79/100/300 GHz for 5G, WiGig, satellite and future wireless systems, digital phase-locked loop (PLL), synthesizable PLL, atomic clock, and ultra-low-power wireless transceivers for Bluetooth low-energy and sub-GHz applications.

Prof. Okada is/was a member of the Technical Program Committees of the IEEE International Solid-State Circuits Conference (ISSCC), the VLSI Circuits Symposium, the European Solid-State Circuits Conference (ESSCIRC), and the Radio Frequency Integrated Circuits Symposium (RFIC). He is also a member of the Institute of Electronics, Information and Communication Engineers (IEICE), the Information Processing Society of Japan (IPSJ), and the Japan Society of Applied Physics (JSAP). He was a recipient or co-recipient of the Ericsson Young Scientist Award in 2004, the IEEE Asian Solid-State Circuits Conference (A-SSCC) Outstanding Design Awards in 2006 and 2011, the ASP-DAC Special Feature Award in 2011, Best Design Awards in 2014 and 2015, the MEXT Young Scientists' Prize in 2011, the JSPS Prize in 2014, the Suematsu Yasuharu Award in 2015, the MEXT Prizes for Science and Technology in 2017, the RFIT Best Paper Award in 2017, the IEICE Best Paper Award in 2018, the RFIC Symposium Best Student Paper Award in 2019, the IEICE Achievement Award in 2019, the DOCOMO Mobile Science Award in 2019, the IEEE/ACM ASP-DAC, the Prolific Author Award in 2020, the Kenjiro Takayanagi Achievement Award in 2020, the KDDI Foundation Award in 2020, the IEEE CICC, Best Paper Award in 2020, and more than 50 other international and domestic awards. He is/was also a Guest Editor and an Associate Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), an Associate Editor of IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (T-MTT), and a Distinguished Lecturer of the IEEE Solid-State Circuits Society (SSCS).