A 4-Element Digital Modulated Polar Phased-Array Transmitter With Phase Modulation Phase-Shifting

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***Abstract*— A novel architecture of a digital modulated polar phased-array transmitter with phase modulation (PM) phase-shifting and feed-forward controlled dynamic matching (FFCDM) is presented in this article. Phase-shifting in a PM signal path is utilized in each element, which shares many components including a phase modulator, baseband, and IF components. The characteristics of the proposed architecture are analyzed. With a constant envelope of PM signals, the implicit nonlinearity of the phase shifter in this architecture has low impact on the linearity performance of a phased-array system. Meanwhile, low phase error can be achieved by high-resolution phase interpolation with the digital predistortion (DPD) technique. Efficiency for both saturated and 6-dB back-off power is enhanced by digital power amplifier (DPA) with FFCDM. As a proof of concept, a 3–7 GHz 4-element phased-array transmitter is designed and fabricated in 40-nm CMOS based on the proposed method. The measured root-mean-square (rms) phase error of 0.3°, effective phase shifting resolution of 9-bit, and peak system efficiency of 38.2% are achieved. For 40 MHz 64-QAM modulation signal, it exhibits EVM of 5.38% and 5.37%, P_{out} of 14.30 and 14.46 dBm, and PAPR of 7.08 and 6.97 at 3.5 and 5.2 GHz, respectively. The measured peak EIRP is 35.6 dBm with a unit antenna gain of 2.98 dBi at 5 GHz. The radiation patterns with 0°, 15°, 30°, and 45° steering are measured based on monopole antennas. Meanwhile, the array achieves <4.7% and <5.9% EVM for 64-QAM signals with bandwidths of 20 and 40 MHz, respectively.**

***Index Terms*— Digital phase shifter, digital power amplifier (DPA), phase modulation (PM) phase-shifting, phased-array, polar transmitter, wideband.**

I. Introduction

PHASED-ARRAY transmitters (TXs) with beam steering, large instantaneous bandwidth, and high spectrum efficiency are highly demanded for high-speed wireless links with wide coverage and multi-standard. It increases the signal-to-noise ratio (SNR) and channel capacity. Low-cost planar antenna array with compact size can be used for phased-array system to enhance the directivity and gain instead of expensive directional antenna (e.g., horn antenna, parabolic antenna) with large size. Larger effective isotropic radiated power (EIRP) is achieved with spatial power combining to overcome the limited output power in deep sub-micrometer CMOS technology displacing large on-chip power combining network [1]. Hence, wider coverage can be achieved.

Radio frequency (RF) phase-shifting [2]–[10], local oscillator (LO) phase-shifting [11]–[18], intermediate frequency (IF) phase-shifting, and baseband (BB) phase-shifting topologies [19]–[25] are conventional phased-array architectures with phase shifters in RF, LO, IF, and BB paths, respectively. For architectures with phase shifters in signal path (i.e., RF and IF phase-shifting), the system linearity and amplitude variation are affected by phase shifters significantly. LO phase-shifting requires extra LO buffers and independent mixers, while the effect of phase shifter nonlinearity on system is prevented due to a constant envelope of LO. Furthermore, spectrum-efficiency phased-array TXs remain challenging for traditional phased-array architectures. Direct digital modulated TXs [26]–[34] exhibit advantages in energy efficiency and compatibility with digital baseband, especially in deep sub-micrometer CMOS technology. The digital modulated Cartesian beamforming architecture [7] with quadrature spatial combining and LO phase shifting exhibits improved efficiency using digital power amplifier (DPA). Nevertheless, the drawbacks of LO phase shifting exist in this topology. The design of phased array TXs with compact circuit size, high linearity, low amplitude variation, and high spectrum efficiency still remains challenges.

The transmitted beam with a specific scanning resolution (θ) shows more significant discontinuity with a larger transmission radius. The beam discontinuity causes degraded array factor and EVM, especially for narrow beam. Insufficient beam-steering resolution in large-sized phased-array will cause SNR degradation [18]. For a larger array size, the higher phase resolution is required. Meanwhile, the scanning resolution can be improved with larger antenna spacing. Hence, phased-array system with high phase resolution can improve the signal integrity in wide transmission range and reduce the system size with smaller antenna spacing. Many techniques are developed to improve the performance of phase shifters. Passive phase shifters [4]–[6] show high linearity with bulky circuit size and relatively lower phase resolution. Active

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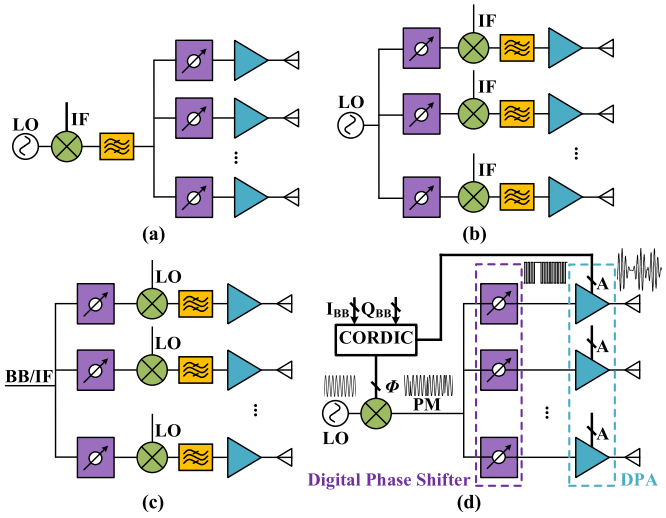

Fig. 1. Phased-array TX architectures with different phase-shifting locations. (a) RF phase-shifting. (b) LO phase-shifting. (c) BB or IF phase-shifting. (d) Simplified block diagram of proposed digital modulated polar phased-array TXs with PM phase-shifting.

phase shifters [2], [3], [8]–[10] with vector-sum achieve better phase resolution with worse linearity. Delay-based phase shifting with $\Sigma\Delta$ delay locked loop [24] is used to realize phase shifting. However, the frequency-dependent phase resolution of the delay step decreases for higher frequency.

To address above issues, a digital modulated phased-array TX prototype with phase modulation (PM) phase-shifting is proposed. With the phase shifter inserted in PM path without amplitude modulation (AM), the impact of phase shifter nonlinearity on TX performance is decreased. PM phase-shifting shares many components (phase modulator, baseband signal processing, etc.) as RF phase-shifting. Thus, the power consumption and circuit size are decreased. Switch mode DPA and feed-forward controlled dynamic matching (FFCDM) are employed to further improve TX efficiency. Digital phase shifter with vector sum achieves high-resolution phase-shifting.

To demonstrate the prototype, a 3–7 GHz 4-element digital modulated polar phased-array TX in 40-nm LP CMOS is designed and fabricated [35]. It achieves 9-bit effective phase resolution with an root-mean-square (rms) phase error of 0.3°, rms amplitude error of 0.2 dB, and peak system efficiency of 38.2%. The drain efficiency (DE) at saturated and 6-dB back-off power achieves maximum 7.2% and 4.6% improvement with FFCDM, respectively. This article is organized as follows. In Section II, we analyze characteristics of the proposed PM phase-shifting architecture. Trade-offs in the system level are also discussed in Section II. The circuit implementation is presented in Section III. The measurement results are discussed in Section IV. Section V is the conclusion.

II. Theory of Operation

A. PM Phase-Shifting

Fig. 1 compares conventional phased-array TX architectures (RF phase-shifting, LO phase-shifting, and IF/BB phase-shifting) with proposed digital modulated polar phased-array TX with PM phase-shifting. RF phase-shifting shares most components (including mixers, IF amplifiers, etc.) before RF signal split into several paths. Therefore, lower power consumption and compact circuit size can be achieved with RF phase-shifting. What is more, both RF phase-shifting and IF phase-shifting employ phase shifters in the signal path. Thus, the characteristics of phase shifters in RF/IF phase-shifting, including $P_{1\,\mathrm{dB}}$, amplitude variation, noise figure, and so on, have impact on system performance, which become one of the bottlenecks of high-performance system. The drawback of phase shifter nonlinearity can be avoided in LO phase-shifting due to the constant envelope of LO. Nevertheless, LO phase-shifting requires a mixer for each element and extra LO buffers with relatively a larger circuit size and power consumption comparing to RF phase-shifting. LO phase-shifting also requires extra efforts to improve the amplitude variation. IF or BB phase-shifting has no shared RF components, which sacrifices the circuit complexity and power consumption. High-resolution phase-shifting can be achieved by baseband processor for BB phase-shifting, which is usually more power efficient than phase-shifting in LO or RF.

To address above issues, digital modulated polar phased-array TX with PM phase shifting is proposed as shown in Fig. 1(d). The circuit topology of the proposed architecture is relatively simple. Only two components (phase shifter and DPA) are located in each TX element before antenna, which is the same as RF phase-shifting. Amplitude (A) and phase (Φ) components are converted from I/Q baseband signals by coordinate rotation digital computer (CORDIC) algorithm. A phase modulator performs up-conversion of Φ and generates PM signal. Phase shifters are inserted in PM path between the phase modulator and DPA. Since the phase shifter is driven by PM signal with a constant envelope, the nonlinearity of a phase shifter has low impact on the system linearity similar as LO phase-shifting. In each element of the phased-array TX, PM signal after phase-shifting and A are combined by DPA to get amplified RF signal. Meanwhile, the PM phase-shifting signal is converted to rail-to-rail signal by digital circuits to drive the switch-cells in DPA. Hence, the amplitude variation from the phase shifter can be suppressed by this architecture.

The proposed architecture of digital modulated polar TX with PM phase-shifting exhibits advantages in efficiency comparing to conventional phased-array architectures. First, DPA as the most power hungry block in the TX has the merit of high efficiency. It is comprised of power combined unit cells switched on/off, which usually operate in switch mode (e.g., Class-D, Class-E) with high efficiency. It breaks the trade-off between efficiency and linearity for conventional switch-class PAs. The conventional phased-array TX usually adopts linear PAs (e.g., Class-A and Class-AB) with better linearity in sacrifice of efficiency to support complex modulations. The linearity is also limited for conventional linear PAs (e.g., Class-A and Class-AB) due to the decreased linear region of transistors with lower supply in advanced CMOS technology. Second, the proposed architecture shares many components as RF phase-shifting. Although some additional digital components, including digital predistortion (DPD), CORDIC, finite impulse responses (FIRs), and so on, could be

required comparing to RF phase-shifting, the power consumption of these digital components is relatively low in advanced CMOS technology.

Therefore, the proposed architecture shows the following advantages: 1) it decreases the impact of nonperfect phase shifters on the system, including nonlinearity and amplitude variation; 2) it shares many components as RF phase-shifting, where the circuit topology is simplified with potentially smaller size and power consumption; and 3) the system efficiency is improved with good linearity by digital modulated polar TX.

B. Phase Shifter Impact on System

For typical RF phase-shifting in Fig. 1(a), the fundamental frequency component of the output signal from single TX element is expressed as

$$S_{\mathrm{RF}} = G_{\mathrm{PS}}(A(t), \varphi_{\mathrm{PS}}(t)) \cdot G_{PA}(A(t)) \cdot A(t) \cdot \cos(\omega_0 t + \Phi(t) + \varphi_{\mathrm{PS}}(t)) \quad (1)$$

where $A(t) \cdot \cos(\omega_0 t + \Phi(t))$ is the input signal of the phase shifter, $\varphi_{\mathrm{PS}}(t)$ is radian of phase shift determined by the phase shifter, $G_{\mathrm{PS}}(A(t), \varphi_{\mathrm{PS}}(t))$ is amplitude $A(t)$ and phase shift $\varphi_{\mathrm{PS}}(t)$ dependent gain of the phase shifter, and $G_{PA}(A(t))$ is $A(t)$ dependent gain of the PA. Therefore, both nonlinearity and amplitude variation are risen by the phase shifter in RF phase-shifting.

For digital modulated polar phased-array with PM phase-shifting in Fig. 1(d), $\cos(\omega_0 t + \Phi(t))$ is PM signal with a constant envelope as the input of the phase shifter. Therefore, the gain of the phase shifter $G_{\mathrm{PS}}(\varphi_{\mathrm{PS}}(t))$ is independent of $A(t)$. It is still related to $\varphi_{\mathrm{PS}}(t)$, which produces amplitude variation of the TX. The fundamental frequency component of the output signal from single TX element is expressed by

$$S_{\mathrm{PM}} = G_{\mathrm{PS}}(\varphi_{\mathrm{PS}}(t)) \cdot G_{\mathrm{DPA}}(A(t)) \cdot \cos(\omega_0 t + \Phi(t) + \varphi_{\mathrm{PS}}(t)) \quad (2)$$

where $G_{\mathrm{DPA}}(A(t))$ is amplitude-dependent gain of the DPA. Compared to (1), the implicit nonlinearity of the phase shifter has no impact on the system. Meanwhile, considering the signal conversion of the PM phase-shifting signal with amplitude variation on rail-to-rail signal by digital operation of the DPA, S_{PM} is approximated by

$$S_{\mathrm{PM}} \approx G_{\mathrm{PS}} \cdot G_{\mathrm{DPA}}(A(t)) \cdot \cos(\omega_0 t + \Phi(t) + \varphi_{\mathrm{PS}}(t)). \quad (3)$$

In this case, the gain of the phase shifter G_{PS} is close to time-invariant. Therefore, the impact of the phase shifter on the system is suppressed in this architecture.

To validate the analysis about nonlinearity, system simulation is done by ADS Ptolemy simulator to compare PM and RF phase-shifting as depicted in Fig. 2. IEEE 802.11a signal with a carrier frequency of 5.2 GHz is adopted. The corresponding simulation model diagram is shown in Fig. 3. Note that a DPA with ideal linearity for PM phase shifting and an ideal analog PA for RF phase shifting are used here to see the impact of the phase shifter. $\varphi_{\mathrm{PS}}(t)$ is set to a constant value. For RF phase-shifting, with decreasing $P_{1\,\mathrm{dB}}$ of the phase shifter, the TX

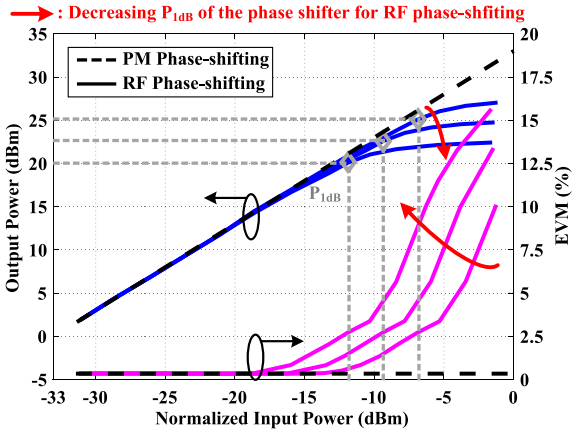

Fig. 2. Simulated nonlinearity impact of the phase shifter for PM phase shifting and RF phase-shifting.

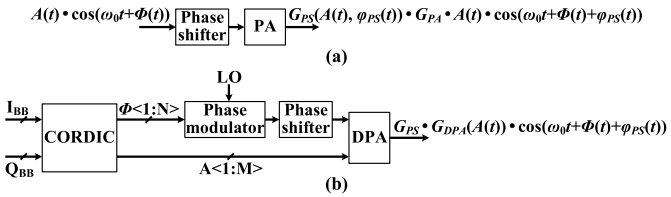

Fig. 3. Simulation model diagram for (a) RF phase shifting and (b) PM phase shifting.

$P_{1\,\mathrm{dB}}$ decreases accordingly. Meanwhile, the nonlinearity of the phase shifter has a large influence on the EVM performance of the system. The peak EVM is worse with lower $P_{1\,\mathrm{dB}}$ of the phase shifter. For PM phase-shifting, no gain compression is observed from the simulation results. The EVM performance would not be deteriorated by the phase shifter in PM phase-shifting. Therefore, the design effort of the phase shifter in the proposed architecture can be focused on phase error and phase shifting resolution rather than $P_{1\,\mathrm{dB}}$ and gain variation.

C. Delay Mismatch

Due to the separated paths of AM and PM signals in polar TX, the delay mismatch Δt between AM and PM signals causes signal integrity and intermodulation deterioration. S_{PM} with delay mismatch is represented by

$$S_{\mathrm{PM}} = G_{\mathrm{PS}} \cdot G_{\mathrm{DPA}}(A(t)) \cdot \cos(\omega_0 t + \Phi(t + \Delta t) + \varphi_{\mathrm{PS}}(t)). \quad (4)$$

Note that nonideality of the phase shifter is omitted (with constant G_{PS}) to simplify the analysis. $\varphi_{\mathrm{PS}}(t)$ is introduced by equivalent RF delay of the phase shifter. Time-variant $\varphi_{\mathrm{PS}}(t)$ in (4) causes signal distortion after demodulation. According to the principle of phased-array, the electromagnetic waves radiated from different elements with various time delays are phase synchronized and energy enhanced at the direction of θ. Hence, the phase shift $\varphi_{\mathrm{PS}}(t)$ is eliminated at the main lobe direction. The electromagnetic waves at other directions canceled each other to a great extent due to different RF phases. Thus, the spatial combined beam with an angle of

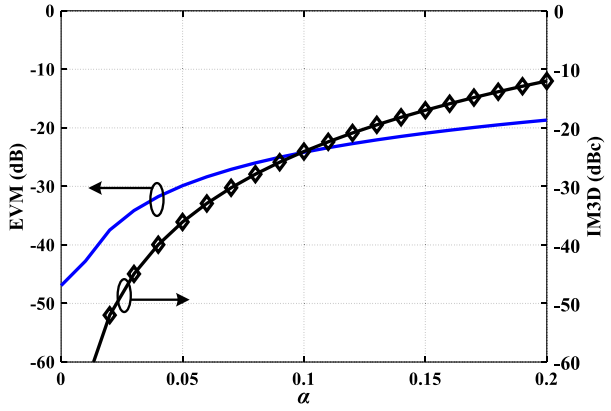

Fig. 4. Calculated EVM and IM3D of 64-QAM signal versus α.

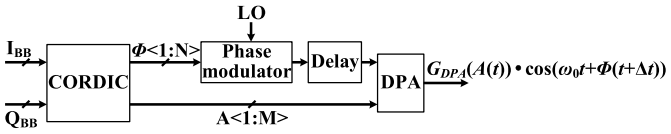

Fig. 5. Simulation model diagram for delay mismatch analysis and AM/PM resolution.

θ is generated with the following propagation signal:

$$S_{\text{Beam}} = G_{\text{AntArray}} \cdot G_{\text{PS}} \cdot G_{\text{DPA}}(A(t)) \cdot \cos(\omega_0 t + \Phi(t + \Delta t)) \quad (5)$$

where G_{AntArray} is the equivalent gain from the antenna array. For single-element TX with the phase shifter, since the sampling rate of $\varphi_{\text{PS}}(t)$ is usually much lower than the baseband signal, $\varphi_{\text{PS}}(t)$ can be seen as a constant value comparing to $\Phi(t + \Delta t)$. Here, as the initial phase of the RF signal, $\varphi_{\text{PS}}(t)$ can be omitted as in (5). Thus, S_{PM} can be represented as

$$S_{\text{PM}} = G_{\text{PS}} \cdot G_{\text{DPA}}(A(t)) \cdot \cos(\omega_0 t + \Phi(t + \Delta t)) \quad (6)$$

Equation (6) is used here for delay mismatch characteristics analysis. Assuming B_{RF} is modulation bandwidth. The delay factor α is defined as

$$\alpha = \Delta t \cdot B_{\text{RF}} = \Delta t / T_{\text{BB}} \quad (7)$$

where T_{BB} is the baseband clock cycle before upsampling. A 64-QAM modulation signal is used here to evaluate the performance. EVM performance related to α is calculated by MATLAB. The calculated EVM versus α according to (6) is plotted in Fig. 4 (blue line). Note that the corresponding simulation model diagram is shown in Fig. 5. It is found that EVM is not related to RF carrier frequency. It is dominated by α. More rigid delay mismatch is required for larger B_{RF} to achieve the same EVM. For 20 MHz B_{RF}, Δ_t < 2.5 nS is necessary for EVM < −30 dB. For 2 GHz B_{RF}, Δ_t <25 pS is necessary for EVM < −30 dB. The intermodulation distortion of two-tone signal with frequency space of B_{RF} is introduced by delay mismatch. The IM3D is determined by [27]

$$\text{IM3D} \approx 2\pi\alpha^2. \quad (8)$$

Calculated IM3D according to (8) is given in Figs. 4 and 6. For 20 MHz B_{RF} and Δt < 2 nS, IM3D of −40 dBc is achieved. For 2 GHz B_{RF}, Δt < 20 pS is required to achieve −40-dBc IM3D.

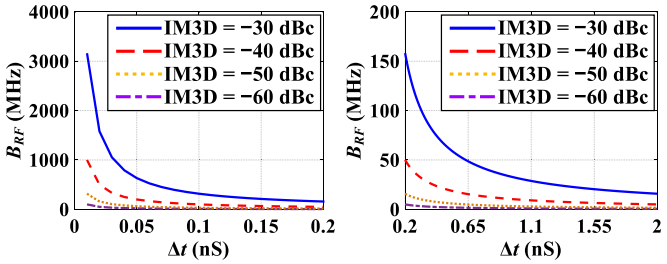

Fig. 6. Calculated impact of Δ_t and B_{RF} on IM3D.

The delay mismatch variation for different element is critical for the scalability to N elements of the proposed architecture, especially for large arrays. With the digital nature of amplitude control word (ACW) and Φ control codes, the delay mismatch between amplitude and PM signals in practical circuit implementation depends on the number of digital buffers in the routings instead of the routing length. Longer routing in large array system usually requires more digital buffers to keep the driving capability. Therefore, to minimize the delay mismatch variation for different element of the array, the same number of buffers for ACW and Φ control codes should be used for each element including the element close to input codes. The power consumption of buffers for ACW and Φ control codes will also increase for larger array.

D. Trade-Offs in Digital Polar Phased-Array TX

The trade-offs of system performance related to amplitude resolution, PM resolution, delay mismatch, and modulation bandwidth are discussed. System simulation is done by 802.11a signal with PAPR of 8.2 in ADS. The corresponding simulation model diagram is shown in Fig. 5. As shown in Fig. 7(a), PM resolution dominates EVM performance compared to AM resolution. With a 5-bit/6-bit PM signal, EVM is only −13.3 dB/−19.2 dB with an AM resolution of 5 to 12-bit. With a PM resolution ≥10-bit, EVM is better than −28 dB with an AM resolution of 5 to 12-bit. The spectrum noise floor is related to the quantization noise determined by resolution. Fig. 7(b) demonstrates TX output spectrum with AM and PM resolutions of 6-bit, 8-bit, 10-bit, and 12-bit. Higher AM and PM resolutions improve out-of-band spectrum significantly. Considering the nonlinearity of DPA and digital phase modulator, the effective number of bits (ENOB) is degraded. Fig. 8 shows the simulated EVM versus delay factor under different resolutions. Note that the required resolution and delay mismatch for the system can be estimated for specific modulation bandwidth.

To analyze the condition with various delay mismatches for different TX elements of the phased-array system, the simulation model of 4-element phased-array TX is used, as shown in Fig. 9. Here, the propagation paths between each TX antenna and RX antenna are assumed to be the same and meet the theoretical definition of a phased array. The delay factors for four channels are defined to be α_A, α_B, α_C, and α_D,

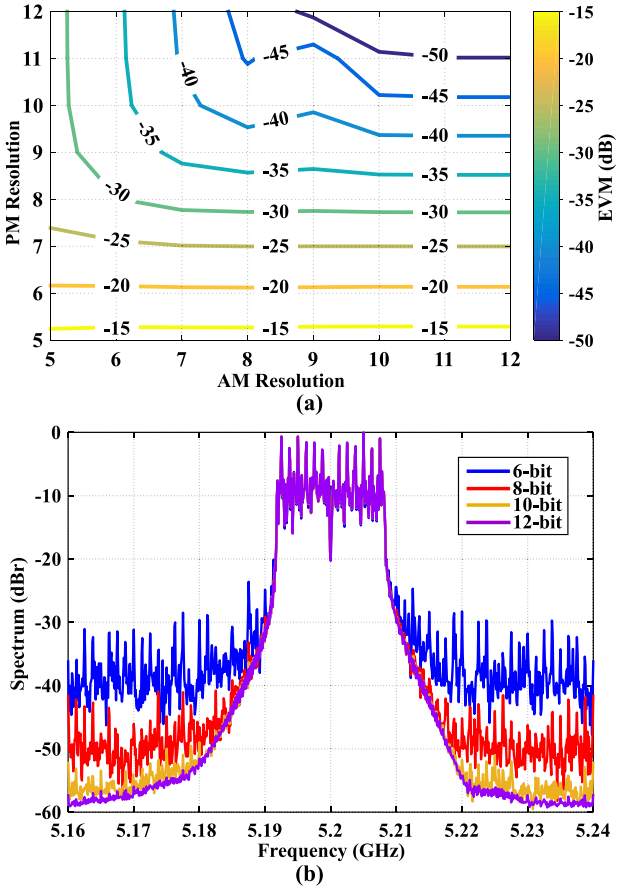

Fig. 7. Simulated (a) EVM contour and (b) spectrum versus AM and PM resolution.

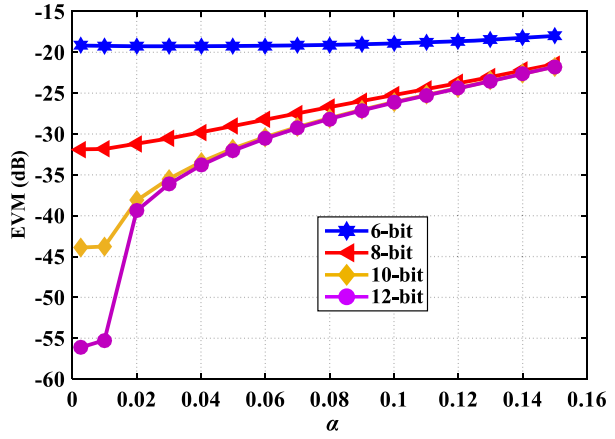

Fig. 8. Simulated EVM versus delay factor under different resolution for 802.11a signal with a 20-MHz bandwidth.

respectively. To simplify the analysis, the variables α_C and α_D are set to be fixed. Then, the calculated effects of α_A and α_B on EVM of phased-array TX are shown in Fig. 10(a) and (b). $\alpha_C = \alpha_D = 0$ in Fig. 10(a), while $\alpha_C = \alpha_D = 0.05$ in Fig. 10(b). The delay factor of each channel affects the EVM, while the EVM is decreasing with decreased delay factors. To further investigate the influence of delay mismatch on the phased-array system, the EVM versus α_{av} is shown in Fig. 11, where α_{av} is the average delay mismatch of four elements, that

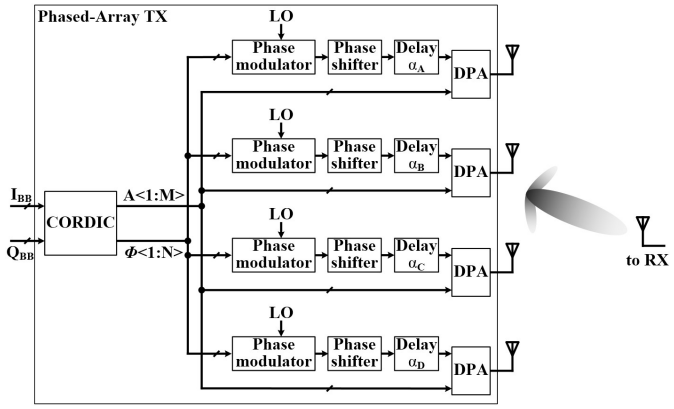

Fig. 9. Simulated model diagram for delay mismatch analysis in 4-element phased-array TX.

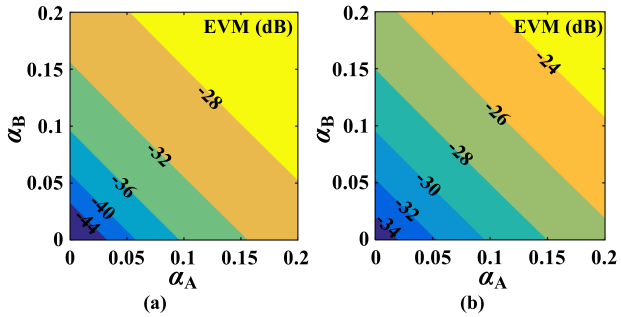

Fig. 10. Calculated impact of α_A and α_B on EVM of 4-element phased-array TX. (a) $\alpha_C = \alpha_D = 0$. (b) $\alpha_C = \alpha_D = 0.05$.

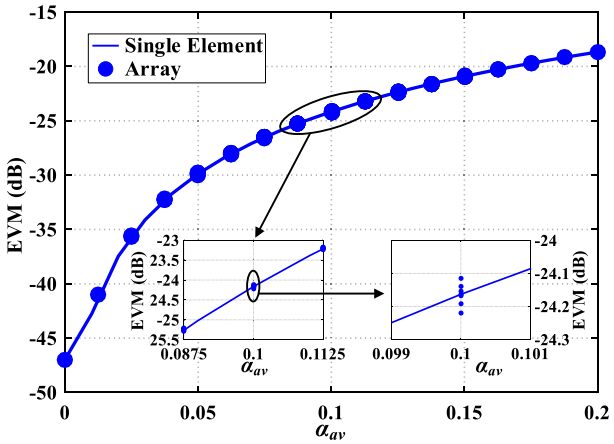

Fig. 11. Calculated impact of α_{av} on EVM of 4-element phased-array TX.

is, $\alpha_{av} = (\alpha_A + \alpha_B + \alpha_C + \alpha_D)/4$. Meanwhile, the EVM of a single element is compared. It is notable that there is a good agreement between the single element and array. Therefore, the delay mismatch requirement for the array level is similar as single-element TX.

III. Circuit Implementation

A. Architecture

The block diagram of the proposed digital modulated polar phased-array TX is shown in Fig. 12. The chip adopts a

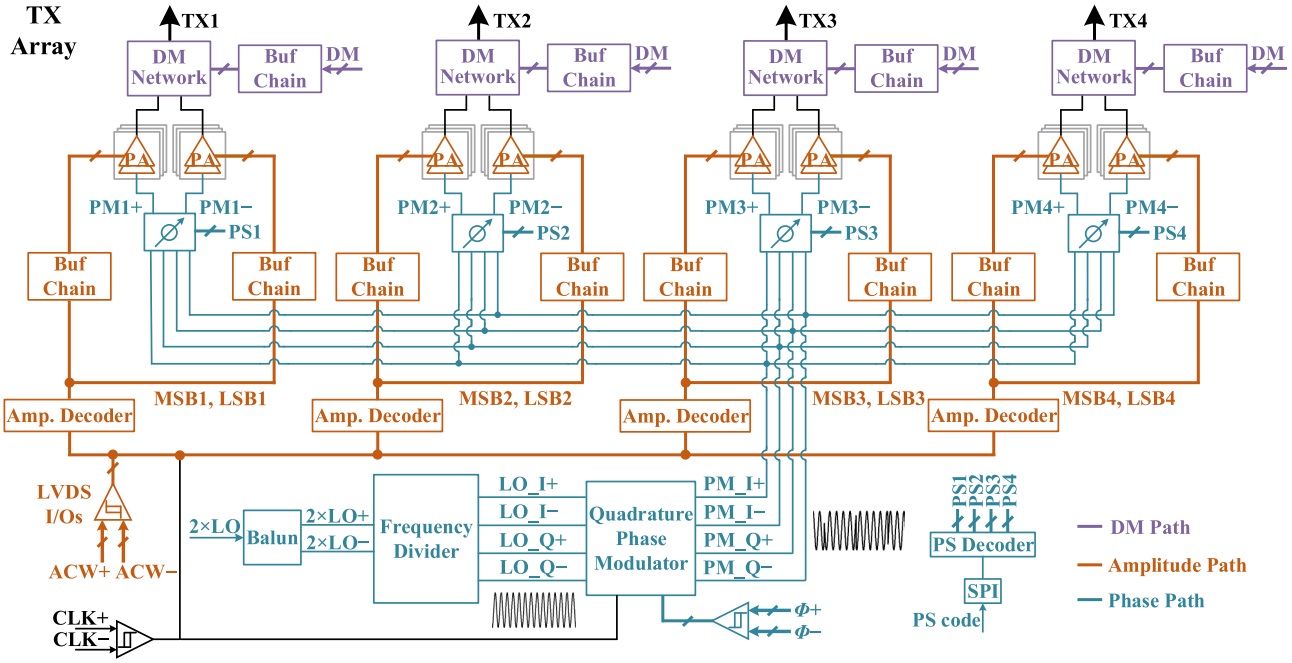

Fig. 12. Block diagram of the proposed digital modulated polar phased-array TX.

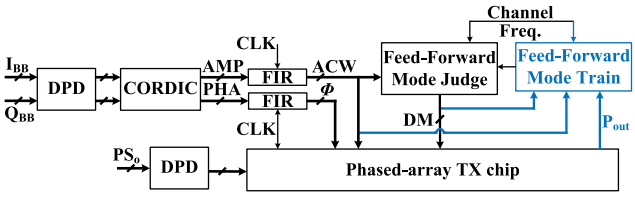

Fig. 13. Digital signal generation for the phased-array TX.

4-element TX array. Each element combines amplitude path, phase path, and dynamic matching (DM) path. The RF signal is reconstructed and amplified with a controllable RF phase for beam steering. According to the system analysis in Section II, 10-bit resolution for AM and PM signals is determined. In the phase path, 2 × LO input is converted to differential signals by a wideband balun. Quadrature signals (LO_I+, LO_I−, LO_Q+, LO_Q−) generated from a frequency divider are interpolated by a quadrature phase modulator to produce quadrature PM signals (PM_I+, PM_I−, PM_Q+, PM_Q−). Four independent phase shifters further perform phase-shifting on the PM signals. The control code of the phase shifter is pre-distorted and sent to the chip through an on-chip serial peripheral interface (SPI) controller. In the amplitude path, the TX envelope is restored and amplified by the digitally activated sub-PA arrays controlled by ACW. The feed-forward controlled DM path is adopted to improve the power efficiency at back-off and saturated power in wideband frequency. AM and PM signals are synchronized by the same clock to decrease the delay mismatch. Buffer chains are employed for amplitude and DM signals in the routing to improve driving capability.

Fig. 13 gives the procedures of external digital signal generation for the proposed phased-array TX chip. DPD is performed for the baseband digital signals I_{BB} and Q_{BB} using a 2-D lookup table. The lookup table is obtained from the PM and AM nonlinearity of TX output signals versus the baseband code. The baseband I/Q signals after DPD are decomposed by the CORDIC to generate AM and PM signals. FIR filters are optional for up-sampling and image filtering of the baseband signals. Amplitude control word (ACW) and PM (Φ) are calculated on a PC, downloaded to an FPGA and injected to the chip through low-voltage differential signaling (LVDS) I/Os. The lookup table for the phase shifters is obtained from the phase nonlinearity of TX output signals versus the phase code. The control code of the phase shifter is pre-distorted and sent to the chip through an on-chip SPI controller. The feed-forward mode is first trained by ACW, DM, channel frequency, and measurement output power as marked as blue in Fig. 13. Based on the trained DM modes, instant DM codes are deducted according to ACW and channel frequency.

B. Wideband Phase Modulator

To support wideband operation for the phased-array TX, the quadrature PM signal generation circuits including balun, frequency divider, and phase modulator in Figs. 14 and 15 should simultaneously meet broadband requirements. To generate quadrature PM signals with enhanced I/Q balance and driving capability for the phase shifter, two identical active phase modulators (PM1 and PM2) are adopted. Quadrature PM signals generating scheme with 90° passive phase-shifting from one differential phase modulator is not chosen due to its high insertion loss, large circuit size, and narrow band response. Each phase modulator is composed of four current digital-to-analog converters (I-DACs) and Gilbert type mixers with switches. Phase interpolation is performed by summing

TABLE I
OPERATION STATES OF THE QUADRATURE PHASE MODULATOR

P_1	P_I	P_Q	0	0
P_2	0	0	P_I	P_Q
P_3	P_Q	0	0	P_I
P_4	0	P_I	P_Q	0
LO States (PM1)	LO_I+	LO_I+	LO_I+	LO_I+
	LO_I−	LO_I−	LO_I−	LO_I−
	LO_Q+	LO_Q+	LO_Q+	LO_Q+
	LO_Q−	LO_Q−	LO_Q−	LO_Q−
LO States (PM2)	LO_Q+	LO_Q+	LO_Q+	LO_Q+
	LO_Q−	LO_Q−	LO_Q−	LO_Q−
	LO_I−	LO_I−	LO_I−	LO_I−
	LO_I+	LO_I+	LO_I+	LO_I+
PM_I+	0°–90°	90°–180°	180°–270°	270°–360°
PM_Q+	270°–360°	0°–90°	90°–180°	180°–270°

quadrature vectors as shown in Fig. 15. The output current of the phase-controlled I-DAC is multiplied by quadrature LO signals (LO_I+, LO_I−, LO_Q+, LO_Q−). The operation states of the quadrature phase modulator are listed in Table I. The lower 8-bit baseband PM signal ϕ<7:0> is converted by the I/Q generator to orthogonal signals $P_I = k\cdot\cos\varphi$ and $P_Q = k\cdot\sin\varphi$ (k is the amplitude of the summed vectors P_I and P_Q). Phase selection is performed for P_I and P_Q according to the sign bits ϕ<9:8>, which are mapped to phase control signals (P_1, P_2, P_3, P_4) for I-DACs. In each operation state, two phase control signals are 0, whose multiplied LO signals are marked in gray as depicted in Table I.

Assuming the I-DAC has linear trans-conductance g_m versus control code, the output current of I-DACs is $k\cdot g_m\cdot\cos\varphi$ and $k\cdot g_m\cdot\sin\varphi$. Therefore, the synthesized PM signals are determined as equations (9)–(10), shown at the bottom of the page, where $S(t)$ is square wave toggling between 0 and 1, $A = k\cdot g_m$. According to Fourier transform of the square wave, the fundamental frequency elements of PM_I+ and PM_Q+ are determined by

$$\mathrm{PM_{Ifund}+} = \begin{cases} \dfrac{2\mathrm{RA}}{\pi}\cos(\omega_{\mathrm{LO}}t-\varphi), & \text{quadrant 1}\\ \dfrac{2\mathrm{RA}}{\pi}\cos(\omega_{\mathrm{LO}}t-\varphi+90^\circ), & \text{quadrant 2}\\ \dfrac{2\mathrm{RA}}{\pi}\cos(\omega_{\mathrm{LO}}t-\varphi+180^\circ), & \text{quadrant 3}\\ \dfrac{2\mathrm{RA}}{\pi}\cos(\omega_{\mathrm{LO}}t-\varphi+270^\circ), & \text{quadrant 4} \end{cases} \tag{11}$$

$$\mathrm{PM_{Qfund}}+ = \begin{cases} \dfrac{2\mathrm{RA}}{\pi}\sin(\omega_{\mathrm{LO}}t-\varphi), & \text{quadrant 1}\\ \dfrac{2\mathrm{RA}}{\pi}\sin(\omega_{\mathrm{LO}}t-\varphi+90^\circ), & \text{quadrant 2}\\ \dfrac{2\mathrm{RA}}{\pi}\sin(\omega_{\mathrm{LO}}t-\varphi+180^\circ), & \text{quadrant 3}\\ \dfrac{2\mathrm{RA}}{\pi}\sin(\omega_{\mathrm{LO}}t-\varphi+270^\circ), & \text{quadrant 4.} \end{cases} \tag{12}$$

It can be seen that 90° phase shifting between $\mathrm{PM_{Ifund+}}$ and $\mathrm{PM_{Qfund+}}$ is realized by swapping phase control codes of PM2 compared to PM1.

A frequency divider with current-mode logic latches and drivers produces LO_I+, LO_I−, LO_Q+, LO_Q−, which works from 2 GHz to 9 GHz (output frequency). A Marchand balun in Fig. 14 (bottom) is proposed to enhance inband phase and amplitude balance from 6 to 14 GHz. $\lambda/4$ transmission sections implemented by thick metals M7 and M6 are coupled with a squared spiral scheme. According to below ideal balance condition [36]

$$\frac{S_{31}}{S_{21}} = -\frac{Z_{\mathrm{even}}-Z_{\mathrm{odd}}}{Z_{\mathrm{even}}+Z_{\mathrm{odd}}} = -1 \tag{13}$$

odd-mode effect (Z_{odd}) should be decreased to improve the phase and amplitude balance. The port-coupled compensation

$$\mathrm{PM\_I}+ = \begin{cases} \dfrac{1}{2}\mathrm{RA}\cos\varphi\left(S\left(t-\dfrac{T_{\mathrm{LO}}}{2}\right)-S(t)\right)+\dfrac{1}{2}\mathrm{RA}\sin\varphi\left(S\left(t-\dfrac{3T_{\mathrm{LO}}}{4}\right)-S\left(t-\dfrac{T_{\mathrm{LO}}}{4}\right)\right), & \text{quadrant 1}\\ \dfrac{1}{2}\mathrm{RA}\sin\varphi\left(S\left(t-\dfrac{T_{\mathrm{LO}}}{2}\right)-S(t)\right)-\dfrac{1}{2}\mathrm{RA}\cos\varphi\left(S\left(t-\dfrac{3T_{\mathrm{LO}}}{4}\right)-S\left(t-\dfrac{T_{\mathrm{LO}}}{4}\right)\right), & \text{quadrant 2}\\ -\dfrac{1}{2}\mathrm{RA}\cos\varphi\left(S\left(t-\dfrac{T_{\mathrm{LO}}}{2}\right)-S(t)\right)-\dfrac{1}{2}\mathrm{RA}\sin\varphi\left(S\left(t-\dfrac{3T_{\mathrm{LO}}}{4}\right)-S\left(t-\dfrac{T_{\mathrm{LO}}}{4}\right)\right), & \text{quadrant 3}\\ -\dfrac{1}{2}\mathrm{RA}\sin\varphi\left(S\left(t-\dfrac{T_{\mathrm{LO}}}{2}\right)-S(t)\right)+\dfrac{1}{2}\mathrm{RA}\cos\varphi\left(S\left(t-\dfrac{3T_{\mathrm{LO}}}{4}\right)-S\left(t-\dfrac{T_{\mathrm{LO}}}{4}\right)\right), & \text{quadrant 4} \end{cases} \tag{9}$$

$$\mathrm{PM\_Q}+ = \begin{cases} \dfrac{1}{2}\mathrm{RA}\cos\varphi\left(S\left(t-\dfrac{3T_{\mathrm{LO}}}{4}\right)-S\left(t-\dfrac{T_{\mathrm{LO}}}{4}\right)\right)-\dfrac{1}{2}\mathrm{RA}\sin\varphi\left(S\left(t-\dfrac{T_{\mathrm{LO}}}{2}\right)-S(t)\right), & \text{quadrant 1}\\ \dfrac{1}{2}\mathrm{RA}\sin\varphi\left(S\left(t-\dfrac{3T_{\mathrm{LO}}}{4}\right)-S\left(t-\dfrac{T_{\mathrm{LO}}}{4}\right)\right)+\dfrac{1}{2}\mathrm{RA}\cos\varphi\left(S\left(t-\dfrac{T_{\mathrm{LO}}}{2}\right)-S(t)\right), & \text{quadrant 2}\\ -\dfrac{1}{2}\mathrm{RA}\cos\varphi\left(S\left(t-\dfrac{3T_{\mathrm{LO}}}{4}\right)-S\left(t-\dfrac{T_{\mathrm{LO}}}{4}\right)\right)+\dfrac{1}{2}\mathrm{RA}\sin\varphi\left(S\left(t-\dfrac{T_{\mathrm{LO}}}{2}\right)-S(t)\right), & \text{quadrant 3}\\ -\dfrac{1}{2}\mathrm{RA}\sin\varphi\left(S\left(t-\dfrac{3T_{\mathrm{LO}}}{4}\right)-S\left(t-\dfrac{T_{\mathrm{LO}}}{4}\right)\right)-\dfrac{1}{2}\mathrm{RA}\cos\varphi\left(S\left(t-\dfrac{T_{\mathrm{LO}}}{2}\right)-S(t)\right), & \text{quadrant 4} \end{cases} \tag{10}$$

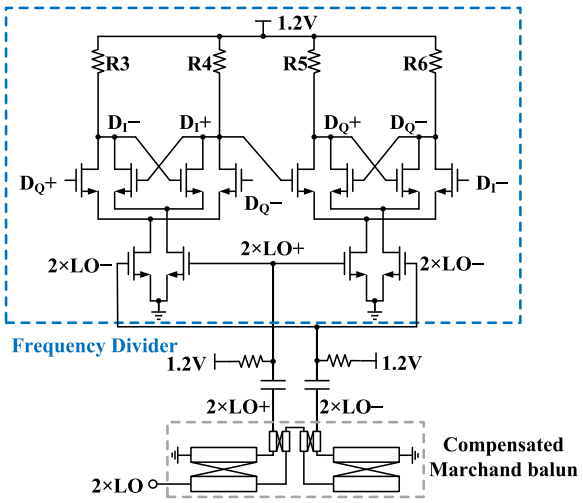

Fig. 14. Quadrature LO signal generation circuits.

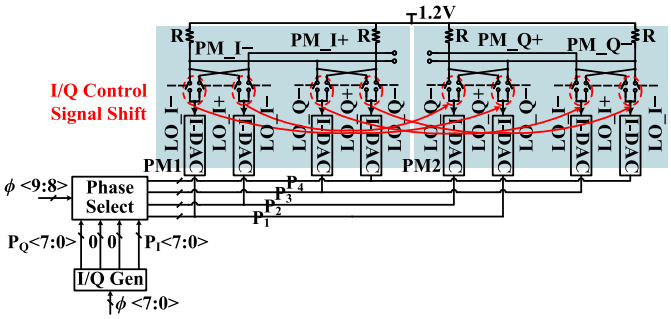

Fig. 15. Quadrature phase modulator.

line and stacked ground-shield are employed to decrease the odd-mode effect. Simulated results with ADS momentum exhibit phase imbalance within ±1.93° and amplitude imbalance within ±0.31 dB, and the insertion loss is from 4.5 to 5.4 dB from 6 to 14 GHz.

C. Digital Phase Shifter

PM signals are split into feed four phase shifters with independent phase control. Based on our previous work [37], the proposed digital phase shifter is implemented with I/Q vector-sum architecture as exhibited in Fig. 16. Its output phase is controlled by the discrete digital signals instead of the analog signal in a conventional phase shifter. The I-DAC converts input logic bits to current and acts as a current source of the multiplication transistors. Phase and amplitude nonlinearity exists for the proposed digital phase shifter, which is caused by trans-conductance nonlinearity versus code and the control algorithm of the orthogonal vectors [37]. Besides, the phase nonlinearity can be calibrated using DPD to further improve the phase error. To suppress the loading effect among input ports of the phase shifters in different channels, input buffers are added for the input PM signals. Due to the high isolation from LO port to RF port in this architecture, the coupling effect among different channels is decreased. Therefore, traditional power divider (e.g. Wilkinson power divider) with larger circuit size is not necessary.

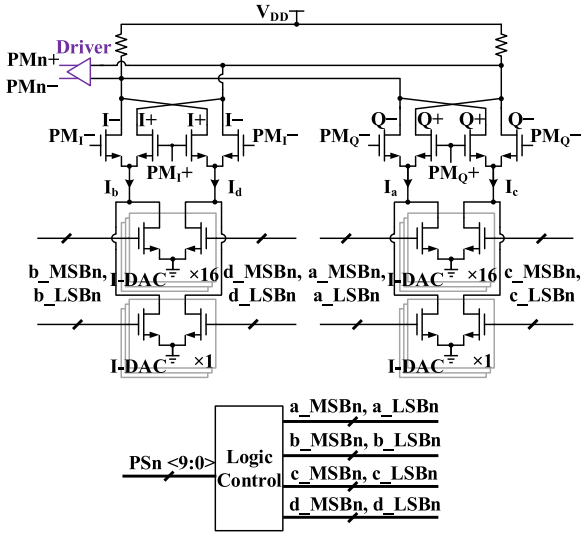

Fig. 16. Schematic of the digital phase shifter.

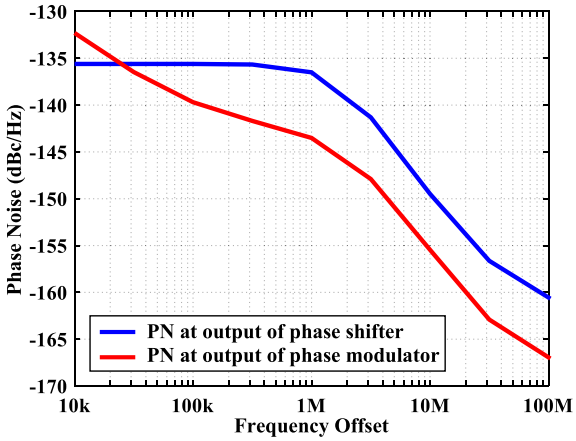

Fig. 17. Simulated PN at output of the phase shifter and phase modulator.

The simulated phase noise (PN) at the output of the phase shifter and phase modulator is shown in Fig. 17 (at 5 GHz), respectively. The output of the phase modulator is connected to the input of the phase shifter. The output PN of the phase shifter at 1 and 100 MHz are worse than the output PN of the phase modulator about 7 dBc/Hz, which shows the inherent PN contribution of the phase shifter. The PN at the output of the phase shifter at 100 kHz, 1 MHz, 10 MHz, and 100 MHz offsets are −135.6, −136.5, −149.5, and −160.5 dBc/Hz, respectively. Note that the PN of the circuits signal source is set to be ideal in this simulation.

D. DPA With FFCDM

The polar DPA with cascode core circuits is controlled by combined ACW and PM signals through digital AND gates and buffers in Fig. 18(a). Optimum load impedance of DPA changes at different ACW and operating frequencies. Following our previous research [38], DM network with switched capacitors and stacked-stepped-impedance transformer is employed to tune the load impedance. As shown

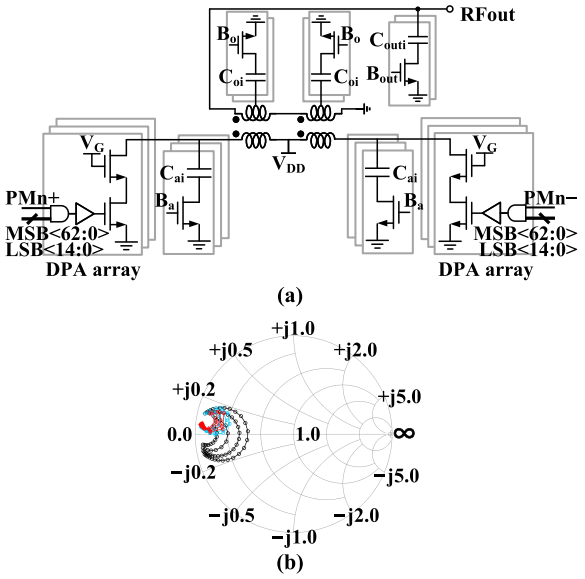

Fig. 18. (a) DPA with FFCDM. (b) Simulated load impedance of the DPA with various matching schemes.

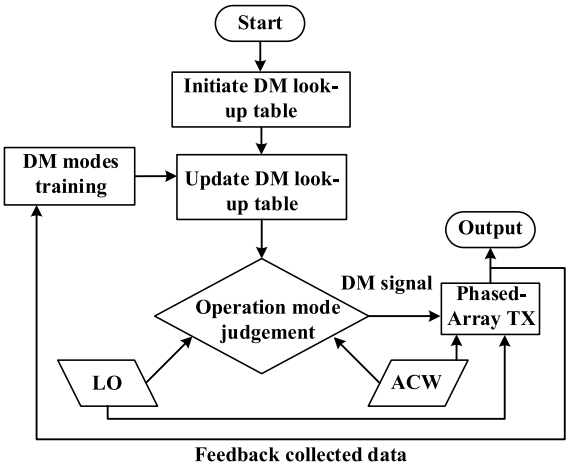

Fig. 19. Operation flowchart of the phased-array TX with feed-forward mode training.

in Fig. 18(b), the DPA load impedance shifts in a specific range by tuning the switched capacitors.

The operation of the DPA with FFCDM, as shown in Fig. 19, is similar to our previous work [38]. The detailed operation is as follows. The feed-forward control modes are trained first to obtain the optimized DM lookup table. The digital PA output is collected from various combinations of ACW, channel frequency, and DM codes. Hence, the DM control signal of the optimized operation mode for the DM network can be determined according to the DM lookup table, real-time ACW, and channel frequency. Detailed feed-forward mode training is concluded as follows. The matching capacitance C_a, C_{out}, and transformer loading capacitance C_o can be tuned by DM codes to achieve proper load impedance of the DPAs at different power levels and frequencies. By sweeping the DM codes, feed-forward signals (i.e., real-time channel frequency and ACW), output power, and corresponding efficiency of

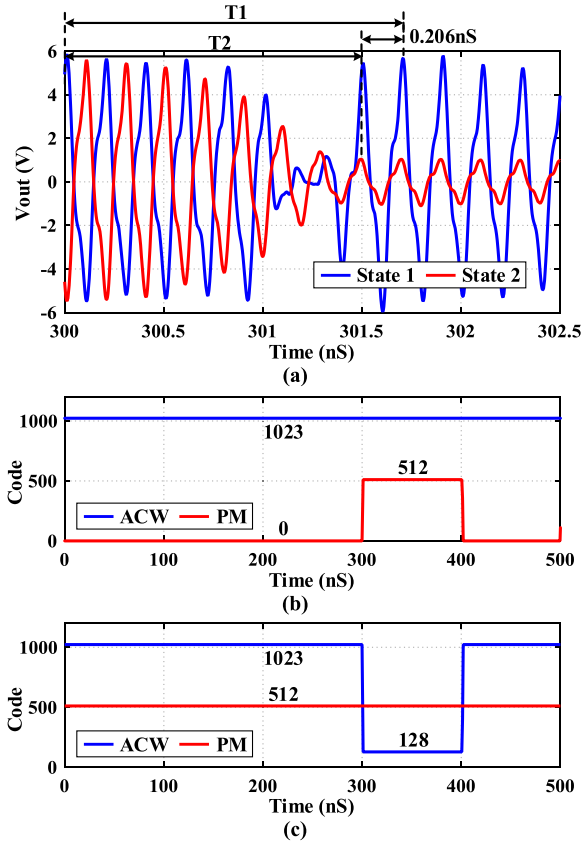

Fig. 20. (a) Simulated delay mismatch between AM and PM paths. ACW and PM settings for (b) state 1 and (c) state 2.

DPA are recorded. The optimized DM lookup table is obtained by choosing optimum matching scheme to improve the output power and efficiency of DPA at different operation frequency and power levels.

E. Delay Mismatch Between AM and PM Paths

Based on the system analysis about EVM and IM3D mentioned in Section II, to support 20-MHz modulation bandwidth with IM3D better than −40 dBc, the delay mismatch between AM and PM paths of less than 2 nS (i.e., Δt < 2 nS) is required. Fig. 20(a) shows the voltage at the 50-Ω output port of the proposed TX under two states. To evaluate the delay mismatch between AM and PM paths, two states (i.e., state 1 and state 2) are used. The ACW and PM settings for states 1 and 2 are shown in Fig. 20(b) and (c), respectively. In state 1, the ACW is fixed to be 1023. The PM code is changed from 0 to 512 at 300 nS to generate 180° phase jump of output voltage. The output voltage waveform (in blue) at state 1 is given in Fig. 20(a) to show the setting time T1, which is related to the PM code. In state 2, the PM code is fixed to be 512. The ACW is changed from 1023 to 128 at 300 nS to generate amplitude jump of output voltage. The output voltage waveform (in red) at state 2 is compared in Fig. 20(a) to exhibit the setting time T2, which is related to the ACW. T1 and T2 are determined according to the first cycle with stable phase and amplitude responses of the output voltage after 300 nS. Since the ACW or PM code is changed at the

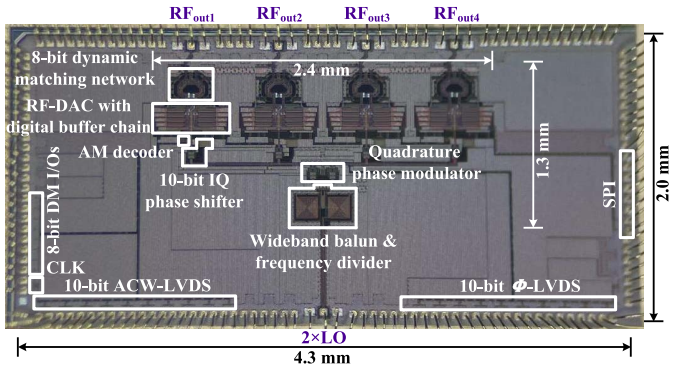

Fig. 21. Chip photograph.

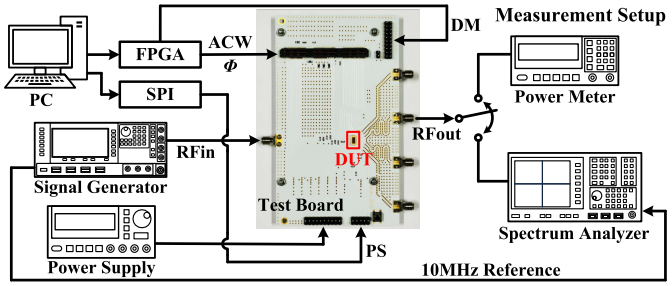

Fig. 22. Measurement setup for single-channel characterizations.

same time (i.e., 300 nS) in state 1 and state 2, the difference between setting time T1 and T2 represents the delay mismatch between AM and PM paths. It can be seen that 0.206 nS Δt is achieved with enough margin.

IV. Measurement Results

The proposed digital modulated polar phased-array TX is fabricated in a 40-nm LP CMOS technology and wire-bonded to a 4-layer PCB for measurement. The chip size is 4.3 × 2.0 mm^2 limited by pads (core area is only 1.3 × 2.4 mm^2), as shown in Fig. 21.

A. Single-Channel Characterizations

Fig. 22 depicts the measurement setup for single-channel characterizations. CLK, ACW, Φ, and DM generated from an external FPGA board are fed into the chip. ACW and Φ are synchronized with CLK to improve spectrum distortion. PS code is set to the chip through a USB-SPI adaptor. Each channel is measured with other three channels terminated by 50-Ω load and the same ACW and Φ codes for the four channels. The power consumption breakdown of the phased-array TX with saturated power at 5 GHz is shown in Table II. Fig. 23 illustrates the measured output power, DE, and system efficiency of the proposed polar phased-array TX for a single channel with and without DM technique under continuous wave (CW). The TX delivers a peak output power of 21.4 dBm with 38% DE and 32.5% system efficiency at 4.5 GHz without DM technique. Meanwhile, it exhibits that the output power is higher than 19.2 dBm and system efficiency is higher than 15.3% from 3 to 7 GHz. To further improve

TABLE II
DC Power Breakdown of the Phased-Array TX

Block	DC Power (mW)
Digital PA (4×)	4×333.8
Buffers, AND gates (4×)	4×45.2
Phase shifter (4×)	4×15.4
Phase modulator	28.4
Divider	4.8
Total	1610.8

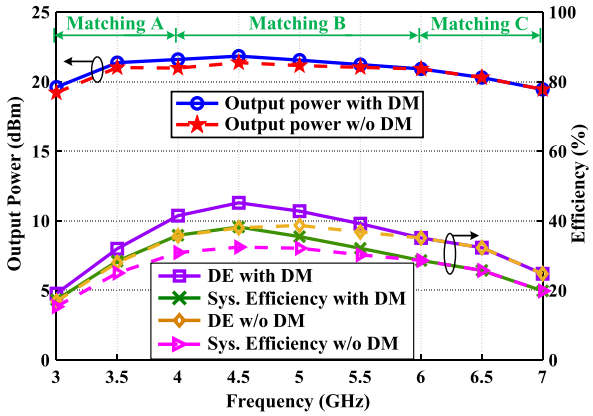

Fig. 23. Measured peak DE and P_{sat} of a single-channel, peak system efficiency of entire phased-array TX under DM modes.

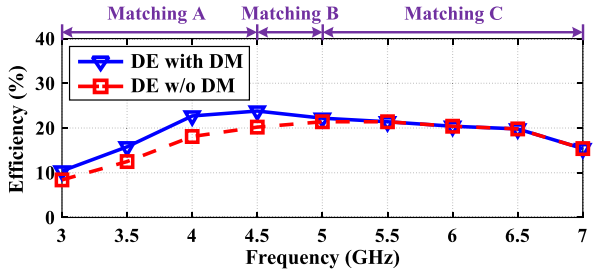

Fig. 24. DE of single channel at 6-dB back-off power.

the wideband performance, 3 DM modes (i.e., matchings A/B/C) are introduced. Note that the matchings A/B/C are optimized at different frequencies. With the proposed DM technique, the output power, DE, and system efficiency achieve maximum 0.6 dB, 7.2%, and 6.7% improvement at 4, 4.5, and 5 GHz, respectively. The TX achieves a peak output power of 21.8 dBm with 45.2% DE and 38.2% system efficiency at 4.5 GHz after DM. To investigate the power back-off performance, DE at 6-dB back-off power with and without DM technique is measured, as shown in Fig. 24. The phased-array TX has a maximum DE at 6-dB back-off power of 21.4% at 5 GHz without DM technique. With the DM technique, the TX at 6-dB back-off power achieves a peak 23% DE and 4.6% DE improvement at 4 GHz. Meanwhile, DE versus output power at 4 GHz with and without dynamic matching technology is depicted in Fig. 25. Note that the matchings A/B/C are different for peak output power and 6-dB back-off power.

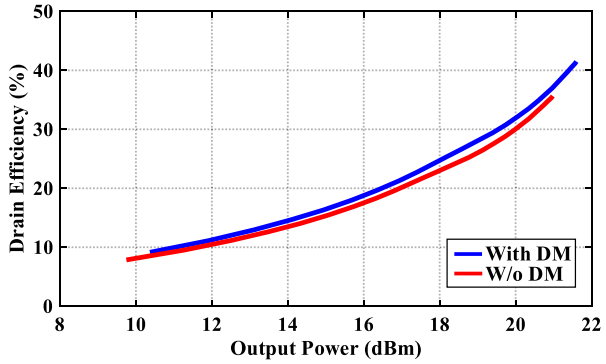

Fig. 25. Measured DE versus output power with and without dynamic matching technology at 4 GHz.

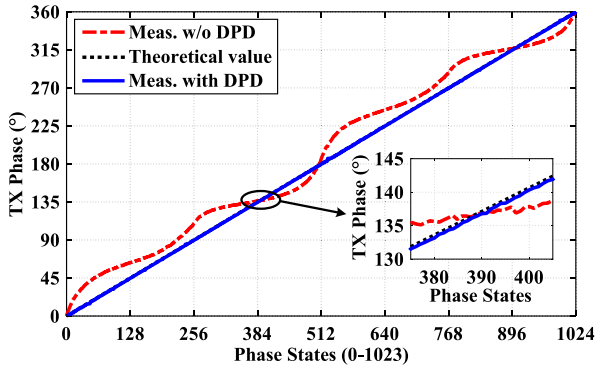

Fig. 26. Comparison of measured TX phase with and without DPD.

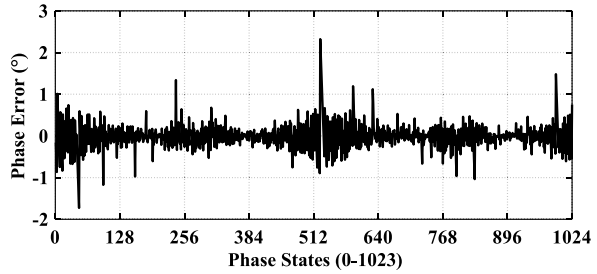

Fig. 27. Measured TX phase error for 1024 phase states with DPD.

The 10-bit phase response is measured as illustrated in Fig. 26. The 0 state phase response is subtracted from all the measured 10-bit phase responses. Besides, the DPD technique is adopted to improve the measured TX phase linearity significantly. After DPD technique, the phase response is close to the theoretical value. Fig. 27 shows the measured TX phase error (i.e., phase difference between the measured phase and the theoretical value) after DPD, which exhibits only a maximum 2.3° phase error for 1024 phase states. The measured rms phase and gain error are below 1.6° and 0.2 dB with 0.35° (10-bit) phase resolution from 3 to 7 GHz, as depicted in Fig. 28. Under a fixed DPD at 5 GHz, the measured rms phase and gain error are below 3° and 0.2 dB from 3 to 7 GHz, as shown in Fig. 29. Different from other phased-array architectures, the phase shifter of the proposed TX is placed between the phase modulator and the digital

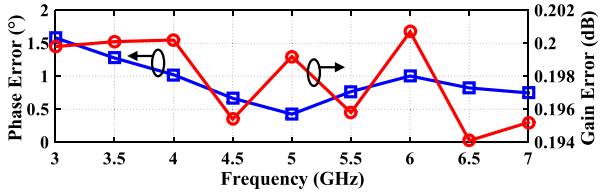

Fig. 28. RMS phase and gain errors.

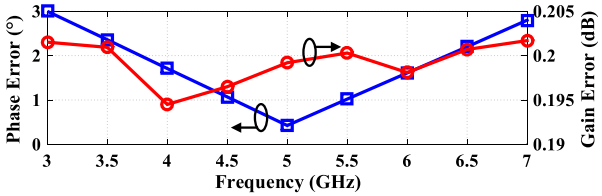

Fig. 29. RMS phase and gain errors with a fixed DPD at 5 GHz.

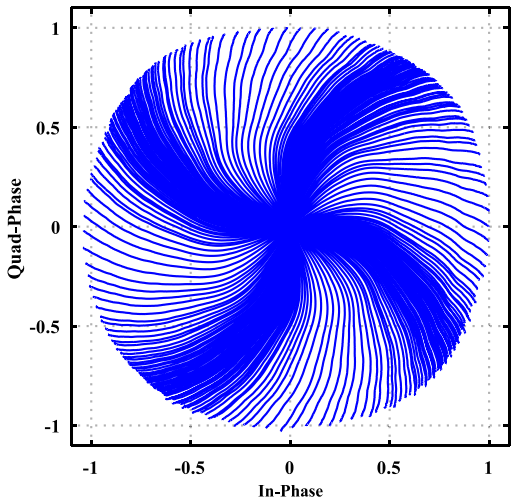

Fig. 30. Measured 2-D distortion characteristics of the phased-array TX (256 PM states).

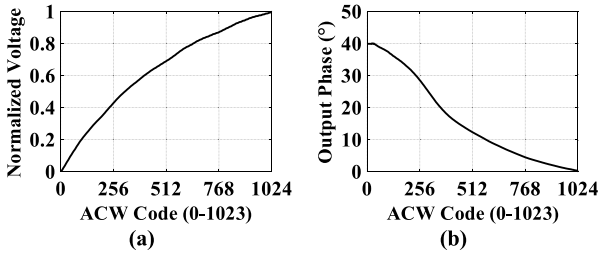

Fig. 31. Measured (a) AM/AM and (b) AM/PM distortions.

power amplifier. Thus, the gain error of the phase shifter would be decreased by the digital power amplifier.

Fig. 30 shows the measured 2-D characteristics of the AM–AM and AM–PM distortion of the TX by sweeping the ACW and PM code. Each line is measured under one PM states by sweeping ACW. Note that only 256 PM states are used to simplify the measurement. Besides, the measured AM/AM and AM/PM distortions are depicted in Fig. 31.

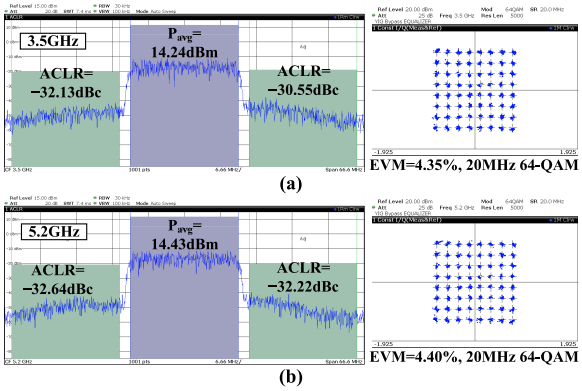

Fig. 32. Measured 64-QAM constellation and spectrum with 20-MHz modulation bandwidths at (a) 3.5 and (b) 5.2 GHz.

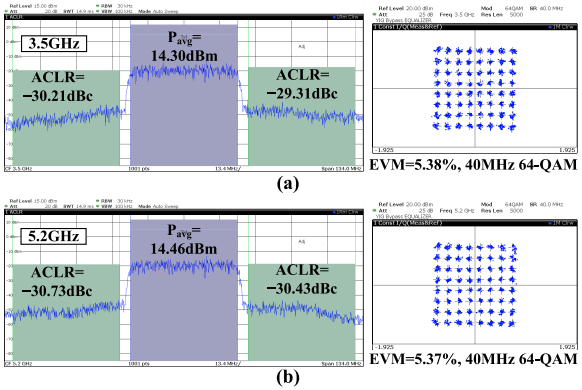

Fig. 33. Measured 64-QAM constellation and spectrum with 40-MHz modulation bandwidths at (a) 3.5 and (b) 5.2 GHz.

Then, the off-chip lookup table is obtained accordingly by DPD techniques. The measured spectrum and constellation at 3.5 and 5.2 GHz are shown in Figs. 32 and 33. The TX exhibits rms-EVM of 4.35% and 4.40% for 64-QAM signals with modulation bandwidths of 20 MHz at a data rate of 120 Mbps, P_{out} of 14.24 and 14.43 dBm, PAPR of 7.14 and 7.00, and a baseband sampling frequency of 100 MHz at 3.5 and 5.2 GHz after DPD, respectively. In addition, the TX exhibits rms-EVM of 5.38% and 5.37% for 64-QAM signals with modulation bandwidths of 40 MHz at a data rate of 240 Mbps, P_{out} of 14.30 and 14.46 dBm, PAPR of 7.08 and 6.97, and a baseband sampling frequency of 200 MHz at 3.5 and 5.2 GHz after DPD, respectively. The measured digital sampling images and mixing spurs of the proposed transmitter are shown in Fig. 34, where the baseband sampling frequency is 100 MHz. Note that the spectrum replicas locate at integer times of baseband sampling frequency, which can be further improved with a larger sampling frequency. Fig. 35 also depicts the measured EVM of 64-QAM with 20 MHz modulation bandwidths versus AM and PM resolutions. The typical constellations and spectrums for 6-bit AM and 6-bit PM, 8-bit AM and 8-bit PM, and 10-bit AM and 10-bit PM signals are shown in Figs. 36(a) and (b) and 33(b), respectively. The lowest four bits of PM and AM are enabled or disabled to obtain desired resolutions of PM and AM. The disabled bit would be set to

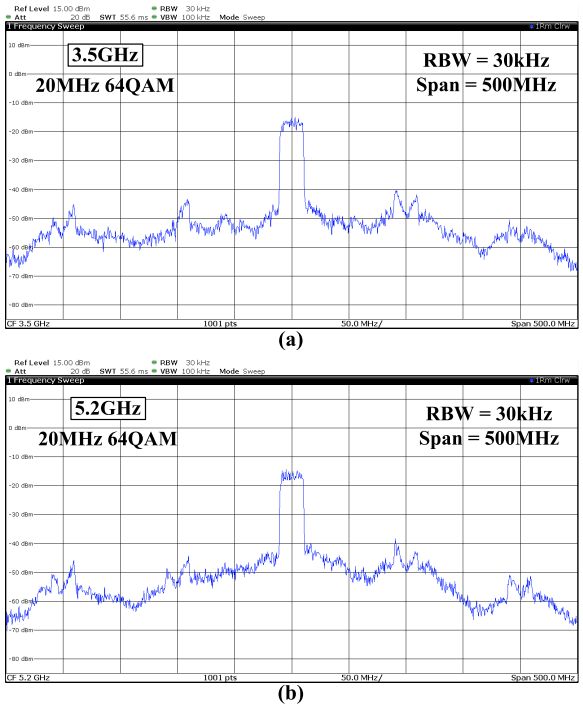

Fig. 34. Measured out-of-band spectrums of 20 MHz 64-QAM signals at (a) 3.5 and (b) 5.2 GHz with a sampling frequency of 100 MHz.

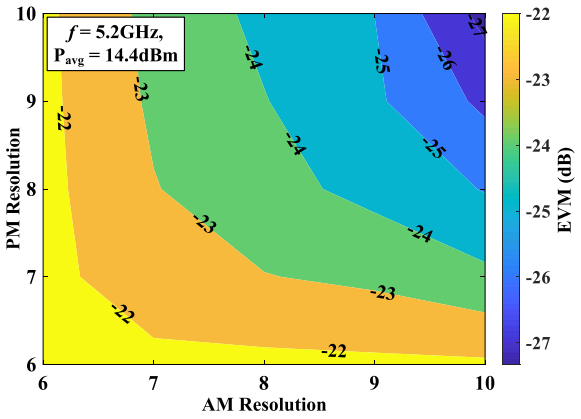

Fig. 35. Measured EVM of 64-QAM with 20-MHz modulation bandwidths versus AM and PM resolutions.

be 0. For example, to obtain the 6-bit PM resolution and 8-bit AM resolution of the polar transmitter, the lowest 4-bit of PM and the lowest 2-bit of DPA are disabled and set to be 0. It is notable that the EVM performance could be significantly improved by increasing the AM and PM resolutions of the TX, which agrees with the theoretical analysis in Section II. A performance summary and comparison with relevant state-of-the-art digital modulated transmitters are shown in Table III. Compared to the counterparts [26]–[29], and [31], the proposed transmitter has the merits of wideband, high efficiency, and high data rate.

B. Array Characterizations

The output power and DE among four channels are illustrated in Fig. 37. During the measurement, the four channels

TABLE III
COMPARISON TABLE WITH RELEVANT STATE-OF-THE-ART DIGITAL MODULATED TXS

Ref.	**This work**	JSSC 2013 [27]	JSSC 2013 [26]	JSSC 2015 [28]	JSSC 2019 [31]	JSSC 2015 [29]
Architecture	**Digital polar phased-array TX**	Digital polar TX	Digital polar TX	Digital polar Doherty TX	Subsampling polar TX	Digital polar TX
CMOS Tech. (nm)	**40**	65	65	65	28	65
Operation Class	**Class-E**	Class-D^{-1}	Class-AB	Class-D^{-1}	Class-D^{-1}	SCPA
On-Chip Matching Technique	**8-bit feed-forward**	1-bit switch impedance	Switched -capacitor	Active load-modulation	Transformer with capacitor	Switched -capacitor
Frequency (GHz)	**3–7**	1.8–2.6	1.5–2.7	3.10–3.98	4.95–6.05	1.7–2.6
Normalized Bandwidth (%)	**80**	36.4	57.1	24.9	20	41.9
Peak P_{out} (dBm)	**21.8**	23.3	20.4	27.3	11	24
Peak Drain Efficiency (%)	**45.2**	43	N/A	32.5	N/A	35
Peak System Efficiency (%)	**38.2***	38	32.3	28.6	N/A	27.6
Modulation Signal	**40MHz 64-QAM**	20MHz 802.11g	20MHz 802.11g	0.5MHz 16-QAM	2.5MHz 1024-QAM	20MHz 802.11g
Data-Rate (Mbps)	**240**	54	54	2	25	54
EVM (%)	**5.38@3.5GHz 5.37@5.2GHz**	3.98@2.2GHz	4.07@2.4GHz	4.4@3.82GHz	0.86@5.56GHz	4.0@2.4GHz
Pre-Distortion	**2-D DPD off-chip**	1-D DPD off-chip	1-D DPD off-chip	1-D DPD off-chip	1-D DPD off-chip	No
Supply Voltage (V)	**1.1/1.2**	1.2	1.2/2	3	0.9	2.1

* Whole system efficiency due to simultaneously active four channels.

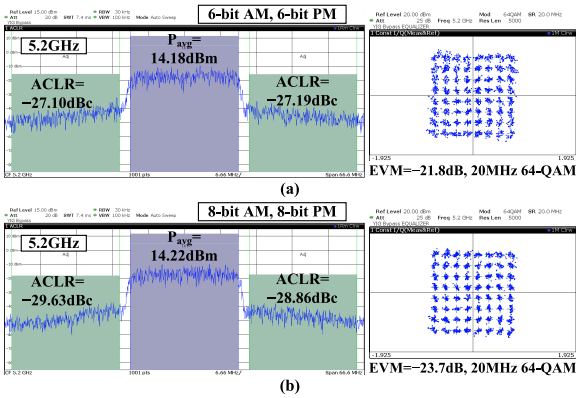

Fig. 36. Measured typical constellations and spectrums at 5.2 GHz. (a) 6-bit AM and 6-bit PM resolution. (b) 8-bit AM and 8-bit PM resolution.

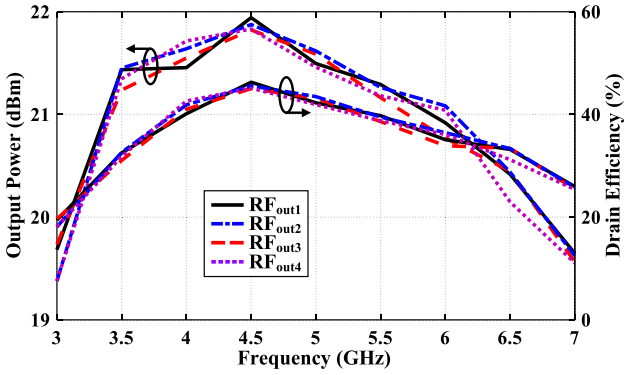

Fig. 37. Output power and DE among different channels.

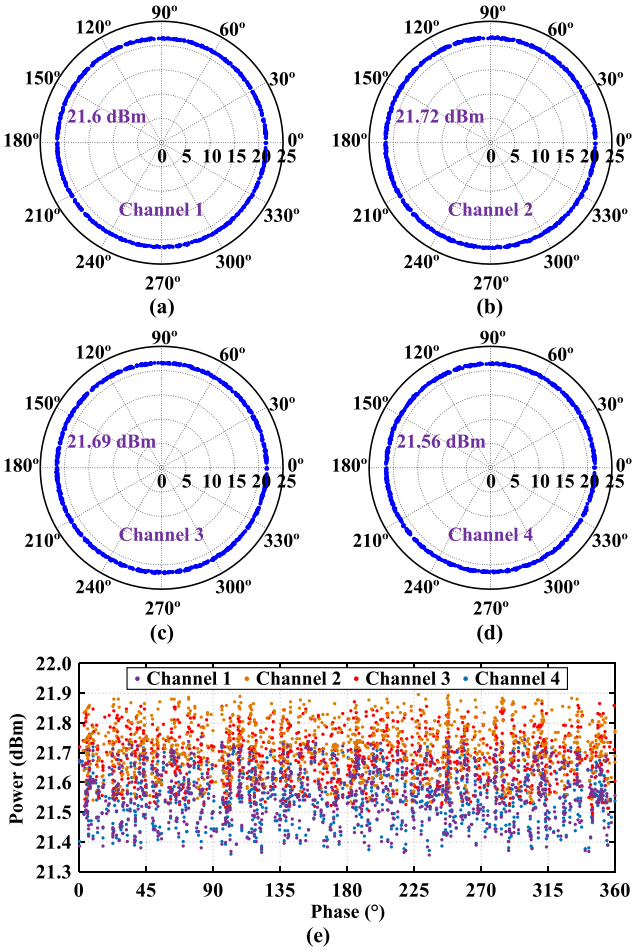

Fig. 38. Polar diagram showing measured phase/power variation at 5 GHz with DPD. (a) Channel 1, (b) channel 2, (c) channel 3, and (d) channel 4. (e) Measured output power versus phase at 5 GHz with DPD of four channels.

are simultaneously turned on. The output power variation is less than 0.36 dB from 3 to 7 GHz, which could be caused by measurement uncertainties such as cable stability and bonding placement errors. Besides, the maximum DE variation is 2.5% at 6 GHz. The polar diagram showing measured phase/power variation after calibration is depicted in Fig. 38. It is notable that four channels have similar responses. Benefited from the proposed PM phase shifting architecture, the polar diagram is close to a circle, which means that the phase change has a

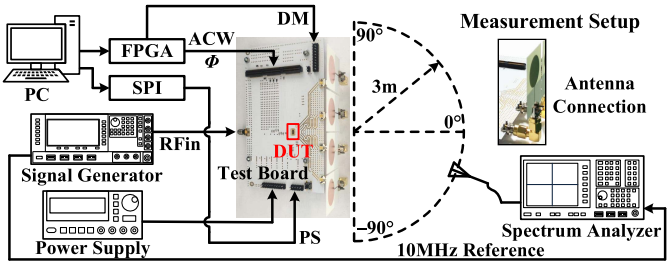

Fig. 39. Measurement setup for array characterizations.

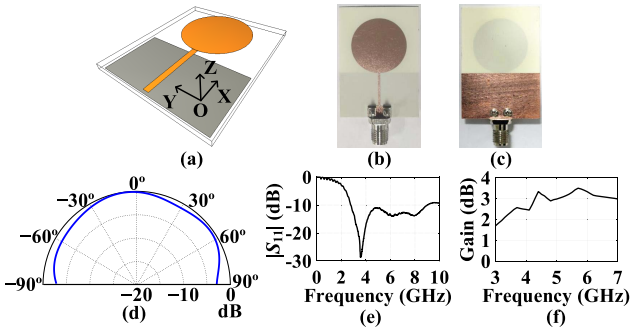

Fig. 40. (a) 3-D view of the TX monopole antenna. The photograph of the TX monopole antenna: (b) top view; (c) bottom view. (d) Measured H-plane (YOZ) radiation pattern of the TX monopole antenna. (e) Measured return loss. (f) Measured gain.

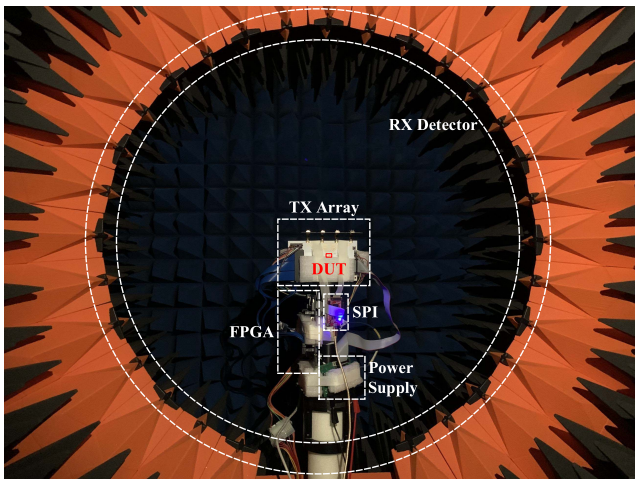

Fig. 41. Measurement environment for radiation patterns.

negligible influence on the output power. The power variation versus phase shifting of each channel is less than 0.4 dB. To further validate the array level performance of the proposed phased-array TX, further measurements with antennas are carried out with the measurement setup in Fig. 39. The TX monopole antenna, as shown in Fig. 40, is utilized for measurement. The TX monopole antenna features a 2.98 dBi antenna gain at 5 GHz and has an omnidirectional radiation characteristic. Meanwhile, the measured bandwidth of the antenna with return loss less than 10 dB is from 2.75 to 8.92 GHz. The radiation patterns are measured in an anechoic chamber, while the test environment is shown in Fig. 41. Here, the RX

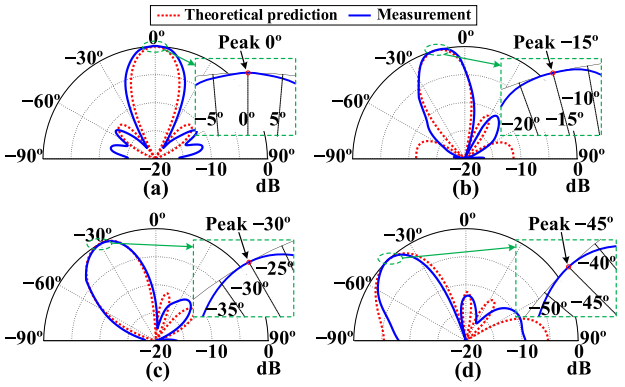

Fig. 42. Measured 4-element radiation patterns at 5 GHz with (a) 0° steering, (b) 15° steering, (c) 30° steering, and (d) 45° steering.

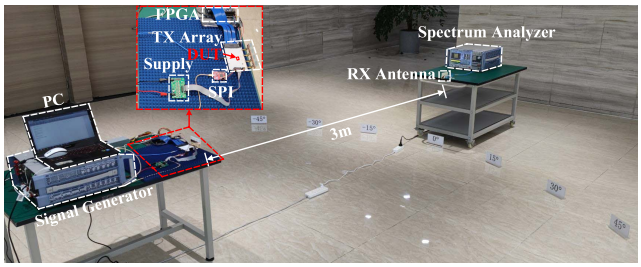

Fig. 43. Measurement environment for constellations.

antennas (i.e., detection points) are implemented around the phased-array TX antenna. The distance between the TX and RX antennas is about 50 cm. Note that the RX detector and the plane would be rotated with a rotation resolution of 1° in measurement. Thus, the resolution of the obtained radiation pattern is 1°. Under the case of antennas with 1/2 wavelength (i.e., 3 cm at 5 GHz), the measured array patterns with 0° steering, 15° steering, 30° steering, and 45° steering are shown in Fig. 42. As the definition of EIRP in [39], the measured EIRP is 35.6 dBm at 5 GHz. The 64-QAM signals with a bandwidth of 20/40 MHz at a data rate of 120/240 Mbps are measured from a 3 m TX-RX distance, as shown in Fig. 43. Besides, a Vivaldi antenna is utilized as the RX antenna, whose gain is 7.51 dBi at 5 GHz. The measured constellations at 5 GHz are depicted in Fig. 44. The phased-array exhibits rms-EVM of 4.60%, 4.62%, 4.63%, and 4.67% and EIRP of 28.1, 27.9, 27.6, and 26.1 dBm for 64-QAM signals with a modulation bandwidth of 20 MHz under 0°, 15°, 30°, and 45° beam steering, respectively. Meanwhile, the phased-array exhibits rms-EVM of 5.76%, 5.79%, 5.88%, and 5.87% and EIRP of 28.2, 27.8, 27.7, and 26.2 dBm for 64-QAM signals with a modulation bandwidth of 40 MHz under 0°, 15°, 30°, and 45° beam steering, respectively. EVM and system efficiency versus EIRP for 64-QAM signals with 20 and 40 MHz modulation bandwidths are shown in Fig. 45(a) and (b), respectively. In the measurement, all the channels are operated simultaneously with the same ACW and phase modulator code. A performance summary and comparison with relevant state-of-the-art phased-array transmitters are shown in Table IV. Comparing to the counterparts [9], [10], [17], [22], and [25],

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON TABLE WITH RELEVANT STATE-OF-THE-ART PHASED-ARRAY TXS

Ref.	**This work**	JSSC 2012 [22]	TMTT 2013 [9]	ISSCC 2019 [17]	RFIC 2020 [25]	RFIC 2019 [10]
Architecture	**Digital modulated polar TX with PM phase-shifting**	UWB TX with vernier delay line	All-RF with 4-bit gain control	SCPA with multi-phase phase-shifting	1-bit DSM+FIR hbridge CSDAC	Phase compensated VGA with PS
Technology	**40nm CMOS**	130nm CMOS	130nm CMOS	65nm CMOS	28nm CMOS	180nm SiGe BiCMOS
Frequency (GHz)	**3–7**	3–5	8.5–10.5	1.45–2.15	6	8-16
Normalized Bandwidth (%)	**80**	50	21	38.9	N/A	66.7
Elements	**4**	4	4	4	8	4
Phase Resolution (°)	**0.35**	10.8*	22.5	0.7	N/A	2.8
RMS Phase Error (°)	**0.3–1.6**	N/A	6	0.32	N/A	2.8
RMS P_{out}/Gain Error (dB)	**0.2**	N/A	0.5	0.15	N/A	0.3
Peak P_{sat} (dBm)	**21.8**	N/A	13.6	24.4	4.7	11.1
Peak System Efficiency (%)	**38.2**	7.5	10.5	24.2	N/A	N/A
Modulation Signal	**40MHz 64-QAM**	N/A	20MHz QPSK	15MHz 64-QAM	23MHz 16-QAM	N/A
Data-Rate (Mbps)	**240**	10–80	40	90	92	N/A
EVM (%)	**5.76@5GHz**	N/A	1.5@8.7GHz	3.7@1.75GHz	2.6@6GHz	N/A
Calibration	**Yes**	Yes	Yes	No	Yes	Yes
Supply Voltage (V)	**1.1/1.2**	1.2	2/3	1.4/2.8	1	3.3
Chip/Core Area (mm^2)	**4.3×2/2.4×1.3**	3×2.4/2.4×1.8#	3×2.9/2.6×2.6#	2×2.5/2.2×1.8#	1.5×1.1/0.9×0.8#	4×4/3.8×3#

*10 ps delay step is converted to 10.8° phase resolution at 3GHz; #Estimated from the figures in reference.

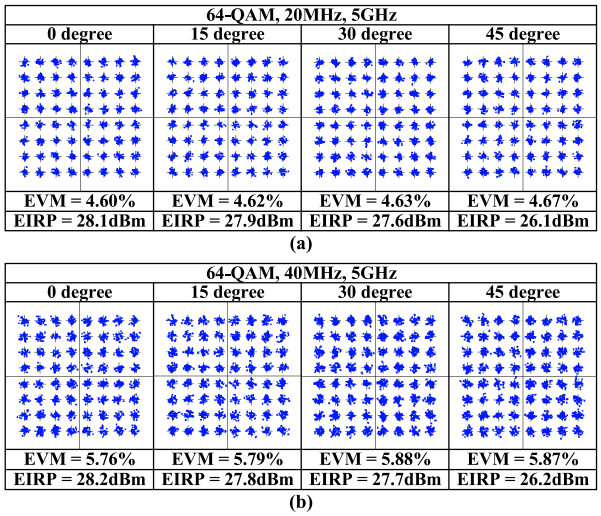

Fig. 44. Measured constellations and EIRP of 64-QAM signals with bandwidths of (a) 20 MHz and (b) 40 MHz from 3 m distance at 5 GHz.

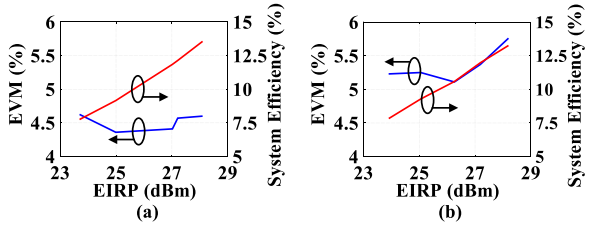

Fig. 45. EVM and system efficiency versus EIRP for signals with (a) 20 MHz and (b) 40 MHz modulation bandwidths at 5 GHz.

our phased-array TX achieves better rms phase and gain error with the highest phase resolution of 0.35°, highest system efficiency, higher data rate, and wider operation bandwidth.

V. CONCLUSION

A digital modulated 4-element polar phased-array TX prototype integrated in a 40-nm LP CMOS is demonstrated. PM phase-shifting independent of the amplitude signal is proposed for power saving, compact circuit design, and less nonlinearity impact for TX performance. With the high-resolution phase-shifting by digital phase shifters based on I-DAC and DPD, it can achieve wider transmission radius for a specific scanning resolution. The efficiency is enhanced with a switch-mode DPA and feed-forward controlled DM network. With the accurate phase response, high system efficiency, and high data rate, the proposed digital modulated polar phased-array TX is attractive in practical wireless system, especially for portable devices.

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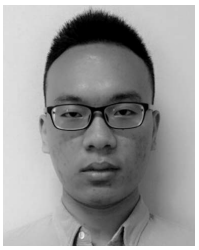

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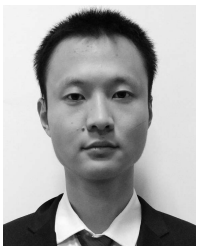

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