A 91.15% Efficient 2.3–5-V Input 10–35-V Output Hybrid Boost Converter for LED-Driver Applications

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***Abstract*— This article presents a hybrid boost converter architecture for improving the efficiency of light-emitting diode (LED) drivers used in mobile applications. By cascading a low-switching frequency time-interleaved series–parallel switched-capacitor (SC)-stage with an inductive-boost converter, we facilitate lower voltage-rated switches, thus significantly reducing the switching losses. Charge-sharing losses of the SC stage are minimized by soft-charging flying capacitors with the inductor of the boost (BST) stage. Fabricated in 180-nm bipolar CMOS DMOS (BCD) process, the prototype converter generates 30-V output voltage from a Li-ion battery source. It can provide a load current in the range of 0–100 mA with an excellent peak power efficiency of 91.15% at 30 mA, which represents a 3% improvement over the state of the art.**

***Index Terms*— DC–DC converter, hybrid converter, light-emitting diode (LED) drivers.**

I. Introduction

RAPID technological advances over the last decade have made the display module an integral part of modern portable electronic devices, such as smartphones and tablets. While these developments have enhanced user experience significantly, they also made the displays by far the most power-hungry blocks in smartphones [1]. A typical display module comprises a backlight and an LCD panel. The backlight consists of strings of series-connected white light-emitting diodes (LEDs). Screen-size and brightness requirements may mandate stacking of up to eight LEDs in each string. With each LED having a forward-bias voltage of about 3.3 V, the required supply voltage needed to drive the chain can be as high as 27 V. Tight volume constraints mandate that such a high output voltage can be generated from a 2.3 to 5 V input voltage provided by a Li-ion battery. To this end, a boost converter is most commonly used to perform the desired dc-to-dc conversion. Since the display module consumes 30%–40% [1] of the total available energy, the efficiency of such a boost converter significantly impacts system power efficiency. Traditionally, an inductor-based switching power converter shown in Fig. 1 is used [2]. It consists of a pair of switches S_1 and S_2, an inductor L, and an output capacitor C. Switches S_1 and S_2 are driven by complementary pulse width modulated (PWM) signals with a duty cycle of D and $(1-D)$ and generates an output voltage given by the following equation:

$$V_{\text{OUT}} = \frac{V_{\text{IN}}}{1-D}. \tag{1}$$

Even though this architecture requires very few off-chip components, its efficiency is fundamentally limited by the switches' high voltage rating. As will be described later, a high switch rating exacerbates both switching and conduction losses, thus limiting the achievable peak efficiency of state-of-the-art display drivers to about 88% [2], [3].

The impact of switch voltage rating on boost converter efficiency can be understood by plotting efficiency versus load current for different output voltages at a fixed input voltage (see Fig. 2). The power switch sizes were optimized for each output voltage. As the switch rating increases (to support the increased output voltage) from 6 to 36 V, peak efficiency degrades by more than 5%. The reduction in the power switch quality increases both the switching and conduction losses, which causes the observed degradation in peak efficiency. One possible approach to overcome this problem would be

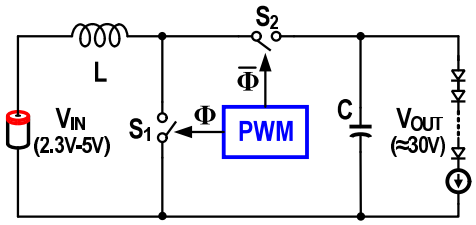

Fig. 1. Conventional boost converter-based LED driver.

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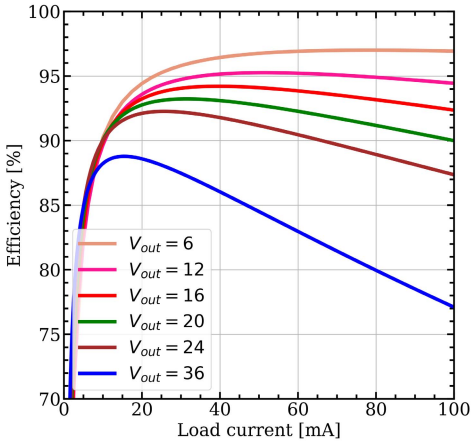

Fig. 2. LED-driver efficiency versus load current for different output voltages and fixed $V_{IN} = 3.7$ V.

to explore architectures that do not require such high-voltage-rated switches. A class of switched-capacitor (SC)-based converters can generate high output voltages using devices rated lower than the output voltage [4], [5]. However, they incur a considerable amount of charge-sharing losses at typical LED driver's operating power levels. The large dc gain requirement increases the number of switches, which significantly increases conduction and switching losses.

Hybrid architectures have recently emerged as an alternative to the SC-based approaches mentioned above. By cascading an SC stage with an inductive stage [6] or by merely placing an inductor between the power source and an SC converter [7], [8], these architectures seek to combine the advantages of inductive- and SC-based converters. Placing the inductor in the path of the charging/discharging current of the flying capacitor reduces hard-charging losses to a great extent. Recent works have effectively used this approach but could not completely eliminate hard-charging losses [9] or output-voltage-rated switches [10].

This article presents a high-efficiency boost converter for LED-driver applications with an input voltage range of 2.3–5 V, an output voltage range of 10–35 V, and a load range of 0–100 mA [11]. The prototype power converter was fabricated in 180-nm technology and occupies an active area of 2.3 mm $\times$ 1.2 mm, and operates at 1-MHz switching frequency. The power converter achieves an excellent peak power efficiency of 91.15% at 3.7-V input and 30-V output with no external gate driver supplies, representing a 3% improvement in peak efficiency over the state of the art. This article supplements the information provided in [11] with a detailed elucidation of the architecture evolution, an in-depth analysis of the output impedance of hybrid architectures, a detailed description of the phase-by-phase operation of the converter, additional details of the zero-crossing detector used to implement discontinuous conduction mode (DCM) operation, and new measurement results pertaining to the improvement in power efficiency in DCM compared to CCM.

The rest of this article is organized as follows. Section II presents a breakdown of the losses in an inductive-boost converter used in conventional LED drivers. Section III presents the proposed architecture. Circuit implementation details of key building blocks are described in Section IV. Experimental results from the test chip are presented in Section V. Key contributions of this article are summarized in Section VI.

II. LED-Driver Losses

Losses in an LED driver depend on the magnitude of input–output voltages, load current, and switching frequency. The typical range of input–output voltages and load current is 2.3–5/12–30 V and 0–100 mA, respectively. Losses can be broadly classified as conduction losses and switching losses. The current source used to set the LED current has to bias with about 200 mV across it, which also incurs an efficiency penalty. However, in LED drivers with V_{OUT} as high as 30 V, the efficiency hit is minimal. These loss mechanisms are investigated for the conventional inductive-boost converter next and later extended to the proposed architecture.

Conduction losses are modeled using the following equation [12]:

$$P_{cond} = i^2_{IND,RMS} \cdot (R_{DCR} + D \cdot R_{LS} + (1-D) \cdot R_{HS} + R_{PCB}) \quad (2)$$

where $i_{IND,rms}$ is the inductor rms current, D is the duty cycle of the low-side switch, and R_{LS} and R_{HS} are the "ON" resistances of the low- and high-side switches, respectively. The value of R_{DCR} depends on the size of the inductor and is typically in the range of 200–300 mΩs for inductors used in space-constrained mobile applications. Such a large R_{DCR} is a significant source of conduction loss, especially at higher load currents.

Switching losses have three components denoted by $P_{transition}$, P_{gate}, and P_{core}. $P_{transition}$ represents losses incurred in a power switch when it transitions from "ON" state to "OFF" state and vice versa and is a result of the current and the voltage through the power device being non-zero during the transition. Using low-side switch M_{LS} Voltage and current waveforms during a turn-on event (see Fig. 3), $P_{transition}$ can be calculated using the following equation [13]–[20]:

$$P_{transition} = 0.5 \cdot F_{SW} \cdot V_{OUT} \cdot I_L \cdot (t_1 + t_2) \quad (3)$$

where V_{OUT} is the output voltage and F_{SW} is the inductor switching frequency. Times t_1 and t_2 are estimated using gate driver current I_{DR} and gate charges Q_{GS} and Q_{GD} as explained in [19]. At large load currents, $P_{transition}$ becomes a significant component of the switching losses. This transition loss equation can be modified to include the reverse recovery loss of the body diode of M_{HS} and that of the parasitic capacitance $C_{DS,LS}$ [21].

P_{gate} represents the power loss during the charging/discharging of the gate terminal of the power switches and can be modeled by the following equation [12]:

$$P_{gate} = C_{gate} \cdot V^2_{IN} \cdot F_{SW} \quad (4)$$

where C_{gate} and V_{IN} are the gate capacitance of the power switch and input voltage to the power converter, respectively.

P_{core} represents the inductor's magnetic losses, and its magnitude depends on the inductor dimensions, with larger height inductors having lower core losses. Core losses can

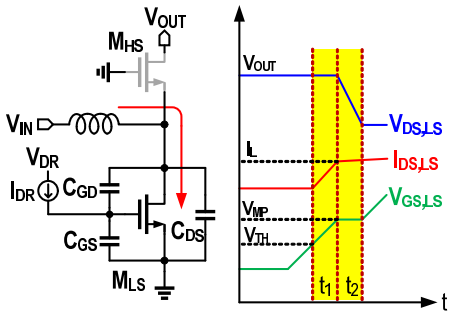

Fig. 3. Transition loss modeling for turn-on event of low-side switch.

be calculated using the Steinmetz expression in the following equation [22]:

$$P_{\text{core}} = K_{\text{FIT}} \cdot F_{\text{SW}}^{\alpha} \cdot (\Delta I_{\text{IND}})^{\beta} \tag{5}$$

where K_{FIT}, α, and β are fitting parameters provided by manufacturers. ΔI_{IND} is inductor current ripple. In addition to the losses described above, other losses, such as dead-time losses, are also incurred during every switching cycle, but their contribution to the total loss is much smaller.

A. Simulated Loss Breakdown

The power converter's efficiency is typically optimized at the most probable load current, which is around 20–40 mA for LED drivers used in smartphones [23]. A 3.7-V input 30-V output conventional inductive-boost power converter was designed to examine the relative contribution of each type of loss, and the simulated variation of conduction and switching losses as a function of the load current is plotted in Fig. 4. Switch sizes were chosen to minimize the total loss (switching + conduction) for a given load current and switching frequency. The pie chart in Fig. 4 shows the relative contribution of each type of losses at 25-mA load current, including the current source losses (I_{SRC} losses). Both the switching and conduction losses contribute significant portions to the total loss at this load current. Because power switch size trades off conduction losses with switching losses, increasing the switch size beyond a certain point does not reduce the total loss. Architectures that allow switches with lower voltage rating ease this tradeoff, thereby presenting a possibility for significantly reducing the losses.

III. Proposed Architecture

A simplified block diagram of the proposed hybrid boost converter architecture is shown in Fig. 5. It consists of an inductive-boost (BST) stage followed by an SC stage. The BST stage provides a dc gain of $M = 1/(1-D)$, where D is the PWM signal's duty cycle, while the SC stage provides a dc gain of N. DC gains, M and N, must be chosen to meet the overall dc gain requirement, which in our application is about 10. Therefore, for instance, $M = 5$ and $N = 2$ would satisfy this requirement. With this choice, all the switches in BST and SC stages experience a maximum voltage of only half the output voltage across them. Thus, switches

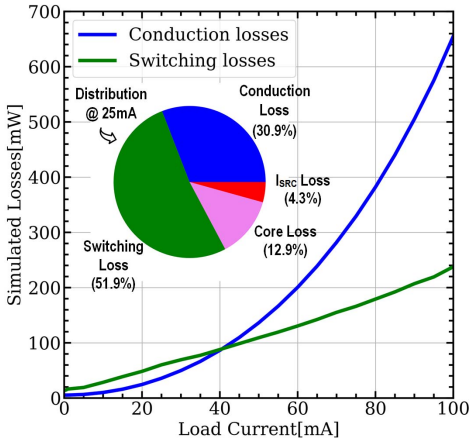

Fig. 4. Electrical switching loss ($P_{\text{transition}} + P_{\text{gate}}$) and conduction loss variation with load current and loss breakdown at 25-mA load ($V_{\text{IN}} = 3.7$ V, $V_{\text{OUT}} = 30$ V) for a conventional inductive-boost power converter.

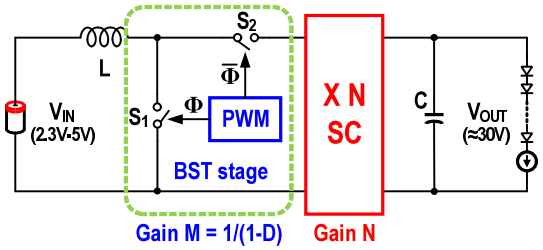

Fig. 5. Hybrid boost converter.

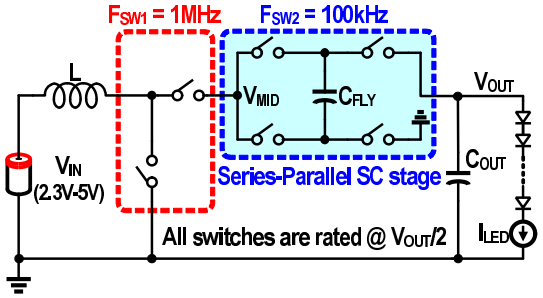

Fig. 6. Proposed boost converter topology.

rated for only 15 V (as opposed to 30 V) can be used. While the proposed architecture has successfully reduced the power switches' voltage rating, the total number of switches has increased. However, with the appropriate choice of the SC-stage architecture and its switching frequency, it is possible to achieve better efficiency, as described next.

A. SC-Stage Architecture Selection

Two important considerations dictate the choice of SC-stage architecture. First, power losses must be low enough not to impact the overall converter efficiency. Second, the architecture must be amenable for simple circuit implementation and must obviate the need for auxiliary power supplies. A series–parallel architecture shown in Fig. 6 meets

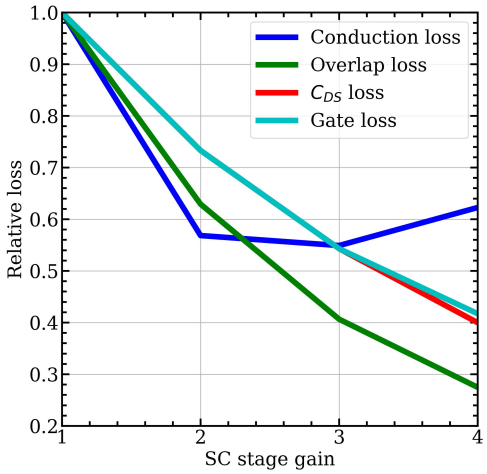

Fig. 7. Relative loss of the proposed architecture with SC-stage gain varying from 2 to 4, normalized to the corresponding losses in conventional inductive-boost converter.

these criteria. The lowest output impedance is achieved across a wide range of dc gains when this architecture is operated in the fast-switching limit region where losses associated with switch resistance dominate [5]. The optimal distribution of the total dc gain between the inductive-BST and SC stages is determined using the approach described in [10]. In this analysis, output voltage and the conversion gain are set at 30 V and 10, respectively; SC stage was assumed to employ the series–parallel architecture. The hybrid converter was optimized for each value of SC-stage gain (N) while keeping the area of the power converter, and the ratio of input–output voltages fixed to perform a fair comparison. Conduction and switching losses normalized to the losses of a conventional inductive-based power converter are plotted for different values of N, as shown in Fig. 7. Switching losses reduce as N (SC-stage gain) is increased. This is expected behavior since the dominant source of switching loss, namely switching losses in the inductive-BST stage, reduces with increasing N. This is because the rating of the switches in the BST-stage is inversely proportional to the SC-stage gain N (V_{OUT}/N). However, the same is not true for conduction losses, which reduces when N is changed from $N = 1$ to $N = 2$ but starts increasing from $N = 3$. This shows that the increased number of switches offsets the advantage obtained in going to lower rated switches as N is increased beyond 3. Therefore, N is chosen to be 2 in our implementation. This topology needs only four extra switches, all of which are rated at $V_{\text{OUT}}/2$. Their gate drivers can be implemented using internally available voltages, as described in Section IV.

B. Choice of Switching Frequency for the BST and SC Stages

The switching frequency of a conventional inductive-boost converter is determined from the ripple requirement, allowed output capacitor, and the load current. Assume that typical parameters of 10 μF (400 nF after de-rating) output capacitor, 25-mA load current, and an output voltage ripple of 50 mV result in a switching frequency of 1 MHz for the BST stage.

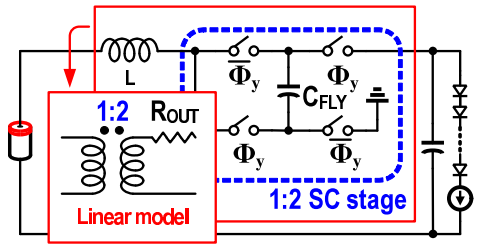

Fig. 8. 1:2 SC converter with inductor at input.

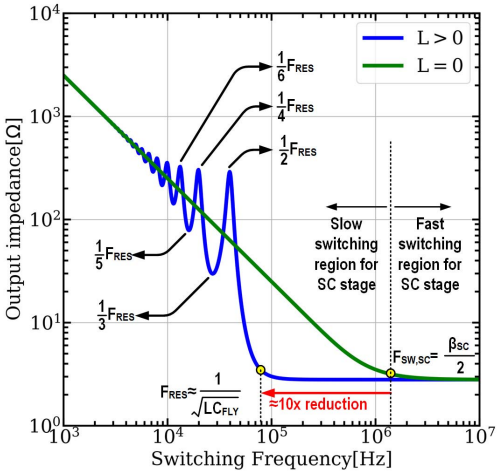

Fig. 9. Comparison of output impedance of basic hybrid converter with that of the traditional SC converter.

For a typical SC power converter with a voltage input, the switching frequency directly impacts the loss of the converter. This can be understood by modeling losses in the 1:2 SC converter with an ideal transformer and an output impedance R_{OUT} (see Fig. 8) [5], [24], [25] and plotting R_{OUT} as a function of switching frequency for two cases: $L = 0$ and $L \neq 0$, as shown in Fig. 9. For the case of $L = 0$, output impedance $R_{\text{OUT,SC}}$ is given by the following equation:

$$R_{\text{OUT,SC}} = \frac{1}{C_{\text{FLY}} F_{\text{SW,SC}}} * \coth \frac{\beta_{\text{SC}}}{4 F_{\text{SW,SC}}} \tag{6}$$

where

$$\beta_{\text{SC}} = \frac{1}{R_{\text{SW,TOT}} C_{\text{FLY}}}$$
$$R_{\text{SW,TOT}} = 2 * R_{\text{SW}}$$

and $R_{\text{SW,TOT}}$ is the total switch resistance in the charging/discharging path, R_{SW} is switch resistance, and $F_{\text{SW,SC}}$ is the switching frequency. The converter operates in the slow-switching limit for switching frequencies below 1 MHz. In this region, charge-sharing losses account for the increase in R_{OUT} with decreasing switching frequency. Beyond 1MHz, losses associated with the switch resistance dominate, as indicated by the flattening of the curve.

Inductance between the input voltage source and the converter fundamentally changes the relationship between the output impedance and the switching frequency. Because inductor current cannot change instantaneously, sudden surges in

capacitor-charging currents present when $L = 0$ are avoided, thus significantly reducing the charge-sharing losses. The output impedance of the hybrid converter is determined by calculating the ratio of average power dissipated $\langle P_{\mathrm{HYB}}\rangle_{T_{\mathrm{sw}}}$ and the average output current $\langle I_{\mathrm{OUT,HYB}}\rangle_{T_{\mathrm{sw}}}$ in each switching cycle as given by the following equation:

$$R_{\mathrm{OUT,HYB}} = \frac{\langle P_{\mathrm{HYB}}\rangle_{T_{\mathrm{sw}}}}{\langle I_{\mathrm{OUT,HYB}}\rangle^2_{T_{\mathrm{sw}}}} \tag{7}$$

where

$$\begin{aligned}
\langle P_{\mathrm{HYB}}\rangle_{T_{\mathrm{sw}}} &= 2F_{\mathrm{SW,SC}}(T_1+T_2+T_3)\\
T_1 &= 0.5\left(k_1^2+k_2^2\right)R_{\mathrm{SW,TOT}}\frac{1-e^{-\alpha T_{\mathrm{sw}}}}{2\alpha}\\
T_2 &= \frac{\alpha B+\beta_{\mathrm{HYB}}C}{2\left(\alpha^2+\beta_{\mathrm{HYB}}^2\right)}\left(1-e^{-\alpha T_{\mathrm{sw}}}\cos(\beta_{\mathrm{HYB}}T_{\mathrm{sw}})\right)\\
T_3 &= \frac{\beta_{\mathrm{HYB}}B-\alpha C}{2\left(\alpha^2+\beta_{\mathrm{HYB}}^2\right)}e^{-\alpha T_{\mathrm{sw}}}\sin(\beta_{\mathrm{HYB}}T_{\mathrm{sw}})\\
\langle I_{\mathrm{OUT,HYB}}\rangle_{T_{\mathrm{sw}}} &= F_{\mathrm{SW,SC}}(P_1+P_2)\\
P_1 &= \frac{\beta_{\mathrm{HYB}}k_1+\alpha k_2}{\alpha^2+\beta_{\mathrm{HYB}}^2}\left(1-e^{-\alpha T_{\mathrm{sw}}}\cos(\beta_{\mathrm{HYB}}T_{\mathrm{sw}})\right)\\
P_2 &= \frac{\beta_{\mathrm{HYB}}k_2-\alpha k_1}{\alpha^2+\beta_{\mathrm{HYB}}^2}e^{-\alpha T_{\mathrm{sw}}}\sin(\beta_{\mathrm{HYB}}T_{\mathrm{sw}})\\
B &= 0.5\left(k_2^2-k_1^2\right)R_{\mathrm{SW,TOT}}\\
C &= k_1k_2R_{\mathrm{SW,TOT}}\\
k_1 &= \frac{\alpha I_{\mathrm{LOAD}}+\Delta V/L}{\beta_{\mathrm{HYB}}}\\
k_2 &= I_{\mathrm{LOAD}}\\
\alpha &= \frac{R_{\mathrm{SW,TOT}}}{2L}\\
\beta_{\mathrm{HYB}} &= \sqrt{\frac{1}{LC_{\mathrm{FLY}}}-\left(\frac{R_{\mathrm{SW,TOT}}}{2L}\right)^2}\\
\Delta V &= \frac{0.5I_{\mathrm{LOAD}}T_{\mathrm{sw}}}{C_{\mathrm{FLY}}}.
\end{aligned}$$

The relationship between $R_{\mathrm{OUT,HYB}}$ and the switching frequency is more complicated compared to the $L = 0$ case (see Fig. 9). At frequencies much lower than the LC-resonant frequency ($F_{\mathrm{RES}} = (LC_{\mathrm{FLY}})^{1/2}/(2\pi)$), the current transient settles down well within the duration of each phase, thereby having no impact on R_{OUT}. As the switching frequency approaches F_{RES}, R_{OUT} exhibits a non-monotonic behavior with peaks at $F_{\mathrm{RES}}/2$, $F_{\mathrm{RES}}/4$, $F_{\mathrm{RES}}/6$, and so on and troughs at $F_{\mathrm{RES}}/3$, $F_{\mathrm{RES}}/5$, $F_{\mathrm{RES}}/7$, and so on. Beyond F_{RES}, charge-sharing losses again fall below the resistive losses of the switches. With proper choice of L and C, F_{RES} can be reduced to be much lower than transition frequency for the $L = 0$ case.

In this work, C_{FLY} was set equal to the expected output capacitance of 400 nF (de-rated) and the inductance is equal to 10 μH. Fig. 9 shows F_{RES} is 10× lower compared to the $L = 0$ case. It is worth noting that the resonance frequency will be much lower than what is predicted by the above analysis because the inductor is switched and will be equal to $F_{\mathrm{RES,SWITCHED}} = F_{\mathrm{RES}} * (1 - D))$, where D is the duty cycle with which the inductor is switched. Consequently, it would seem like the SC stage that can be switched at much lower frequency than 70 kHz. However, lowering the switching frequency increases the inductor rms current significantly, which increases the conduction losses. Because of this tradeoff, losses due to inductor RMS current and the switching losses in the SC stage are better balanced when $F_{\mathrm{SW,SC}} = F_{\mathrm{RES}}$. Another practical consideration in choosing $F_{\mathrm{SW,SC}}$ involves preventing the inductor from being connected to the SC stage when the flying capacitors are changing phases. This can be guaranteed if $F_{\mathrm{SW,SC}}$ is made an integer sub-multiple of $F_{\mathrm{SW,BST}}$. Thus, considering the above, $F_{\mathrm{SW,SC}}$ was chosen to be 100 kHz, which is the closest sub-multiple of $F_{\mathrm{SW,BST}}$ (1 MHz).

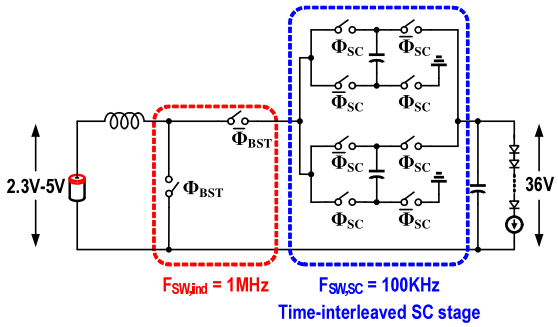

Fig. 10. Time-interleaving of the SC stage to mitigate large output voltage ripple.

C. Time-Interleaved SC Stage

While operating the SC-stage at 100 kHz can potentially reduce its switching losses, it has a detrimental effect on the output ripple. For instance, a 50% duty cycle 100-kHz clock for the SC stage results in the output capacitor floating for a duration of 5 μs, which results in an unacceptably large peak-to-peak ripple of 0.25 V at a typical load of 25 mA and a worst case ripple of 1 V at 100-mA load with 0.5-μF output capacitance. In conventional boost converters, the headroom of the LED bias current source must be increased ($\mathrm{V_{HR}} = \mathrm{V_{D,SAT}} + \mathrm{V_{RIPPLE}}$) to absorb the excessive ripple and prevent it from affecting the backlight quality. However, this degrades LED-driver power efficiency and causes perceivable flicker in the backlight. One possible way to avoid this large ripple is to ensure that the lost charge in the output capacitor is replenished faster. This can be achieved by splitting the single SC stage into two time-interleaved sections that alternately connect to the output capacitor. The operation of the converter is described in detail in Section III-E. The final architecture of the proposed boost converter is shown in Fig. 10. It consists of ten power switches, all rated at $V_{\mathrm{OUT}}/2$, and two additional external flying capacitors C_{FLY}.

D. Efficiency and Loss Breakdown

Theoretical power efficiency plots comparing the proposed hybrid boost converter with the conventional boost converter are shown in Fig. 11(a). These plots show a marked improvement in efficiency across the entire load range with about 5% and 8% peak efficiency improvement at nominal and high loads, respectively. The improvement in conduction and

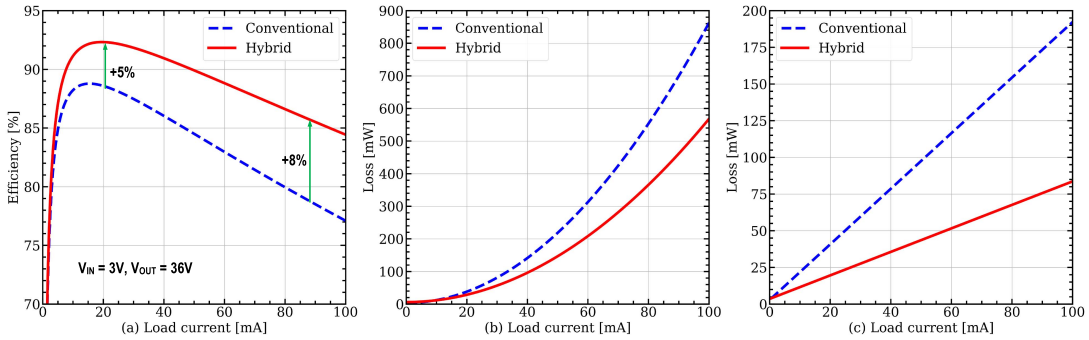

Fig. 11. (a) Efficiency plots of the hybrid and conventional architectures. (b) Conduction loss comparison. (c) Switching loss comparison.

TABLE I
PERCENTAGE REDUCTION IN LOSSES WITH RESPECT TO CONVENTIONAL INDUCTIVE-BOOST CONVERTER

Loss	% Reduction	Cause
Conduction	30	Device rating
Switching	52	Device rating+low $F_{SW,SC}$
Core	22.6	Inductor current ripple reduced

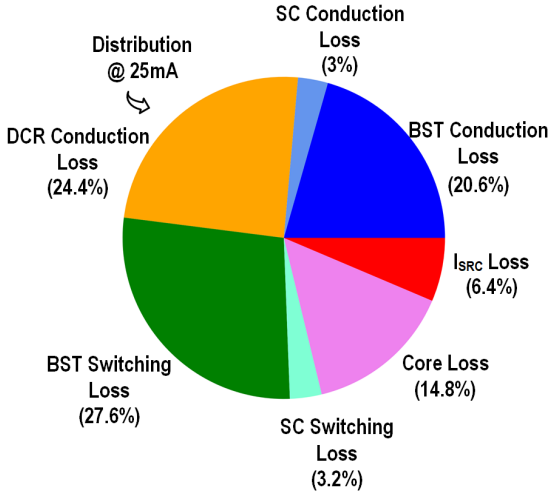

Fig. 12. Simulated power loss breakdown at 25-mA load for the proposed converter.

switching losses is captured in Fig. 11(b) and (c). They show a significant reduction in switching losses and modest improvement in conduction losses, both of which illustrate that higher quality switches and the SC-stage's low-switching frequency indeed help improve efficiency. The simulated power loss breakdown for the proposed converter at 25-mA load is shown in Fig. 12, and the percentage reduction in losses normalized to those of a conventional inductive-boost converter is shown in Table I.

E. Phase Operation

The converter operates in four phases, Φ_1, Φ_2, Φ_3, and Φ_4 (see Fig. 13). We describe the operation starting with phase Φ_1 in which both the BST- and SC-stage clocks ϕ_{BST} and ϕ_{SC} are high. During this phase, inductor and C_{FLY2} are connected to the ground, while C_{FLY1} is connected to the output. The duration of this phase is equal to $D * T_{\text{BST}}$, where D is the duty cycle of the clock ϕ_{BST} and T_{BST} is the period of ϕ_{BST}. Because the inductor is disconnected from the load, the LED current source discharges the output capacitor. When ϕ_{BST} goes low, the converter enters Φ_2 phase during which inductor is connected to the SC stage. As $V_{\text{OUT}} = 2 * V_{\text{MID}}$, half the inductor current flows through the output capacitor through C_{FLY1} and the other half flows through C_{FLY2}. This causes V_{MID} voltage to ramp-up as shown in the waveforms on the right in Fig. 13. The kink in the ramp is caused by the voltage drop across the power devices in the SC stages. Since switching frequency of the SC stage is much smaller than the BST stage, ϕ_{BST} changes its phase five times in one half of ϕ_{SC}. Consequently C_{FLY1} and C_{FLY2} get discharged and charged, respectively, five times during Φ_2.

In the Φ_3 phase, C_{FLY1} and C_{FLY2} exchange positions. Since the voltages across C_{FLY1} and C_{FLY2} always add up to V_{OUT}, this change in positions of the flying capacitors do not affect the output voltage. The voltage at V_{MID} on the other hand always reflects voltage across C_{FLY2} in ϕ_{SC} and across C_{FLY1} in $\overline{\phi_{\text{SC}}}$. This node experiences a voltage jump when the flying capacitors exchange their positions because the inductor current cannot change suddenly. The voltage jump's magnitude is equal to the voltage difference between the voltages across C_{FLY1} and C_{FLY2} at the end of Φ_2. After this change in flying capacitor positions, the rest of the operation is exactly the same as described before, except now for the next five cycles of ϕ_{BST}, and C_{FLY1} is charged and the inductor current discharges C_{FLY2}. This marks the end of one complete cycle of ϕ_{SC}. The BST stage provides a dc gain of $1/(1-D)$, and the SC stage provides a gain of 2. Therefore, the relation between the output voltage and the BST stage's duty cycle is given by $2/(1-D)$.

IV. CIRCUIT IMPLEMENTATION

The complete schematic of the proposed converter is shown in Fig. 14. It consists of three main components: the power devices used in the BST and SC stages, the gate drivers for these power devices, and circuitry to regulate the converter's output voltage.

A. Power Switches

All the power devices in this architecture are rated at 20 V. The maximum voltage stress seen by each switch is

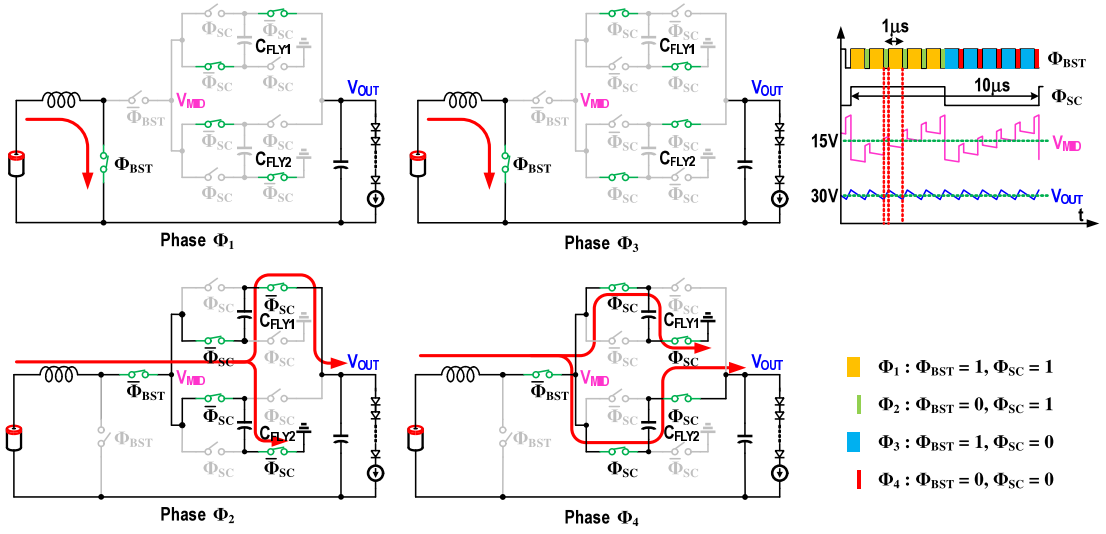

Fig. 13. Phase-by-phase operation and associated waveforms.

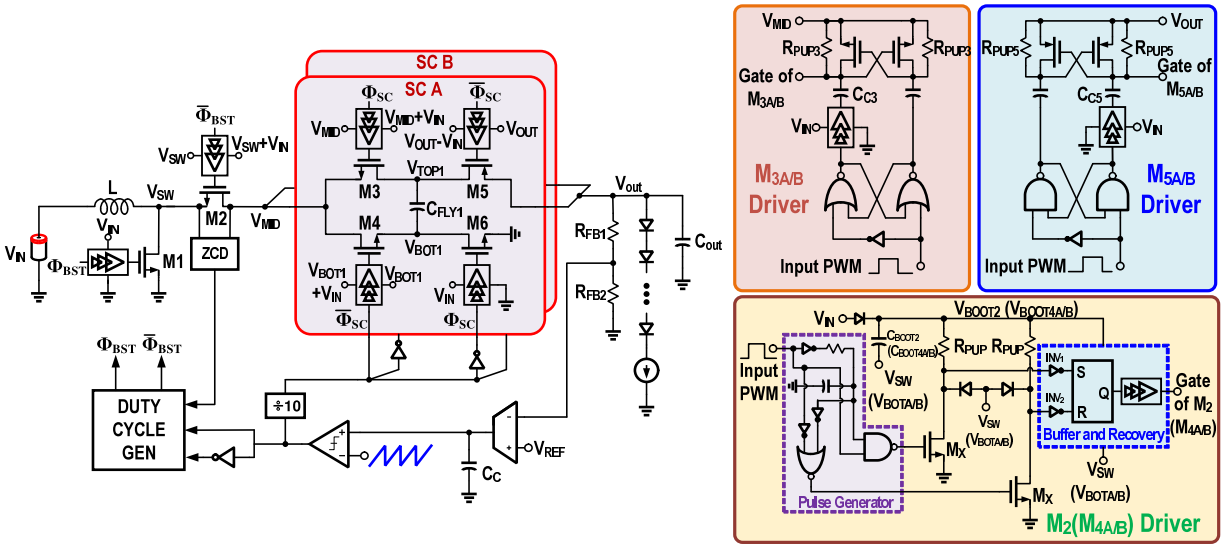

Fig. 14. Complete circuit schematic of the converter (left) and associated gate drivers (right).

given by $V_{\mathrm{OUT,max}}/2 + I_{\mathrm{OUT,max}} * 0.25 * T_{\mathrm{SW,SC}}/C_{\mathrm{FLY}}$ and is equal to 18.6 V. $T_{\mathrm{SW,SC}}$ $(1/F_{\mathrm{SW,SC}})$ is the switching period of the SC stage. Switch sizing was optimized to achieve peak efficiency at $I_{\mathrm{LOAD}} = 25$ mA. The BST stage's low-side switch is sized for an $r_{\mathrm{DS,ON}}$ of 123 mΩ, while the rest of the switches are sized for an $r_{\mathrm{DS,ON}}$ of 350 mΩ. The power devices occupy an area of 2.76 mm^2. Flip-chip packaging and careful routing of the power rails at both the chip and the PCB level were employed to reduce parasitic resistance and inductance.

B. Gate Drivers

The interleaved SC stage limits the maximum voltage across the power switches to $V_{\mathrm{OUT}}/2$, enabling the use of devices rated at $V_{\mathrm{OUT}}/2$ with lower $R_{\mathrm{DS,ON}}$ and smaller parasitic capacitance. Leveraging this topological benefit for improving efficiency without affecting device reliability requires carefully designed gate driver circuits. Fig. 14 shows these circuits used for driving power devices, M_2, $M_{3A/B}$, $M_{4A/B}$, $M_{5A/B}$, and $M_{6A/B}$, with the desired voltage levels of V_{SW}-to-$(V_{\mathrm{SW}} + V_{\mathrm{IN}})$, V_{MID}-to-$(V_{\mathrm{MID}} + V_{\mathrm{IN}})$, $V_{\mathrm{BOTA/B}}$-to-$(V_{\mathrm{BOTA/B}} + V_{\mathrm{IN}})$, $(V_{\mathrm{OUT}} - V_{\mathrm{IN}})$-to-$V_{\mathrm{OUT}}$, and 0-to-$V_{\mathrm{IN}}$, respectively. Drivers for M_1 and M_6 are implemented using tapered buffers operating with V_{IN} as their supply. M_2 $(M_{4A/B})$ driver is implemented using a dynamic level shifter [26] with bottom plate of the boot-strapping capacitor C_{BOOT2} $(C_{\mathrm{BOOT4A/B}})$ connected to V_{SW} $(V_{\mathrm{BOT1/2}})$. Transistor M_X (rated at $V_{\mathrm{IN}} + V_{\mathrm{OUT}}/2$) and pull-up resistor R_{PU} are sized such that swing at the inverter $(\mathrm{INV}_{1/2})$ input is about V_{IN}. To minimize static power, input PWM signal is converted into two narrow pulses and recovered using an set-reset (SR) latch. M_3 and M_5 drivers are implemented using capacitively coupled level shifters [26] in which coupling capacitors C_{C3} and C_{C5} hold voltages V_{MID} and V_{OUT},

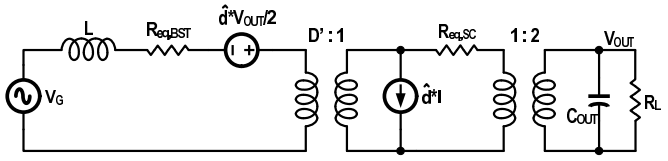

Fig. 15. Small-signal model for the proposed architecture in continuous conduction mode.

respectively. Pull-up resistors pre-charge capacitors ($C_{C3/5}$) to the required voltage levels before the start of each switching cycle. The coupling capacitors C_{C3} and C_{C5} and the boot-strap capacitors C_{BOOT2} ($C_{\text{BOOT4A/B}}$) are off-chip as they needed to be about ten times the gate capacitance of the power device they were driving. Both the bootstrap and coupling capacitors are implemented using 1.5-nF 0201 packaged surface-mount capacitors (0.02 in $\times$ 0.01 in).

C. Regulation Loop

A voltage-mode integral-control loop is used for regulating the output voltage. Note that a current source sets the LED current, and as a result, using a voltage-mode compensator has no bearing on the LED bias current as long as the output voltage is sufficiently high to forward bias all the LEDs and guarantee the desired voltage headroom for the current source. A transconductance-C stage integrates the difference between the converter output voltage and the reference voltage and generates a control voltage (V_{CTRL}). The value of compensation capacitor C_C is equal to 20 nF and it is implemented off-chip. PWM comparator compares V_{CTRL} with an externally fed 1 MHz sawtooth signal and produces a duty cycle for the low-side device of the BST stage. The loop bandwidth is about 1 kHz. The clock for the SC stage is generated by dividing the BST stage PWM signal by 10. A ring counter that generates a divide-by-five clock followed by a divide-by-two stage produces the divided-by-ten signal (100 kHz) with 50% duty cycle. The small-signal model for the proposed architecture has been derived based on the procedure in [12] and is shown in Fig. 15. The duty cycle to V_{OUT} transfer function is given by the following equation:

$$G_{\text{vd}} = \frac{V_{\text{OUT,DC}}}{2D'} \frac{1 - s\frac{4L}{D'^2 R_L}}{1 + s\left(\frac{4L}{D'^2 R_L} + \frac{4C_{\text{OUT}} R_{\text{eq}}}{D'^2}\right) + s^2 \frac{4LC_{\text{OUT}}}{D'^2}} \quad (8)$$

where $D' = 1 - D$, D being the duty cycle of the low-side switch of the BST stage.

D. Discontinuous Conduction Mode

The converter was operated in the DCM to improve the efficiency under light-load conditions (less than 5 mA). A zero-crossing detector circuit shown in Fig. 16 detects the voltage drop across the high-side power device and translates it to current. This voltage drop appears as a difference in V_{GS} of M_3 and M_4, which is then converted into a current equal to $i_{\text{SENSE}} = g_{M3,4}\Delta V_{\text{GS}}$. Trans-impedance amplifier (TIA) implemented using M_7–M_{10} transistors along with the post amplifier (M_{11} and M_{12}) converts i_{SENSE} into a rail-to-rail

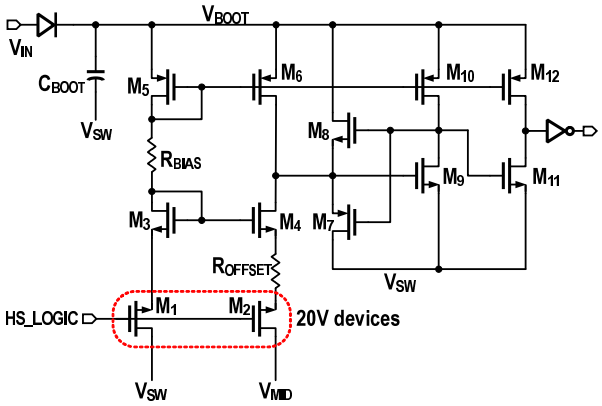

Fig. 16. Zero-crossing detector circuit used in the DCM.

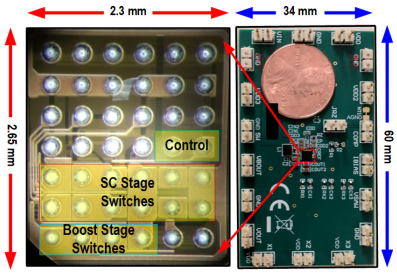

Fig. 17. Die micrograph and evaluation board.

voltage output. R_{BIAS} is used to generate an internal bias current, and R_{OFFSET} is used to create an intentional offset to account for the delay in the zero-crossing detector. M_1 and M_2 act as shielding devices to protect rest of the 5-V devices when the V_{SW} node goes to ground potential. The DCM mode improves efficiency by about 10% over the CCM mode at loads near 1 mA.

V. Measurement Results

A prototype converter was fabricated in a 180-nm process and attached to the test board using a flip-chip package (see Fig. 17). The active area is 2.8 mm^2.

Flying capacitors (C_{FLY1} and C_{FLY2}) were placed very close to the chip. During start-up, since all the initial flying-capacitor voltages are much lower than their steady-state values, the inductor current increases in both its switching phases, resulting in huge initial inductor current of the order of 2 A [see Fig. 19(b)]. Since the voltage at V_{MID} toggles between the two flying capacitor voltages, the initial inductor current surge can cause voltage at node V_{MID} to exceed the device rating. To avoid this, the SC-stage switching frequency is initially increased to 500 kHz, which is five times the steady-state switching frequency and reduced back to 100 kHz after $C_{\text{FLY,1}}$ and $C_{\text{FLY,2}}$ are charged to $V_{\text{OUT}}/2$ and the output capacitor is charged to V_{OUT}. In addition to the fast SC-stage switching during start-up, it would also be beneficial to employ an over-current protection scheme to limit the inductor current under a safe value. To this end, a simple over-current protection scheme based on a conventional resistor-based current sensing

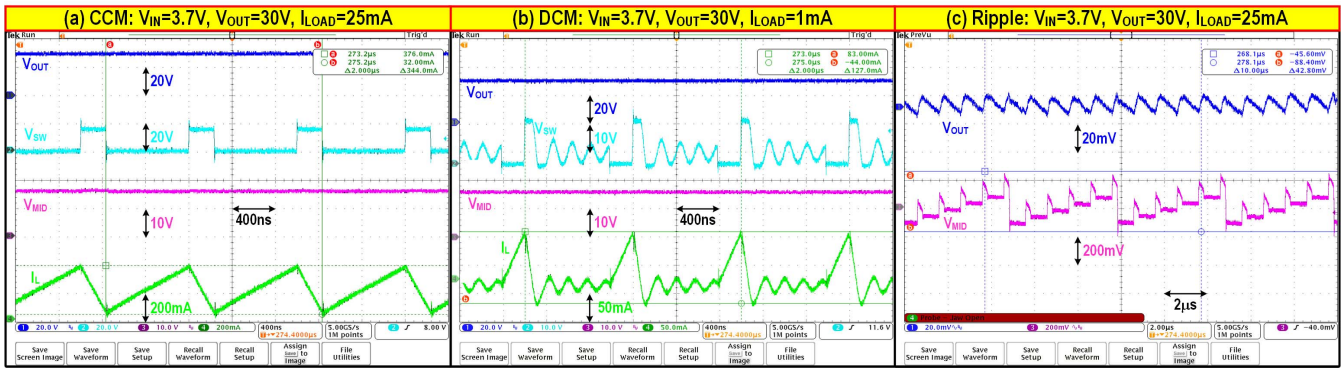

Fig. 18. Steady-state waveforms in (a) CCM, (b) DCM, and (c) ripple in CCM at 25-mA load.

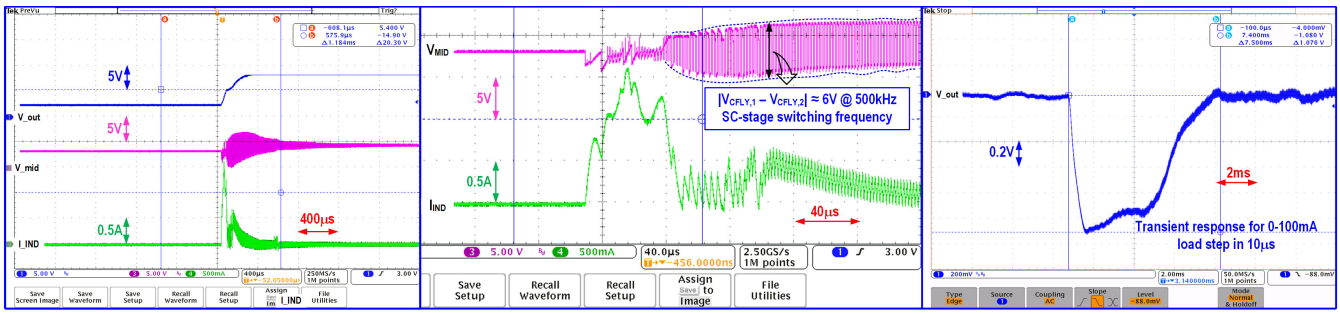

Fig. 19. Start-up waveforms (a) V_{OUT}, V_{MID} and I_{IND}, (b) V_{MID} and I_{IND} zoomed, and (c) load-step response.

at the LS power-FET of the BST stage [27] can be employed. Current sensing can also be performed by a sense-FET-based current sensor [28] by placing the sense-FET across the LS power-FET of the BST stage. Relevant steady-state voltages of the converter with $V_{IN} = 3.7$ V, $V_{OUT} = 30$ V, and $I_{LED} = 25$ mA in both CCM and DCM modes are shown in Fig. 18(a) and (b), respectively. Output voltage (V_{OUT}), switching node of the BST stage (V_{SW}), and voltage at the intermediate node between the BST and the SC stages (V_{MID}) along with the inductor current (I_L) waveforms are shown. V_{OUT} and V_{MID} have settled at 30 and 15 V, respectively, for both CCM and DCM operations. In the DCM operation, the ZCD circuit cuts off the high-side switch when the current through it crosses zero. This results in oscillations in V_{SW} and I_L as shown in Fig. 18(b) because the parasitic capacitance at V_{SW} node was still charged to V_{OUT} after the high-side switch was turned off. This provided a non-zero initial condition to the LC tank formed by the parasitic capacitance at V_{SW} and inductor L. This results in a small undershoot below zero in the inductor current.

Fig. 18(c) shows the small-signal ripple on the V_{OUT} and V_{MID} nodes. The expected shapes of ripple on V_{MID} and V_{OUT}, as explained in Section III E, prove the effectiveness of the time-interleaving approach to avoid large ripple on the output voltage. Even though V_{MID} experiences large voltage jumps ($\sim$ 200 mV at $I_{LED} = 25$ mA) caused by the flying capacitors exchanging positions, due to interleaving of the SC-stage, output voltage ripple remains less than 20 mV. Fig. 19(a) shows the start-up transients for V_{OUT}, V_{MID}, and inductor current I_{IND}. Fig. 19(c) shows a full-load step of 0–100 mA causing about 1-V droop. This is primarily because of the low-bandwidth voltage-mode control loop. Efficiency over a load current range of 0.5–100 mA was measured under different values of V_{IN} and V_{OUT}, and the results are plotted in Fig. 20(a). These results were obtained by using a 504 015 casing (5.0 mm $\times$ 4.0 mm $\times$ 1.5 mm) 10-μH inductor (DCR = 140 mΩ). Efficiency curves plotted with $V_{OUT} = 30$ V and $V_{IN} = 2.5$, 3.7 and 5 V show the peak efficiency of 91.15% at $V_{IN} = 3.7$ V/$I_{LED} = 30$ mA and 92.42% at $V_{IN} = 5$ V/$I_{LED} = 45$ mA. The converter is functional at $V_{IN} = 2.5$ V to guarantee overall system functionality even when the battery is almost fully discharged. Efficiency curves measured across three temperatures (0 °C, 25 °C, and 85°C), shown in Fig. 20(b), indicate that efficiency degrades by less than 2% across the temperature range.

Peak efficiency greater than 90% at $I_{LED} = 30$ mA was obtained even when a smaller volume inductor (25 201 casing with DCR = 350 mΩ) is used [see Fig. 20(b)]. The efficiency in DCM- and CCM-modes is shown in Fig. 20(c). Efficiency is improved by 10% at 1-mA load current in the DCM mode, thus proving the effectiveness of the zero-current detector. Summary of the achieved performance and comparison with state-of-the-art high-efficiency LED drivers is shown in Table II. This work achieves more than 3% efficiency improvement compared to [2] and [29], which have comparable input and output voltages. Compared to [10], the proposed converter's output voltage is 1.7$\times$ larger and does not require an extra inductor. In an attempt to have some comparison data, we measured the performance of our converter at V_{IN}/V_{OUT} of 5/20 V

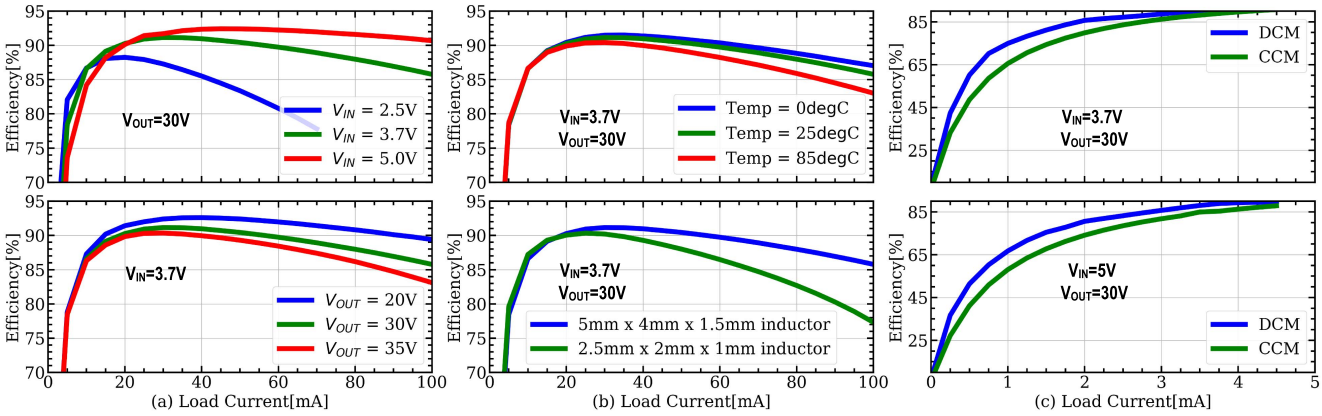

Fig. 20. Measured efficiencies with (a) different input and output voltages, (b) different temperature and external inductance at $V_{\text{IN}} = 3.7$ V and $V_{\text{OUT}} = 30$ V, and (c) DCM efficiency at loads less than 5 mA.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART LED DRIVERS

	This Work		LM36274 [29]	LM36923 [2]	JSSC '20 [10]	TPE '19 [9]	TPS6118 [3]
Technology	180 nm BCD		180 nm BCD	180 nm BCD	350 nm CMOS	–	–
Input Volt. [V]	2.3–5		2.7–5	2.7–5	2–4.4	6–18	5–24
Max Output Volt. [V]	35		29	28	20	50	40
Load Range [mA]	0–100		0–100	0–100	10–250	70–100	0–120
Conversion Ratio	2/(1-D)		1/(1-D)	1/(1-D)	2/(1-D)	(3-D)/(1-D)	1/(1-D)
Switching Freq.[Hz]	1M/100K		1M	1M	2M	$\leq$ 0.82M	1M
Output capacitor [μF]	20*		10	10	10	10	4.7
Flying Capacitor [μF]	2×2.2		–	–	2×0.47	2×260	–
Inductor [μH]	10		10	10	2×3.3	18	10
DCR [mΩ]	140	350	140	230	166	–	75
Inductor Vol. [mm^3]	$5 \times 4 \times 1.5$	$2.5 \times 2 \times 1$	$5 \times 4 \times 1.5$	$4 \times 3.2 \times 1.2$	–	–	$5.2 \times 5.2 \times 3$
Efficiency [%]	91.15 (93.6)	90.33	88	88	93.5	89.5	93
Load @ peak eff.[mA]	30 (50)	25	55	40	100	100	100
V_{IN} @ peak eff.[V]	3.7 (5)	3.7	3.7	3.7	4.2	6	11
V_{OUT} @ peak eff.[V]	30 (20)	30	28	28	18.9	30	28.8
Control	Voltage		Current	Current	Voltage	External	Current
Active area [mm^2]	2.76		3.95	2.27	0.89	8	–

* Unfortunately, a larger capacitor was used due to an oversight/error during the PCB design. There is no degradation in efficiency in using a smaller output capacitor.

and 50-mA load current. The peak efficiency was 93.6% when using the 140-mΩ 10-μH inductor. It is difficult to fairly compare this work with [10] because of the differences in the conversion gain (4.5 versus 10), output voltage (20 versus 35 V), load current (100 versus 25 mA), and switch ratings (10 versus 20 V). However, comparing [10] and this work at a conversion gain of 4.5 and load current of 25 mA (after down-scaling the losses reported at 100 mA in [10] and keeping the area equal) shows that the total losses in this works are 18% less compared to [10].

VI. CONCLUSION

We presented a new hybrid boost converter architecture for improving the efficiency of LED drivers used in mobile applications. By cascading a low-switching frequency time-interleaved series–parallel SC-stage with an inductive-boost converter, we demonstrated that switching losses can be greatly reduced. Charge-sharing losses of the SC stage are minimized by soft-charging flying capacitors with the inductor of the BST stage. Fabricated in 180-nm bipolar CMOS DMOS (BCD) process, the prototype converter generates 30-V output voltage from a Li-ion battery source and can provide a load current in the range of 0–100 mA with an excellent peak power efficiency of 91.15% at 30 mA. Compared to state-of-the-art designs, the proposed converter achieves a 3% improvement in peak power efficiency.

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In 2004, he joined National Semiconductor Corporation, Phoenix, AZ, USA, as an Analog Designer working on display power, communication interfaces, and power audio amplifiers. Since 2011, he has been working at Texas Instruments Inc., Phoenix, and continued to work in Texas Instruments Inc., Manchester, NH, USA, from 2019, developing mobile display backlight drivers, mobile power management integrated circuits (PMICs), and monolithic dc–dc buck regulators. He also has extensive verification experience, including system verilog (SV) and verilog and analog and mixed signal (VAMS) analog behavioral models and methodologies for fast full-chip regressions.

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Nathanael Griesert received the M.S.E.E. degree from the University of California at Davis, Davis, CA, USA, in 2001.

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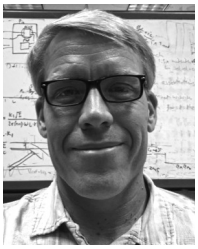

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Dr. Pilawa-Podgurski has been a member of the ISSCC Power Management Committee since 2018. He is the coauthor of ten IEEE prize papers. He received the Chorafas Award for outstanding MIT EECS Master's thesis, the Google Faculty Research Award in 2013, and the 2014 Richard M. Bass Outstanding Young Power Electronics Engineer Award of the IEEE Power Electronics Society, given annually to one individual for outstanding contributions to the field of power electronics before the age of 35. He received the Air Force Office of Scientific Research Young Investigator Award in 2015, the UIUC Dean's Award for Excellence in Research in 2016, the UIUC Campus Distinguished Promotion Award in 2017, and the UIUC ECE Ronald W. Pratt Faculty Outstanding Teaching Award in 2017. He was a recipient of the IEEE Education Society Mac E. Van Valkenburg Award given for outstanding contributions to teaching unusually early in one's career in 2018. From 2014 to 2019, he served as an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.

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Dr. Hanumolu is also the Editor-in-Chief of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.