Resolution-Related Design Considerations for a 120-GS/s 8-bit 2:1 Analog Multiplexer in SiGe-BiCMOS Technology

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***Abstract*— This article presents a 120-GS/s 2:1 8-bit analog multiplexer (AMUX) in SiGe-Bipolar CMOS (BiCMOS) technology that exhibits the highest effective resolution reported for an AMUX in any kind of semiconductor technology. This article presents the design considerations that have led to this high resolution. In particular, it contains a discussion on the choice of an AMUX circuit concept to support high linearity. A frequency-domain explanatory model for the signal contribution to the effective number of bits (ENoB) in the presence of mismatch errors is presented and applied to the analysis of timing and signal gain mismatch in the AMUX setup. Typical ENoB versus frequency characteristics were identified and utilized to speed up ENoB simulations and to develop calibration procedures for the different mismatch types in the AMUX setup. The results of the analysis and the performance of the AMUX in the calibrated setup were proven by measurement results.**

***Index Terms*— Analog multiplexer (AMUX), digital-to-analog-converter (DAC), effective number of bits (ENoB), high speed, linearity explanatory model, SiGe-Bipolar CMOS (BiCMOS).**

I. Introduction

ANALOG multiplexers (AMUXs) are used to double or quadruple the output signal bandwidth and sampling rate of digital-to-analog-converters (DACs) by time interleaving. As shown in the state of the art in Table I, sampling rates up to 168and 120 GS/s can be reached by a realization in InP technology [1] and SiGe-Bipolar CMOS (BiCMOS) technology [3], respectively. Currently, the main application area of AMUXs is to increase the transmission capacity per bandwidth in optical communication systems [1], [2]. In [3], we reported a 2:1 AMUX design that was realized to explore the performance limits of AMUXs in the SiGe-BiCMOS technology toward a targeted 8-bit resolution and a 50-GHz signal bandwidth. This AMUX was applied to a system-level testbed to develop the design considerations for next-generation high-speed optical transmission systems beyond 1 Tbit/s [4], [5]. Fig. 1 shows the setup of the AMUX with two DACs, DAC1 and DAC2 (commonly referred to as DAC1,2) driving the AMUX input as it is used in the system-level testbed as well as for the AMUX characterization in this article. In addition to twice the sampling rate and signal bandwidth, the ideal AMUX should sustain the effective resolution of the driving DACs in terms of ENoB=(SINAD-1.76)/6.02, that is, the SINAD ratio of signal-to-noise-and-distortion (NAD) power should be larger or at least equal to the one of the DACs. The aim of this article is to present the circuit design, the simulation, and the calibration considerations that have led to the comparatively high effective number of bits (ENoB) results of the AMUX in the setup of Fig. 1.

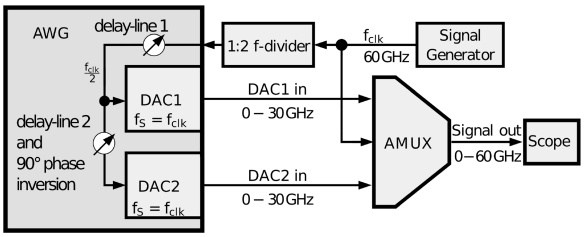

Fig. 1. AMUX setup used for the measurements in this article. The frequencies in the figure correspond to a sampling rate of 120 GS/s.

In a suchlike setup, there are three major sources that impair the SINAD at the AMUX output either by reducing the signal or by increasing the NAD power. First, there is the NAD of the driving DACs that is mapped onto the AMUX output. As this NAD is fixed by the given DACs, it is not a part of the AMUX design and, therefore, not considered in this article; however, it is an inevitable part of the ENoB measurement results of the AMUX (see Fig. 17). A further contribution to the NAD is the total harmonic distortion (THD) that originates from nonlinear AMUX signal paths between the DAC1,2 outputs and the AMUX output. Section II presents the design considerations for a low THD of these signal paths. If the THD is low, clock offset and mismatches in the AMUX and the setup become the major source of the ENoB impairment. Depending on the kind of mismatch, the ENoB degradation over frequency shows a specific characteristic, as shown in Fig. 2. The ENoB characteristics in subfigure (a) diverge from (d-type) or join with (j-type) the ideal ENoB versus frequency curve. These patterns and the related ENoB optimization were already described in [3] and could be traced back to clock offset (d-type) and layout-related clock delay (j-type). In this article, three further severe root causes

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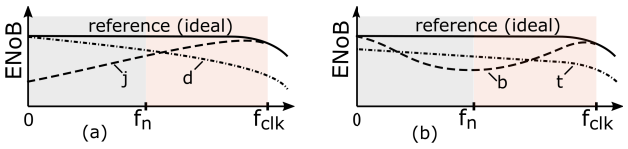


Fig. 2. Basic types of ENoB versus frequency characteristics of an AMUX. (a) Diverge, d-, and join—j-type. (b) Tilted and translated, t-, and bathtub—b-type.

for AMUX ENoB degradation, which relate to the AMUX circuit design as well as to the whole AMUX setup, will be analyzed. In Sections IV and V, the impact of signal-to-signal and clock-to-signal timing mismatches as well as signal gain mismatch is analyzed. A systematic mathematical analysis of mismatch errors was already presented in [6] by means of signal processing equations. The analysis in our article is based on the explanatory model in Section III. It creates a link to the circuit design by modeling the AMUX by idealized mixers and it allows to analyze the frequency characteristics of the amplitudes of wanted and unwanted tones in the AMUX output spectrum. The results show for the first time how the different kinds of mismatch errors affect these amplitudes and thereby lead to the characteristic ENoB versus frequency patterns in Fig. 2(b). Moreover, the analyses show how these characteristics are utilized to identify the root cause of an ENoB degradation, how to speed up time-consuming circuit simulations on transistor level, and how to develop the mismatch calibration procedures in Section VI for the AMUX setup in Fig. 1. Finally, Section VII shows the measurement results of the AMUX and demonstrates the mismatch characteristics as well as the effect of the calibration on the AMUX performance.

II. Circuit Concept and Linearity Considerations

Currently, two basic AMUX concepts can be found in the literature. In [7], a comparatively complex concept based on explicit generation and addition of return-to-zero (RZ) signals is shown, which reaches 100 GS/s and 4.9 ENoB at a comparably small power consumption of only 0.53 W if operated as a 2:1 AMUX. For the design presented in this article, power consumption was not a primary concern because the project targets are on the exploration of the effective resolution limit of the AMUXs in SiGe-BiCMOS technology at the highest possible circuit speed. Therefore, we have chosen a comparably simple selector-circuit concept that reaches a maximum resolution and a sampling rate of 7.7 ENoB and 120 GS/s, respectively. A detailed comparison of the pros and cons of both concepts can be found in [7, Sec. II].

The block diagram of our differentially operated AMUX design is shown in Fig. 3. It consists of the selector circuit of Fig. 4 in the 2:1 AMUX core and a clock buffer chain, which were designed based on the cell-based design methodology in [8]. The clock buffer chain consists of four differentially operated buffer cells, each realized by a load resistor pair at the input followed by two emitter follower (EF) pairs, a current switch (CS), and a common base stage (CBS) at the output.

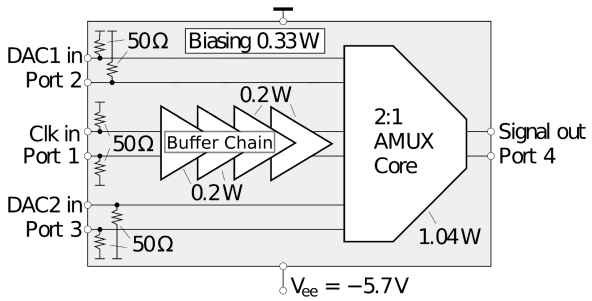


Fig. 3. Block diagram of the 2:1 AMUX IC.

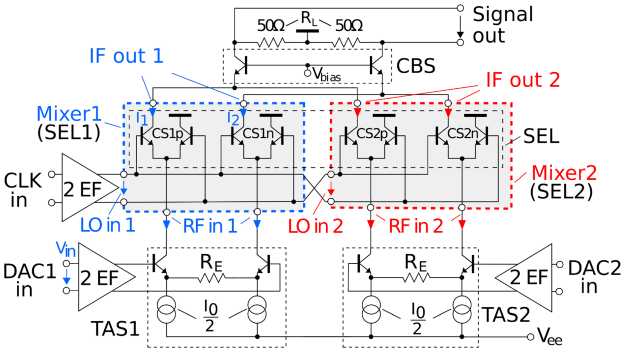


Fig. 4. Circuit principle of the 2:1 AMUX core realized by the clocked-SEL concept.

Each buffer consumes a power of 0.2 W at a supply voltage of −5.7 V.

The circuit diagram of the 2:1 AMUX core in which a clocked selector-stage (SEL) performs the actual AMUX function is shown in Fig. 4. This clocked-SEL circuit concept was preferred to the competing clocked transadmittance (clocked-TAS) concept [1], [9]–[11] shown in Fig. 5. As will be shown hereunder, the choice between both concepts is basically a tradeoff between a high sampling rate and a high linearity.

In the clocked-SEL concept of Fig. 4, two linear transadmittance stages (TAS1,2) at the signal input convert the input voltage into a differential output current. Each TAS operates with a bias current $I_0 = 24$ mA and utilizes series feedback resistors $R_E = 66\ \Omega$ for linearization. This results in a low THD and a related ENoB in excess of the targeted 8-bit resolution in the frequency range of the first Nyquist band of the driving DACs for differential input amplitudes up to 500 mV (1Vpp). As explained in [12] (see Section III-A), high bias currents of 2×4 mA and 2×14 mA are used for the first and second EF-pair to sustain the inherently high linearity of the EFs at high frequencies for driving the capacitive input impedance of TAS1,2. For the EF-pairs at the clock input, high bias currents of 2×8 mA and 2×20 mA are chosen to drive the high capacitive load represented by the four SEL1,2 CSs. The emitter length of all transistors is chosen according to a peak-fT of 10 mA/μm^2. The output signal currents of TAS1,2 drive the SEL1 and SEL2 (SEL1,2) subcircuits of the SEL stage at the AMUX output. As shown in [3], each of SEL1,2 basically represents an unbalanced mixer, whose effect is considered in the explanatory model in Section III by

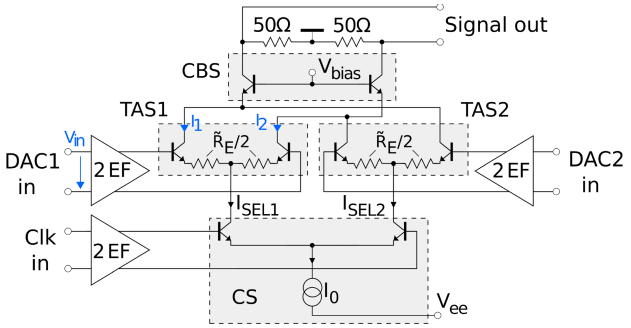


Fig. 5. Circuit principle for an alternative 2:1 AMUX core based on the clocked-TAS concept.

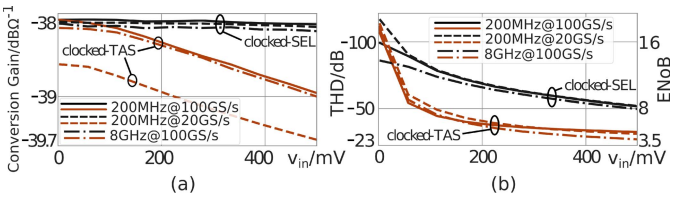


Fig. 6. (a) Comparison between the simulated conversion gains of a signal path for a signal frequency $f_1 = 200$ MHz at 20 and 100 GS/s and $f_1 = 8$ GHz at 100 GS/s and (b) corresponding ENoB between the clocked-TAS and the clocked-SEL concept.

a multiplication of the SEL1,2 input current by an idealized 1/0 clock sequence. The function of the CBS at the output is based on its low input impedance. It sums up the differential SEL1 and SEL2 output signal currents and it improves the isolation between SEL output and the clock input. Thereby, it reduces the intermodulation products in the AMUX output spectrum. The bias currents at a −5.7-V supply voltage result in a total power consumption of 1.04 W for the AMUX core cell (i.e., 48% of the total AMUX power consumption). This fairly high power consumption was in line with the project target to explore the performance limits of SiGe AMUXs in terms of speed and resolution. Fig. 5 shows an alternative selector concept with a clocked-TAS. Here, the signal path from AMUX input to the CBS at the output consists of only the two TAS1,2 stages. In contrast to the clocked-SEL concept, the bias currents $I_{\mathrm{SEL1,2}}$ of the TAS1,2 input stages of the clocked-TAS concept in Fig. 5 are clocked.

In the ideal case, the clock signal causes these bias currents to alternate between I_0 and 0 and thereby turn TAS1,2 ON and OFF. This dynamic biasing leads to the intended alternating selection (interleaving) of both linear signal paths and represents the basic AMUX function. In comparison to the clocked-SEL, this concept requires only one static bias current source I_0 to bias both, TAS1 and TAS2. If the transistors in the clock-CS and their bias current source I_0 are considered ideal (i.e., without parasitic capacitances), the choice $I_0 = 24$ mA would lead to the same bias current during the ON-state of TAS1,2 as for the clocked-SEL concept. For real transistors, it is shown in [13] (see Fig. 3) that the dynamic CS output currents $I_{\mathrm{SEL1,2}}$ can exceed the static bias current level by a dynamic overshoot that depends on the total capacitance at the emitter node of the CS and the rise and fall times of the clock signal at the CS input. This increased dynamic bias current also increases the signal gain of TAS1,2. For a fair comparison in terms of linearity hereunder, this gain has to be reduced to the level of the clocked-SEL concept. This could be done either by reducing I_0 or by raising the emitter degeneration resistance $\tilde{R}_E$ over the level of R_E in the clocked-TAS. In view of an overly fair comparison, we have chosen the second option that increases the linearity of the clocked-TAS in contrast to the first option. According to these considerations, the CS is biased by $I_0 = 24$ mA and $\tilde{R}_E = 106\ \Omega$ is chosen for TAS1,2, which results in the same conversion gain for both concepts as shown in the linearity comparison hereunder. Corresponding to the clocked-SEL design, high bias currents of 2×4 mA and 2×14 mA are used for the first and second EF-pair in the signal path as well as 8 and 20 mA for the first and second EF-pair that drive the clock-CS, respectively. Again, the emitter length of all transistors is chosen according to a peak-fT of 10 mA/μm^2.

The clocked-TAS concept requires only one current source I_0 to equivalently bias TAS1,2. This results in half of the power consumption of the SEL concept. In terms of sampling speed, the clocked-TAS concept is also the superior choice because the speed limiting input capacitance of only one CS instead of four needs to be driven. These are big advantages in comparison with the clocked-SEL concept; however, the clocked-SEL concept was the preferred choice for the AMUX core due to its superior linearity as will be shown in the following.

An adequate method to compare the linearity between both clocked concepts, which basically act like unbalanced mixers, is based on the conversion gain $20\log(I_{\mathrm{IF}}(f_1)/V_{\mathrm{in}}(f_1))$, which is determined by a transient simulation at a signal frequency f_1 applied to one of the DAC1,2 inputs. In the following, the DAC1 input is chosen. In this definition, $V_{\mathrm{in}}(f_1)$ is the amplitude of a sinusoidal differential voltage at the DAC1 input at a frequency f_l and $I_{\mathrm{IF}}(f_1)$ is the related amplitude in the spectrum of the differential output current $I_{\mathrm{IF}}(f_1) = I_1 - I_2$ of the respective concept, with the input and output signals V_{in}, I_1, and I_2 of the signal paths defined in Figs. 4 and 5. A low and a high signal frequency of $f_1 = 200$ MHz and 8 GHz are chosen to eliminate frequency-dependent effects and to show the high-frequency performance. The clock input is driven either by a 10- or 50-GHz signal corresponding to an AMUX sampling rate of 20 and 100 GS/s. Fig. 6(a) shows the respective conversion gains of the two concepts in dependence on the signal input amplitude V_{in} for 20 and 100 GS/s. The simulation results show that the conversion gain of the preferred clocked-SEL concept is nearly constant over a 0.5-V input amplitude range for all sampling rates and input frequencies. At low input amplitudes, the conversion gain of the clocked-TAS at 100 GS/s exhibits the same conversion gain as the clocked-SEL. At 100 mV, the gain starts to decrease and falls at 500 mV by about 1 dB below the gain of the clocked-SEL concept. The same degradation over the input amplitude can also be seen at 20 GS/s; however, the conversion gain is about 0.5 dB smaller over the entire input voltage range due to the reduced dynamic overshoot

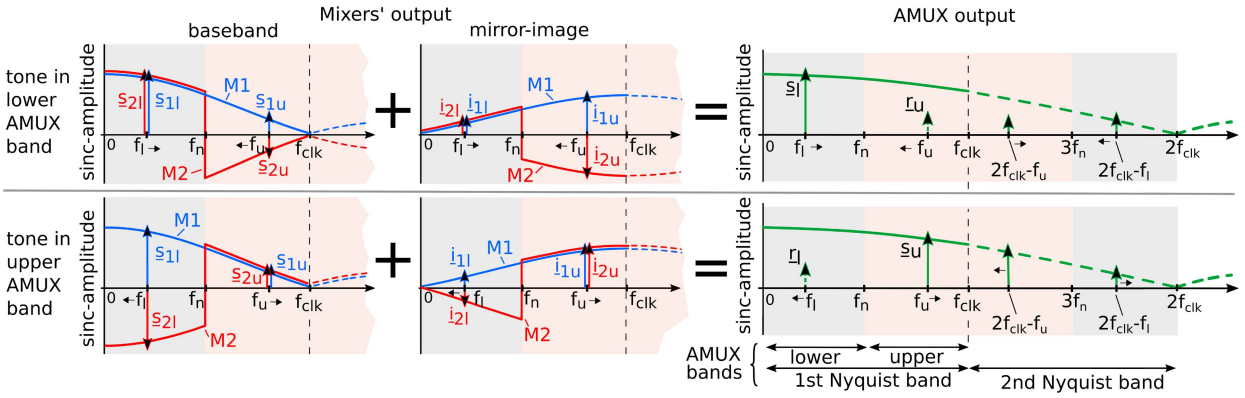


Fig. 7. Spectra at the AMUX-output. Column 1: baseband spectra at IF-output of Mixer1 (M1) and Mixer2 (M2). Column 2: mirrored image of the basebands (clock of M2 is inverse to M1). Column 3: AMUX output spectrum by the superposition of baseband and image spectra considering a residue $\underline{r}_u, \underline{r}_l$ of the unwanted tone. First/second row: spectra of a tone created at f_l/f_u in the lower/upper AMUX frequency band.

at the lower sampling rate. The non-linearity caused by the reduced gain at high input amplitudes rises the THD at the output of the clocked-TAS in comparison to the clocked-SEL, as shown in Fig. 6(b). The resulting ENoB for 200 MHz and 8 GHz signals at 20 and 100 GS/s is shown in Fig. 6(b). At low input amplitudes, both concepts show about the same high ENoB in the vicinity of 16 bit at all sampling rates and signal frequencies; however, in the range of the maximum signal input amplitude, 400…500 mA, the clocked-TAS concept reaches a resolution of only 5 ENoB, whereas the clocked-SEL ENoB is about 8 bit. This higher resolution is the reason why the clocked-SEL concept was chosen for the AMUX core. The lower linearity of the clocked-TAS is mainly caused by the base–emitter capacitance of the TAS transistors and the output capacitance of the clock-CS in conjunction with the clocked bias currents $I_{\mathrm{SEL1,2}}$ (see Fig. 5). It can be shown by circuit simulations that the portion of $I_{\mathrm{SEL1,2}}$ through these capacitances increases with a rising signal voltage at the TAS1,2 inputs. This current fraction is missing in the actual bias current of the intrinsic TAS1,2 transistor and thereby leads to a reduced output amplitude at higher TAS1,2 input voltages. This constitutes the nonlinear behavior of TAS1,2 where mainly the third harmonic contributes to the THD and the related ENoB.

III. Frequency-Domain Mismatch Considerations

The ENoB characteristics of the AMUX can be analyzed by means of a simple frequency-domain explanatory model. The basic approach of this model was presented in [3] and is summarized hereunder together with modifications that are tailored to the analysis in this article. The model addresses only the fundamental operation of the AMUX given by the effect of the SEL1,2 stages in Fig. 4 to gain qualitative explanations in conjunction with the analysis in Sections IV and V.

1) The effect of the SEL1,2 stages in Fig. 4 is modeled by ideal unbalanced mixers (Mixer1,2). The mixers' RF-input signals are represented by the differential output currents of TAS1,2. This allows to consider a potential gain and delay mismatches due to TAS1,2 as a part of the input signal path.
2) The LO-inputs of the mixers are driven by the AMUX clock signal with a frequency f_{clk}, which is twice the Nyquist frequency f_{n} of DAC1,2. The idealized effect of the clock signal leads to an IF-output signal that equals the multiplication of the RF-input signal by a 1/0 clock sequence.
3) The baseband spectra at the Mixer1,2 IF-outputs are shown in column 1 of Fig. 7. They represent a replica of the respective RF-input spectrum, which corresponds to the DAC1,2 output signals that drive the AMUX signal inputs. The signal phase in the second Nyquist band of Mixer2 is inverted due to the 90° phase shift of the DAC2 clock (see Fig. 1).
4) The DAC1,2 output signals are modeled by zero-order-hold (ZOH) reconstruction functions whereby their amplitude spectrum follows the $\mathrm{sinc}(f_{\mathrm{clk}}) := \sin(\pi f_{\mathrm{clk}})/\pi f_{\mathrm{clk}}$ envelopes shown by the blue solid and red curves in columns 1 and 2 of Fig. 7.
5) The mirror-image spectra in column 2 of Fig. 7 represents the lower sidebands of the mixers' IF-output signals, which are the mirror images of the respective basebands shown in column 1. The Mixer2 mirror-image spectrum is phase-inverted due to an inverted clock at the Mixer2 LO-input.
6) For each row in Fig. 7, the superposition of the Mixer1,2 basebands and their related mirror images results in the AMUX output spectra on the right-hand side of this figure. The amplitudes of the superposed spectra approximately follow a $\mathrm{sinc}(2\ f_{\mathrm{clk}})$ envelope. This yields the intended doubling of the DAC1,2 Nyquist frequency f_{n} by the AMUX.
7) Tones in all spectra are represented by phasors with the 0° reference phase shown in an upright position. Phasors of Mixer1,2 at the same tone are referred to as phasor pairs. Ideally, phasor pairs have the same amplitude and either constructively add up (equal phase) to create a wanted tone or cancel out each other (inverted phase) to discard an unwanted tone. The phase inversion of the second Nyquist band of Mixer2 is shown by flipping the ZOH reconstruction function (sinc envelopes) upside down.

8) The AMUX output frequency range consists of a lower and an upper frequency band that join at the DAC1,2 Nyquist frequency f_n.
   a) A tone at a frequency f_l in the lower frequency band is created (see Fig. 7, row 1) by generating the sinusoidal waveform of this tone in the digital code domain of DAC1,2 with equal amplitude and phase. Due to the ZOH reconstruction function of DAC1,2, this tone appears also as a mirror image at $f_u = f_{clk} - f_l$ in the second Nyquist band of the DAC1,2 output signals. These tones constitute according to (3) the baseband spectra and phasor pairs $(\underline{s}_{1l}, \underline{s}_{2l})$ and $(\underline{s}_{1u}, \underline{s}_{2u})$ and according to (5) also the mirror image and phasor pairs $(\underline{i}_{1l}, \underline{i}_{2l})$ and $(\underline{i}_{1u}, \underline{i}_{2u})$, at the Mixers' output in Fig. 7. The superposition of these spectra creates according to (6) the AMUX output tone at f_l.
   b) A tone at a frequency f_u in the upper frequency band (see Fig. 7, row 2) is likewise created by generating a tone at $f_l = f_{clk} - f_u$ in the digital code domain of DAC1,2 with equal amplitudes but with inverted phases.
   c) A complete AMUX output spectrum with tones in the lower and upper bands is created by the superposition of the respective digital domain data for tones f_l and f_u in the lower and upper bands according to (a) and (b). In terms of phasors, this results for DAC1 in the superposition $\underline{s}_{1l} + \underline{s}_{1l} = 2\underline{s}_{1l}$ and for DAC2 in $\underline{s}_{2l} + (-\underline{s}_{2l}) = 0$, that is, DAC1 has to generate a waveform according to $2\underline{s}_{1l}$, while DAC2 is silent.
9) Residual image tones in the output spectra appear if the phasor pairs with inverted phase, $(\underline{s}_{1u}, \underline{s}_{2u})$, $(\underline{i}_{1u}, \underline{i}_{2u})$ and $(\underline{s}_{1l}, \underline{s}_{2l})$, $(\underline{i}_{1l}, \underline{i}_{2l})$ for a tone in the lower and the upper band, respectively, do not ideally cancel out each other due to a mismatch in amplitude or phase. These residues always appear in the AMUX band complementary to one of the generated tones.
10) The AMUX output spectrum of the explanatory model only considers the generated signal tones $\underline{s}_l$ and $\underline{s}_u$ and their related unwanted residual image tones $\underline{r}_u$ and $\underline{r}_l$ that account for the NAD for a tone in the lower and upper AMUX bands, respectively. Consequently, the SINAD calculated by this model is given by the respective ratios $|\underline{s}_l/\underline{r}_u|^2$ and $|\underline{s}_u/\underline{r}_l|^2$.

The ENoB calculated by this SINAD definition represents the effective resolution due to only mismatch errors, whereas the actual ENoB might be altered by the NAD of the driving DAC1,2 as well as by the THD of the AMUX signal path. However, as long as the power of these two contributions is small in comparison to the power of the mismatch-related residual image tone, the ENoB calculated by the explanatory model represents a good approximation of the actual AMUX ENoB. This is, e.g., the case in the measured AMUX output spectrum in Fig. 18(a) for the AMUX setup without mismatch calibration. Furthermore, in such a case, the SINAD equals the spurious-free dynamic range (SFDR) and the rejection ratio of the signal to the residual image tone (SIRR). In the measurement results of the actual ENOB in Fig. 19, the quality of this approximation can be judged by comparing the ENoB results calculated by the SINAD with those calculated by the SIRR and SFDR.

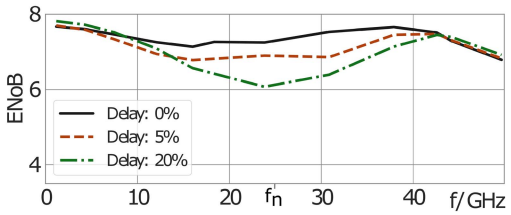


Fig. 8. Impact of a clock delay on the simulated ENoB at 100 GS/s for ideal DAC1,2 signals with 8-bit resolution.

Finally, it shall be noted that all simulated and measured ENoB characteristics in this work were obtained without the use of a sinc compensation or any pre-filtering of the input signals.

IV. Timing-Related Resolution Impairments

A. Clock-to-Signal Timing

A delay of the clock signal in relation to the ideal clock-to-input signal timing can lead to a resolution degradation of the AMUX design. This is shown in Fig. 8 by the result of an ENoB simulation at 100 GS/s for the optimal timing in comparison with a clock delay of 5% and 20% in relation to the 50-GHz clock signal period. Note that all simulation results presented in this section are carried out based on transistor models of the foundry's design kit and include all relevant layout parasitics. The result shows that the ENoB degrades mainly in the middle of the AMUX output frequency range, which refers to the basic b-type (bathtub) ENoB pattern in Fig. 2. The maximum degradation at f_n amounts to 0.4 and 1.2 bit for a 5% and a 20% clock delay, respectively.

As will be shown in the following, the underlying root cause always leads to a maximum ENoB degradation at f_n because of the coherent sampling of the DAC1,2 signal. The explanation hereunder is based on the conclusions of the explanatory model and applies to both AMUX signal paths that are commonly referred to by the index term 1,2.

The timing relations for a tone at f_l or f_u at a large distance to the center frequency f_n (i.e., $f_l \to 0$, $f_u \to 2\ f_n$) are shown in Fig. 9(a) and for a tone close to f_n (i.e., f_l, $f_u \approx f_n$) in Fig. 9(b). Both subfigures of the top row show the respective RF-input current of Mixer1,2 that contains the idealized ZOH reconstruction function of the DAC1,2 output signals. This input current is multiplied by the 1/0-clock sequence of Mixer1,2 (see (2) of the explanatory model). The multiplication by 1 creates a window in time during which the RF-input current appears at the IF outputs (see IF out 1,2 in Fig. 4). The resulting IF output current is shown in the second and third rows of Fig. 9 for ideal (blue shaded time slots) and worst case (red shaded time slots) timing, respectively. Since the mixers' LO-frequency equals the DAC1,2 sampling rate (coherent sampling), the timing between the window and the DAC1,2 ZOH-samples is fixed,

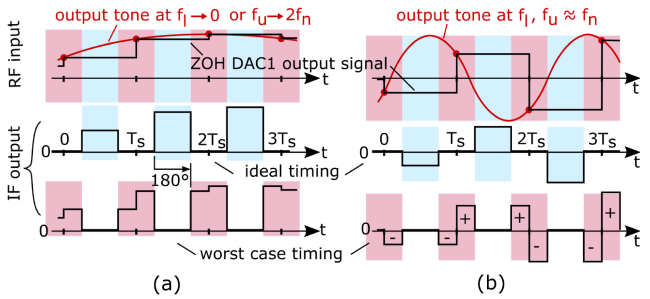


Fig. 9. Timing between the ZOH DAC1,2 output signal samples and the AMUX clock at the LO-inputs of Mixer1,2 for (a) tone generated at a large distance and (b) tone close to the DAC1,2 Nyquist frequency. DAC1,2 output signals are shown on top, and Mixer1,2 IF output signals at ideal and worst case timing are shown in the middle and at the bottom, respectively.

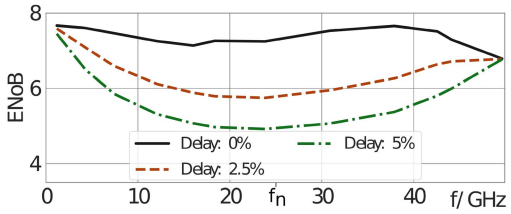


Fig. 10. Impact of a signal delay on the simulated ENoB at 100 GS/s for ideal DAC1,2 signals with 8-bit resolution.

that is, only the amplitude levels in Fig. 9 change if the frequency of the generated tone is changed.

In case of ideal timing, the window is centered in time at the middle of a constant ZOH interval between two consecutive samples that appear at integer multiples of $T_S = 1/f_{\text{clk}}$. In this case, the IF-output amplitude in this window equals the constant amplitude of the respective ZOH section (see the second row in Fig. 9).

The worst timing case, shown at the bottom of Fig. 9, occurs if this ideal timing is delayed by 180° whereby the center of the window is located at the time of the sampling. Thus, the amplitudes in both halves of the window relate to the consecutive amplitudes of the ZOH waveform. For a tone at a large distance to the center frequency f_n in Fig. 9(a), the difference between both amplitudes in a window is small. Due to bandwidth limitations, this difference will be averaged out whereby the amplitude mean in the window represents a good approximation of the original ZOH DAC1,2 output signal.

This is not the case if the generated tone is close to the center frequency. Since in this case f_l, $f_u \approx f_n$, consecutive ZOH-samples are at similar amplitudes (they become equal if f_l, $f_u = f_n$) but at opposite signs. This creates a bipolar pulse shape pattern with the respective positive and negative amplitudes inside a window [+/− signs inside the pulses at the bottom of Fig. 9(b)]. This pulse train mainly contains a doubled clock frequency component (averages out considering bandwidth limitations) and only a residual fraction of the original ZOH amplitude.

Since these considerations apply to both AMUX signal paths, the respective IF output currents of both mixers and thereby the AMUX output signal contain in this worst case scenario only a residue of the actual signal amplitude. Therefore, it is mainly the signal amplitude that reduces the SINAD; however, a rise of the NAD-related amplitude may also contribute due to the harmonic content of the bipolar pulse train. Finally, the reduced SINAD leads to a degraded ENoB. The maximum degradation appears in the extreme case for a tone generated at f_l, $f_u = f_n$. Under worst case timing, the negative and positive amplitudes become equal and exactly average out without any residue of the original ZOH amplitude whereby the generated tone vanishes.

The ENoB for 5% and 20% delay, shown in Fig. 8, corresponds to less extreme phase shifts of 18° and 72°. In this case, the bipolar amplitudes in each window only partially average out whereby a significant residual of the original ZOH amplitude remains at the IF outputs. This results in a moderate reduction of the signal amplitude in the SINAD and thereby in a moderate dip of the ENoB at f_n.

As a result of this analysis, the maximum ENoB degradation under a clock-to-signal timing misalignment appears at the center frequency f_n of the AMUX frequency range, whereas for frequencies at a large distance to f_n, the degradation becomes negligible. This behavior finally constitutes the b-type characteristic of the ENoB. Because ENoB simulations on transistor level are rather time-consuming, the maximum degradation due to this timing misalignment can be found by only one ENoB simulation at f_n.

B. Signal-to-Signal Timing

In comparison with the clock delay, already small delays between the signals at the mixers' IF-input can lead to a significant degradation of the effective resolution of the AMUX's output signal. Fig. 10 shows a simulation result of the ENoB at 100 GS/s with no delay between the input signals (0% reference) in comparison with delays of 0.5 and 1 ps, which correspond to delays of 2.5% and 5% related to the DAC1,2 sampling rate of $T_S = 1/(50\ \text{GS/s})$. The ENoB degradation in this figure clearly exhibits a bathtub characteristic with a maximum degradation of 1.6 and 2.4 bit for 2.5% and 5% delay, respectively, at f_n. At the boundaries of the AMUX frequency range, both curves reach the ideal ENoB of the 0% reference curve. Although signal-to-signal and clock-to-signal delay exhibit a b-type characteristic, the following analysis will show that the root cause and thereby the related optimization procedure differ.

The root cause can be identified by means of the spectra in Fig. 11, which are modified versions of the ones in Fig. 7 that account for a delay between the two signal paths by a phase difference between a phasor pair. A constant delay τ between the IF-input signals results in a frequency-dependent phase shift $\Theta = 2\pi f \tau$ between a phasor pair. In the baseband, this alters the ideal phase relation of 0° and 180° in the pairs $(\underline{s}_{1l}, \underline{s}_{2l})$ and $(\underline{s}_{1u}, \underline{s}_{2u})$ at f_l and f_u by a phase difference of $\Theta_l = 2\pi f_l \tau$ and $\Theta_u = 2\pi f_u \tau$, respectively. Note that Θ_u/Θ_l is proportional to f_u/f_l. In the mirror image of this baseband, the phasor pairs $(\underline{i}_{1u}, \underline{i}_{2u})$ and $(\underline{i}_{1l}, \underline{i}_{2l})$ at f_u and f_l carry the

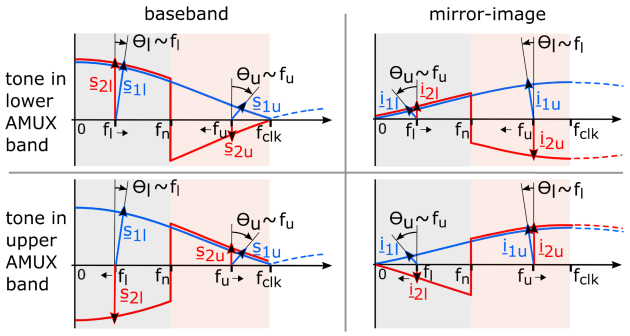


Fig. 11. Modified phasor diagrams of Fig. 7 considering a frequency proportional phase shift between the two signal paths of the AMUX.

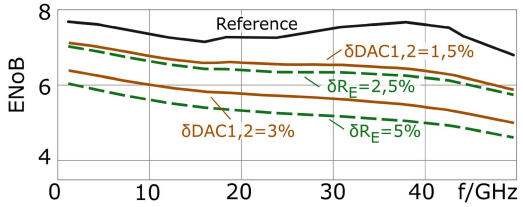


Fig. 12. Simulation result for an R_E-mismatch of $\delta R_E = 2.5\%$ and 5% and a DAC1,2 output amplitude mismatch of δDAC1, $2 = 1.5\%$ and 3% between both AMUX input signal paths in comparison with the ideal reference ENoB at 100 GS/s.

phase difference Θ_l and Θ_u of the corresponding pairs in the baseband.

The following analysis applies to signal tones at a frequency f_l generated in the lower AMUX band, which is illustrated in the first row of Fig. 11. Due to a mirror symmetry, the results do likewise apply to the upper AMUX band. The AMUX output signal amplitude

$$|\underline{s}_l| = |(\underline{s}_{1l} + \underline{s}_{2l}) + (\underline{i}_{1l} + \underline{i}_{2l})| \tag{1}$$

results from the sum of the phasor pairs at f_l in the lower AMUX band, whereas the sum of the phasor pairs in the upper band causes the residual amplitude

$$|\underline{r}_u| = |(\underline{s}_{1u} + \underline{s}_{2u}) + (\underline{i}_{1u} + \underline{i}_{2u})| \tag{2}$$

of the unwanted tone at f_u, which is the main contributor to the NAD power in the SINAD. The ratio $|\underline{s}_l|/|\underline{r}_u|$ approximates the SINAD and thereby determines the frequency characteristics of the ENoB (i.e., (10) of the explanatory model).

At low frequencies f_l, the signal output amplitude is mainly determined by the phasor pair $(\underline{s}_{1l} + \underline{s}_{2l})$ because the phasor pair $(\underline{i}_{1l} + \underline{i}_{2l})$ at f_l in the mirror image has a negligibly small amplitude caused by the sinc envelope. This explains why despite the large phase shift Θ_u of this pair the signal amplitude at a low f_l is not altered.

The same consideration applies to the NAD related amplitude $|\underline{r}_u|$ in (2) where the phasor pair $(\underline{i}_{1u} + \underline{i}_{2u})$ almost perfectly cancels out because of $\Theta_l \to 0$. In contrast, the pair $(\underline{s}_{1u} + \underline{s}_{2u})$ does not cancel out due to the large phase shift Θ_u; however, the small amplitude of the related sinc envelope in this frequency range renders the contribution of this pair to $|\underline{r}_u|$ negligible. Because of the negligible impact of the phase differences Θ_l, Θ_u, the ENoB curves in Fig. 10 start at low frequencies at the ideal 0% reference curve.

Based on this explanation, the rapid decay of the ENoB over frequency of the 2.5% and 5% delay curves can be explained. It is caused by a decrease of the signal amplitude $|\underline{s}_l|$ due to a rising Θ_l and a Θ_u which is decreasing but is still larger than Θ_l in the lower AMUX band. Due to these phase differences, the resulting amplitudes of the phasor pairs in (1) are reduced compared to their 0% reference amplitude.

Even more important for the rapid decay of the ENoB over frequency is the increase of the NAD-related amplitude $|\underline{r}_u|$. This is due to the rising amplitude of the pair $(\underline{s}_{1u} + \underline{s}_{2u})$ along the sinc envelope as well as to the increasing phase difference Θ_l of the pair $(\underline{i}_{1u} + \underline{i}_{2u})$. These effects and thereby the ENoB degradation increase over frequency until the signal frequency f_l reaches the upper end of the lower AMUX band at f_n (i.e., the center of the AMUX output frequency range).

For the subsequent upper AMUX band, no further analysis is required because there exists a mirror symmetry to the spectra of the lower AMUX band. As shown in Fig. 11, the spectra of diagonally opposed diagrams in both rows (i.e., for tones in the lower and upper AMUC bands) are mirror-symmetrical such that there is a correspondence between the set of phasor pairs $(\underline{s}_{1l}, \underline{s}_{2l})$, $(\underline{s}_{1u}, \underline{s}_{2u})$, $(\underline{i}_{1l}, \underline{i}_{2l})$, $(\underline{i}_{1u}, \underline{i}_{2u})$ and the respective set $(\underline{i}_{1u}, \underline{i}_{2u})$, $(\underline{i}_{1l}, \underline{i}_{2l})$, $(\underline{s}_{1u}, \underline{s}_{2u})$, $(\underline{s}_{1l}, \underline{s}_{2l})$. This results in a mirror symmetry of the ENoB characteristics between the lower and upper AMUX bands that determine the b-type pattern observed in Fig. 10.

The analysis shows that in case of a signal-to-signal mismatch, the ENoB degradation is due to raised residual amplitude. This is in contrast to the degradation under a clock-to-signal mismatch, which is caused by fading signal amplitude. Likewise the clock-to-signal timing, valuable time in circuit simulation can be saved because the maximum degradation due to this timing misalignment can be found by only one ENoB simulation in the vicinity of f_n.

V. Signal-Path Gain Matching

The effective resolution of the AMUX is very sensitive to a gain mismatch between both input signal paths. Each path not only includes the respective circuitry on the AMUX chip but also the entire signal path to the driving DAC1,2 chips in the arbitrary waveform generator (AWG) (see Fig. 1). Since the gain of a signal path is mainly determined by the emitter degeneration resistors R_E of TAS1 and TAS2 (see Fig. 4), any R_E mismatch directly impairs the ENoB. This is shown in Fig. 12 by the result of an ENoB simulation at 100 GS/s for a mismatch of 2.5% and 5% between R_E of TAS1 and TAS2. Note that the simulation results presented in this section are carried out based on the transistor models of the foundry's design kit and include all relevant layout parasitics. Such mismatch numbers can result from a technology-related mismatch if only little attention is paid to the mismatch criteria. In the design of the AMUX, a one-σ mismatch of 0.7% was achieved by a large resistor area of 28.35 μm^2 for $R_E = 66\ \Omega$ and an equally oriented resistor placement. To prevent additional mismatch caused by a temperature

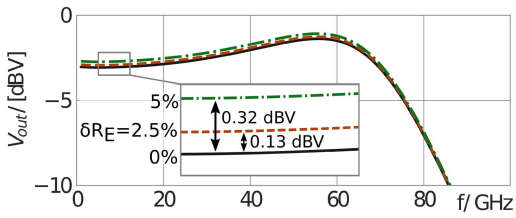


Fig. 13. Impact of 0%, 2.5%, and 5% R_E variation on the gain of an AMUX signal path from a DAC signal input to the AMUX signal output.

gradient, a thermally symmetrical layout is aimed at and the resistors in both paths are placed along isothermals. The effect of a mismatch residual is compensated by the calibration procedure given in Section VI-C. Fig. 12 shows that the ENoB in case of a mismatch exhibits a tilted and vertically translated characteristic (i.e., the t-type of Fig. 2) compared to the reference curve without mismatch impairment. The effect of the R_E mismatch on the gain is shown by the simulated frequency response in Fig. 13. Although the gain mismatch in this figure appears almost negligible, it causes a tremendous effect on the ENoB in Fig. 12.

A further source of a t-type ENoB characteristic originates from different output amplitudes of the DAC1,2 components. This is because the different amplitudes can be considered as the effect of an equivalent gain mismatch, which introduces the t-type characteristic. This is confirmed in Fig. 12, which shows the simulation results for a frequency-independent mismatch of 1.5% and 3% between the DAC1,2 output amplitudes.

The root cause that explains the underlying t-type characteristic can be found by means of the spectra in Fig. 7. Therein, a frequency-independent gain mismatch results in a different scaling (by a constant positive real number) of all the baseband and image phasor amplitudes of Mixer1,2. The main effect of this scaling results in residues of the unwanted tone because the related phasor pairs do no longer ideally cancel out. These residues determine the SINAD and thereby the ENoB. According to the final sinc envelope that determines the phasor amplitudes at the AMUX output (column 3 of Fig. 7), a tone in the lower AMUX band has a higher signal amplitude at f_{l} and a lower residue amplitude at f_{u} than a tone in the upper AMUX band. Furthermore, the signal amplitude of the wanted tone continuously decreases over frequency, whereas the residue amplitude rises. Hence, the SINAD ratio of the signal to the residue amplitude starts at low frequencies with a certain degraded ENoB that degrades further over frequency. This results in the tilted vertically translated ENoB characteristic of the simulation result in Fig. 12. For the circuit simulation, this result shows that an ENoB simulation in the frequency range close to f_{clk} contains the maximum impairment due to gain mismatch.

VI. Mismatch Calibration

By the optimization of the signal-path linearity described in Section II, the THD of the AMUX is low enough to result in an ENoB in excess of 8 bit in the first AMUX band (see Fig. 6). However, this resolution cannot be reached by the final AMUX setup mainly for two reasons. One relates to the NAD contributed by the driving DAC1,2, which is considered as a given fixed degradation that is mapped into both AMUX bands (see Fig. 17). The other source of impairments is the timing and gain mismatches discussed in Sections IV and V. As shown by the ENoB measurement results in Fig. 19, even moderate mismatch numbers can severely alter the signal and the residual image amplitude and thereby determine the SINAD and the related ENoB. Depending on the kind and quality of the hardware (e.g., mismatches between DAC1 and DAC2 or cables) and the particular layout of the AMUX setup (e.g., phase errors caused by cable bends), these mismatch numbers are subject to change and therefore cannot be addressed by a fixed setting. As a consequence, we have addressed the anticipated mismatch variations by the following calibration procedures that are based on the results of Sections IV and V.

A. Clock-to-Signal Timing

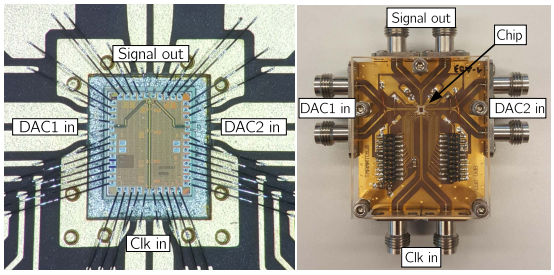
The clock-to-signal timing can be adjusted by delay line 1 as a part of the DAC1,2 setup in Fig. 1 with a resolution of 15 fs (i.e., 0.0075% of T_S) over a range of 21.325 ps. This range is sufficient to shift the DAC1,2 clock phase over a full 50-GS/s sample period when the AMUX operates at 100 GS/s. According to the result of Section IV-A, the maximum ENoB degradation under a clock-to-signal timing misalignment appears at the center frequency f_{n} of the AMUX frequency range and is caused by a reduced amplitude of the generated tone. Therefore, the optimal delay setting is determined by maximizing the amplitude of the tone generated around f_{n}. This is accomplished by a simple software calibration routine that determines this amplitude and adjusts the delay via an SPI interface until the maximum amplitude is reached.

B. Signal-to-Signal Timing

In the design of the AMUX setup, the signal-to-signal timing can be adjusted by delay line 2 in Fig. 1. This delay line is identical to delay line 1, which is used for the clock-to-signal timing. As shown in the analysis in Section IV-B, a signal-to-signal mismatch mainly raises the residue of the unwanted tone. The related maximum ENoB degradation appears at the center frequency f_{n}. Therefore, the optimal delay setting is determined by a software calibration routine that minimizes the residual amplitude of the unwanted tone at a frequency around f_{n}.

C. Gain Mismatch

In the AMUX setup, any gain mismatch is compensated by independent settings of the DAC1 and DAC2 output amplitudes, which can be adjusted in 1.5-mV steps in a range of 200–600 mV via an SPI interface to a computer. According to Section V, the worst ENoB degradation of the t-type pattern appears at the maximum AMUX output frequency and is mainly caused by the residue of the unwanted tone. This results in a calibration routine that adjusts the relation between the DAC1,2 output amplitudes in a way that minimizes the



(a) (b)

Fig. 14. (a) AMUX IC bondwire assembly. (b) RF-module.

amplitude of the unwanted tone for a signal tone generated close to the maximum output frequency 2 f_n.

VII. Measurement Results

Based on the design considerations presented in this article and in [3], the AMUX-chip was designed and fabricated in ST Microelectronic's 55-nm BiCMOS technology (f_T/f_{max} = 325 GHz/375 GHz). The chip in Fig. 14(a) consumes 2.17 W at a single supply voltage of −5.7 V and was mounted into an RF-module [see Fig. 14(b)] with a Teflon substrate and a bondwire assembly [3]. Fig. 16(a) shows the impact of the module packaging at the AMUX output by a comparison between the measured differential output reflection coefficient S_{44}^- at the module's V-connector and the simulation results for the reflection coefficient of the bare chip output, including pad capacitance with and without the bondwire interface. As can be seen, the bondwire interface with a length of about 0.38 mm significantly improves the reflection coefficient in the frequency range up to 50 GHz and causes a moderate degeneration of about 2.9 dB at 60 GHz. A measurement on a coupled microstrip line similar to the one at the output of the AMUX in the RF-module shows a frequency proportional attenuation that reaches 1.3 dB at 50 GHz. In a worst case estimation where only the generated tone at 50 GHz is attenuated while the NAD is not affected, the SINAD and ENoB would be reduced by only 1.8 dB and 0.3 bit, respectively. Fig. 1 shows the complete AMUX setup consisting of a MICRAM two-channel 8-bit DAC5 AWG representing the DAC1,2 that drive the AMUX signal inputs and the distribution of the clock signal generated by a Keysight E8257D signal generator. The differential voltage swings at the AMUXs' signal and clock inputs are both 1Vpp. Time-domain measurement results of the AMUX output signal are taken by a Keysight DCA-X N1000A sampling oscilloscope. By means of this setup, the high-speed performance of the AMUX was characterized.

Fig. 15 shows the AMUX output for PAM-4 signals at symbol and sampling rates of 100 GBd/100 GS/s and 120 GBd/120 GS/s, respectively. The latter result represents the highest symbol and sampling rate achieved by an AMUX in SiGe-BiCMOS technology. These already in [3] shown results were achieved after a full mismatch calibration according to Section VI and without pre-filtering the DAC1,2 output signals. Each eyediagram contains 40 repetitions of a 4096-bit (four levels of order 6) De Bruijn sequence. Without the calibration, no eye-opening would be visible, whereas with calibration, the clock-to-signal phase can be shifted by 7.5 and 3 ps, corresponding to clock phase margins of 270° and 130° at 100- and 120-GS/s sampling rates, respectively, until the eye openings in Fig. 15 are closed. The same margins are measured for a signal-to-signal phase shift.

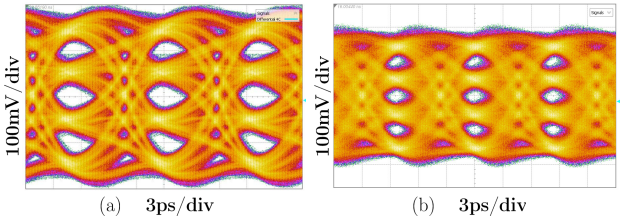


Fig. 15. Differentially measured eyediagrams at (a) 100 GBd/100 GS/s PAM-4 and (b) 120 GBd/120 GS/s PAM-4.

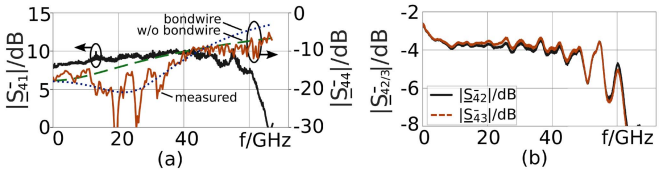


Fig. 16. Odd-mode S-parameters of the AMUX module. (a) Transmission S_{41}^- of the clock path to the AMUX output and output reflection coefficient S_{44}^- in comparison with a simulation result of the bare chip with and without bondwires. (b) Transmission S_{42}^-, S_{43}^- of both signal paths to the AMUX output.

Most of the references in Table I provide the S-parameter measurement results on the clock- and signal-path transmission. To support a comparison by means of these performance figures, the respective measurement results on the AMUX-module are shown in Fig. 16 and Table I. The measurements were taken on the AMUX module by a Keysight E8361A vector network analyzer. Fig. 16(a) shows the odd-mode forward transmission S-parameter of the clock signal. For this measurement, the input signals are replaced by a static differential bias voltage of 480 mV at each signal input, which represents the level of the maximum signal amplitude. Due to a total voltage gain of 20, the clock path is operated in the limiting mode and thereby gains a sufficiently high cutoff frequency of 64 GHz. Note that this cutoff frequency includes also the effect of parasitic capacitance and bondwire inductance at the AMUX output, which are not part of the clock path under normal AMUX operation.

Fig. 16(b) shows the odd-mode forward transmission S-parameters of the signal channels. The differential input and output ports are represented in this measurement by the DAC1,2 inputs and the AMUX output, respectively. Likewise, the clock-path measurement of the clock signal is replaced by a static differential bias voltage of 480 mV, which represents the level of the clock signal amplitude. Both signal channels exhibit a 3-dB bandwidth of about 50 GHz that is limited by multi-reflection ripple caused by the parasitics of the V-connectors of the RF-module and the bondwire interface at the AMUX chip. It should be noted that this result does not represent the signal transmission characteristic under normal

TABLE I
STATE OF THE ART

	Technology (f_T/f_{max})/GHz	Sampling rate	ENoB at $(f_{low}$ - $f_{high})^{***}$	Bandwidth clock path	Bandwidth signal path	diff. output voltage swing	Power / Supply voltage
[9]	0.5 µm-InP(290/320)	80 GS/s	-	50 GHz	-	-	0.5 W/ −4.5 V
[10]	0.5 µm-InP(290/320)	128 GS/s	-	64 GHz	67 GHz	0.5 Vpp	0.54 W/ −4.5 V
[1]	0.25 µm-InP(460/480)	168 GS/s**	-	99 GHz	> 110 GHz	1.5 Vpp	0.9 W/ −4.5 V
[14]	0.7 µm-InP(340/410)	100 GS/s	-	-	-	1.1 Vpp	-
[15]	0.13 µm-SiGe(300/500)	56 GS/s*	-	60 GHz*	> 67 GHz*	0.75 Vpp	1.06 W/ −4.5 V
[7]	55 nm-SiGe(320/370)	100 GS/s	4.9 - 4.25	≥ 50 GHz	73 GHz	0.4 Vpp	0.7 W/ 2.5 V
This work, [3]	55 nm-SiGe(325/375)	120 GS/s	7.7 - 4.1	64 GHz	50 GHz	0.7 Vpp	2.17 W/ −5.7 V

(*Measured on chip) (**using pre-filtered input signals) (*** f_{low}/f_{high} is the smallest/highest measured frequency for the ENoB)

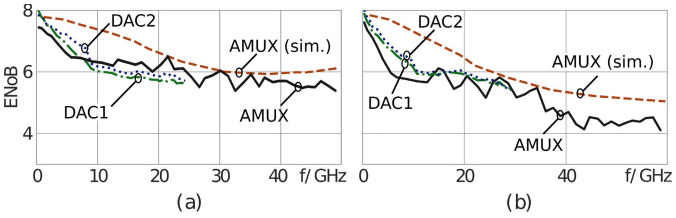


Fig. 17. ENoB measurement and simulation results of the AMUX and DAC1,2 at (a) 100 GS/s and (b) 120 GS/s.

AMUX operation where the mixers are active. However, it can show, as in this case, that the bandwidth of the signal path is sufficiently high to transmit also the second Nyquist band from DAC1,2 to the mixer inputs of the AMUX. Without this frequency band, a substantial part of the AMUX output spectrum is missing (see Section III).

Fig. 17 shows the AMUX ENoB measurement results mentioned in [3] at 100 and 120 GS/s in comparison with the simulated performance and the DAC1,2 input signals as a reference for the following results. These results were achieved after a full mismatch calibration of the AMUX setup. The ENoB of the AMUX in both subfigures starts at 7.7 bit and drops down to about 6 bit already in the frequency range below 10 GHz. This degradation is introduced by the ENoB characteristic of the DAC1,2 components that drive the AMUX. Fig. 17 shows that this characteristic is similarly mapped into the lower and upper AMUX bands. At high frequencies, the ENoB reaches 5.1 bit at 48.8 GHz and 4.1 bit at 58.6 GHz at 100 and 120 GS/s, respectively. In comparison with the state of the art presented in Table I, this is the highest effective resolution reported for an AMUX in any kind of semiconductor technology.

Fig. 18 shows the output spectra of the AMUX with calibrated timing mismatches before and after the calibration of a 6% gain mismatch for a signal tone at 2.37 GHz and 100 GS/s. Before the calibration, the ENoB in Fig. 18(a) is mainly determined by the comparatively strong amplitude of the unwanted residual image tone, which leads to approximately the same SINAD, SFDR, and SIRR of 36.2 dB and a corresponding ENoB of 5.8 bit. In this uncalibrated case, the ENOB characteristic corresponds to the result of the analysis based on the explanatory model, which is clearly visible in the measurement result of Fig. 19(a). After calibration, the residual image tone in Fig. 18 is reduced to about the level of the harmonic distortion of the AMUX and one additional spur at 26 GHz that originates from DAC1,2. In this case, the residual image tone no longer dominates the resulting ENoB of 7.2 bit that relates

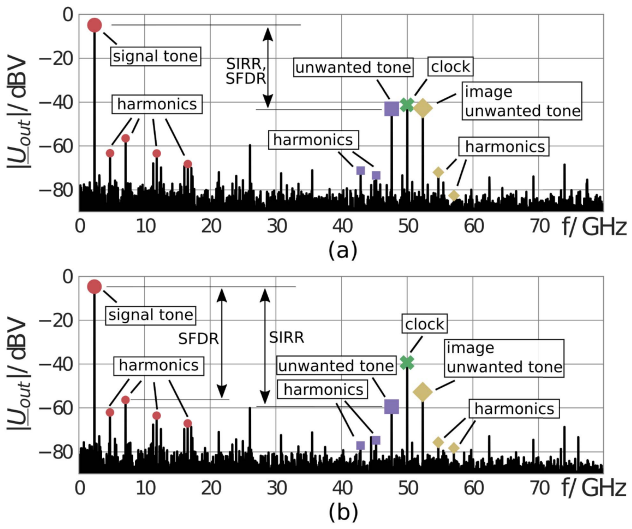


Fig. 18. Spectra at the AMUX output for a tone generated at 2.37 GHz at 100 GS/s with (a) uncalibrated and (b) calibrated AMUX. The spur at 26 GHz originates from the DAC1,2 output noise.

to an SINAD of 45.1 dB, whereas the SIRR of 54.8 dB due to the residual image tone is even slightly below the SFDR of 51.8 dB, which is given by the third harmonic at 7.11 GHz. Fig. 19 shows the ENoB measurement results for examples of moderate timing and gain mismatches; however, the actual mismatch numbers depend on the individual components and the layout of the setup. For our particular measurement setup in Fig. 1, gain and signal-to-signal mismatch were measured to be at 4% and 2.7 ps (13.5%), respectively. The clock-to-signal mismatch in the setup depends on the individual delay of each component in the signal and clock path. Instead of designing these delays for a small mismatch, we decided to match the clock-to-signal delay by means of the calibration procedure described in Section VI; however, without calibration, the respective mismatch is arbitrary and ranges between 0% and 100% in relation to the clock signal period. For the example in Fig. 19(a), moderate mismatch of 20% is chosen.

The reference ENoB in this figure is identical to the AMUX ENoB in Fig. 17(a) after calibration. The solid ENoB curves under a mismatch are determined by introducing the respective mismatch into this calibrated AMUX setup and calculating the ENoB by the SINAD. These curves agree well with the result of the analysis in Sections IV and V. In Fig. 19(a), the b- as well as t-type ENoB pattern is clearly visible by the difference between the reference and the impaired ENoB curve. As further references, also the ENoB calculated by

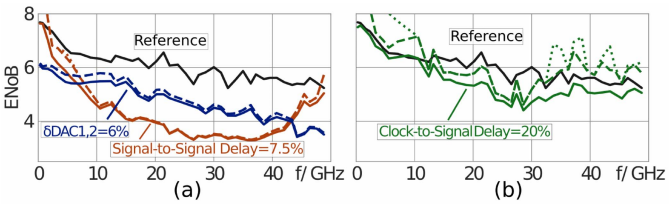


Fig. 19. ENoB characteristics of the AMUX setup at 100 GS/s. (a) Signal-to-signal-delay mismatch of 7.5% and a signal gain mismatch $\delta DAC1,2 = 6\%$. (b) 20% clock-to-signal-delay mismatch. In both figures, the ENoB for a fully calibrated AMUX setup is shown as a reference. For comparison, also the SFDR (dashed) and SIRR (dotted)-based ENOB curves are shown.

the SFDR and SIRR is shown by the dashed and dotted curves, respectively. Because of the dominating amplitude of the residual image tone, these curves are almost identical to the actual ENoB. However, in the respective regions of the ENoB patterns where the degradation due to mismatch is low, also THD and DAC1,2 contribute to the NAD, and thus, the actual ENoB falls below these reference curves. Fig. 19(b) shows the ENoB degradation due to a clock-to-signal-delay mismatch by the solid curve that exhibits the predicted b-type pattern with a maximum ENoB degradation in the middle of the AMUX frequency range. Also, both the SFDR- and SIRR-based ENoB reference curves exhibit this pattern. However, their ENoB numbers are higher than the actual SINAD-based ENoB. This is because, according to the analysis, a clock-to-signal mismatch mainly reduces the signal amplitude instead of creating a dominating residual image tone. In this case, also THD of the AMUX and the NAD of DAC1,2 substantially contribute to the SINAD-based ENoB, whereas those contributions are underestimated by the SFDR- and SIRR-based ENoB.

VIII. Conclusion

In this article, a 120-GS/s 8-bit 2:1 AMUX in SiGe-BiCMOS technology and the design considerations that have led to its record resolution were presented. It was shown how to design the AMUX signal path for a high linearity and why a clocked-SEL concept is a superior choice in this regard. An explanatory frequency-domain model for the signal contribution to the ENoB in the appearance of mismatch errors was presented and applied to the analysis of timing and signal gain mismatch. Typical ENoB versus frequency characteristics were identified and utilized to speed up ENoB simulations and to develop calibration procedures for the different mismatch types that appear in an AMUX setup. The results of the analysis were proved by measurement results and applied to the calibration of the AMUX setup.

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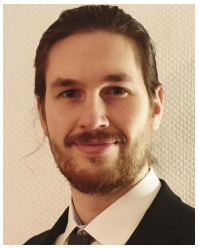

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