A 0.35-V 5,200-μm^2 2.1-MHz Temperature-Resilient Relaxation Oscillator With 667 fJ/Cycle Energy Efficiency Using an Asymmetric Swing-Boosted *RC* Network and a Dual-Path Comparator

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***Abstract*— This article describes a 2.1-MHz relaxation oscillator (RxO) for energy-harvesting Internet-of-Things (IoT) sensor nodes. The RxO features an asymmetric swing-boosted *RC* network and a dual-path comparator to surmount the challenges of sub-0.5-V operation while achieving temperature resilience. The former enables alternating the common-mode voltages at the output of the *RC* network to facilitate the sub-0.5-V operation, while the latter is outfitted with a delay generator for tracking the temperature-sensitive delay of the comparator. Prototyped in 28-nm CMOS, the RxO occupies a tiny footprint of 5,200 μm^2. The power consumption is 1.4 μW at 0.35 V. The measured temperature stability is 158 ppm/°C (average of seven chips) over −20 °C–120 °C. It scores the best energy efficiency (667 fJ/cycle) among the reported MHz-range RxOs and has a figure-of-merit (181 dB) that compares favorably with the state-of-the-art.**

***Index Terms*— Asymmetric *RC* network, CMOS, energy-harvesting, Internet-of-Things (IoT), relaxation oscillator (RxO), swing-boosting, temperature resilience, ultra-low-power, ultra-low-voltage (ULV).**

I. Introduction

FOR the crystal-less Internet-of-Things (IoT) node [1] and wake-up receiver [2], low-power and fully integrated kHz-to-MHz clock sources with moderate frequency inaccuracy are pivotal to their operations. For instance, in [2], a frequency reference with ∼2.5% frequency accuracy is required to calibrate the digitally controlled oscillator of the wake-up receiver. Although the crystal oscillator offers better frequency stability, a typical MHz-range crystal oscillator can consume tens of μW, which is impermissible for the always-on module of an IoT node. In fact, a μW-range power budget is expected in the standby mode [3]. Also, the presence of an OFF-chip crystal can restrict the volume miniaturization of the IoT nodes.

Among the fully integrated oscillators, the ring oscillator is a viable solution due to its outstanding power efficiency, tuning range, and compactness [4]. Yet, the oscillating frequency of the ring oscillator is prone to PVT variations that require extra circuitry for compensation. For the *LC* oscillator, it has a proper balance between the integration level and frequency stability [5], [6]. Yet, the *LC* tank is too bulky for the MHz-range applications.

The recent relaxation oscillators (RxOs) [7]–[15] proved their potentials by attaining a fast settling time, moderate intrinsic frequency stability, tiny footprints, and high energy efficiency. A typical RxO consists of a period-defining network, amplifiers, and logic gates. The period-defining network periodically (dis)charges the capacitors therein, and the amplifiers compare the voltages on the capacitors with a reference voltage. The logic gates read the output from the amplifiers and generate the required output correspondingly.

For IoT nodes powered by sub-0.5-V energy-harvesting sources, such as the thermoelectric generator and solar cell [16], ultra-low-voltage (ULV) operation adds to the RxO design constraints. Existing RxO architectures [7]–[12] do not favor sub-0.5-V operation. At sub-0.5 V, the voltage headroom is severely confined. Hence, the linearity and accuracy of the current and voltage references are inferior and their degraded precisions can affect the RxO's stability. Also, at high temperature, the transistor's leakage current (I_{Leak}) limits the performance of the current/voltage reference.

Recently, a swing-boosted differential RxO was proposed [13]. It features a symmetric swing-boosted *RC* network to define the period of the RxO, enabling no current or voltage reference while delivering a swing-boosted output to improve the noise performance. As this architecture does not entail current or voltage reference, it allows scaling down of the

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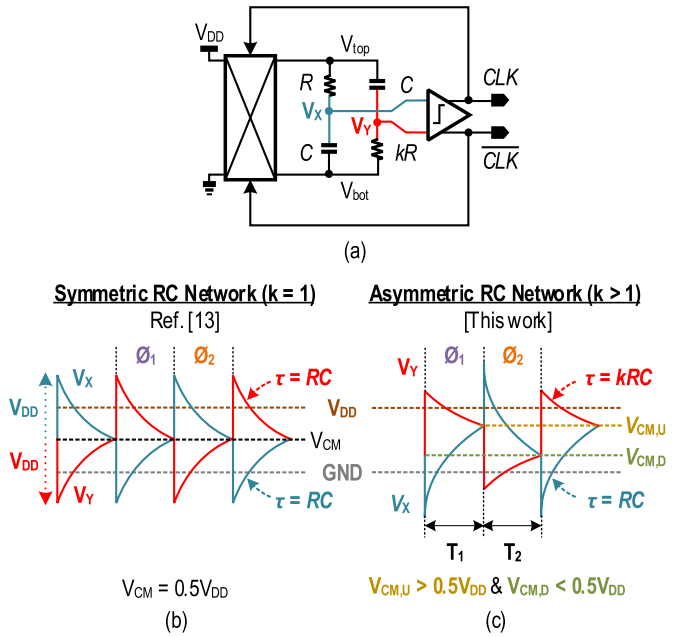

Fig. 1. (a) Simplified schematic of the swing-boosted differential RxO. (b) Timing diagram of the output of the *RC* network with $k = 1$, where V_{CM} is fixed at 0.5 V_{DD}. (c) Timing diagram of the output of the *RC* network with $k > 1$, such that $V_{CM,U}$ and $V_{CM,D}$ suit the design of the subsequent ULV comparator (this work).

V_{DD} without affecting the *RC* network precision. Nevertheless, it has the common-mode voltage (V_{CM}) of the *RC* network restricted to mid-V_{DD}, which implies $V_{CM} < 0.25$ V for sub-0.5-V operation, thereby hindering the operation of its subsequent comparator.

This article proposes an RxO that surmounts the challenges of sub-0.5-V operation and achieves high area and energy efficiencies. The key techniques are: 1) an asymmetric *RC* network to free the V_{CM} restriction while preserving a swing-boosted output and 2) a dual-path comparator with delay compensation to allow temperature resilience. Prototyped in 28-nm CMOS, the RxO occupies a tiny area (5,200 μm^2) and achieves superior energy efficiency (667 fJ/cycle) and figure-of-merit ($FoM_1 = 181$ dB), with respect to prior art.

After the introduction, Section II provides a mathematical treatment of the asymmetric swing-boosted *RC* network. Section III presents the circuit implementation of the ULV RxO. Section IV demonstrates the measurement results of the fabricated chips and compares it with the state-of-the-art RxOs. Finally, section V concludes this article.

II. Asymmetric Swing-Boosted RC Network

The schematic of the swing-boosted *RC* network is shown in Fig. 1(a). As demonstrated in [13], the RxO utilizing this *RC* network exhibits a low jitter (σ_{jit}) attributed to its swing-boosted output voltages ($V_{x,y}$) from the symmetric *RC* network ($k = 1$).

Consider $\emptyset_1$ [Fig. 1(b)] where V_x is initially at the ground and V_{top} connects to V_{DD}, whereas V_y is initially at V_{DD} and V_{bot} connects to the ground. V_x charges to V_{DD} and V_y charges to the ground with time constant (τ) *RC*. When they cross at V_{CM}, such that $V_y < V_x$, the comparator inverts its outputs. Hence, the chopper alternates the connections, where V_{top} now connects to the ground and V_{bot} connects to V_{DD}. As the charges across the capacitors conserve, V_x and V_y change to $V_{CM} + V_{DD}$ and $V_{CM} - V_{DD}$ after the transition. The process in $\emptyset_2$ is complementary, and the operation repeats $\emptyset_1$ after another transition. Hence, the differential signal $V_{x,y}$ has a swing of $2 \times V_{DD}$. Since the σ_{jit} of the RxO is inversely proportional to the slope of $V_{x,y}$ at the threshold (S_{xy}), raising the swing of $V_{x,y}$ increases S_{xy} and improves the σ_{jit}.

Due to the *RC* network symmetry, V_{CM} is restricted to mid-V_{DD}, regardless of the oscillation phases ($\emptyset_{1,2}$). As V_{DD} decreases to <0.5 V, the V_{CM} shrinks to <0.25 V, which is insufficient to properly bias a differential pair with a tail current source. To break this limit, we propose an asymmetric *RC* network ($k > 1$), in which one *RC* branch has a larger τ. As shown in Fig. 1(c), this act facilitates $V_{x,y}$ to (dis)charge at different τ. The leaps on V_x and V_y after the chopping are still $\pm V_{DD}$, whereas the V_{CM} of V_x and V_y alternate between $V_{CM,U}$ and $V_{CM,D}$ in $\emptyset_1$ and $\emptyset_2$, respectively. As such, we can design k that allows proper $V_{CM,U}$ ($V_{CM,D}$), thereby favoring the operation of the subsequent ULV comparator.

Analyzing the waveform in Fig. 1(c), we can derive four equations governing the (dis)charge of the asymmetric *RC* network

$$\left(V_{CM,D} + V_{DD}\right)e^{-\frac{T_1}{kRC}} = V_{CM,U} \tag{1}$$

$$\left(V_{CM,D} - 2V_{DD}\right)e^{-\frac{T_1}{RC}} + V_{DD} = V_{CM,U} \tag{2}$$

$$\left(V_{CM,U} + V_{DD}\right)e^{-\frac{T_2}{RC}} = V_{CM,D} \tag{3}$$

$$\left(V_{CM,U} - 2V_{DD}\right)e^{-\frac{T_2}{kRC}} + V_{DD} = V_{CM,D}. \tag{4}$$

Assume that $T_1 = T_2$, solving (1)–(4) leads to

$$\left(\frac{V_{DD} - V_{CM,D}}{V_{DD} + V_{CM,D}}\right)^k = \frac{V_{CM,D}}{2V_{DD} - V_{CM,D}} \tag{5}$$

$$\left(\frac{V_{CM,U}}{2V_{DD} - V_{CM,U}}\right)^k = \frac{V_{DD} - V_{CM,U}}{V_{DD} + V_{CM,U}} \tag{6}$$

$$k = \frac{T}{2RC} / \ln\left(\frac{1 + 3e^{-T/2RC}}{1 - e^{-T/2RC}}\right) \tag{7}$$

where $T_1 = T_2 = T/2$. Hence, we can calculate the required k to achieve a sufficient separation of $V_{CM,U}$ ($V_{CM,D}$) by numerically solving (5) and (6), as well as the corresponding T by (7). The $V_{CM,U}$, $V_{CM,D}$, and T versus k are shown in Fig. 2(a).

The S_{xy} around the threshold crossing determines the σ_{jit} by the following equation [17]:

$$\sigma_{jit} = \alpha \frac{V_{n,xy}}{S_{xy}} \tag{8}$$

where α is a constant of proportionality and $V_{n,xy}$ is the equivalent noise from the *RC* network and the subsequent comparator appeared at the output of the *RC* network. The S_{xy} can be found by solving for the difference between the derivative of V_x and V_y when $t = T/2$ (the time when crossing occurs)

$$S_{xy} = \frac{dV_{x,y}}{dt}\left(t = \frac{T}{2}\right). \tag{9}$$

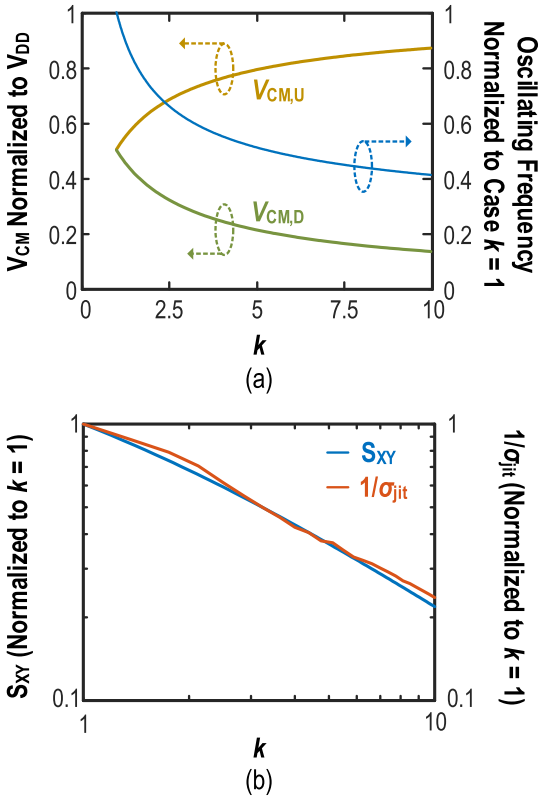

Fig. 2. (a) Simulated $V_{CM,U}$, $V_{CM,D}$, and the oscillating frequency versus k. Choosing a $k > 1$ enables a lower (higher) $V_{CM,D}$ ($V_{CM,U}$), facilitating the ULV operation. (b) S_{xy} from mathematical modeling and simulated $1/\sigma_{jit}$ from an ideal RxO with asymmetric RC network versus k. Overdesigning k decreases the S_{xy} and thus aggravates σ_{jit}.

For instance, in $\emptyset_2$, V_x and V_y are expressed as

$$V_x(t) = \left(V_{CM,U} + V_{DD}\right)e^{-\frac{t}{RC}} \tag{10}$$

$$V_y(t) = \left(V_{CM,U} - 2V_{DD}\right)e^{-\frac{t}{kRC}} + V_{DD} \tag{11}$$

where we set $t = 0$ as the beginning of $\emptyset_2$. Taking the derivative of V_x with respect to t and substituting $t = T/2$, we get

$$\frac{dV_x}{dt}\left(t = \frac{T}{2}\right) = -\frac{1}{RC}\left(V_{CM,U} + V_{DD}\right)e^{-\frac{T}{2RC}}. \tag{12}$$

Substituting (3) into (12)

$$\frac{dV_x}{dt}\left(t = \frac{T}{2}\right) = -\frac{1}{RC}V_{CM,D}. \tag{13}$$

Similarly, we can obtain the slope of V_Y at $t = T/2$

$$\frac{dV_y}{dt}\left(t = \frac{T}{2}\right) = -\frac{1}{kRC}\left(V_{CM,D} - V_{DD}\right). \tag{14}$$

Hence, S_{xy} in $\emptyset_2$ is

$$S_{xy} = -\frac{1}{RC}\left(V_{CM,D} - \frac{V_{CM,D}}{k} + \frac{V_{DD}}{k}\right) \tag{15}$$

where the relationship between $V_{CM,D}$ and k can be found from (5). Note that when $k = 1$ (symmetric RC network as in [13]), $S_{xy} = -V_{DD}/RC$, showing that a higher V_{DD} improves S_{xy} and thus σ_{jit}. Fig. 2(b) shows the S_{xy} as a function of k. Under the identical RC and V_{DD}, increasing k results in a decreasing S_{xy}. Similarly, S_{xy} in $\emptyset_1$ can be found, provided that $T_1 = T_2$, S_{xy} in $\emptyset_1$ should be equivalent (in negative) to S_{xy} in $\emptyset_2$.

Based on Fig. 2(a) and (b), we can have the following takeaway: a large k allows $V_{CM,U}$ ($V_{CM,D}$) to approach V_{DD} (ground), easing the use of an NMOS (PMOS) input amplifier for comparisons. Yet, upsizing k penalizes σ_{jit} since $\sigma_{jit} \propto 1/S_{xy}$. In addition, pushing $V_{CM,U}$ ($V_{CM,D}$) close to V_{DD} (ground) saturates the input pairs of the subsequent amplifiers. Thus, there is a trade-off between the minimum V_{DD} and σ_{jit} for the RxO utilizing the asymmetric RC network. The minimum gate voltage at the NMOS input amplifier is ~0.2 V (i.e., 0.1 V for the tail current source + 0.1 V for the gate–source voltages of the differential pair), and the minimum V_{DD} of the comparator is ~0.35 V (explained in Section III-A). To yield a minimum $V_{CM,U}$ of 0.2 V to drive the NMOS input amplifier with 15% margin, we choose $k = 2.4$, such that $V_{CM,U}$ is 0.23 V ($0.66 \times V_{DD}$). During the fabrication, a mismatch between the resistors diverts $V_{CM,U}$ ($V_{CM,D}$) from their desired values. Nevertheless, since k is the ratio between the resistors, its variation can be minimized by the delicate layout and the common centroid technique. Hence, this 15% margin is adequate to safeguard the operation of the RxO. Correspondingly, $V_{CM,D}$ positions at $0.33 \times V_{DD}$ to favor the PMOS input amplifier.

With $k = 2.4$ in Fig. 2(b), S_{xy} is reduced by 39%. To verify the degradation of σ_{jit}, we built an ideal RxO utilizing the asymmetric RC network with a noise source and simulated the σ_{jit} with different values of k. The simulated $1/\sigma_{jit}$ of such RxO is shown in Fig. 2(b). The $1/\sigma_{jit}$ decreases (hence σ_{jit} increases) at a similar rate of k with S_{xy}. The $1/\sigma_{jit}$ at $k = 2.4$ decreases by 36%, thus verifying our analysis here.

III. Circuit Implementation

A. ULV Comparator With Dual-Path Amplifiers

In [13], the RxO utilizes an inverter-based amplifier for voltage comparison. Although this amplifier has excellent noise performance, it is not suitable for ULV operation as it requires a minimum voltage headroom of $2(V_{GS} + V_{DS})$. We have proposed the asymmetric RC network in Section II for ULV operations, where $V_{CM,U}$ ($V_{CM,D}$) can be adjusted according to k. To cope with different V_{CM} at two phases of oscillations under a ULV headroom, we utilized a comparator with dual-path amplifiers to handle the voltage comparisons across $V_{x,y}$. The comparator consists of an NMOS input amplifier, a PMOS input amplifier, and logic gates to generate the CLK signal. The NMOS input amplifier, enabled in $\emptyset_1$, is capable of handling a higher input V_{CM}, where V_x and V_y cross at $V_{CM,U}$, with the PMOS input amplifier disabled. The complementary operation happens in $\emptyset_2$. As such, the amplifiers can compare V_x and V_y under the ULV headroom. Compared with the case using $k = 1$ and only a PMOS input amplifier, the variation of the RxO's oscillating period (T_{OSC}) reduces by ~40%.

Fig. 3(a) and (b) shows the proposed ULV RxO. Each amplifier is built by cascading three gain stages, each formed by a fully differential common-source (CS) amplifier [Fig. 4(a)],

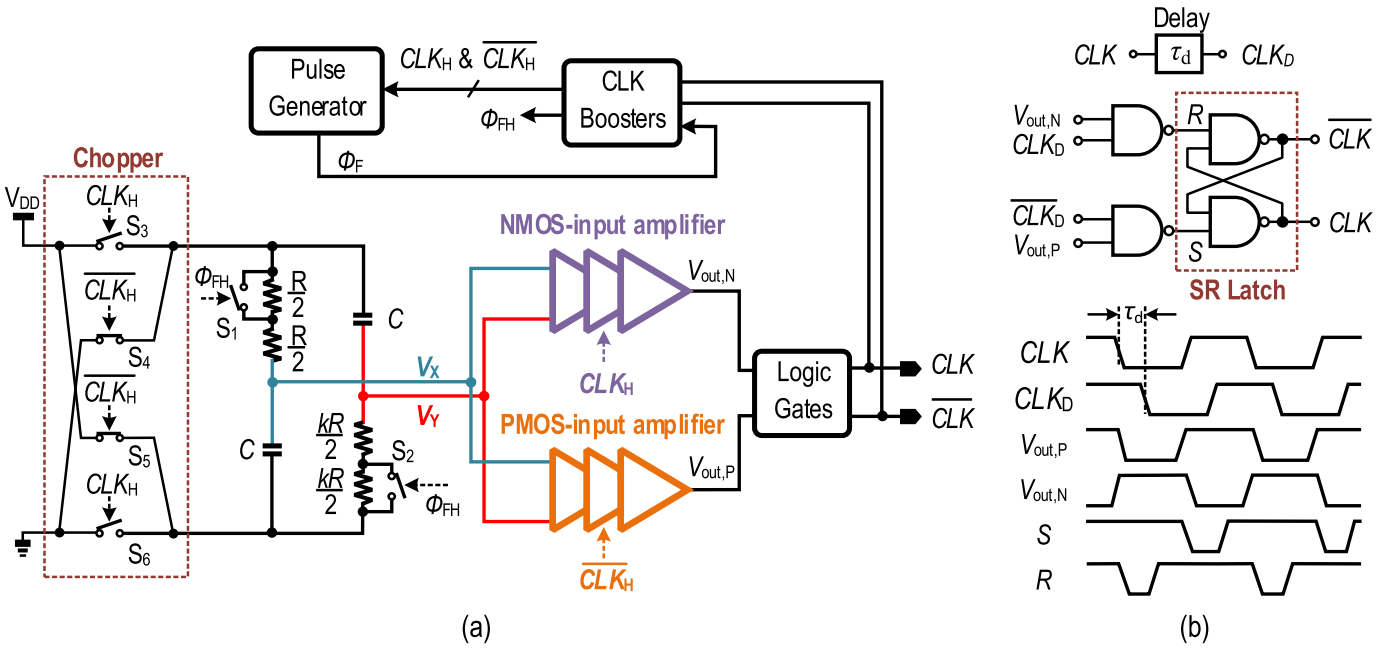

Fig. 3. (a) Proposed ULV swing-boosted RxO featuring an asymmetric *RC* network and a dual-path comparator. The delays of the amplifiers are tracked to tackle the frequency fluctuation against temperature and voltage variations. (b) Schematic of the logic gates. The SR latch, together with the delay unit, guarantees that the RxO only generates desired oscillating signal without glitch.

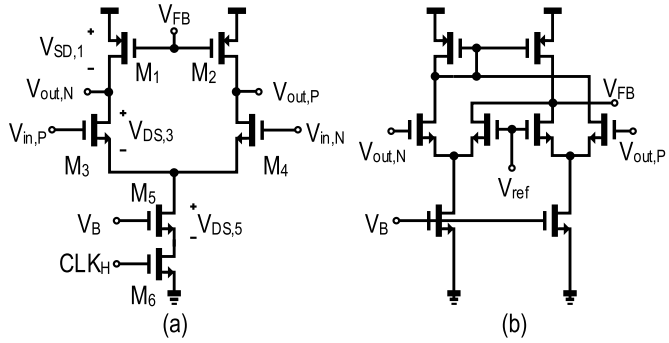

Fig. 4. (a) Schematic of the differential CS amplifier (NMOS). (b) CMFB circuit for the NMOS CS amplifier.

to boost the overall voltage gain. The simulated gains of the cascaded amplifiers are >27 dB from the simulation. Following the amplifiers, the logic gates generate the CLK signals and operate the chopper of the *RC* network after boosting to CLK_H (as explained in Section III-C).

As the $V_{\text{CM},U}$ ($V_{\text{CM},D}$) of *RC* network can be adjusted between V_{DD} and ground by choosing an appropriate k, the minimum V_{DD} of the RxO is mainly limited by two factors: the dual-path amplifier and the logic gates. Assuming that the transistors are all biased in the sub-threshold region and the gate voltages are bounded between V_{DD} and ground, the minimum V_{DD} of the differential CS amplifier is $V_{\text{SD},1} + V_{\text{DS},3} + V_{\text{DS},5}$ [as shown in Fig. 4(a)] if we assume the V_{DS}-drop on M_6, the transistor for power-gating, is negligible. To maintain operations in the sub-threshold region, the $|V_{\text{DS}}|$ of a transistor should be $> 3 \times V_T$, where V_T is the thermal voltage. The V_T reaches 34 mV at 120 °C. Hence, the minimum V_{DD} of the differential CS amplifier is 306 mV in theory. We leave a ~10% margin for the design and choose the V_{DD} of 0.35 V. On the other hand, the requisite V_{DD} for the logic gates to operate under the desired oscillating frequency also limits the minimum V_{DD}. In the selected CMOS 28-nm process, the delay of the logic gates with V_{DD} of 0.35 V varies <1% of T_{OSC} from −20 to 120 °C, evincing the V_{DD} of 0.35 V is sufficient to power the logic gates.

The comparator's delay (t_{delay}) affects the T_{OSC} stability. As described later, a delay generator compensates t_{delay} at different operating conditions. Here, we target a maximum $\Delta t_{\text{delay}} \sim 25\%$ of T_{OSC} across −20 °C to 120 °C such that the resultant T_{osc} variation after compensation is <2.5%, reserving a 10% mismatch margin between t_{delay} and the delay generator. The simulated t_{delay} (N + P channel) ranges from 17 ns at 120 °C, to 146 ns at −20 °C under a power consumption of 500 nW (at 27 °C), with a variation of ~10% above the target.

The gate voltages of M_3 and M_4 determine the operating region of M_5 [Fig. 4(a)]. To guarantee that M_5 operates in the sub-threshold region, $V_{\text{DS},5}$ needs to be higher than $3 \times V_T$. We can either increase $V_{\text{in},P}$ ($V_{\text{in},N}$), which is the *RC* network output for the first amplifier, by upsizing k, or decrease the V_{GS} of M_3 and M_4. As explained in Section II, upsizing k deteriorates the σ_{jit}. On the other hand, under the same bias current and channel length, decreasing V_{GS} incurs a wider $M_3(M_4)$. Thus, the t_{delay} and the RxO's frequency stability are exacerbated. From the simulation, the amplifier's delay raises by 26% with the V_{GS} of $M_3(M_4)$ reduced by 10 mV [with the width of $M_3(M_4)$ enlarged]. We aim for a V_{GS} of 0.1 V for $M_3(M_4)$ to achieve a proper trade-off between the t_{delay} and σ_{jit}.

Since each amplifier is only responsible for comparing V_x and V_y in one phase, they can be power-gated based on the CLK state to reduce the power consumption. For instance, in $\emptyset_1$, where CLK is high and the common-mode voltage of V_x and V_y is at $V_{\text{CM},U}$, the NMOS input amplifier is enabled

for comparison, while the PMOS input amplifier is powered down. The operation reverses in $\emptyset_2$. This duty-cycling scheme saves 26% of the total RxO power budget.

To ensure that M_1 and M_2 operate in the sub-threshold region, their gate voltages are generated by a common-mode feedback (CMFB) circuit [Fig. 4(b)]. The CMFB circuit compares the common-mode output voltage of the amplifier to V_{ref} and corrects V_{FB}. The transistors' sizes of the CMFB circuit are scaled from the main amplifier, such that the PVT variations have the same effect on the amplifier and CMFB circuit to enhance its robustness.

A SR latch is utilized to read the results from the amplifiers and yield the desired state of CLK. Also, a delayed CLK ($\overline{\text{CLK}}$) signal CLK_D ($\overline{\text{CLK}_D}$) is used to mask out the glitches to avert undesired transition of CLK due to glitches from the amplifiers during the switching. For instance, as shown in Fig. 3(b), before the end of $\emptyset_1$ (CLK and CLK_D are high), both S and R of the SR latch are high and maintain the state of CLK. Therein, the NMOS input amplifier is enabled, whereas the PMOS input amplifier is disabled. Once $V_x > V_y$, R becomes low and S is still high (since $\overline{\text{CLK}_D}$ is low), which forces CLK to a low. Then, the PMOS input amplifier is enabled, while the NMOS input amplifier is disabled. During the switching of the amplifiers, there may be undesired transition on $V_{\text{out},N}/V_{\text{out},P}$. The CLK_D signal and the NAND gates guarantee that these undesired glitches do not affect the state of CLK. After a delay of τ_d, CLK_D goes low. Both S and R are high again, and the SR latch maintains the state of CLK until $V_{\text{out},P}$ goes high ($V_X < V_Y$). The operation repeats after another transition of CLK. The delay unit is implemented by simple RC circuit and inverters with τ_d of $\sim$80 ns. The τ_d is selected such that it gives a sufficient margin before the zero-crossing point of $V_{x,y}$ and does not affect the comparison, yet it is long enough to filter out the glitches from the amplifiers during the switching amid PVT variation.

A constant g_m bias circuit aids the amplifiers to withstand voltage and temperature variations [18]. The bias circuit is powered by a switched-capacitor voltage doubler [Fig. 5(a)], which extends the voltage headroom ($2 \times V_{DD} \approx 0.7$ V). As the CLK signal from the RxO itself can be reused to operate the voltage doubler, the power (11%) overhead is low. During the startup, there is no CLK signal yet to drive the voltage doubler and hence there would be no output from the bias circuit if no auxiliary signal is provided. Thus, a startup pulse (duration $\sim$1 μs, generated ON-chip after V_{DD} rises) enables an auxiliary ring oscillator (RO) to operate the voltage doubler in this startup phase [Fig. 5(b) and (c)]. The V_{2X} is boosted up to $\sim 2 \times V_{\text{DD}}$ and the bias circuit functions properly within this period. Then, the startup pulse and the auxiliary RO are disabled and the RxO starts to operate. As such, the RO does not pose interference to the RxO nor affects the accuracy of the RxO's frequency. The RO's frequency ranges from 15.2 to 35.1 MHz across -20 °C–120 °C.

B. Delay Generators

The temperature dependence of t_{delay} affects RxO's T_{OSC}. Ideally, T_{OSC} is only dependent on the RC network. However, the t_{delay} after the zero-crossings of $V_{x,y}$ prolongs the duration

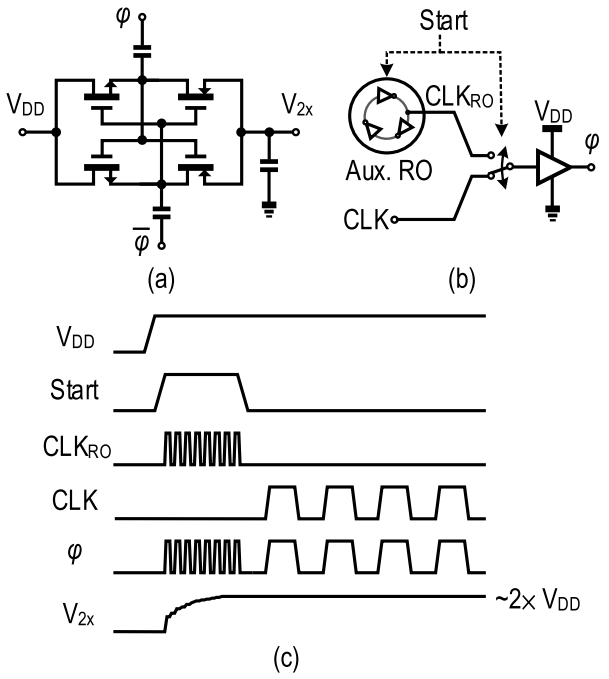

Fig. 5. (a) Schematic of the switched-capacitor voltage doubler. (b) Auxiliary RO that drives the voltage doubler during the startup. (c) Timing diagram of the auxiliary RO and the voltage doubler.

of each phase. As t_{delay} is temperature-dependent, it deteriorates the RxO's frequency stability. Raising the amplifiers' power budget can diminish the ratio $t_{\text{delay}}/T_{\text{OSC}}$, but it penalizes the RxO energy efficiency. In [10], a period controller compensates t_{delay} by doubling the current injected into the period-defining capacitors, in which the current injection duration tracks t_{delay}. As such, it can correct T_{OSC} to minimize its temperature sensitivity. Yet, the period controller entails an extra comparator for copying t_{delay}, penalizing the power budget.

Since the delay of an amplifier relates to its bias current, we introduced a delay generator to create a pulse, with its width inversely proportional to the bias current. As shown in Fig. 6(a), two delay generators (for NMOS and PMOS input amplifiers) with scaled currents from the main amplifiers generate the pulses after the edges of CLK_H. From the simulation, the width of the pulses $\emptyset_F$ closely tracks t_{delay} (error <7.6% of t_{delay}, or <2.3% of T_{OSC}). To compensate t_{delay}, we halve the τ of the RC branches when $\emptyset_{\text{FH}} = 1$ by closing switches S_1 and S_2 in Fig. 3(a). The open-loop compensation scheme alleviates the long settling time of the oscillator. Furthermore, this compensation method can even off the temperature dependence of the resistors in the RC network, avoiding area-hungry composite resistors to obtain a zero-temperature coefficient (TC) [10], [14].

The delay-controlling capacitors C_N and C_P are implemented as 4-bit capacitor banks. Their values can be programed to balance the process variation once after the fabrication. The tuning ranges of the capacitances are designed such that they can cover the variations of t_{delay} amid process variations. The t_{delay} of NMOS input and PMOS input amplifiers vary from 15 to 45 ns and 36 to 60 ns, respectively, from the Monte Carlo simulation (100 runs, at 27 °C).

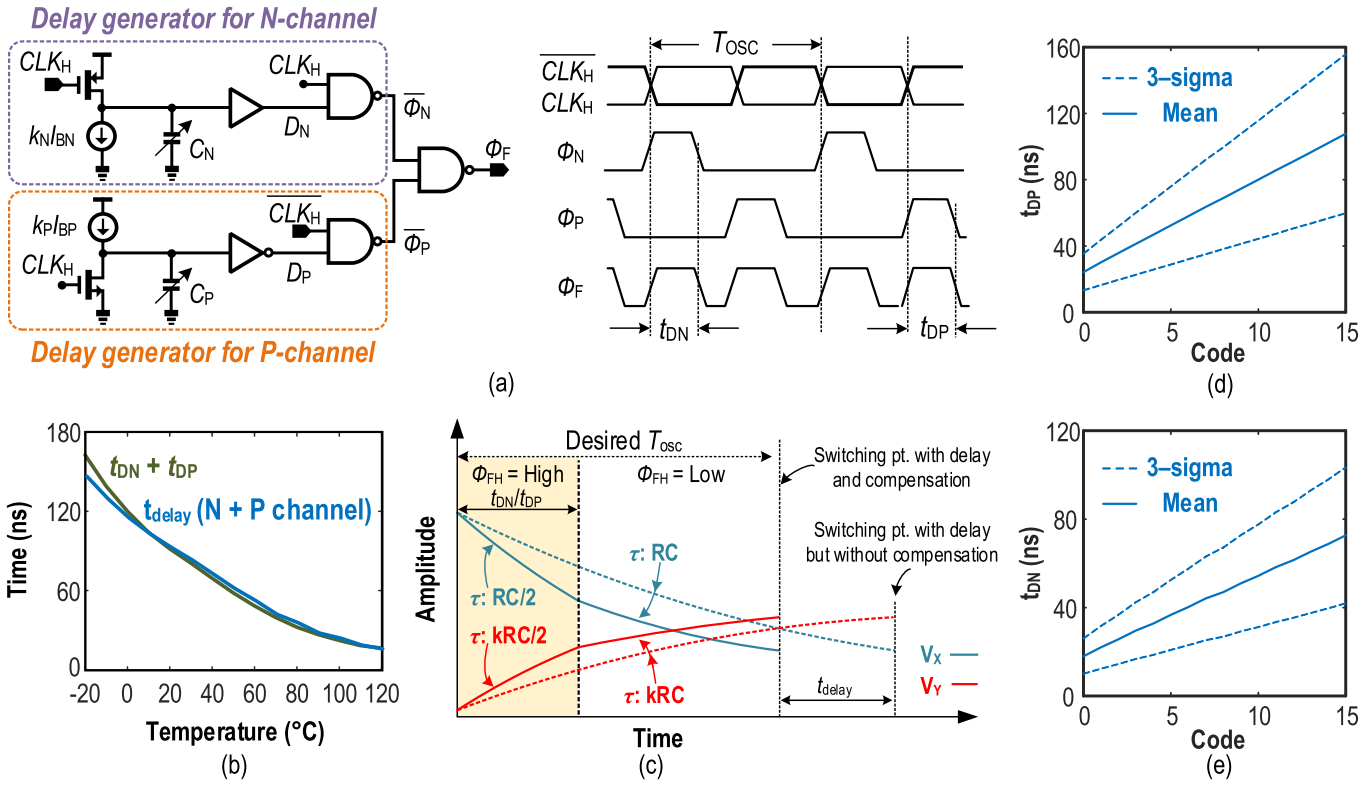

Fig. 6. (a) Proposed delay generator to track the t_{delay} at different operating conditions and its timing diagram. (b) Matching between t_{delay} and $t_{DN} + t_{DP}$ against temperature variation (under nominal case). (c) Principle of the delay compensation: when $\emptyset_{FH}$ is high, τ of the RC branches halved thus $V_{x,y}$ (dis)charge at a double rate to compensate t_{delay}. (d) and (e) The Monte Carlo-simulated t_{DP} and t_{DN} (100 runs) at 27 °C with different input codes for the capacitor bank.

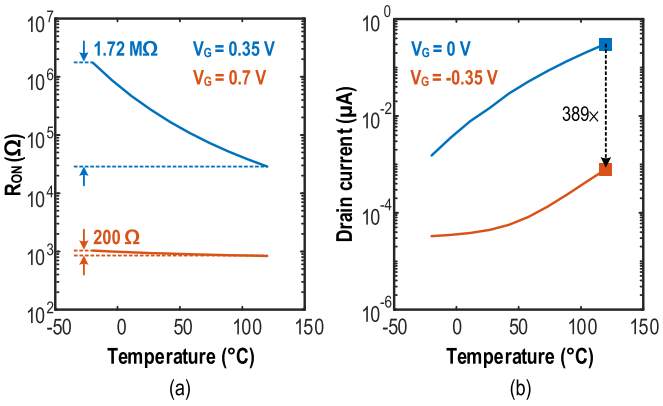

Fig. 7. (a) R_{ON} of an NMOS from −20 to 120 °C with different V_G. For both cases, $V_D = V_S = 0.175$ V. The increased swing on V_G reduces the variations of R_{ON} by 8600×. (b) I_{Leak} of the same NMOS in (a) in the OFF-state. With a negative V_G, the I_{Leak} is reduced by 389× at 120 °C. For both cases, $V_D = 0.35$ V and $V_S = 0$ V.

Hence, we design the delay generator and the capacitor banks capable of generating pulses of width in this range by adjusting their codes correspondingly [Fig. 6(d) and (e)]. With the proposed compensation scheme, the simulated variation of T_{OSC} decreases from 25% to 2.1% over −20 °C–120 °C. For the constant g_m biasing, the current decreases with temperature. Hence, both I_{BN} and I_{BP}, the biasing currents of the NMOS input and PMOS input amplifiers, are minimum at −20 °C. Consequently, the t_{DN} and t_{DP} are largest at −20 °C and decrease to their minimum toward 120 °C.

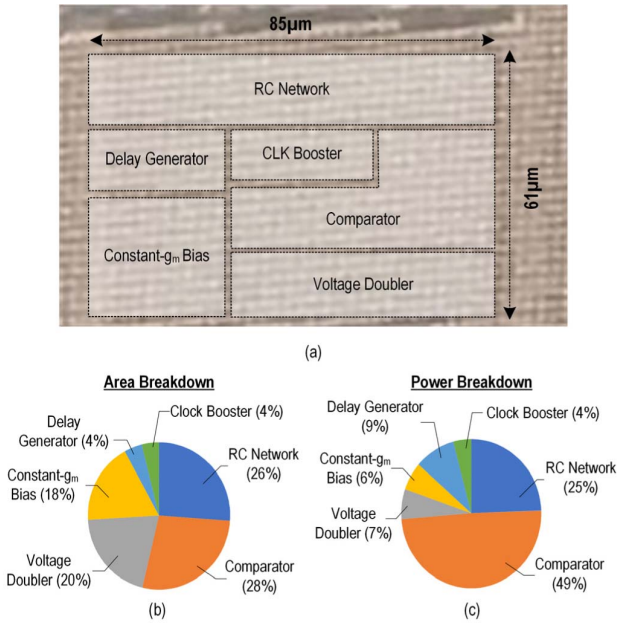

Fig. 8. (a) Chip micrograph of the fabricated RxO in 28-nm CMOS. (b) Area breakdown of the RxO. (c) Power breakdown (from simulation) of the RxO.

Therefore, the overall resolutions of t_{DN} and t_{DP} are confined at low temperature (7 ns and 13 ns). Still, these resolutions are sufficient to uphold the 2.5% frequency error requirement. The number of bits of the capacitor banks can be increased for the case where a finer resolution is desired.

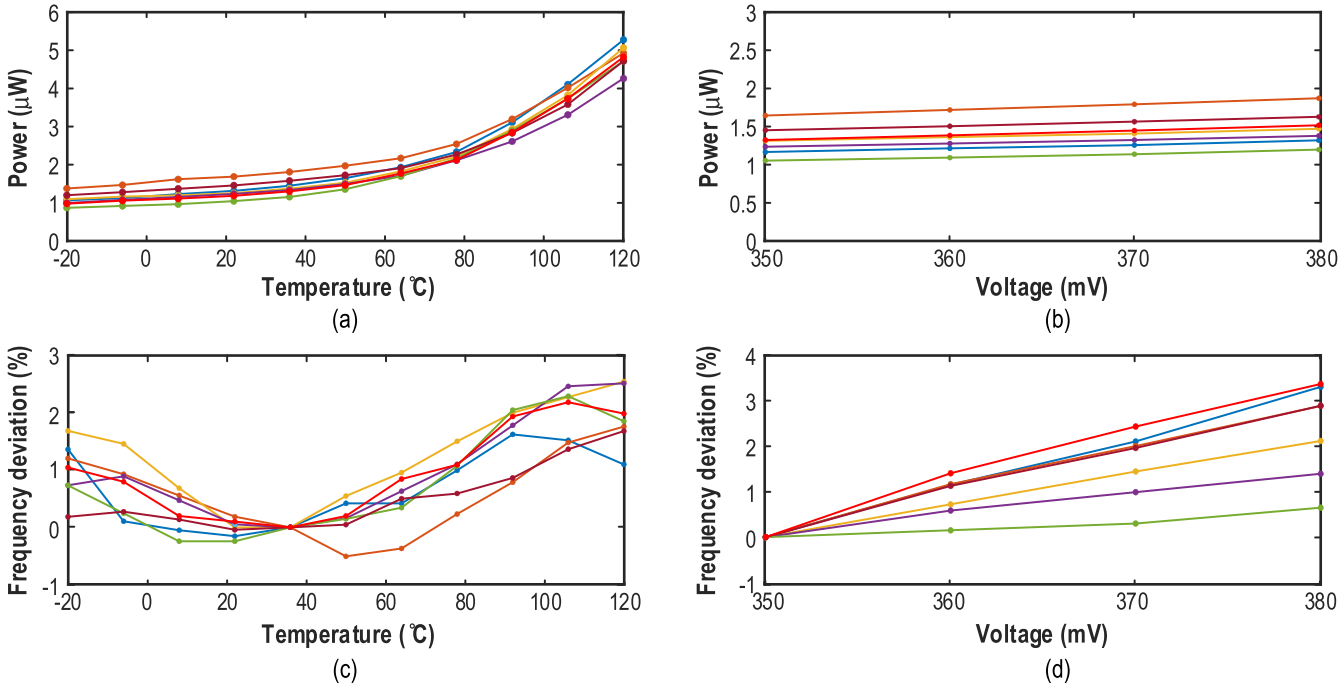

Fig. 9. Measured performance of the RxO from seven chip samples. (a) Power consumption versus temperature. (b) Power consumption versus V_{DD}. (c) Frequency stability versus temperature. (d) Frequency stability versus V_{DD}.

C. CLK Boosters

The non-idealities of the switches influence the performance of the RxO. For example, the non-zero ON-resistances (R_{ON}) of the transistors that constitute switches S_{1-6} [in Fig. 3(a)] affect the τ of the *RC* network. Under sub-0.5V, the transistors work in the sub-threshold region. Hence, the situation is pronounced as R_{ON} increases exponentially with $-(V_{GS} - V_{TH})$, where the worst case of $|V_{GS}|$ is $0.5 \times V_{DD}$ without any boosting technique. Furthermore, as R_{ON} is prone to temperature variations (R_{ON} increases with a decreasing temperature), the frequency stability of the RxO is inevitably affected. To alleviate their impact, R_{ON} should be minimized compared with R in the *RC* network. The R_{ON} could be reduced by upscaling the widths of the transistors that compose the switches. Yet, this act leads to another problem: in the deep submicrometer CMOS process, the I_{Leak} in the OFF-state, especially at a high temperature, restricts the RxO's performance and operation range. Considering the switches S_{1-2} in Fig. 3(a) again, at a high temperature, the transistors with a high I_{Leak} equivalently reduce τ. Altogether, there is a trade-off between their R_{ON} at a low temperature and I_{Leak} at a high temperature.

To tackle this challenge, we employed clock boosters [19] to triple the swing of the digital signals (CLK_H, $\overline{CLK_H}$, and $\emptyset_{FH}$). The clock booster, powered from V_{DD}, increases the swing of the periodic signal (high: $2\times V_{DD}$, low:$-V_{DD}$) without additional power supply. With a boosted swing, the worst $|V_{GS}|$ for the transistors now becomes $1.5 \times V_{DD}$. Besides, being benefitted by the negative voltage ($-V_{DD}$) at the logic low level, it effectively suppresses I_{Leak}, even at 120 °C. For example, this scheme not only tightens the variations of the R_{ON} of an NMOS switch across −20 °C–120 °C by 8600× [$V_D = V_S = 0.5 \times V_{DD}$, Fig. 7(a)], but also shrinks I_{Leak} in the OFF-state at 120 °C from 307 to 0.8 nA [Fig. 7(b)], rendering the RxO robust in the extreme environment.

IV. Measurement Results

We prototyped the RxO in 28-nm CMOS 1P10M technology. It occupies a core area of 5,200 μm^2, dominated by the comparator (28%) and *RC* network (26%) [Fig. 8(a) and (b)]. The RxO consumes 1.4 μW at 22 °C on average ($N = 7$) [Fig. 9(a) and (b)], which is dominated by the comparator (49%, from the simulation) [Fig. 8(c)]. After fabrication, we applied a three-point trim to the capacitor banks of the delay generator based on the measured frequency of the RxO.

Peripheral equipment such as the oscilloscope (for observing the waveform in real time) and the frequency counter (for measuring the frequency f) have high input capacitances. The digital buffers with a V_{DD} of 0.35 V and reasonable sizing are not capable of driving these equipment. Hence, we utilize ON-chip level shifters to raise the output signals to swings of 0.9 V. The signals are then fed to digital buffers with a V_{DD} of 0.9 V (supplied independent of the RxO's V_{DD}) to drive the peripheral equipment.

The mean oscillating frequency of the RxO is 2.1 MHz. It has an energy efficiency of 667 fJ/cycle, rendering it the most energy-efficient RxO reported in the MHz range. After calibrations, the deviations of the RxOs' frequencies were <2.5% from −20 °C to 120 °C [Fig. 9(c)]. The resulting TC is 158 ppm/°C on average. The mean variation of the RxO's frequencies from 0.35 to 0.38 V (∼9% of V_{DD}) is 2.5% [Fig. 9(d)]. The line sensitivity, where we also take the supply voltage into account, $[(\Delta f/f)/(\Delta V/V)]$, is 26.8%. The large sensitivity of the RxO to voltage variation is attributable to the sub-threshold operation and low V_{DS} across the transistors of the amplifiers. From the simulation, the bias current of the NMOS input amplifier increases by 25% from 0.35 to

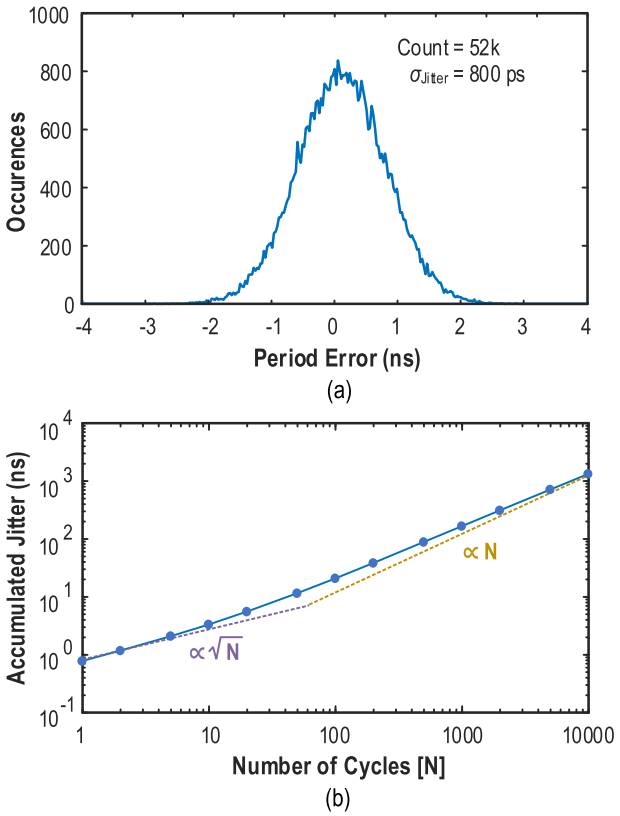

Fig. 10. (a) Measured period jitter of the RxO (52 000 hits on the oscilloscope). (b) Accumulated jitter of the RxO.

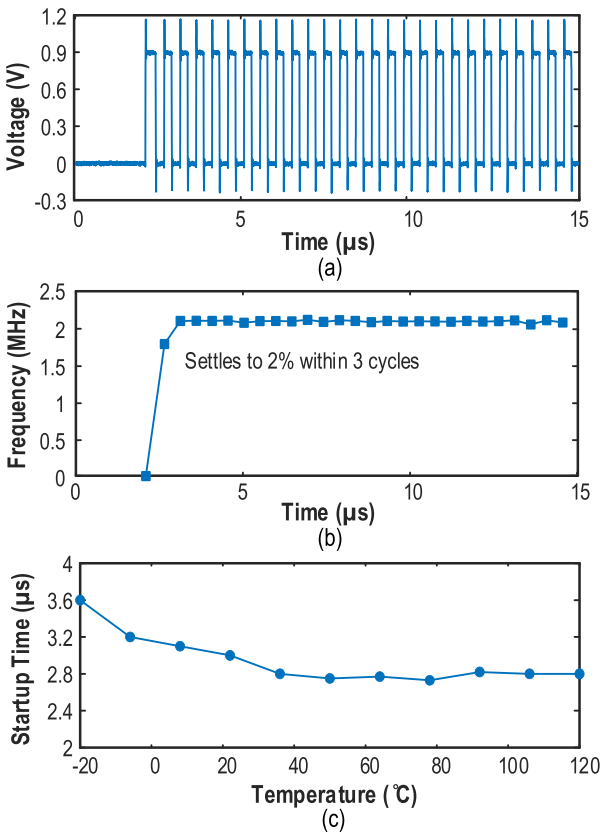

Fig. 11. (a) Startup waveform of the RxO. V_{DD} is switched on at $t = 0$ s. (b) Transient frequency during startup. The RxO reaches a steady state within three clock cycles, or 3.6 μs after enabling V_{DD}. (c) The startup time of the RxO at different temperatures.

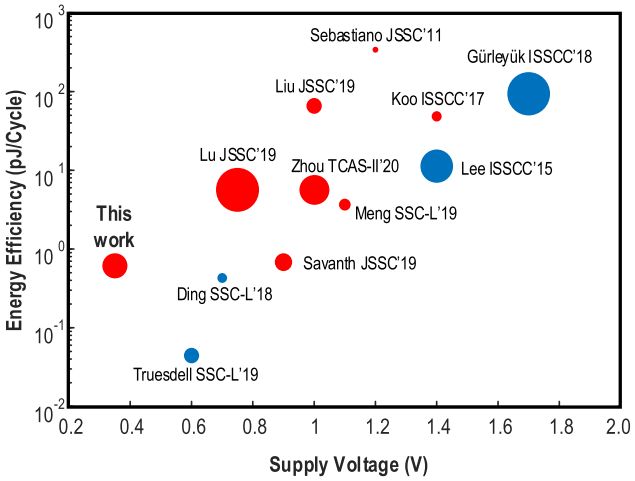

Fig. 12. Comparison with the state-of-the-art fully integrated oscillators. Red circle: RxO; blue circle: frequency-locked-loop type oscillator. A larger circle implies a relatively higher oscillating frequency. The figure only shows selected oscillators with frequencies between 0.1 and 10 MHz.

0.38 V, hence affecting the t_{delay} and the RxO's frequency. Still, the 0.35 to 0.38 V range is sufficient for IoT devices powered by solar cells and installed in the typical indoor environment (e.g., home and office), as the open-circuit voltage of a solar cell varies 30 mV amid a change in light intensity of ~3× [20], [21]. If the requirement on frequency stability is relaxed or recalibration of the frequency at different V_{DD} is feasible, the working range of the RxO can extend to 0.5 V, which is then limited by the breakdown voltage of the CMOS process (1 V) due to the voltage doubler and clock booster.

The rms period jitter of the RxO is 800 ps (0.15% of T_{OSC}) [Fig. 10(a)]. The accumulated jitter increases at a rate of $\sqrt{N}$ up to ~60 cycles, in which the thermal noise is the dominant noise source [Fig. 10(b)]. Compared with [13], the high period jitter is attributable to the low voltage supply, low power, and different amplifiers handling the comparison in $\emptyset_1$ and $\emptyset_2$. Still, the RxO is well suited for the devices in which ULV and ultra-low-power are the priorities (e.g., the wake-up receiver [2]). The long-term stability is 210 ppm (gating time >0.1 s). To characterize the supply–noise rejection of the RxO, we superposition a sinusoidal signal on V_{DD} and measure the corresponding period jitter. In the presence of a 20-mV_{pp} sinusoidal signal (1 kHz) at the supply, the period jitter of the RxO exhibits 2 ns.

We also characterize the startup time of the RxO, which is crucial if the RxO is power gating to further suppress the power consumption of the IoT node. As the asymmetric *RC* network needs finite clock cycles to produce a consistent output signal, the RxO's frequency settles after the third clock pulse [Fig. 11(a) and (b)]. Over the entire temperature range, the RxO enters into the steady state within 3.6 μs after enabling V_{DD} [Fig. 11(c)].

Herein we benchmark the RxO using two FoM. First, we evaluated the RxO using the FoM proposed in [12]:

$$\text{FoM}_1 = 10\log\left(\frac{f \cdot T_{\text{range}}}{\text{Power} \cdot \text{TC}}\right) \tag{16}$$

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART RXOS

	Koo, ISSCC'17 [11]	Mikulić, ESSCIRC'17 [8]	Liu, JSSC'19 [12]	Savanth, JSSC'19 [9]	Lee, JSSC'20 [13]	This work
Process (nm)	180	350	65	65	180	28
Frequency (MHz)	0.44	1	1.05	1.2	10.5	2.1
V_{DD} (V)	1.4 – 3.3	3 – 4.5	0.98 – 1.02	0.9 – 1.8	1.4 – 2.0	**0.35 – 0.38**
Power (µW)	21.3	210	69	0.82	219.8	1.4
Energy efficiency (pJ/cycle)	48.4	210	65.7	0.68	20.9	**0.67**
T_{range} (°C)	–20 to 100	–40 to 125	–15 to 55	–20 to 125	–40 to 125	–20 to 120
TC (ppm/°C)	169	24.3	4.3	100	137	158
Variation across V_{DD}	0.04%	0.42%	0.17%	±0.54%	2.64%	2.3%
Line sensitivity $(\frac{\Delta f}{f}/\frac{\Delta V}{V})$	0.03%	0.84%	4.25%	±0.54%	6.16%	26.8%
Area (µm^2)	58,000	40,000	51,000	5,000	15,000	**5,200**
Period jitter (ps_{rms})	1,060	-	160	-	9.86	800
Startup time (µs)	-	1[§]	8	10	-	**3.6**
No. of samples	100	5	-	7[#]	15	7
FoM_1 (dB)	162	165	174	183	168	**181**
FoM_2 (dBc/Hz)	–152.7 (@10 kHz)	-	-	-	–157.7 (@1 kHz)	–143.4 (@ 10 kHz)

[#]For temperature stability measurement.

[§]Deduced from the numbers of cycles to start, which may underestimate the true startup time.

with the temperature range (T_{range}). This FoM takes account of the trade-off among f, power, T_{range}, and TC. The FoM_1 of the proposed RxO is 181 dB, which is comparable to the state-of-the-art, in spite of the ULV V_{DD} of 0.35 V. Then, we evaluated the RxO using the conventional FoM:

$$\text{FoM}_2 = \text{PN} - 20\log\left(\frac{f}{f_{\text{offset}}}\right) + 10\log\left(\frac{\text{Power}}{1\,\text{mW}}\right) \quad (17)$$

where PN is the phase noise at the offset frequency from the carrier f_{offset}. The PN of our RxO at 10-kHz offset is -68.4 dBc/Hz, resulting in an FoM_2 of -143.4 dBc/Hz.

The performance of the RxO is summarized in Table I and compared with recent art. Our work is the first sub-0.5-V temperature-resilient (<2.5%) RxO achieving a high-power efficiency of 667 fJ/cycle (Fig. 12). Compared with the RxO with symmetric swing-boosted *RC* network [13], our RxO operates at a 4× less V_{DD}, while achieving a comparable TC after compensation.

V. CONCLUSION

We presented a 2.1-MHz temperature-resilient RxO with a 0.35-V supply voltage for ultra-low-power IoT nodes. An asymmetric swing-boosted *RC* network and a dual-path comparator are jointly proposed to tackle the challenges of ULV (<0.5 V) operation. The temperature-sensitive delay of the comparator is compensated by the open-loop delay generator. Fabricated in the 28-nm CMOS process, it has an active area of only 5,200 μm^2 and achieves the best energy efficiency (667 fJ/cycle) among the reported MHz-range RxOs in the literature. Furthermore, it also has a high figure-of-merit of 181 dB, despite the ULV headroom and can settle within 3.6 μs after enabling the supply voltage.

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