First Demonstration of Distributed Amplifier MMICs With More Than 300-GHz Bandwidth

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***Abstract*— This article reports on the first demonstration of distributed amplifier monolithic microwave integrated circuits (MMICs) with a bandwidth (BW) of more than 300 GHz. The three presented circuits utilize a uniform traveling-wave amplifier topology with six, eight, and ten unit cells, respectively. In this article, the impact of the connection between the gate line and the transistors on the achievable performance is investigated. It is demonstrated that a short connection clearly provides a more favorable combination of BW, input matching, and losses on the gate line. Thus, it is possible to extend the BW beyond 300 GHz while utilizing transistors with a gate width of 2×10 μm. The MMICs are fabricated in a 35-nm gate-length InGaAs metamorphic high-electron-mobility transistor technology. The MMIC with six unit cells exhibits a noise figure (NF) between 3.5 and 8.2 dB for a noise-optimized bias from 1 GHz up to the measurement limit of 308 GHz. The MMIC with ten unit cells achieves a minimum NF of 2 dB for frequencies of around 50 GHz and stays below 10 dB for the entire band. Furthermore, for a power-optimized bias, the same circuit generates an output power between 8.7 and 14.8 dBm for a frequency range from 1 to 250 GHz.**

***Index Terms*— Distributed amplifiers (DAs), high-electron-mobility transistors (HEMTs), low-noise amplifiers (LNAs), metamorphic HEMTs (mHEMTs), millimeter wave (mmW), monolithic microwave integrated circuits (MMICs), power amplifiers (PAs), thin-film microstrip transmission lines (TFMSLs), traveling-wave amplifiers (TWAs).**

I. Introduction

DISTRIBUTED amplifiers (DAs) are key components in a multitude of ultrawideband applications, including wireless and optical communication, measurement equipment, and high-resolution radar systems. In recent years, wideband applications have been pushing the limits to even higher operating frequencies with first commercial products exceeding a bandwidth (BW) of 200 GHz, e.g., a single-sweep vector network analyzer from 70 kHz to 220 GHz [1]. Apart from scenarios with a required relative BW of close to 200%, one should also consider DAs for banded applications with still large absolute BWs where, in contrast to reactively matched amplifiers, DAs can easily provide a valuable tradeoff between BW, gain, output power, and noise performance.

For DAs with high absolute BWs [2]–[14], two key enablers are high cutoff frequencies, especially a high maximum-oscillation frequency ($f_{\max}$) and a thin-film microstrip transmission line (TFMSL) environment. The first of which can be seen from gain approximations as given, e.g., in [15] and [16] where the transconductance and the input capacitance (as part of the input-line impedance) of an active device dominate the performance of common implementations. When entering the field of DAs with BWs of several hundreds of gigahertz, compactness is essential. Classical transmission line (TL) concepts, such as grounded coplanar waveguide or microstrip transmission line (MSL) in the wafer as a substrate, suffer from the problem of strong coupling effects when realizing compact layouts. This favors TFMSLs that enable compact layouts with good high-frequency performance.

It is the aim of this work to investigate limiting effects that might be part of common implementations of DAs with the goal to extend the absolute frequency BW into the range of beyond 300 GHz. State-of-the-art results are mostly based on heterojunction bipolar transistor (HBT) technologies and achieve BWs of up to 235 and 241 GHz [2], [3]. Table I shows an overview of previously published DA monolithic microwave integrated circuits (MMICs) with a BW of more than 150 GHz. The demonstrated output power (P_{out}) is in most cases below 10 dBm except for [8], [9], which achieves values of up to 11.4 and 17.8 dBm. This comes, however, at the price of a limited BW of less than 200 GHz. MMICs based on CMOS technologies demonstrate P_{out} of up to 23 dBm, whereas the BW does not exceed 120 GHz [10], [12]. Since state-of-the-art results are mainly based on HBT technologies, the demonstrated noise figures (NFs) are prone to be higher than values one would expect for high-electron-mobility-transistor-based (HEMT) solutions. Even though individual MMICs exhibit minimum NFs of 4 dB, a majority considerably exceeds the values of 10 dB at least for some part of the band.

In this work, we demonstrate DA MMICs that exceed BWs of 300 GHz with low NFs and an output power level of more than 10 dBm. The article is organized as follows. Section II summarizes the key features of the utilized in-house 35-nm gate-length InGaAs metamorphic HEMT (mHEMT) technology. Section III describes the design of the presented MMICs

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TABLE I
OVERVIEW OF STATE-OF-THE-ART DA MMICS WITH >150 GHz BW

Reference	Technology	Bandwidth (GHz)	S_{21} (dB)	$P_{dc,q}$ (mW)	P_{out} (dBm)	NF (dB)
[9]	InP DHBT	1–160	avg. 10.5	288	14.6–17.8 (< 110 GHz)	10.1–20 (< 110 GHz)
[8]	500-nm InP DHBT	0.1–170	12	180	7.7–11.4	8–14.6 (@ 3–150 GHz)
[7]	130-nm SiGe BiCMOS	1–170	10	108	9 (< 50 GHz)	4–6 (@ 50–67 GHz)
[6]	130-nm SiGe BiCMOS	0.5–181	15.7–18.7	86	2.5 (@ 100 GHz)	6 (@ 60 GHz)
[5]	250-nm InP DHBT	10–207	11.5–15.5	210	5.5 (@ 195 GHz)	n/a
[4]	250-nm InP HBT	40–222	10	105	8.5 (@ 134 GHz)	n/a
[3]	250-nm InP DHBT	2–237	16 (14–18)	117	n/a	9–12.6 (< 195 GHz)
[2]	250-nm InP DHBT	1–242	10	387	10.5 (@ 10 GHz)	n/a
This work (AMP6)*	35-nm InGaAs mHEMT	1–335	avg. 11 avg. 9.2	215 90	6.4–11.5 n/a	3.9–9.2 3.5–8.2
This work (AMP8)*	35-nm InGaAs mHEMT	1–330	avg. 13 avg. 11.2	346 144	8–13.4 n/a	2.8–10.7 2.4–9.6
This work (AMP10)*	35-nm InGaAs mHEMT	1–315	avg. 14.1 avg. 13.1	512 210	8.7–14.8 n/a	2.3–10.9 2–10

* P_{out} and NF are given for frequencies of up to 250 and 308 GHz, respectively. The upper and lower rows refer to the standard and noise-optimized bias, respectively.

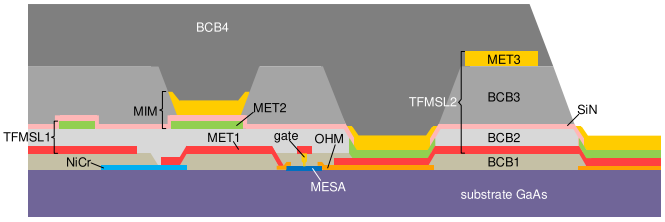

Fig. 1. Simplified cross section of the layer stack of the utilized 35-nm gate-length mHEMT technology.

and analyzes BW-limiting design parameters. An extensive set of small- and large-signal on-wafer measurements is presented in Section IV before concluding the results of this article in Section V.

II. 35-nm mHEMT TECHNOLOGY

The presented work is based on the Fraunhofer IAF 35-nm gate-length $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ mHEMT technology and features a maximum transconductance and drain current density of 2500 mS/mm and 1300 mA/mm, respectively. The maximum transition frequencies (f_T) and f_{max} exceed 500 and 1000 GHz, respectively (measured for a 2×10 μm device). The HEMT layers are grown by molecular beam epitaxy on 100 mm semi-insulating GaAs wafers. A metamorphic buffer is used to adapt the lattice constant of GaAs to the value of InP. A detailed description of the front-end-of-line process is given in [17].

The utilized technology features a back-end-of-line (BEOL) process, including three interconnection gold layers, metal–insulator–metal (MIM) capacitors, and 50-Ω/□ NiCr thin-film resistors. A simplified cross section of the layer stack is shown in Fig. 1. The metal layers are separated by benzocyclobutene (BCB). The first BCB layer (BCB1) encapsulates the T-gate. On top, the first metal layer (MET1) is evaporated and used as an additional gate head reducing the gate-line resistance. As described in [18], this three metal-layer process enables mainly two different versions of TFMSLs. A MET1 layer, used as a ground plane, has to be opened only in the area of active devices or wire bond pads. A major benefit of an almost uninterrupted MET1 ground plane is a strongly reduced impact of the wafer material and back-side process on the circuit performance. TFMSL1 uses MET2 as signal strip and the 1.4-μm-thick BCB2 as a substrate. The thin-film substrate of TFMSL2 combines BCB2 with the thicker BCB3 layer and uses the 2.7-μm-thick MET3 as signal strip. The MIM capacitors are realized with MET2 and MET3 electrodes, which are separated by an 80-nm-thick silicon nitride layer. This allows series and shunt capacitors in both TFMSL environments without opening the MET1 ground plane. On top of MET3, BCB4 is coated as a final protection layer. After finishing the front-side process, the wafers are thinned to a thickness of 135 μm.

III. DA MMIC DESIGN

This section presents the key design features of three uniform DA MMICs. The two considered TFMSL stacks of the used 35-nm mHEMT technology are discussed in Section III-A. The design of the unit cell is described in Section III-B and includes an investigation of BW-limiting effects of high-frequency DAs. In Section III-C, the design of the entire MMICs is presented. The design goals are a covered BW of at least 300 GHz starting near dc, S_{21} of more than 10 dB, a minimal NF (ideally less than 6 dB up to 170 GHz), and P_{out} of more than 10 dBm at least for the lower half of the BW.

A. Thin-Film Microstrip TLs

The BEOL process mainly enables two TFMSL environments. TFMSL1 offers the advantage that signals can be

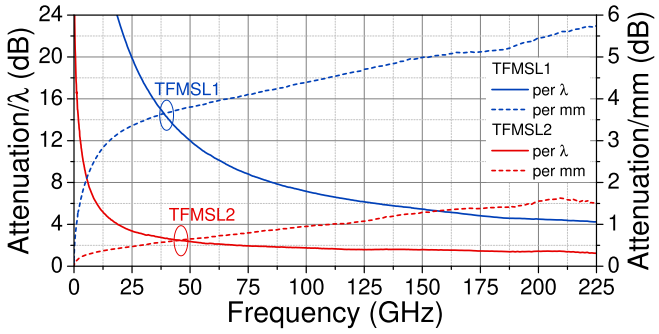

Fig. 2. Measured attenuation per effective wavelength and per millimeter versus frequency of TFMSL1 and TFMSL2. The characteristic impedance of both TLs is approximately 50 Ω.

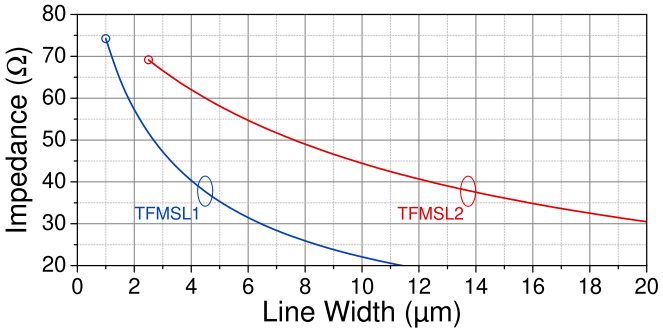

Fig. 3. Simulated characteristic impedance of TFMSL1 and TFMSL2 at 300 GHz versus linewidth. The circles indicate the thinnest allowed linewidth.

routed with a distance of only a few micrometers with almost no interaction allowing very compact designs. However, this comes at the price of higher losses. Fig. 2 shows a comparison of the attenuation per wavelength (λ) and per geometric length as a function of the operating frequency for both TFMSLs. The data are extracted using a multiline thru–reflect–line calibration algorithm [19] and five line standards with lengths ranging from 0 to 1.9 mm. As shown in Fig. 2, the attenuation per λ of TFMSL2 is, e.g., at 100 GHz by a factor of four better than the value of TFMSL1. At lower frequencies, this is even more pronounced. This makes TFMSL2 the best option for bigger matching networks or low-loss gate and drain lines in DAs. In addition, the current rating of MET3 (used for TFMSL2) is by a factor of five larger compared to MET2 (used for TFMSL1). This is an essential characteristic for the drain line of DAs or output matching networks.

Fig. 3 shows the simulated impedance versus linewidth. The data are extracted from simulations at 300 GHz using the frequency-domain port-mode solver of CST Microwave Studio. The necessary material parameters for the metals and dielectrics are based on the same measurements that were used for the loss extraction in Fig. 2. For both TFMSLs, the characteristic impedance that can be realized range from about 30–70 Ω for realistic linewidths. TFMSL1 covers a slightly wider range, which might be beneficial for, e.g., low-impedance matching networks. Design rule restrictions limit the highest impedance of TFMSL1 and TFMSL2 to approximately 74 and 69 Ω, respectively. In summary, both TFMSL environments offer a wide range of usage. TFMSL1 is mainly beneficial for very compact and high-frequency design tasks,

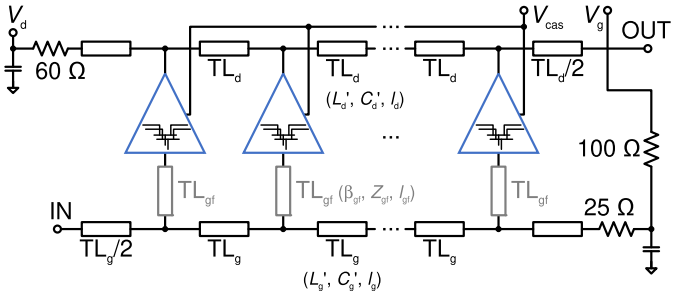

Fig. 4. Block diagram of a uniform DA MMIC as it is used in this work.

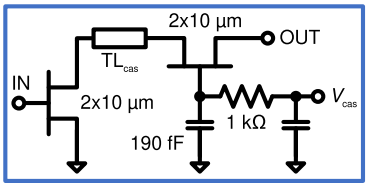

Fig. 5. Simplified schematic of the active part of the unit cell.

whereas TFMSL2 provides a superior low-loss performance and dc current handling.

B. Unit Cell Design

The unit cell is the essential core of a uniform DA MMIC. Fig. 4 shows a block diagram of a uniform DA. The basic design of the unit cell and, subsequently, of the MMICs follow standard design strategies of DAs where the input gate line and output drain line are considered as artificial TLs (ATLs) [15], [16], [20]. A more detailed focus is spent on BW-limiting effects, especially of the gate line.

The per-unit-length inductance (L') and capacitance (C') of the gate and drain ATLs determine the fundamental parameters of a DA, such as the impedance and the cutoff or Bragg frequency (f_{bragg}) of the gate and drain ATLs that are given as [16], [21]

$$Z \approx \sqrt{\frac{L'}{C'}} \tag{1}$$

$$f_{\text{bragg}} \approx \frac{1}{\pi\sqrt{L'C'}}. \tag{2}$$

For both equations, the major design task concentrates on C', which is a sum of the per-unit-length capacitance of the used TL and a part correlated with the input or output capacitance of the active device. For the gate ATL, C' equals $C'_g + C_{\text{in}}/l_g$, where C'_g is the per-unit-length capacitance of the gate TL (TL_g), C_{in} is the input capacitance of the active device (as exemplified in Fig. 5), and l_g is the geometric length of TL_g. The term for the drain ATL follows correspondingly ($C'_d + C_{\text{out}}/l_d$). Equations (1) and (2) also illustrate that TLs with a high characteristic impedance are beneficial since it either allows a larger total gate width for a given BW or increases the BW for the same devices size without capacitive division at the input.

In general, the implementation of DA unit cells can be classified into two groups—with and without a capacitive division at the input. In this work, a dc-coupled unit cell without capacitive division is used for two reasons. First,

for the aimed design, the low-frequency NF is important. A series capacitor and the necessary gate-bias network before the transistor would degrade the NF toward lower frequencies. Second, as demonstrated by Agarwal *et al.* [22], the overall amplifier gain scales linearly with the capacitive-division ratio $C_{\text{ser}}/(C_{\text{ser}}+C_{\text{in}})$, where C_{ser} is a series capacitor that is used to reduce C' of the gate ATL. Since for a high-frequency DA, providing sufficient gain is already a challenge, a further reduction of S_{21} is avoided.

For most HEMT technologies, the input capacitance is much larger than the corresponding output capacitance. Therefore, the achievable BW of the chosen DA topology (without capacitive division) is mainly determined by the gate ATL. The impedance of the gate ATL and the Bragg frequency of a DA are given as

$$Z_g = \sqrt{\frac{L_g}{C_g + C_{\text{in}}}} \tag{3}$$

$$f_{\text{bragg}} = \frac{1}{\pi\sqrt{L_g\left(C_g + C_{\text{in}}\right)}} \tag{4}$$

where L_g and C_g are the parameters of TL_g per unit cell and equal $L'_g l_g$ and $C'_g l_g$, respectively.

Commonly, C_{in} is considered to be C_{gs} or, in some cases, the impact of the gate–drain capacitance is included. However, as the next paragraph demonstrates, for designing DAs with several hundreds of gigahertz BW, considerably small gate-feeding structures can already have an important impact on the performance. These gate-feeding structures can be, for instance, a designed TL, a section of TL the transistor layout includes by default, a small TL that separates the gate line and the transistor to reduce coupling, or a vertical connection of the TL level to the active device. If a coplanar waveguide environment is used, this can be even the small section of TL the T junction contains to bridge the gap between the actual connection and the commonly used reference plane. In this work, this effect is considered as an additional TL (TL_{gf}) as it is shown in Fig. 4. For the following analysis, the input impedance of the transistor or gain cell ($Z_{\text{in,FET}}$) is approximated as a simple series RC network:

$$Z_{\text{in,FET}} = R_{\text{in}} - \frac{i}{\omega C_{\text{in}}}. \tag{5}$$

$Z_{\text{in,FET}}$ is transformed by TL_{gf} so that the effective input impedance ($Z_{\text{in,cell}}$), which has to be considered for the gate ATL, is

$$Z_{\text{in,cell}} = Z_{\text{gf}}\frac{Z_{\text{in,FET}} + i\,Z_{\text{gf}}\tan\left(\beta_{\text{gf}} l_{\text{gf}}\right)}{Z_{\text{gf}} + i\,Z_{\text{in,FET}}\tan\left(\beta_{\text{gf}} l_{\text{gf}}\right)} \tag{6}$$

where Z_{gf} is the characteristic impedance, β_{gf} is the phase constant, and l_{gf} is the geometric length of TL_{gf}.

In general, the propagation constant of the gate ATL is given as [21]

$$\gamma_g \approx \frac{1}{2}R_{\text{in}}(\omega C_{\text{in}})^2\sqrt{\frac{L_g}{C_g + C_{\text{in}}}} + \text{i}\omega\sqrt{L_g\left(C_g + C_{\text{in}}\right)}. \tag{7}$$

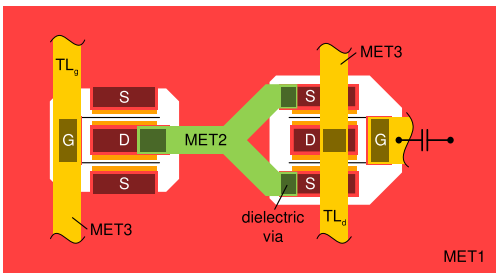

Fig. 6. Simplified layout of the utilized unit cell. Gate, source, and drain of the HEMTs are indicated by "G," "S," and "D," respectively.

Based on (6) and the transformation by TL_{gf}, R_{in} and C_{in} that have to be considered in (7) are

$$R_{\text{in}} = \Re(Z_{\text{in,cell}}) \tag{8}$$

$$C_{\text{in}} = -\frac{1}{\omega\Im(Z_{\text{in,cell}})}. \tag{9}$$

Using (3) and (9), the impedance of the gate ATL and the corresponding input return loss to a system impedance of 50 Ω can be determined. The real and imaginary parts of (7) describe the attenuation constant (α_g in nepers per unit cell) and the phase constant per unit cell. It is important to note that the losses of TL_g are not considered in (7) and adds up to the real part. For achieving the attenuation of the drain ATL, a similar investigation can be done. However, in general, the output conductance is considerably high so that the drain-line losses can be neglected [22]. This is especially true for cascode configurations.

The given analysis shows that the propagation constant and by that the attenuation at the gate line, the input matching, and the achievable BW depends on TL_{gf}. The next paragraphs exemplify that, especially for high-frequency DAs, this impact is important to consider.

For the actual design of the unit cell, the following decisions have been made. For a high S_{21}, the unit cell is based on a symmetric cascode configuration where each two-finger transistor has a total gate width of 20 μm. A simplified layout of a unit cell is shown in Fig. 6. The connection between the two HEMTs (TL_{cas}) is realized in TFMSL1 to reduce a possible coupling with the gate-feeding part of the first transistor, which could otherwise increase the parasitic gate–drain capacitance. The RF termination capacitor at the gate of the second HEMT is 190 fF. The value is designed in combination with the length of TL_{cas} so that a stable operation and a maximum possible gain are achieved. The gate bias of the first transistor is supplied via the gate line. For the second transistor, the gate voltage (V_{cas}) is fed via a 1 kΩ resistor, which is sufficiently high to present an RF-open-like circuit. The linewidth of TL_g and the drain TL (TL_d) is set to 4 μm. This corresponds to a characteristic impedance of approximately 62 Ω and L' and C' of 325 $\text{nH}\cdot\text{m}^{-1}$ and 85 $\text{pF}\cdot\text{m}^{-1}$, respectively. The linewidth was chosen as a compromise between a smallest possible linewidth for a high impedance and a sufficiently wide line to avoid a possible impact on the design due to process tolerances. Furthermore, current-rating rules require a minimum linewidth of 4 μm for TL_d. The length of TL_g is determined to be 71 μm. This design decision is explained

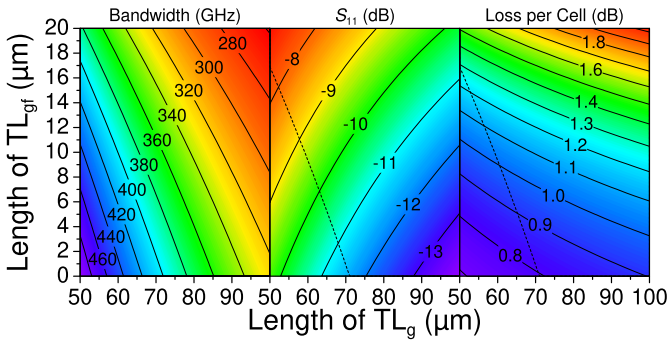

Fig. 7. Contour plots describing the impact of TL_{gf} on the achievable BW, input matching, and loss per unit cell on the gate ATL. The dashed line indicates the corresponding parameters for a constant BW of 403 GHz.

in the next paragraph. To fulfill synchronism of signals in the gate and drain line ($\beta_g l_g \approx \beta_d l_d$), the length of TL_d is 111 μm.

For the investigation of the impact of TL_{gf} on crucial performance parameters, Fig. 7 shows the contour plots of the achievable BW, the input matching, and the loss per unit cell in the gate ATL. It clearly illustrates that the three parameters are correlated with each other and are strongly affected by TL_{gf}. The required input resistance and capacitance of the active part of the unit cell are extracted at 300 GHz from simulations, which are supported by 3-D electromagnetic (EM) simulations (CST Microwave Studio). R_{in} and C_{in} are 4 Ω and 21 fF, respectively. In Fig. 7, the phase constant (β_{gf}) and characteristic impedance (Z_{gf}) of TL_{gf} are assumed to have the values of a 50-Ω TFMSL2 at 300 GHz. Based on the given analysis and the above-discussed design parameters, a theoretical BW of 403 GHz can be achieved for a zero-length TL_{gf}. This ensures that a BW of at least 300 GHz can be achieved also taking imperfections and additional losses into account. Fig. 7 highlights as well the importance of a shortest-possible TL_{gf}. For the given example, the achievable absolute BW decreases by approximately 1% for each additional micrometer of TL_{gf}. For an only 10-μm-long TL_{gf}, this would mean that the BW, S_{11}, and the loss per unit cell degrade from 403 GHz, -11.6 dB, and 0.8 dB to 362 GHz, -10.2 dB, and 1.1 dB. One of each parameter can be, of course, adjusted by, e.g., reducing l_g, however, still with a negative impact on the DA performance. In Fig. 7, dashed lines indicate the corresponding S_{11} and the loss per unit cell for a constant BW of 403 GHz. For the above example, this would mean that the loss per unit cell increases slightly (1 dB), and however, the input matching degrades even stronger (-9.2 dB). Furthermore, the reduction of l_g has also practical limitations. The transistors and the associated circuitry have a minimal-required width. Below this value, l_g cannot be decreased. For the given reasons, it is essential for high-frequency DAs to avoid even small TL_{gf} or similar effects as much as possible. Therefore, the layout of the utilized unit cell is shown in Fig. 6. A major feature is that TL_g is directly above the gate connection of the common-source HEMT, which reduces the above-described effect to a minimum. Even though the impact of a series-connected TL at the drain line is less pronounced, TL_d uses a similar feature. TL_d crosses the upper transistor orthogonally and connects the drain region of the upper transistor vertically. Furthermore, this allows connecting the gate capacitor of the upper HEMT in line with the gate fingers and by that simplifies the layout of the unit cell. TL_g is designed as a straight line, whereas TL_d is meandered to adapt the different length of both TLs.

C. MMIC Design

A major question for the design of an entire DA MMIC is the number of unit cells. In [21], an approximation of the maximum number of unit cells (n_{max}) is given as

$$n_{max}\alpha_g \leq 1 \tag{10}$$

$$\Rightarrow n_{max} \leq \frac{2}{R_{in}(\omega C_{in})^2 Z_g}. \tag{11}$$

The equation is based on the assumption that, due to the attenuation constant of the gate ATL, the transistor of the $(n_{max}+1)$th cell is almost not driven by the injected input signal. It is important to note that, due to the dependence of n_{max} on α_g, n_{max} depends as well on TL_{gf}, which emphasizes the importance of keeping TL_{gf} as electrically short as possible. For the designed unit cell, n_{max} equals 10.9. Thus, for gain reasons, a number of unit cells of close to n_{max} are advantageous. In general, the saturated output power benefits as well from more unit cells. However, for a low NF at the upper band edge, it is commonly better to reduce the number of unit cells. In addition, the linearity of a uniform DA without capacitive division at the input of each unit cell is expected to degrade when approaching n_{max}. Therefore, to investigate these tradeoffs, three DA MMICs are designed with six, eight, and ten cells. Corresponding to the used number of cells, the MMICs are named AMP6, AMP8, and AMP10. A chip photograph of each MMIC is shown in Fig. 8. The comparison of the measurement results of the three amplifiers will allow an investigation of the scaling of important performance parameters, such as S_{21}, NF, P_{out} at 1 dB gain compression ($OP_{1\,dB}$), and the output third-order intercept point (OIP3).

The termination resistors at the end of the gate and drain lines are 25 and 60 Ω, respectively. The resistors are chosen to trade gain flatness, NF, and return loss at low frequencies against each other. In order to avoid the limitation of possible applications and allow the operation toward very low frequencies, the RF input and RF output are dc-coupled to the gate and drain lines of the MMICs. The gate voltage (V_g) and drain voltage (V_d) are fed via the termination resistors. Therefore, the resistor at the end of the drain line is chosen sufficiently wide to allow the required dc drain current also for AMP10. Large MIM capacitors are used to present an RF ground after the termination resistors. Since the area of on-chip capacitors is limited, the lower band edge is determined to approximately 1 GHz. However, additional off-chip shunt capacitors can be used to extend the low-frequency performance. Thus, the lower band edge is not limited by the design per se.

IV. Measurement Results

The MMICs are characterized on wafer and biased identically for all measurements unless otherwise stated. V_g and V_d are supplied via the gate- and drain-line termination resistors and are controlled so that V_d at HEMT level of 1.6 V and a quiescent I_d of 400 mA/mm is achieved. The measured

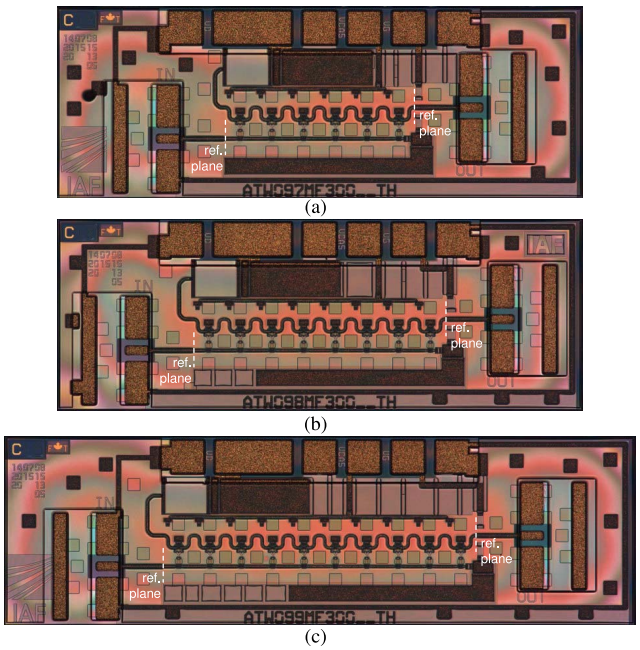

Fig. 8. Chip photographs of the fabricated MMICs of (a) AMP6, (b) AMP8, and (c) AMP10 with a total size of (a) and (b) 1.25 × 0.5 mm^2 and (c) 1.5 × 0.5 mm^2. The occupied chip area of the amplifier cores without pads of (a)–(c) is 0.5 × 0.28, 0.65 × 0.28, and 0.8 × 0.28 mm^2, respectively. The reference planes for the S-parameter measurements are indicated by white dashed lines.

TABLE II
SUMMARY OF MMIC MEASUREMENTS

	AMP6	AMP8	AMP10
BW (GHz)	1–335[‡]	1–330[‡]	1–315[‡]
S_{21} (dB)	9.2–12 (avg. 11) 7–11 (avg. 9.2)	10–14.5 (avg. 13) 8–13.4 (avg. 11.2)	10–16.5 (avg. 14.1) 9.8–15.3 (avg. 13.1)
NF[*] (dB)	3.9–9.2 (4.1, 3.6, 5.4, 8.9) 3.5–8.2 (3.9, 3.4, 4.9, 7.8)	2.8–10.7 (3.9, 3.6, 5.7, 10.2) 2.4–9.6 (3.6, 3.2, 5.1, 9)	2.3–10.9 (3.8, 3.8, 5.4, 10.3) 2–10 (3.3, 3.3, 6.3, 9.4)
P_{out}[†] (dBm)	6.4–11.5 (10.6, 10.1, 8.2, 7.1) n/a	8–13.4 (12.2, 11.8, 10, 8.5) n/a	8.7–14.8 (13.7, 13, 11.2, 9.2) n/a
$OP_{1\,dB}$[$] (dBm)	6.8–8.5 (avg. 7.6) n/a	7.4–8.9 (avg. 8) n/a	8.2–9.7 (avg. 9) n/a
OIP3[#] (dBm)	17.1–20.3 (avg. 19) n/a	17.8–20.3 (avg. 18.9) n/a	15.4–18.8 (avg. 17) n/a
$P_{dc,q}$ (mW)	215 (77)[•] 90 (36)[•]	346 (102)[•] 144 (48)[•]	512 (128)[•] 210 (60)[•]

The upper and lower rows of each measurement refer to the standard and noise-optimized bias, respectively.
[*] Noise setups: 0.1–50, 75–110, 110–150, 160–205, and 250–308 GHz. The average NFs of the waveguide bands are shown in parentheses in ascending order. | [†] Power setups: 1–68, 75–110, 115–170, and 175–250 GHz (average values in parentheses). | [$] $P_{1\,dB}$ setup: 5–110 GHz. | [#] Intermodulation setup: 5–49 GHz. | [‡] Extension of lower band edge possible with additional off-chip capacitors. | [•] If biased via an external drain bias tee.

power consumption and efficiency include the voltage drop across the drain-line termination resistor. To give an overview, Table II summarizes the measured performance of the presented MMICs. The upper rows of each measurement refer to the standard bias, whereas the lower rows indicate the values for a noise-optimized bias. The quiescent power consumptions ($P_{dc,q}$) of the MMICs are listed in Table II for both bias conditions. The values in parentheses show $P_{dc,q}$ if the drain bias is supplied via the RF output of the MMICs. This might be of interest for banded applications where an additional bias tee, such as an RF-shorted stub, can be easily integrated on the same MMIC.

A. Small-Signal Measurements

The S-parameters are measured in two bands—from 0.01 to 200 GHz with an Anritsu VectorStar system (ME7838G) and from 200 to 335 GHz with a Keysight PNA-X and VDI WR-3.4 waveguide extenders. The calibration reference planes for the S-parameters are indicated by white dashed lines in Fig. 8. For the calibration, a line-reflect-reflect-match (LRRM) algorithm and on-wafer calibration standards are used. Fig. 9 shows the S-parameters of the presented MMICs. AMP6, AMP8, and AMP10 exhibit an average S_{21} of 11, 13, and 14.1 dB for BWs of 334, 329, and 315 GHz, respectively. For AMP6, this equals a 3-dB BW. For the given BW of AMP8 and AMP10, S_{21} of more than 10 dB is achieved. As explained in Section III-C, the lower band edge is determined by the integrated MIM capacitors and can be extended toward lower frequencies by adding off-chip capacitors. In the presented implementation, the performance is flat down to 1 GHz, where then, e.g., S_{21} increases. For the most part of the band, the input return loss is better than 10 dB. The same is true for the output return loss for frequencies of up to approximately 160 GHz. Above, the output return loss drops, which is not predicted by the simulations. Since the deviation occurs mainly at higher frequencies, this is interpreted as an interaction between the two RF probes of the measurement system. In addition, it can be observed that the deviation between the measured and simulated S_{22} shifts toward lower frequencies when increasing the number of unit cells and by that the distance between the two RF probes. Similar effects were reported previously, e.g., in [18]. Apart from that, a good agreement between measurements and simulations can be observed.

Fig. 10 shows a scatterplot of the measured S_{21} for an entire wafer mapping with a variation of less than only 2 dB for most cells and a corresponding yield of better than 80%. It shows as well that, for the higher part of the covered frequency band, S_{21} saturates, and AMP8 and AMP10 provide almost similar values. This is in line with the investigation given in Section III-C, where a maximum number of cells of ten are predicted.

The NF is characterized using various on-wafer setups for different frequency ranges. From 0.1 to 50 GHz, the NF is measured with a Keysight PNA-X setup using the vector-corrected cold-source method [23]. The banded setups (75–110, 110–150, 160–205, and 250–308 GHz) use the Y-factor method. For the first three bands, the noise generators are ELVA-1 waveguide noise diodes. For the highest band, an in-house-built noise-generator WM-864 module is used containing an active hot-/cold-load MMIC. A similarly working MMIC, operating in W-band (75–110 GHz), is described in [24]. The actual NFs are measured with a Keysight NF analyzer and commercially available down-converter modules.

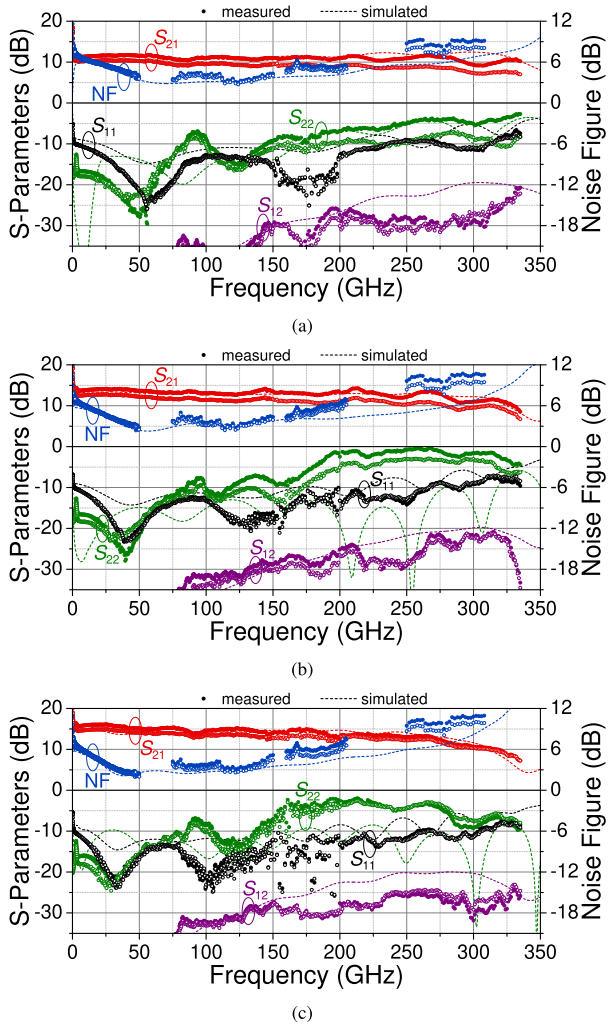

Fig. 9. Measured (symbols) and simulated (dashed lines) S-parameters and NFs of (a) AMP6, (b) AMP8, and (c) AMP10 from 0.01 to 335 GHz. The data for the standard bias ($V_d = 1.6$ V and $I_d = 400$ mA/mm) and the noise-optimized bias ($V_d = 1.2$ V and $I_d = 250$ mA/mm) are indicated by closed and open symbols, respectively.

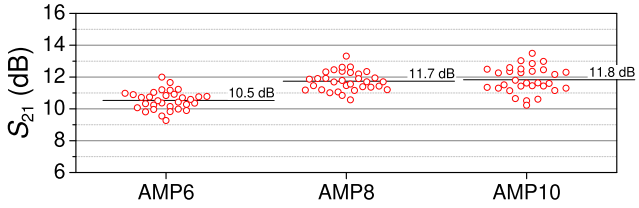

Fig. 10. Wafer mapping of the measured S_{21} in the WM-864 waveguide band including 32 cells (31 cells for AMP10) out of 37 cell on a wafer. For the scatterplot, S_{21} is averaged over the BW of the amplifiers from 200 GHz up to the corresponding upper band edge. The amplifiers use standard bias conditions.

The measured NFs are calibrated to the RF probe tips and by that include the loss of RF pads and access lines (in total, approximately 0.1, 0.2, and 0.3 dB at 100, 200, and 300 GHz, respectively). The measurement results of the three amplifiers are shown in Fig. 9. A summary is given in Table II (including the average NFs for the waveguide bands in parentheses). The NFs for the standard bias are indicated by closed symbols. When biasing the MMICs with a drain voltage at HEMT level of 1.2 V and an I_d of 250 mA/mm, the NFs,

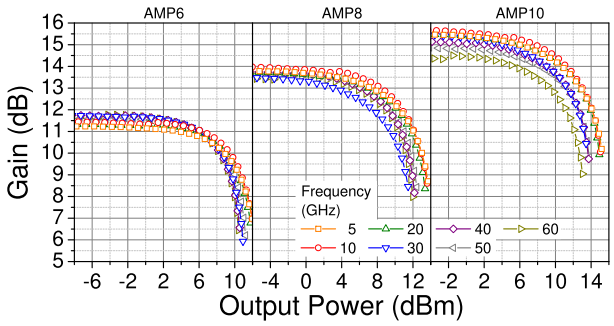

Fig. 11. Measured transducer gain versus single-tone continuous-wave (CW) output power for standard bias and operating frequencies between 5 and 60 GHz.

especially at higher frequencies, can be optimized. In Fig. 9, the corresponding results are shown by open symbols. A major difference between the MMICs is that, on the one hand, AMP10 exhibits a lower NF, of about 2 dB, for frequencies of around 50 GHz and reaches the lowest NF also for lower frequencies as compared to AMP8 or even AMP6. On the other hand, AMP6 achieves by more than a decibel lower NFs at the upper part of the band compared to the other two MMICs. Over the entire measured band, the NF of AMP6 is below 9.2 and 8.2 dB for standard and noise-optimized bias, respectively.

B. Large-Signal Measurements

The single-tone large-signal measurements were performed in the following frequency ranges: 1–68, 75–110, 115–170, and 175–250 GHz. The first setup comprises a Keysight signal generator and an Anritsu spectrum analyzer (MS2760A) as a frequency-selective power sensor. The latter three setups are based on waveguide components. The signal generation is done with waveguide extender modules. For the highest two frequency ranges, additional amplifier modules are used to boost the available input power. The waveguide power meters are from Keysight (E4416A + W8486A), ELVA-1 (DPM06), and VDI-Erickson (PM5B). The two-tone measurements are done with two Keysight signal generators. The signals are combined with a broadband directional 10-dB coupler. The output signal is measured with a Keysight spectrum analyzer (N9030A). All setups are calibrated to the RF probe tips.

For frequencies between 5 and 60 GHz, Fig. 11 shows a power sweep with transducer gain (G_t) versus P_{out}. It can be observed that the saturated output power, at least for frequencies up to 20 GHz, scales with approximately 2 dB per additional two unit cells. However, at the same time, it can be noticed that amplifiers with more unit cells show a softer compression behavior. This indicates that AMP6 might be more suited for scenarios with high linearity requirements and AMP10 has a stronger preference on a high P_{out}. These observations are also confirmed in Fig. 12. It depicts the single-tone output power for a compression of G_t of 1 dB ($\text{OP}_{1\,\text{dB}}$) and 4 dB ($\text{OP}_{4\,\text{dB}}$) and the two-tone input power (IIP3) and output power (OIP3) for the third-order intercept point. The increase of $\text{OP}_{1\,\text{dB}}$ between AMP6 and AMP10 is slightly above 1 dB. $\text{OP}_{4\,\text{dB}}$ scales almost ideally with the number of unit cells. AMP6 exhibits an average $\text{OP}_{4\,\text{dB}}$ of 10.8 dBm.

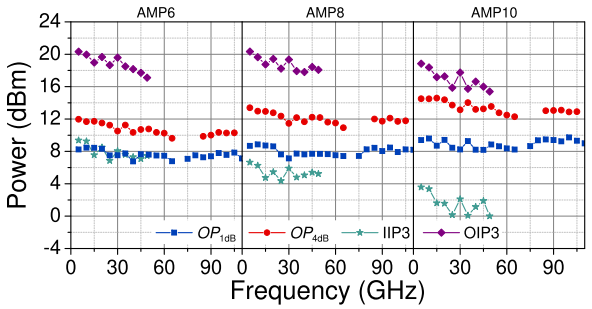

Fig. 12. Measured single-tone CW $OP_{1\,dB}$ and $OP_{4\,dB}$ and two-tone CW IIP3 and OIP3 versus operating frequency between 5 and 110 GHz.

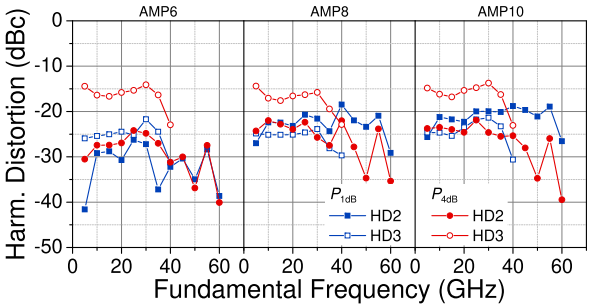

Fig. 13. Measured single-tone CW HD2 and HD3 at $P_{1\,dB}$ and $P_{4\,dB}$ versus fundamental frequency.

AMP8 and AMP10 achieve the corresponding output power levels of 1.4 and 2.7 dB, respectively, above the value of AMP6. As expected already from the results of the single-tone power sweeps, AMP6 shows the best linearity when referring to OIP3. AMP6 and AMP8 perform with an average of 19 and 18.9 dBm very comparable. For AMP10, OIP3 is by 2 dB reduced.

The generation of the unwanted second- (HD2) and third-harmonic frequency (HD3) in relation to the wanted fundamental output frequency is given in Fig. 13 for a G_t compression of 1 dB ($P_{1\,dB}$) and 4 dB ($P_{4\,dB}$). It can be observed that HD3 is for all MMICs very comparable with only minor differences. In addition, the generation of the third harmonic is higher for $P_{4\,dB}$ compared to $P_{1\,dB}$ so that HD3 is, even in relation to the increased fundamental frequency, stronger for a higher compression level. For AMP6, HD2 almost does not change over compression with slightly lower values for $P_{1\,dB}$ compared to $P_{4\,dB}$. Furthermore, a clear trend is that the more unit cells the DAs contain the higher is HD2, in general, and the more this characteristic is pronounced for $P_{1\,dB}$.

In Fig. 14, P_{out}, G_t, and the power-added efficiency (PAE) are shown versus operating frequency for two constant input power levels, which are approximately at $P_{1\,dB}$ and $P_{4\,dB}$ (chosen from the lower frequency part). AMP8 and AMP10 exhibit an output power of more than 8 and 8.7 dBm over the entire measured band with a peak P_{out} of 13.4 and 14.8 dBm, respectively. More details, including average values for the individual bands, are given in Table II.

C. Discussion

In summary, based on the measured small- and large-signal performance, the presented DA MMICs can be categorized according to possible applications. AMP6 is highly suitable

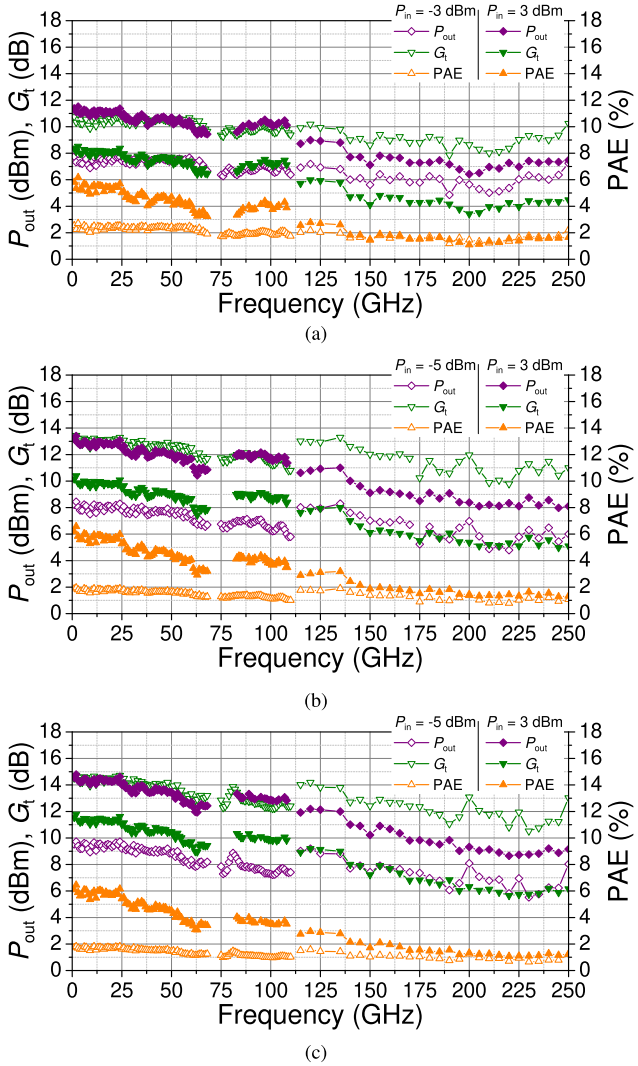

Fig. 14. Measured single-tone CW large-signal performance versus operating frequency of (a) AMP6, (b) AMP8, and (c) AMP10 for constant input power levels of −5 dBm/−3 dBm (open symbols) and 3 dBm (closed symbols).

for receive purposes with an NF of less than 9.2 dB even at operating frequencies of about 300 GHz, the best OIP3 of the presented MMICs, and an almost similar $OP_{1\,dB}$ with better harmonic distortion values. AMP10 represents the limit of a suitable maximum number of unit cells for the given design example and HEMT technology. While having a good NF, the main purpose of AMP10 is the generation of broadband output power. AMP8 presents a beneficial tradeoff between the diverse performance parameters. The NF of AMP8 is at low frequencies almost at the level of AMP10 while having an NF of only approximately 1 dB above AMP6 at the upper band edge. Furthermore, AMP8 provides a 2 dB higher S_{21} compared to AMP6 with nearly the same BW and P_{out} of more than 8 dBm up to 250 GHz.

V. Conclusion

This article demonstrates the first DA MMICs with a BW of more than 300 GHz. The design and performance of three MMICs are presented. This article includes an investigation of BW limiting effects especially in the input line

of high-frequency DAs and demonstrates the importance of an electrically short connection of the active device to the input line. Compared to the state of the art, AMP6 improves the absolute BW from 241 to 334 GHz by more than 38% with an even 1 dB higher S_{21}, a higher output power, and 44% less dissipated power. Furthermore, the three MMICs exhibit the lowest NF and the highest output power for DAs with BWs of more than 150 and 170 GHz, respectively. Moreover, also for banded applications, the obtained results demonstrate an appealing combination of small- and large-signal performances, such as an average NF and P_{out} of about 3.5 dB and 10 dBm, respectively, for AMP8 in D-band. Thus, the presented results can help to extend the frequency range of today's ultrawideband systems and mark an interesting alternative to reactively matched amplifiers for banded applications with a need for a tradeoff between the achievable BW, gain, NF, linearity, and output power.

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