A 36-Channel Auto-Calibrated Front-End ASIC for a pMUT-Based Miniaturized 3-D Ultrasound System

Jihee Lee, *Member, IEEE*, Kyoung-Rog Lee, *Member, IEEE*, Benjamin E. Eovino, Jeong Hoan Park, *Member, IEEE*, Luna Yue Liang, Liwei Lin, *Member, IEEE*, Hoi-Jun Yoo, *Fellow, IEEE*, and Jerald Yoo, *Senior Member, IEEE*

***Abstract*— We present an area- and power-efficient application-specific integrated circuit (ASIC) for a miniaturized 3-D ultrasound system. The ASIC is designed to transmit pulse and receive echo through a 36-channel 2-D piezoelectric Micromachined Ultrasound Transducer (pMUT) array. The 36-channel ASIC integrates a transmitter (TX), a receiver (RX), and an analog-to-digital converter (ADC) within the 250-μm pitch channel while consuming low-power and supporting calibration to compensate for the process variation of the pMUT. The charge-recycling high-voltage TX (CRHV-TX) in standard CMOS generates up to 13.2-V_{PP} pulse while reducing 42.2% peak TX power consumption. Also, each CRHV-TX automatically calibrates excitation voltage according to acoustic pressure of pMUT. The dynamic-bit-shared ADC (DBS-ADC) shares the most significant bits (MSBs) among four channels based on the signal similarity between adjacent channels. The analog front end (AFE) with a received signal sensitivity indicator (RSSI) changes its gain adaptively in real time depending on input signal strength. The ASIC consumes 1.14-mW/channel average power with 1-kHz pulse repetition frequency (PRF) and three TX pulses per cycle. The ASIC in 0.18-μm 1P6M Standard CMOS has been verified with both electrical and acoustic experiments with a 6 × 6 pMUT array.**

Manuscript received June 8, 2020; revised September 14, 2020 and November 17, 2020; accepted December 21, 2020. Date of publication January 29, 2021; date of current version May 26, 2021. This article was approved by Associate Editor Nick van Helleputte. This work was supported in part by the A∗STAR AME Wavefront Computing under Grant A19E9b0102 and in part by the National University of Singapore through the Hybrid Flexible Electronic Systems (HiFES) Program under Grant R-263-501-011-133/731. *(Corresponding author: Jerald Yoo.)*

Jihee Lee was with the School of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 34141, South Korea. She is now with the Samsung Electronics, Hwaseong 18200, South Korea (e-mail: jihee.lee@kaist.ac.kr).

Kyoung-Rog Lee and Hoi-Jun Yoo are with the School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 34141, South Korea.

Benjamin E. Eovino is with Chirp Microsystems, Berkeley, CA 94710 USA.

Jeong Hoan Park was with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117585. He is now with Samsung Electronics, Hwaseong 18200, South Korea.

Luna Yue Liang was with the Department of Mechanical Engineering, University of California at Berkeley, Berkeley, CA 94720 USA. She is now with Apple Inc., Shenzhen, Guangdong, China.

Liwei Lin is with the Department of Mechanical Engineering, University of California at Berkeley, Berkeley, CA 94720 USA.

Jerald Yoo is with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117585, and also with the N.1 Institute for Health, Singapore 117456 (e-mail: jyoo@nus.edu.sg).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2021.3049560.

Digital Object Identifier 10.1109/JSSC.2021.3049560

***Index Terms*— Analog-to-digital converter (ADC), application-specific integrated circuits (ASIC), calibration, charge recycling, dynamic bit-shared ADC, in-probe digitization, low power, piezoelectric micromachined ultrasound transducer (pMUT), time gain compensation (TGC), ultrasound imaging.**

I. Introduction

RECENTLY, demands on miniaturized 3-D ultrasound systems, such as transesophageal echocardiography (TEE) [1], intracardiac echocardiography (ICE) [2], and intravascular ultrasound (IVUS) [3], are increasing due to their real-time imaging with relatively low cost and decent resolution (see Fig. 1). Imaging resolution and its field-of-view (FoV) can be improved by integrating more transducer channels; however, as the channel number increases, the power consumption becomes an issue. For an implantable/in-body ultrasound system, overall power consumption (both peak and average), which contributes to the overall self-heating of the system, should be kept below 0.5 W, which is the power requirement of the TEE [4], to avoid excessive tissue temperature elevation [5]. Therefore, a 36-channel system should consume less than 13.9 mW/channel. Especially, localized hot spots should be avoided to prevent cell damages [6], [7]. Previous works that integrate a power-consuming transmitter (TX) and centralized analog-to-digital converter (ADC) [8] can cause localized hotspots; therefore, it is more suitable to have each transceiver (TRX) integrated in-pixel to minimize such hot spots. Moreover, the in-pixel TRX design also supports the vertical connection between transducers and the CMOS [9]–[11], which relieves bulky, cumbersome wire connection and parasitic resistance/capacitance. Also, the integration of the in-pixel ADC does not limit the beamforming (BF) algorithms. To achieve the in-pixel TRX design, a major challenge is the integration of a TX, a receiver (RX), and an ADC within the tight area budget.

Unlike previous works that adopt lead zirconate titanate (PZT) or a capacitive Micromachined Ultrasound Transducer (cMUT) as a transducer, we utilize the bimorph piezoelectric Micromachined Ultrasound Transducer (pMUT). The bimorph pMUT requires a lower driving voltage to generate the acoustic pressure as its driving sensitivity is better than other transducers [12]. Therefore, the power consumption of the TX, which is the most peak-power-consuming block,

can be reduced. Moreover, unlike the cMUT that requires a high dc biasing (30–200 V) [13] that results in a complicated power management unit (PMU) and leakage issue, the pMUT does not need dc biasing.

However, the pMUT suffers from large process variations in physical dimensions and film thickness, which significantly impacts their acoustic pressures, especially in the multi-channel array [14]. To avoid degradation of image resolution, the application-specific integrated circuit (ASIC) must compensate for the variation by calibrating its excitation voltage.

To resolve the aforementioned issues, we present an ultrasound TRX ASIC for the bimorph pMUT array. The ASIC is optimized in both system and circuit levels [15]. As a proof of concept, 36 channels are integrated as a prototype, while the design is scalable to a larger aperture. The dedicated ASIC is composed of 36-channel ultrasound transceivers that are designed to match 250-μm pMUT pitch while including all a TX, an RX, and an ADC within each channel. To reduce the average power consumption of each channel, the dynamic-bit-shared ADC (DBS-ADC) shares the most-significant bits (MSBs) among four adjacent channels. Moreover, the charge-recycling high-voltage TX (CRHV-TX) reuses the charge, which is used to deflect the pMUT membrane to reduce peak power consumption. The CRHV-TX is compatible with standard CMOS that is free from the bulky diffusion area. To compensate for the process variation of the pMUT, each CRHV-TX calibrates its excitation voltage corresponding to the measured acoustic pressure. Using higher frequency provides better resolution but at the cost of fewer penetration depths. To handle this tradeoff, the ASIC has a programmable TX frequency of 1, 2, 5, and 10 MHz that translates to the theoretical penetration depth of 25, 12.5, 5, and 2.5 cm, respectively. To generate acoustic pressure for such a target, we drive the bimorph pMUT with a unipolar 5-MHz 13.2-V_{PP} TX pulse, and 36 pMUT channels were focused to increase acoustic pressure. As a result, 0.2-MPa sound pressure was generated for a 5-cm penetration depth (a 10-cm propagation) at a 5-MHz center frequency.

The functionality of the ASIC, as well as the effectiveness of the proposed techniques, has been successfully demonstrated by both electrical tests and an ultrasonic imaging experiment.

The rest of this article is organized as follows. In Section II, the proposed 3-D ultrasound systems will be introduced. Section III discusses the key building blocks of the proposed ultrasound ASIC: 1) a CRHV-TX; 2) four-channel DBS-ADC; and 3) a received-signal sensitivity-indicator adaptive gain control front end (RSSI-AGC). Section IV shows the implementation and measurement results, and finally, Section V concludes this article.

II. Miniaturized 3-D Ultrasound System Overview

A. System Architecture

Fig. 2 shows the overall block diagram of the proposed miniaturized 3-D ultrasound ASIC. It consists of 36-channel ultrasound TRXs to control the pMUT array, an RSSI to measure the input signal strength in real time, a PMU, a phase-locked loop (PLL), and a digital controller. Each

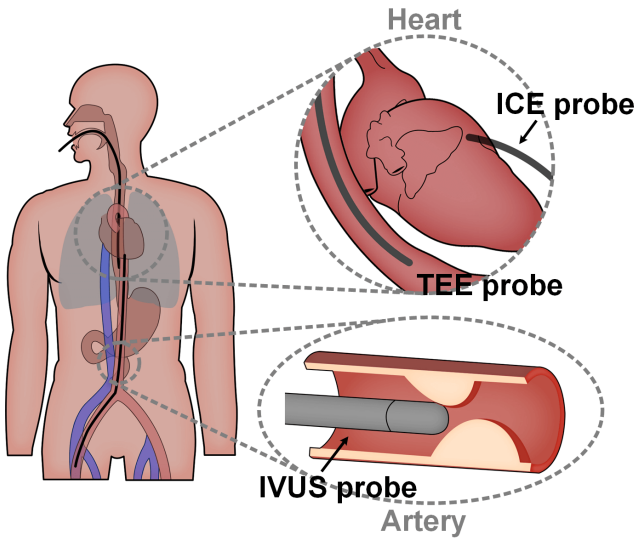


Fig. 1. Examples of miniaturized 3-D ultrasound system: TEE, ICE, and IVUS.

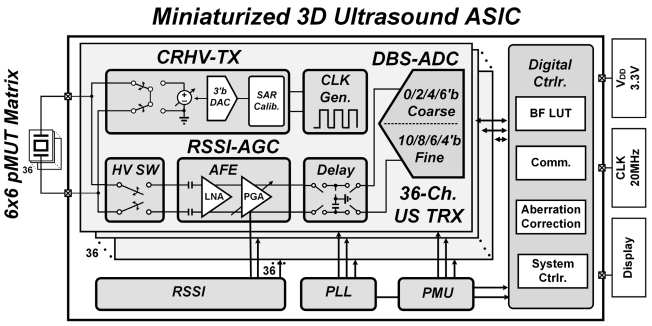


Fig. 2. Overall block diagram of proposed miniaturized 3-D ultrasound ASIC.

ultrasound TRX is composed of a CRHV-TX, an HV TX/RX switch, an low noise amplifier (LNA), a programmable gain amplifier (PGA), an analog delay cell, and a 10-bit successive-approximation-register (SAR) ADC; the TRX has three key features: 1) a CRHV-TX to reduce power consumption and calibrate process variation of the pMUT, 2) an SAR-based DBS-ADC to reduce power consumption, and 3) an RSSI-AGC to calibrate the gain based on the input signal magnitude in real time. A PMU generates high supply voltages (2 V_{DDH}, 3 V_{DDH}, and 4 V_{DDH}), which is used for the CRHV-TX and the TX/RX switch. The topology of the PMU is a cross-coupled switched capacitor [16], and the PMU can be turned off if the user wants to use an external supply. A PLL generates a 200-MHz internal system clock by a 20-MHz external clock. The 200-MHz internal system clock is used to control the analog delay cell and the digital controller, and the 20-MHz external clock is used to control the digital controller. The digital controller communicates with an external imaging device, correct pMUT aberration, and control TRX BF and system. As the speed variation of each pMUT channel can cause phase aberration that results in imaging degradation, the aberration correction calibrates the time-of-flight variance of each channel [17].

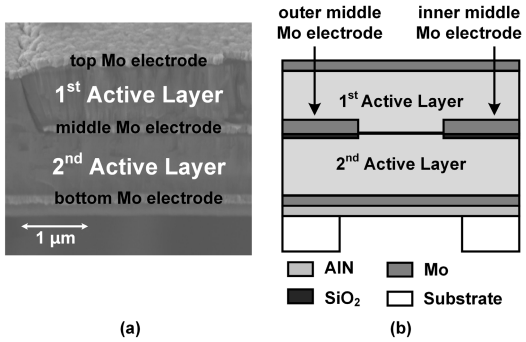
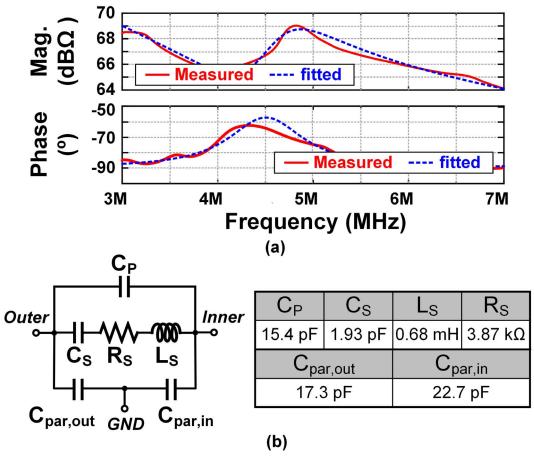


Fig. 3. pMUT matrix. (a) Cross section micro-scope image. (b) Cross-sectional diagram.



C_P	C_S	L_S	R_S
15.4 pF	1.93 pF	0.68 mH	3.87 kΩ
$C_{par,out}$		$C_{par,in}$	
17.3 pF		22.7 pF	

Fig. 4. (a) Measured and fitted impedance characteristics of the pMUT (solid line: measured; dotted line: fitted). (b) BVD equivalent electrical modeling.

B. pMUT Analysis

The pMUT matrix is fabricated in the silicon wafer and consists of aluminum nitride (AlN) bimorph membranes that formed the active transducer layers [12], [18]. The cross section micro-scope image of the transducer and its cross-sectional diagram are shown in Fig. 3(a) and (b), respectively. The AlN/Mo/AlN layers are stacked with a thickness of 805, 130, and 855 nm. A top electrode and a bottom electrode are grounded, and two middle inner and outer electrodes are connected to the ASIC to control active piezoelectric layers. The size of the pMUT matrix is 1.5 mm × 1.5 mm, and its channel pitch is 250 μm. Four (2 × 2) pMUT elements are connected in parallel in a channel to increase acoustic pressure, and each element has a circular shape whose diameter is 120 μm. As the current channel pitch of 250-μm is larger than the optimal transducer pitch of 150-μm, it can cause a grating-lobe issue. However, the transducer matrix pitch of 250-μm was the smallest pitch of the pMUT with the 5-MHz frequency that we had at the time of development. The transducer pitch is expected to decrease further as the transducer develops, and the ASIC channel pitch would also need to shrink accordingly.

Fig. 4(a) and (b) shows the impedance characteristic of a pMUT channel and its equivalent electrical model. The pMUT device is designed for a center frequency

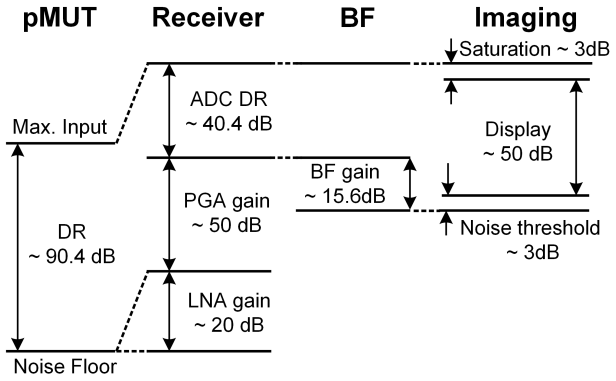


Fig. 5. Gain and DR requirements for ultrasound imaging.

of 5 MHz, and its resonance frequency is measured to be 4.81 MHz. A Butterworth-Van Dyke (BVD) model [19] with two additional parasitic capacitors is used for a simplified model of pMUT, and it consists of six components: shunt capacitor C_P (15.4 pF), C_S (1.93 pF), L_S (0.68 mH), R_S (3.87 kΩ), $C_{par,out}$ (17.3 pF), and $C_{par,in}$ (22.7 pF). The curve fitting is drawn above the measured impedance characteristics above Fig. 4(a).

The excitation voltage for the pMUT is decided by the required acoustic pressure for target penetration. The 13.2-V_{PP} excitation pulse is used to drive the pMUT, which generates 0.2 MPa for 5-cm penetration depth. All 36 pMUT elements are excited, and another pMUT matrix is placed at the focal point in vegetable oil. The pMUT receives 0.63-kPa acoustic pressure after 10-cm propagation. The receive sensitivity of the pMUT is measured into 82 mV/kPa, and its corresponding input signal is 52 mV. As the pMUT operates under 13.2 V_{PP}, which is less than a well breakdown voltage of the standard CMOS, the ASIC for the pMUT can be integrated into standard CMOS. The standard CMOS offers more design feasibility, and the ASIC can use a more advanced process node if the required excitation voltage is below breakdown voltage [20].

C. Design Parameters

The signal attenuation of ultrasound (A_{att}) can be expressed as follows:

$$A_{att} = \alpha \times 2 \times d \times f \tag{1}$$

where α is the acoustic attenuation coefficient, d is the imaging depth, and f is the frequency of the ultrasound. As the absorption is proportional to ultrasound frequency, a higher frequency ultrasound has a limited depth of penetration while showing high spatial resolution. In this work, the system is optimized for a 5-MHz ultrasound operation to provide enough resolution with decent penetration depth (5 cm). However, this ASIC also supports programmable frequency (1, 2, and 10 MHz) for other applications. As the acoustic signal penetrates through the body with an attenuation rate of 1 dB/MHz/cm [21], the signal attenuation is 50 dB for a 5-MHz center frequency and a 5-cm penetration depth. Also, the minimum display resolution of 50 dB is required to distinguish the characteristics of the

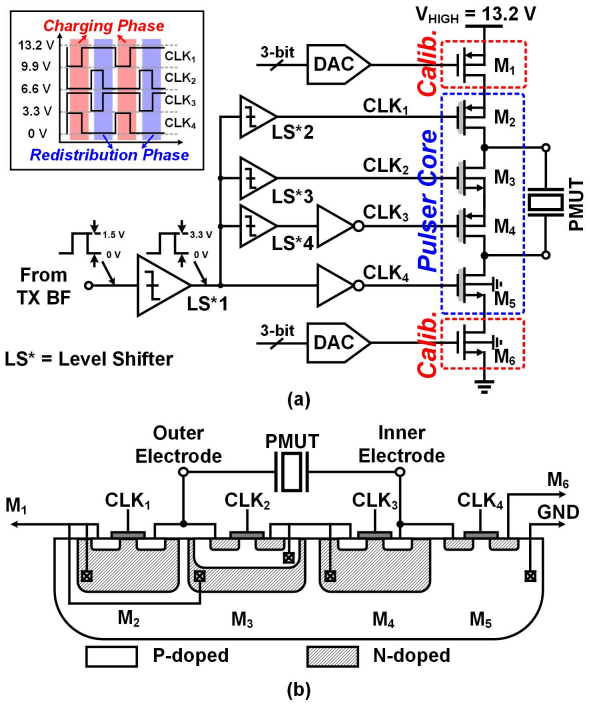


Fig. 6. (a) Schematic and (b) cross section of the CRHV-TX.

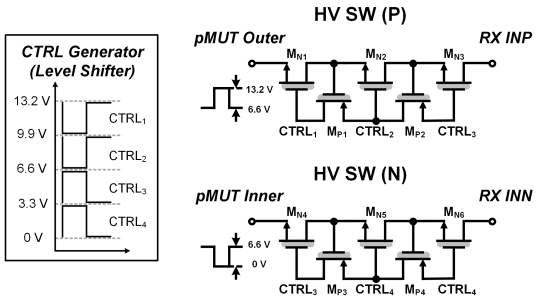


Fig. 7. Schematic of the HV TX/RX switch.

human organ [22]. On the other hand, an additional dynamic range (DR) can be achieved through BF since it combines and averages the signals. A total of 36 channels increase the DR by 15.6 dB ($20\log\sqrt{36}$ dB). Therefore, a total target DR of 90.4 dB can be obtained by calculating the signal attenuation of 50 dB, the minimum display resolution of 50 dB, imaging saturation allowance of 3 dB, the noise threshold of 3 dB, and BF of 15.6 dB (see Fig. 5) [23].

The gain of an LNA should be determined by the ratio of the ADC input and the maximum amplitude of the LNA as follows:

$$\text{Gain}_{\text{LNA}} = 20 \cdot \log_{10}\left(\frac{\text{Max. ADC Input}}{\text{Max. LNA Input}}\right) + \text{Margin}. \quad (2)$$

In this work, the maximum input of the LNA is assumed to be 300 mV, and the maximum ADC input is set to its supply voltage, 1.5 V. Thus, the required gain of the LNA is 14 dB + Margin, and the gain of LNA is determined to 20 dB with a 6-dB margin [24]. The maximum gain of the PGA is limited by 50 dB since the PGA compensates for signal

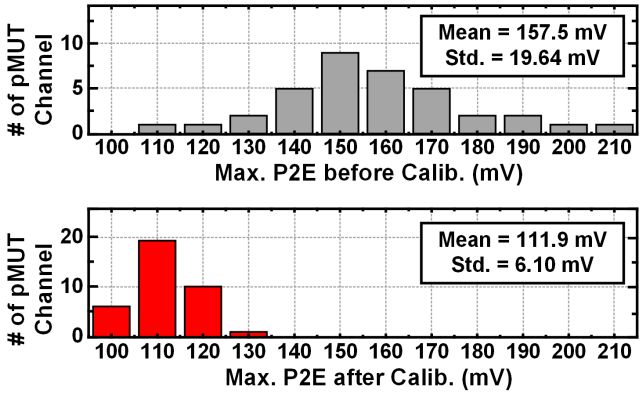


Fig. 8. Histogram of acoustic pressure variation of 36-channel pMUT.

attenuation along with the depth of the target penetration depth. Therefore, the required DR of the ADC is 40.4 dB.

III. Hardware Implementation

A. Charge-Recycling High-Voltage TX

The CRHV-TX drives the transducer to generate an ultrasound wave while showing higher power and area efficiency. The frequency of the CRHV-TX is programmable among 1, 2, 5, and 10 MHz to control the penetration depth and spatial resolution. Figs. 6 and 7 show the schematic of CRHV-TX with its cross-sectional view and the schematic of the HV TX/RX switch. The proposed miniaturized 3-D ultrasound system requires a power-efficient TX, which is compatible with standard CMOS. The previous works utilized large-size high voltage double-diffused MOS (DMOS) with bipolar-CMOS-DMOS (BCD) process to facilitate high voltage operation [25]. However, large-size DMOSs are hard to integrate into area-hungry ASIC channels. Moreover, the TX cannot be integrated into the most advanced process node and suffers from process cost and parasitic components from the diffusion area [26]. In contrast, the proposed CRHV-TX and the HV TX/RX switch are fully compatible with standard CMOS, where the stacked I/O transistors always operate within their normal operating voltage range. By adapting the pMUT whose required excitation voltage is 13.2 V_{PP}, the maximum voltage difference between p-well and n-sub is less than well breakdown voltage with approximately 30% margin. In the CRHV-TX, M_2–M_5 thick-oxide transistors are stacked with staggered well potential, and the stress of each transistor is dispersed, thereby compatible with the standard CMOS process. To control M_2–M_5 transistors, the level shifters LS^1–LS^4 generate clock signals in the proper voltage domain, and an internal PMU supplies $2V_{DDH}$, $3V_{DDH}$, and $4V_{DDH}$ to the level shifters. Similar to CRHV-TX, the main path of the HV TX/RX switch is also composed of stacked I/O transistors M_{N1}–M_{N6} to reduce the burden of each transistor under the well breakdown voltage. The M_{P1}–M_{P4} transistors are used to control the voltages of the stacked transistors correctly. The measured ON-resistance of the HV TX/RX switch is 64-Ω, which is slightly larger than the ON-resistance of the conventional HV TX/RX switch [27].

Noting that the majority (83.5%) of the peak power dissipation in the ultrasound system comes from TX [28], a power-efficient TX is crucial for safety [8]. The recurring large power consumption of the TX can cause localized hotspots, which leads to tissue temperature elevation. The proposed CRHV-TX is configured with HV switches, operating in two separate phases: In the charging phase, the outer electrode and the inner electrode of the pMUT are connected to V_{HIGH} and ground, respectively. In the redistribution phase, the outer electrode and the inner electrode are shorted together [17]. The piezoelectric membrane returns to its initial position due to resilience and does not generate the acoustic wave. In the next charging phase, the outer electrode charges from the intermediate voltage

$$V_X = \frac{C_{\text{par,out}}}{C_{\text{par,out}} + C_{\text{par,in}}} V_{\text{HIGH}} \tag{3}$$

instead of full V_{HIGH} swing. For the conventional unipolar HV pulser, the required power P_{CONV} to drive the transducer is as follows:

$$P_{\text{CONV}} = fC_p V_{\text{HIGH}}^2 + fC_{\text{par,out}} V_{\text{HIGH}}^2. \tag{4}$$

On the other hand, the power consumption of the proposed charge-recycling pulser P_{PROP} can be described follows:

$$\begin{aligned} &P_{\text{PROP}} \\ &= fC_p V_{\text{HIGH}}^2 + \frac{1}{T}\int_0^T i(t) V_{\text{HIGH}} dt \\ &= fC_p V_{\text{HIGH}}^2 + \frac{V_{\text{HIGH}}}{T}[TfC_{\text{par,out}} V_{\text{HIGH}} - TfC_{\text{par,out}} V_X] \\ &= fC_p V_{\text{HIGH}}^2 + f\frac{C_{\text{par,out}} C_{\text{par,in}}}{C_{\text{par,out}} + C_{\text{par,in}}} V_{\text{HIGH}}^2 \end{aligned} \tag{5}$$

where T is the period and $i(t)$ is the current flows to charge $C_{\text{par,out}}$. As the voltage to charge the parasitic capacitors to the ground on both electrodes is halved, the total power consumption of the HV pulser can be decreased. In the measurement, the total power consumption of the CRHV-TX is reduced by 42.6% compared to conventional TX with a 1-cm external wire connection. As the proposed CRHV-TX reduces power wasted in charging parasitic capacitors, the further parasitic reduction from vertical integration can reduce the percentage of the TX power consumption.

As the pMUT suffers from the process variation in physical dimension and thickness, its acoustic pressure varies even with identical excitation voltage. Fig. 8 shows the histogram of the pulse-to-echo (P2E) maximum amplitudes of 36 pMUT channels under the same excitation voltage, 13.2 V_{PP}. The mean P2E maximum amplitude is 157.5 mV, and its standard deviation is 19.64 mV, corresponding to a relative standard deviation of 12.47%. As the non-uniformity of the acoustic pressure degrades the efficiency of BF and causes an increased level of side-lobes and image blurring [29], it is important to equalize the acoustic pressure of each pMUT. In the CRHV-TX, the calibration transistors M_1 and M_6 are used to control the pMUT excitation voltage at the channel level (see Fig. 9). The gate voltages of M_1 and M_6 are decided by the 3-bit DACs, and the DACs are controlled by SAR digital logic

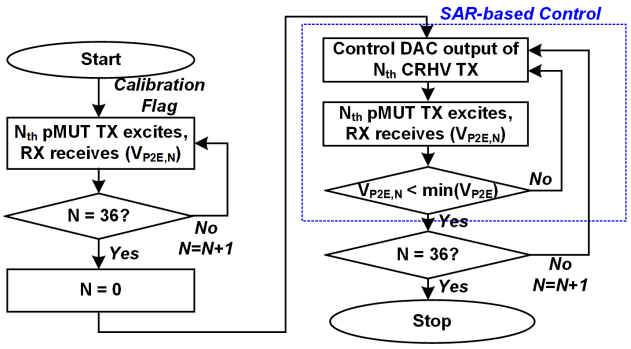


Fig. 9. pMUT acoustic pressure calibration algorithm.

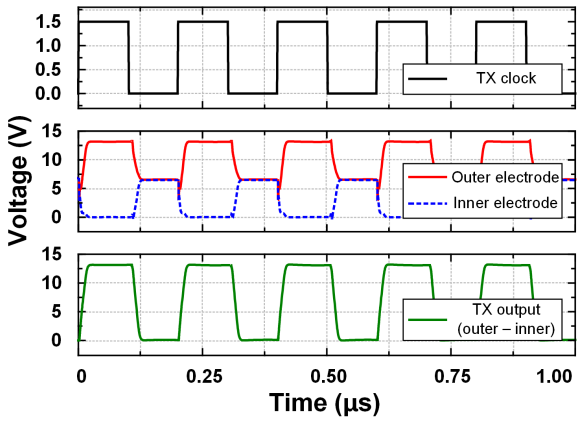


Fig. 10. Measured CRHV-TX output voltage.

automatically. If the calibration flag is transferred from an external controller, each CRHV-TX is ready to control the gate voltages of calibration transistors one by one. After placing a metal plate right above the pMUT matrix, the generated acoustic wave from the pMUT is directly reflected from the surface of the metal plate, and the RX receives the reflected echo. The received echo is digitized by an ADC and stored in the digital controller. This process is repeated 36 times for whole pMUT channels, and the controller calculates the minimum P2E amplitude among the 36 results. Then, for the pMUT channel whose P2E amplitude is larger than the minimum amplitude, the gate voltages are controlled by SAR logic until it reaches the nearest P2E amplitude. The change of gate voltages of M_1 and M_6 increases the drain voltages of M_1 and M_6, resulting in decreased TX excitation voltage. To control the current by the DAC, the calibration transistors are operating in the linear region. As a result, the maximum P2E amplitude of each pMUT channel, corresponding to the round-trip signal amplitude, is equalized.

To provide the scalability of the TX calibration, it is crucial to select the outliers among whole channels. As the TX acoustic pressure is equalized to the lowest element, the outliers whose generated TX pressure is too small can degrade the whole TX efficiency during the TX calibration. The controller decides whether the channel is dead or not based on the RX output signal. If the digitized RX output signal is too small, the algorithm regards the channel as dead.

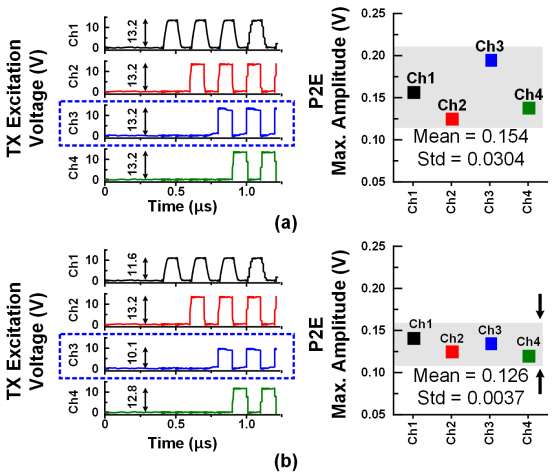


Fig. 11. pMUT acoustic pressure variation (a) without and (b) with the calibration.

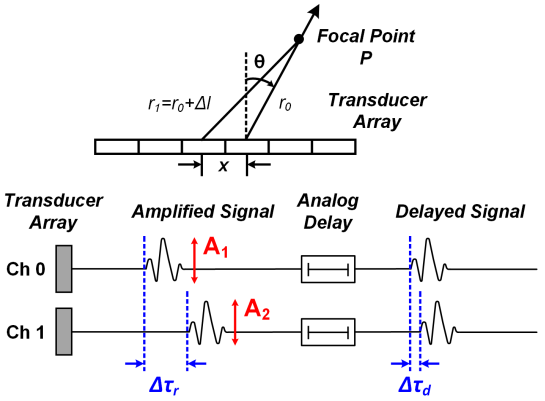


Fig. 12. Received signal similarity between the two adjacent channels.

Fig. 10 shows the measured CRHV-TX output while transmitting 5-MHz, 13.2-V_{PP} excitation voltage, which results in the generation of 0.2-MPa acoustic waves from the pMUT. The solid line and dashed line in the second sub-graph depict the output waveforms of the middle outer and inner electrodes of pMUT, respectively. The solid line in the third sub-graph represents the subtraction of the outer electrode from the inner electrode, corresponding to the transferred pulse in the aspect of the pMUT. In the charging phase, the output voltages of the outer electrode and the inner electrode are 13.2 and 0 V, resulting in the membrane deflection of the pMUT. In the charge redistribution phase, on the other hand, the inner electrode and the outer electrode are shorted together while relaxing the pMUT membrane. Fig. 11 shows the acoustic pressure calibration of the pMUT. In Fig. 11(a), the acoustic pressures of four-channel pMUTs vary under the same excitation voltage, 13.2 V_{PP}. The mean of P2E maximum amplitude is 154 mV, and its standard deviation is 30.4 mV. After calibration, the four-channel pMUTs are driven by 11.6-, 13.2-, 10.1-, and 12.8-V excitation voltages, respectively. As shown in Fig. 11(b), the standard variation is reduced to 3.7 mV, and the acoustic pressure of the pMUT matrix is equalized. In Fig. 11, channel 3 shows the drifting because of the leakage current. A resistor in parallel with the pMUT shunt capacitor is measured in the damaged pMUT channel. The resistor causes leakage current, resulting in loss of charge stored in the pMUT and parasitic capacitors $C_{par,out}$. The intermediate voltage at the charge redistribution phase decreases, and the efficiency of the charge redistribution reduces when leakage current occurs. Fig. 8 shows the P2E maximum amplitude change of the 36 pMUT channels before and after the calibration. Before the acoustic pressure calibration, the mean of P2E maximum amplitude is 154.5 mV, and its standard variation is 19.64 mV. After the calibration, the mean and standard variation is 111.9 and 6.10 mV, respectively. The generated acoustic pressure is decreased but equalized.

B. Dynamic Bit-Shared-ADC

The implementation of the ADC inside tight pixel is required to provide per-channel raw data accessibility without limiting the BF algorithm and be robust to analog noise corruption. The previous analog subarray BF or analog time-division multiplexing limits the applicable BF algorithms or reduces the imaging frame rate [10], [25]. However, the ADC is the most energy-hungry block among the transceiver blocks as the RX operating time in cardiac is 10–20 times longer than the TX excitation time [9]. To reduce the power consumption of the ADC, the adjacent channels can share the MSBs. When the transmitted beam is focused, the echo signals are received from one direction, and the received echoes have a high correlation as they penetrate similar medium circumstances. Fig. 12 shows the received signal similarity between two adjacent channels when the BF is adapted with focal point P. The fractional distance Δl between two adjacent channels can be expressed as follows:

$$\Delta l(t) = \sqrt{r(t)^2 + 2 \cdot r(t) \cdot x \cdot \sin(\theta) + x^2} - r(t) \tag{6}$$

where r_n is a distance of the channel n to the focal point P, θ is the angle of focusing, and x is a distance of the channel to the reference point. The fractional delay $\Delta\tau$ of the channel can be obtained from the fractional distance Δl and the acoustic speed c

$$\Delta\tau(t) = \frac{\Delta l(t)}{c}. \tag{7}$$

Therefore, the phase difference of the received echoes between two adjacent channels is $\Delta\tau_r = 2\Delta\tau$, where the prefactor 2 accounts for the return path. The amplitude difference is calculated by the fractional distance Δl and the signal attenuation based on (1). As two received echoes from adjacent channels have similar amplitudes with deterministic delay, the signal difference can be reduced after an analog delay that operates under a 200-MHz clock frequency. The analog-delay $\Delta\tau_d$ can be expressed as follows:

$$\Delta\tau_d(t) = \mathrm{mod}(\Delta\tau_r(t), t_d) \tag{8}$$

where t_d is an analog delay resolution, 5 ns, in the 200-MHz operating clock. The remaining delay after the analog-delay $\Delta\tau_d$ and the amplitude ratio of two inputs determines the signal similarity between two adjacent channels. The signal

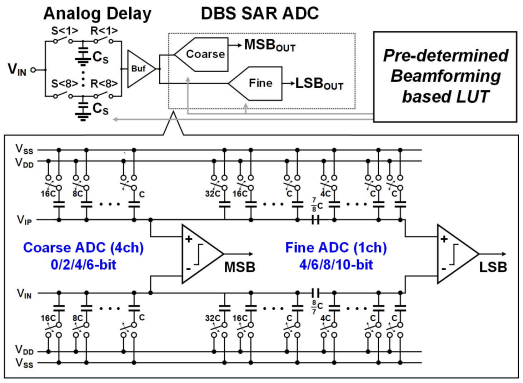


Fig. 13. Schematic of the DBS-ADC.

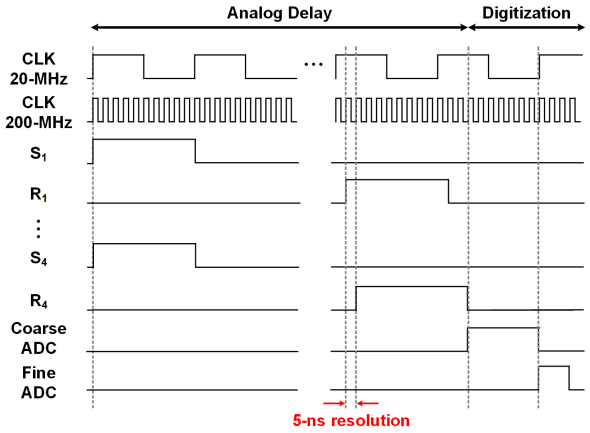


Fig. 14. Timing diagram of the DBS-ADC.

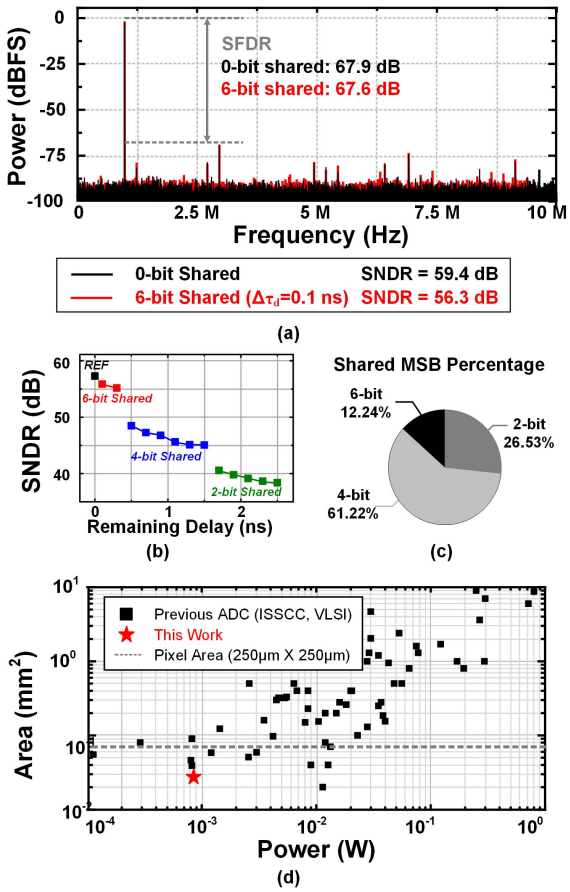


Fig. 15. (a) Measured output spectrum of the DBS-ADC with a 0.97-MHz input frequency. (b) Measured SNDR of the DBS-ADC regarding remaining delay $\Delta\tau_d$. (c) Percentage of the number of shared MSB in FoV 60°. (d) State-of-the-art comparison (area versus power) for ADC (bandwidth: 10–30 MHz; SNDR: 40∼70 dB).

difference between two adjacent channels $\Delta V_{\max}$ can be described as follows:

$$\Delta V_{\max} = \max\left(V_I \cdot A_{\text{AFE}}\left(\sin(2\pi f t) - \frac{\sin(2\pi f t + \Delta\tau_d)}{\alpha \times 2 \times \Delta l(t) \times f}\cdot\right)\right) \quad (9)$$

where V_I is an input signal voltage and A_{AFE} is the gain of the LNA and the PGA. Therefore, the sharable-bit between adjacent channels can be calculated by the ratio P of the voltage difference $\Delta V_{\max}$ to the amplified signal voltage V_{AFE} as follows:

$$\text{Sharable bit} = 2 \times \text{QUOTIENT}\left(\frac{\Delta V_{\max}}{\Delta_{\text{LSB}}}, 2\right) \quad (10)$$

where Δ_{LSB} is the step size of the LSB. For example, the phase difference between two adjacent channels is 90.9 ns, the amplitude ratio of two received signal is 0.984 when the transducer pitch x is 250 μm, the BF angle θ is 15°, the penetration depth is 50 mm, and its medium is biomedical soft tissue. The remaining delay $\Delta\tau_d$ is 0.91 ns, and the maximum voltage difference $\Delta V_{\max}$ is 49.1 mV with a full-swing input range. The ratio P is 0.016, and the sharable-bit between two adjacent channels is up to 4.9 bit among 10 bit.

Figs. 13 and 14 show the proposed DBS-ADC schematic and its timing diagram, respectively. The ADC is implemented

TABLE I
SNDR MEASUREMENT ENVIRONMENT EXAMPLE [SEE FIG. 15(B)]

Beamforming	Ratio P	Delay $\Delta\tau_d$	Shared Bit	SNDR
$\vartheta_l = 25°, \vartheta_e = 0°$	0.0252	1.74 ns	2	40.57 dB
$\vartheta_l = 14°, \vartheta_e = 0°$	0.0151	0.54 ns	4	48.49 dB
$\vartheta_l = 3°, \vartheta_e = 0°$	0.0044	0.1 ns	6	55.86 dB
			0 (Ref)	56.93 dB

with the differential structure to reduce the common-mode noise. A buffer is located between the analog delay cell and the coarse/fine ADC to drive the ADC. The coarse ADC is shared between four (2 × 2) adjacent channels to reduce power consumption. The fine ADC is implemented inside each channel to provide a per-channel digitized signal. The resolutions of the coarse ADC and the fine ADC can be selected among 0/2/4/6 and 10/8/6/4 bit, respectively. The number of sharable bits and the required delay time of the analog delay cells are determined by the look-up table (LUT) which stores pre-determined 49 BF points. When the input is received and amplified by the analog front-end (AFE), the signal is sampled and held by the analog delay cells with eight memory capacitors. The sampling switch $S_K\langle 1\text{–}8\rangle$ samples and holds the data with a 50-ns resolution. After the predetermined delay, the readout switch $R_K\langle 1\text{–}8\rangle$ of the analog

TABLE II
COMPARISON OF ULTRASOUND ADC

	[31] JSSC '17	[32] JSSC '18	[33] VLSI '19	This Paper	
				0-bit shared	6-bit shared, 0.1ns delay
ENOB	9.66 bit	8.31 bit	7.98 bit *	9.57 bit	9.06 bit
FOM_1	7.77×10^{11}	9.52×10^{9}	3.79×10^{9}	1.52×10^{10}	1.07×10^{10}
FOM_2	8.60×10^{-15}	1.63×10^{-13}	3.01×10^{-13}	8.09×10^{-14}	7.78×10^{-14}

* AFE included

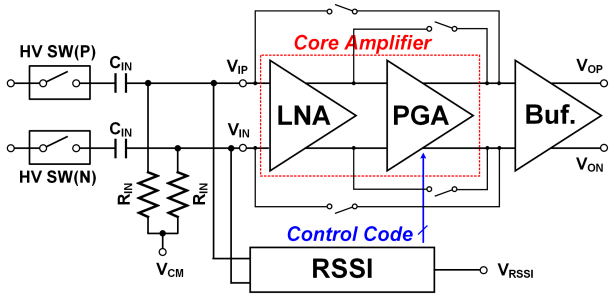


Fig. 16. Block diagram of the ultrasound receiver chain.

delay cells transfers the data to the coarse ADC with a 5-ns delay resolution. Since the readout switch operates with a 5-ns delay, the remaining delay $\Delta\tau_d$ is less than 5-ns, increasing the sharable bits between adjacent channels. The coarse ADC input is connected to the upper-left channel, and the digitized MSBs are used to determine the switch polarity of the four fine ADCs. The offset variation of the comparator degrades the ADC performance. As four channels share one coarse ADC, the offset difference in fine ADCs can degrade the SNDR of each channel and cause the nonuniformity of the SNDR.

Fig. 15(a) shows the measured output spectrum of the DBS-ADC when 0-bit MSB is shared and 6-bit MSBs are shared with 0.1-ns remaining delay $\Delta\tau_d$ (lateral BF angle: 3° and elevation BF angle: 0°). The input signal is a 0.97-MHz sinusoidal test input. The DBS-ADC achieves the peak SNDR of 59.4 dB and the SFDR. Fig. 15(b) illustrates the SNDR degradation with MSB sharing. The SNDR of DBS-ADC under the same shared bit can differ according to the remaining delay $\Delta\tau_d$. As remaining delay increases, the signal similarity between channels decreases; the sharable bit of DBS-ADC decreases. The remaining delay between adjacent channels can cause signal clipping, resulting in the SNDR degradation of the ADC. As the focal point approaches the edge of the FoV, the sharable bit of the DBS-ADC decreases. Consequently, the SNDR of the DBS-ADC decreases. The detailed examples of measurement environments of Fig. 15(b) are described in Table I. Fig. 15(c) shows the percentage of shared MSBs of the proposed DBS-ADC. The 61.22% of the precalculated BF points share 4-bit MSBs, and the sharing of the 2- and 6-bit MSBs occupies 26.53% and 12.24%, respectively. The comparison with similar BW and SNDR [30] is shown in Fig. 15(d), where the dashed line depicts a target pixel area of 250 × 250 μm^2. The SAR-based DBS-ADC occupies 0.026 mm^2, which is smaller than the target pixel area while consuming a minimum of 0.83 mW/channel. The ADC without bit-sharing consumes 1.23 mW. On the other hand, the ADC with 2-, 4-, and 6-bit sharings consumes 1.12, 0.98, and 0.83 mW, respectively. With a 60° FoV, the average power consumption of the DBS-ADC is 1 mW; therefore, an average 18.7% of the ADC power consumption is reduced with a 60° FoV. Table II illustrates the comparison between the DBS-ADC and the state-of-the-art ultrasound ADC. This work shows similar ENOB and FOM compared to previous works.

C. RSSI Adaptive Gain Control Front End

Fig. 16 shows the block diagram of the receiver chain. The main path of the ultrasound receiver consists of an LNA and a PGA, with the PGA transferring its output to the analog delay cell through the buffer. To provide a large DR, the LNA and the PGA can be bypassed by the switches that are controlled by a digital controller. Conventionally, the gain of the PGA is controlled by time, as the signal attenuation can be calculated by received time and the acoustic attenuation ratio in the deterministic medium. However, the medium of surgical ultrasound imaging is heterogeneous, which is hard to assume the acoustic property. The acoustic attenuation varies greatly depending on the tissue, where the attenuation rate of blood, bone, cardiac, connective tissue, and muscle is 0.20, 9.94, 0.52, 1.57, and 1.09 dB/cm/MHz, respectively [34]. Instead of using pre-determined time-based gain control, an RSSI-AGC changes its gain adaptively based on input signal strength in real time. The output of the RSSI compares with threshold voltages and generates digital codes to control the gain of the PGA. A certain change of echogenicity can change the PGA gain control, resulting in brightness change in ultrasound imaging, which is undesirable. To prevent the brightness change, the gain code of the PGA updates only one step at a time. Also, the gain control code of each channel is stored and transmitted to the external imaging device to avoid loss of amplitude information.

The schematic diagrams of the LNA and the PGA are shown in Fig. 17(a) and (b), respectively. As the area is constrained, the open-loop topology has been used to reduce the occupying area. The gain of the PGA is controlled by four steps, and a 2-bit digital code generated by the RSSI changes the switching polarity of the G_m-cell. As the pMUT process variation also affects its receiving sensitivity, the currents of the LNA and the PGA are programmable to compensate manually. The measured input-referred voltage noise density at the highest AFE gain setting is 19.3 nV/$\sqrt{}$Hz, which is less than

TABLE III
COMPARISON OF THE STATE-OF-THE-ART ULTRASOUND ASIC

	[10] JSSC '18	[25] ISSCC '18	[17] ASSCC '16	[31] JSSC '17	[32] JSSC '18	[36] TBCAS '14	[33] VLSI '19	**This Work**
Process	180 nm	180 nm HV	65 nm	28 nm	180 nm	130 nm	180 nm	**180 nm**
Transducer	2D PZT	PZT / cMUT	pMUT	2D cMUT	2D PZT	2D cMUT	2D PZT	**2D pMUT**
Center Frequency	5 MHz	7 MHz	0.1-5 MHz	5 MHz	5 MHz	3 MHz	5 MHz	**5 MHz**
In-Pixel Design	Yes (150-μm)	No	No	Yes (250-μm)	Yes (150-μm)	No	Yes (150-μm)	**Yes * (250-μm)**
TX/RX per Ch.	RX	TX / RX	TX / RX	RX	RX	RX	RX	**TX / RX**
ADC per Ch.	X (1ADC/4Ch.)	X	X	O	O	X	O	**O**
ADC Architecture	SAR	-	-	ΔΣ	ΔΣ	-	SAR+SSS	**SAR**
Area / ch.	0.025 mm^2	0.45 mm^2	0.13 mm^2	0.0625 mm^2	0.025 mm^2	0.303 mm^2	0.023 mm^2	**0.0625 mm^2**
On-Chip Calib.	No	No	Yes	No	No	No	No	**Yes** **
Max. TX Voltage	-	60 V	6 V	-	-	-	-	**13.2 V**
SNR/channel	51.8 dB	N/A	N/A	58.9 dB ***	47 dB	N/A	49.8 dB	**57.9 dB (0-bit shared)** ****
								54.6 dB (6-bit shared) ****
TX Power/ch.	-	N/A	N/A	-	-	-	-	**2.02 mW (5 V_{PP})**
								12.8 mW (13.2 V_{PP})
RX Power/ch.	0.91 mW [1]	N/A	N/A	17.5 mW	0.80 mW	17.81 mW	1.54 mW	**0.95 mW** *****, [2]
TRX BF	RX	TX	TX	RX	-	RX	RX	**TX / RX**

* Out-of-pixel connection.
** On-chip calibration is necessary because of pMUT usage
*** ADC only, excluding the analog front-end.
**** 52-dB PGA gain setting, 5-MHz signal, 0.1ns residual delay $\Delta\tau_d$
***** Sharing 6-bit MSBs between adjacent channels.
[1] 6.3 nV/√Hz input-referred noise density @ 5-MHz
[2] 19.3 nV/√Hz input-referred noise density @ 5-MHz

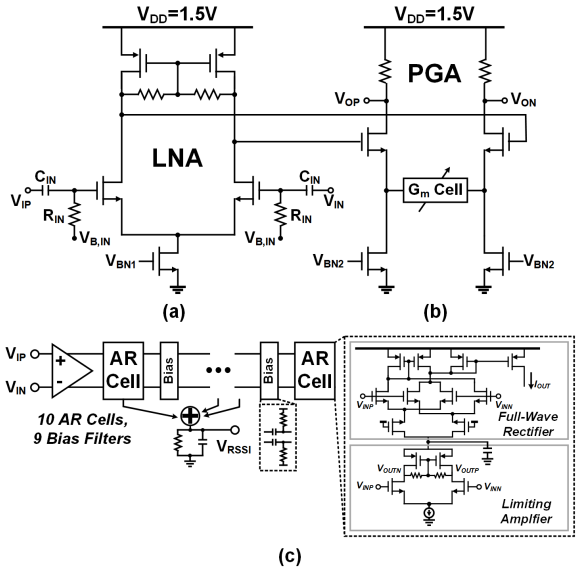


Fig. 17. Schematic of (a) LNA, (b) PGA, and (c) RSSI.

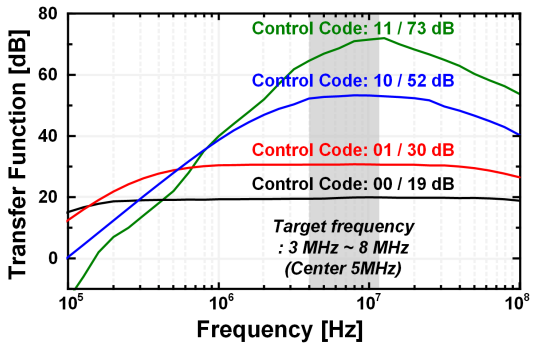


Fig. 18. Measured receiver transfer function at four gain settings.

the target DR of 91 dB. Due to power and area restrictions, the noise of the RX path was not optimized. The main contribution of the noise is the LNA as the size of the input transistors and the current of the LNA are insufficient; On the other hand, the size of the HV TX/RX switch is large to reduce the ON-resistance of the switch, and the gain of the PGA is large. Fig. 17(c) shows the schematic of the RSSI [35]. The RSSI is composed of ten amplifier-rectifier (AR) cells that utilize charge-reusing techniques to reduce power consumption, nine bias filters, a current summer, and a ripple reduction filter. The corner frequency of the ripple reduction filter decides the ripple amplitude and the delay. The delay time of the RSSI is set to 0.7 μs, and the hysteresis is adapted in the design of the comparator to avoid a frequent change in gain due to the ripple. Because of the delay time of the RSSI-AGC, the RSSI-AGC cannot change its gain within one echo but changes between the echoes. The gain of the further echoes is determined by the previous echo. Therefore, if the reflector distance is too long, the gain of the RSSI-AGC can be insufficient to amplify the next echoes. The input of the RSSI is connected to the closest lower-right pMUT electrodes, and the output of RSSI is quantized by four comparators. The gain of the closest pixel is controlled by the output of the RSSI directly. On the other hand, the gain of other pixels is decided by the delayed RSSI output, and the delay is pre-determined according to the pixel location.

Fig. 18 shows the measured receiver transfer function at four gain settings (19/30/52/73 dB), with an overall mid-band gain range of 54 dB that satisfies the design parameter explained in Section II-D. Because of the power and area restriction, the worst AFE bandwidth with 73 dB gain is up

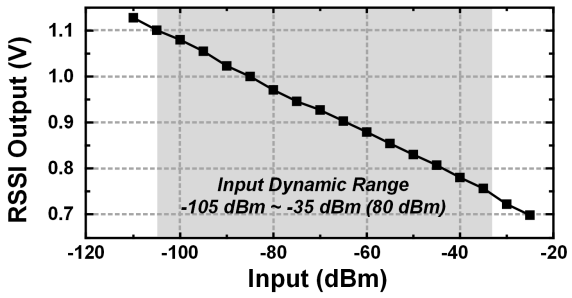


Fig. 19. RSSI output voltage versus the input power.

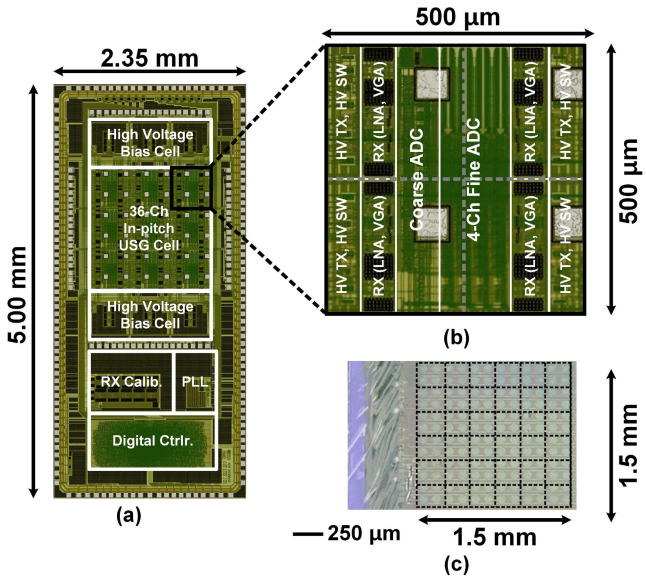


Fig. 20. Microphotograph of (a) ASIC, (b) four TRX channels, and (c) pMUT matrix.

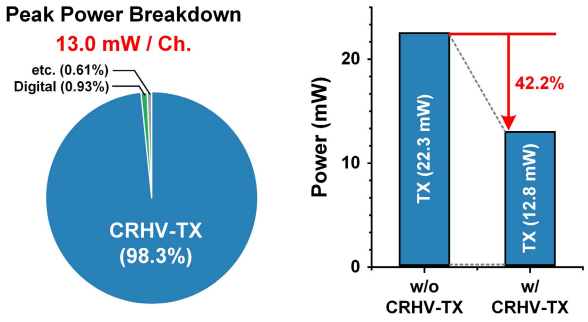


Fig. 21. Peak power breakdown of one channel.

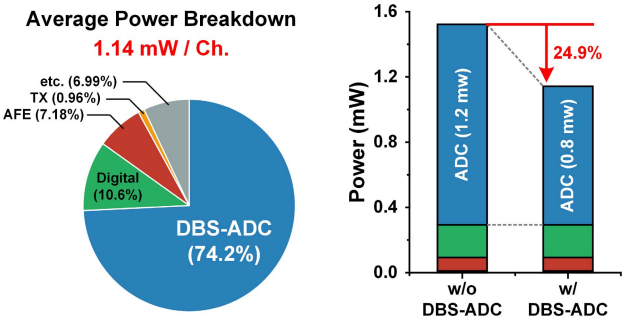


Fig. 22. Average power breakdown of one channel.

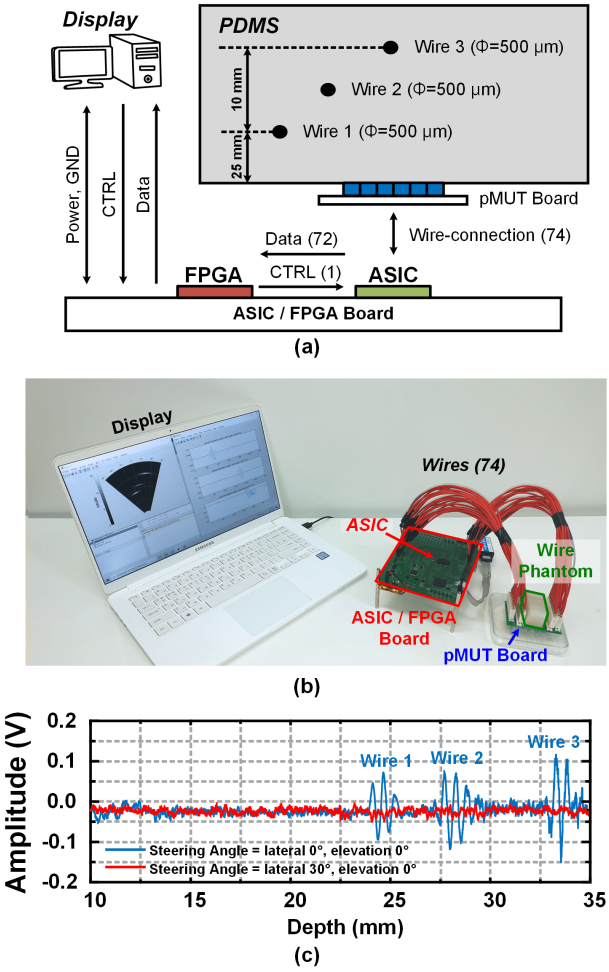


Fig. 23. (a) B-mode imaging P2E measurement setup. (b) Photograph of the B-mode imaging measurement setup. (c) Received echo signal with a different angle in the lateral direction.

to 13 MHz, which results in noise folding. The RSSI output is plotted (see Fig. 19) where the RSSI output range is set from 0.70 to 1.12 V. The received signal sensitivity was measured from −110 to −25 dBm. Its linearized input DR is −105 to −35 dBm. As the RSSI measures the input signal on a logarithmic scale, its DR is enough to measure the input signal of the ultrasound.

D. Measurement and Implementation Results

The 6 × 6 ultrasound transceiver ASIC is integrated into 0.18-μm 1P6M standard CMOS process while occupying an area of 2.35 × 5 mm^2. Fig. 20 shows the ASIC micrograph, including the detailed photo of the 2 × 2 subarray transceivers and the microphotograph of the pMUT matrix. The area of each channel is 0.0625 mm^2. The CRHV-TX and the TX/RX switch are occupying 0.02 mm^2, 32% of a channel area. Also, the area of the ADC and the AFE is 0.026 mm^2 (41%) and 0.017 mm^2 (27%), respectively. Each channel is connected to the pMUT with two terminals. One terminal was integrated above the channel. The other terminal is routed to a separate pad located in the ASIC pad ring because the required bonding

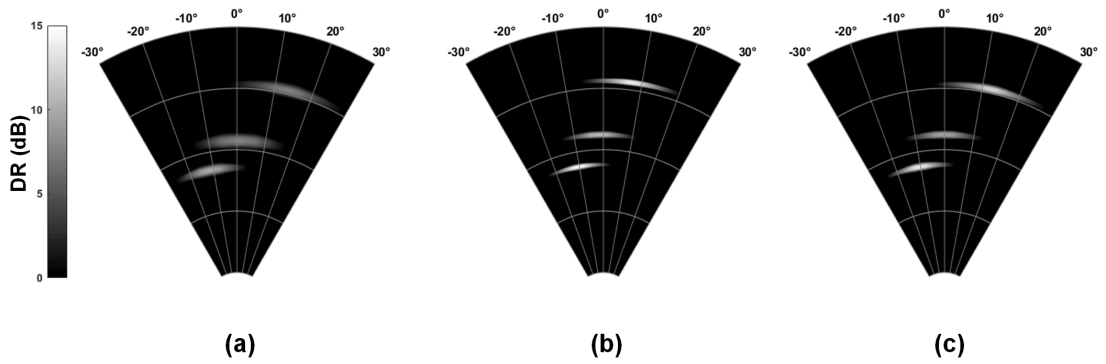


Fig. 24. Reconstructed B-mode images that measured (a) without TX calibration and DBS-ADC, (b) with TX calibration and without DBS-ADC, and (c) with TX calibration and DBS-ADC.

distance for the vertical integration restricts the number of pads in the channel. In case of a unimorph pMUT, a pad inside the channel can be connected to the pMUT with vertical integration, and the routed pads are connected altogether. On the other hand, a die-to-die connection between ASIC-pMUT through routed pads can be utilized for bimorph pMUT. As a bimorph connection requires outer routing pads, the ASIC array is hard to provide further scalability. However, this article aims to open the door for further development and the development of the vertical implementation can solve the limitation of the outer bonding.

Table III illustrates the comparison of this article with the state-of-the-art ultrasound ASIC for 3-D ultrasound imaging systems. Based on Table III, this is the first work to propose an in-pixel channel that integrates all TX, RX, and ADC. While driving, the CRHV-TX consumes 2.02 and 12.8 mW when its excitation voltage is 5 and 13.2 V_{PP}, respectively. The power consumption of the CRHV-TX is less than 13.9 mW to satisfy the peak power consumption restriction. Also, the CRHV-TX supports per-channel calibration, and it is compatible with the 180-nm standard CMOS process. While receiving, the RX with an in-pixel ADC consumes 0.93 mW, which is similar power with the previous four-channel shared ADC [10]. The obtained RX SNR is 57.9 and 54.6 dB when the DBS-ADC shares 0- and 6-bit MSBs, respectively.

Figs. 21 and 22 show the peak power breakdown and the average power breakdown of a channel, respectively. The peak power breakdown is measured when a CRHV-TX insonifies 13.2-V_{PP} pulse and an RX sleeps; 98.4% of the peak power consumption is dissipated by CRHV-TX. Due to CRHV-TX, 42.2% of the peak power consumption is reduced. The average power breakdown is measured when TX insonifies 13.2-V_{PP} pulse and DBS-ADC shares 6-bit MSBs between four adjacent channels. The pulse repetition frequency (PRF) is 1 kHz, and the number of TX cycles per pulse is 3. Unlike the peak power consumption (dominated by TX), the RX including the AFE and the ADC consumes 81.3% of the total average power as the RX operating time is much longer than the TX; due to DBS-ADC, 24.9% of the average power consumption is reduced. As the TX operating duration is much shorter, the power reduction of the TX is not the dominant factor for the overall power consumption; nevertheless, the TX power reduction increases as the PRF, and the number of TX cycle pulses increases.

TABLE IV
MEASURED IMAGE PERFORMANCE OF FIG. 24

	Fig. 24 (a)	Fig. 24 (b)	Fig. 24 (c)
Normalized Dynamic Range	8.73 dB	13.3 dB	12.2 dB
Angular resolution	16.3°	13.7°	14.8°
Lateral resolution	1.27 mm	0.57 mm	0.83 mm

The functionality of the full chip has been evaluated with b-mode imaging of the three-wire phantom [see Fig. 23(a) and (b)]. The phantom is constructed with polydimethylsiloxane (PDMS) that is an elastomeric polymer widely used for biomedical sciences. Three wires with a diameter of 500 μm are inserted inside PDMS, and the wires are located 25, 28, and 35 mm above the bottom, respectively. The pMUT matrix is placed below the PDMS, and the pMUT matrix is connected to the ASIC board by the 74 external wires (72 wires for the bimorph pMUTs, two wires for the ground). The acoustic waves are transmitted from the 36-channel 5-MHz pMUTs using 5-V_{PP} excitation voltage. The PRF is 1 kHz, and the number of TX cycles per pulse is 3. The P2E signals are recorded at $-30°$ to $+30°$ BF steering angle with 1° spacing. The RSSI-AGC is enabled, and the sharable bit of the DBS-ADC is determined according to the LUT. The digitized signals are transferred to the field-programmable gate array (FPGA) by 72 wires. The FPGA data are transferred to the external imaging device. The standard delay-and-sum (DAS) algorithm is used to perform BF in this measurement.

Fig. 23(c) shows the received digital outputs of the channel with different angles in the lateral direction. The recorded data show clear echo signals when the beam is steered toward the wire, whereas no echo signal appears when the beam is steered out of the wire. Even though the worst AFE bandwidth is less than the Nyquist frequency, the third wire, which is measured with a 73-dB gain, is still clearly distinguishable. Finally, Fig. 24 illustrates three reconstructed B-mode images in the lateral direction with different conditions, and Table IV describes the measured performance of Fig. 24. As shown in

Fig. 24(a), the reconstructed image without TX calibration is less focused and more blurred compared to Fig. 24(b). By utilizing the TX calibration, the image resolution and DR are significantly improved. Fig. 24(c) shows the effectiveness of the DBS-ADC. The number of shared bits in Fig. 24(c) is angle-dependent and predetermined by LUT. The measured DR and the resolution are comparable with Fig. 24(b) while reducing power consumption.

IV. Conclusion

In this article, an ultrasound ASIC with a 6 × 6 pMUT matrices has been designed and implemented for a miniaturized 3-D ultrasound system. The proposed ASIC successfully demonstrates the proof-of-concept, an in-pixel TRX channel with the ADC. The proposed CRHV-TX recycles the charge to improve the power efficiency while supporting the calibration of TX acoustic variation in standard CMOS. The DBS-ADC shares coarse ADC with adjacent four channels, in which the number of MSB varies based on BF angle. The gain of the RSSI-AGC is adaptively controlled by input signal strength in real time. The peak power consumption of the TX is 12.8 mW/channel while exciting 13.2-V_{PP} TX pulse, which is reduced by 42.2%. The average power consumption of the ASIC is 1.14 mW with 1-kHz PRF and three pulses per cycle. Both peak and average power consumptions satisfy the power regulation of the 3-D ultrasound system of 13.9 mW/channel. The proposed ASIC occupies 11.75 mm^2 in 180-nm standard CMOS technology and is incorporated with 6 × 6 pMUT arrays. The ASIC demonstrates state-of-the-art power efficiency and integration level and has been successfully applied in an imaging experiment.

Acknowledgment

The authors acknowledge Dr. Judyta B. Tillak for her technical comments.

References

[1] A. L. Kelin *et al.*, "Use of transesophageal echocardiography to guide cardioversion in patients with atrial fibrillation," *New England J. Med.*, vol. 344, no. 19, pp. 1411–1420, May 2001.

[2] D. Wildes *et al.*, "4-D ICE: A 2-D array transducer with integrated ASIC in a 10-fr catheter for real-time 3-D intracardiac echocardiography," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 63, no. 12, pp. 2159–2173, Dec. 2016.

[3] G. Gurun *et al.*, "Single-chip CMUT-on-CMOS front-end system for real-time volumetric IVUS and ICE imaging," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 61, no. 2, pp. 239–250, Feb. 2014.

[4] C. Chen *et al.*, "A prototype PZT matrix transducer with low-power integrated receive ASIC for 3-D transesophageal echocardiography," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 63, no. 1, pp. 47–59, Jan. 2016.

[5] *Guidance for Industry and FDA Staff Information for Manufacturers Seeking Marketing Clearance of Diagnostic Ultrasound Systems and Transducers*, Food Drug Admin., Washington, DC, USA, Sep. 2008. Accessed: Dec. 25, 2016.

[6] J. H. Park, J. S. Y. Tan, H. Wu, and J. Yoo, "34.2 1225-channel localized temperature-regulated neuromorphic retinal-prosthesis SoC with 56.3 nW/channel image processor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2020, pp. 508–509.

[7] J. H. Park, J. S. Y. Tan, H. Wu, Y. Dong, and J. Yoo, "1225-channel neuromorphic retinal-prosthesis SoC with localized temperature-regulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 6, pp. 1230–1240, Dec. 2020.

[8] Y. Igarashi *et al.*, "Single-chip 3072-element-channel transceiver/128-subarray-channel 2-D array IC with analog RX and all-digital TX beamformer for echocardiography," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2555–2567, Sep. 2019.

[9] C. Chen *et al.*, "A front-end ASIC with receive sub-array beamforming integrated with a 32×32 PZT matrix transducer for 3-D transesophageal echocardiography," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 994–1006, Apr. 2017.

[10] C. Chen *et al.*, "A pitch-matched front-end ASIC with integrated subarray beamforming ADC for miniature 3-D ultrasound probes," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3050–3064, Nov. 2018.

[11] A. Bhuyan *et al.*, "3D volumetric ultrasound imaging with a 32×32 CMUT array integrated with front-end ICs using flip-chip bonding technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2013, pp. 396–397.

[12] S. Akhbari, F. Sammoura, B. Eovino, C. Yang, and L. Lin, "Bimorph piezoelectric micromachined ultrasonic transducers," *J. Microelectromech. Syst.*, vol. 25, no. 2, pp. 326–336, Apr. 2016, doi: 10.1109/JMEMS.2016.2516510.

[13] G. G. Yaralioglu, A. S. Ergun, B. Bayram, E. Haeggstrom, and B. T. Khuri-Yakub, "Calculation and measurement of electromechanical coupling coefficient of capacitive micromachined ultrasonic transducers," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 50, no. 4, pp. 449–456, Apr. 2003.

[14] J. Tillak and J. Yoo, "A 23 μW digitally controlled pMUT interface circuit for Doppler ultrasound imaging," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Lisbon, Portugal, May 2015, pp. 1618–1621.

[15] J. Lee *et al.*, "A 5.37 mW/channel pitch-matched ultrasound ASIC with dynamic-bit-shared SAR ADC and 13.2 V charge-recycling TX in standard CMOS for intracardiac echocardiography," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2019, pp. 190–192.

[16] P. Favrat, P. Deval, and M. J. Declercq, "A high-efficiency CMOS voltage doubler," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 410–416, Mar. 1998.

[17] J. Tillak, S. Akhbari, N. Shah, L. Radakovic, L. Lin, and J. Yoo, "A 2.34 μJ/scan acoustic power scalable charge-redistribution pMUT interface system with on-chip aberration compensation for portable ultrasonic applications," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Toyama, Japan, Nov. 2016, pp. 189–192.

[18] B. E. Eovino *et al.*, "Broadband ring-shaped PMUTS based on an acoustically induced resonance," in *Proc. IEEE Int. Conf. Micro Electro Mech. Syst. (MEMS)*, Las Vegas, NV, USA, Jan. 2017, pp. 1184–1187.

[19] K. Smyth and S.-G. Kim, "Experiment and simulation validated analytical equivalent circuit model for piezoelectric micromachined ultrasonic transducers," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 62, no. 4, pp. 744–765, Apr. 2015.

[20] A. Banuaji and H.-K. Cha, "A 15-V bidirectional ultrasound interface analog front-end IC for medical imaging using standard CMOS technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 8, pp. 604–608, Aug. 2014.

[21] S. Wilhelm, *Ultrasonography in Vascular Diagnosis: A Theory-Oriented Textbook and Atlas*, 2nd ed. Berlin, Germany: Springer-Verlag, 2011.

[22] H. B. Meire, *Basic Ultrasound*. Hoboken, NJ, USA: Wiley, 1995.

[23] T.-C. Cheng and T.-H. Tsai, "CMOS ultrasonic receiver with on-chip analog-to-digital front end for high-resolution ultrasound imaging systems," *IEEE Sensors J.*, vol. 16, no. 20, pp. 7454–7463, Oct. 2016.

[24] I. Kim *et al.*, "CMOS ultrasound transceiver chip for high-resolution ultrasonic imaging systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 5, pp. 293–303, Oct. 2009.

[25] G. Jung *et al.*, "Single-chip reduced-wire active catheter system with programmable transmit beamforming and receive time-division multiplexing for intracardiac echocardiography," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 188–190.

[26] H.-K. Cha, D. Zhao, J. H. Cheong, B. Guo, H. Yu, and M. Je, "A CMOS high-voltage transmitter IC for ultrasound medical imaging applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 6, pp. 316–320, Jun. 2013.

[27] *High-Voltage Protection T/R Switch With Clamp Diodes, MD0101 Datasheet*, Microchip, Chandler, AZ, USA, Feb. 2020.

[28] K. Chen, H.-S. Lee, and C. G. Sodini, "A column-row-parallel ASIC architecture for 3-D portable medical ultrasonic imaging," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 738–751, Mar. 2016.

[29] P. Castellini *et al.*, "Acoustic beamforming: Analysis of uncertainty and metrological performances," *Mech. Syst. Signal Process.*, vol. 22, no. 3, pp. 738–751, Apr. 2008.

[30] B. Murmann, "ADC performance survey 1997–2020," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers VLSI Symp.* Accessed: Aug. 2, 2020. [Online]. Available: https://web.stanford.edu/~murmann/adcsurvey.html

[31] M.-C. Chen *et al.*, "A pixel pitch-matched ultrasound receiver for 3-D photoacoustic imaging with integrated delta-sigma beamformer in 28-nm UTBB FD-SOI," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2843–2856, Nov. 2017.

[32] M. D'Urbino *et al.*, "An element-matched electromechanical $\Delta\Sigma$ ADC for ultrasound imaging," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2795–2805, Oct. 2018.

[33] J. Li *et al.*, "A 1.54 mW/element 150μm-pitch-matched receiver ASIC with element-level SAR/shared-single-slope hybrid ADCs for miniature 3D ultrasound probes," in *Proc. Symp. VLSI Circuits*, Kyoto, Japan, Jun. 2019, pp. 220–221.

[34] M. O. Culjat, D. Goldenberg, P. Tewari, and R. S. Singh, "A review of tissue substitutes for ultrasound imaging," *Ultrasound Med. Biol.*, vol. 36, no. 6, pp. 861–873, Jun. 2010.

[35] J. Jang *et al.*, "A 540-μW duty controlled RSSI with current reusing technique for human body communication," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 4, pp. 893–901, Aug. 2016.

[36] J.-Y. Um *et al.*, "An analog-digital hybrid RX beamformer chip with non-uniform sampling for ultrasound medical imaging with 2D CMUT array," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 6, pp. 799–809, Dec. 2014.

Jihee Lee (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2015, 2017, and 2020, respectively.

She is currently a Staff Engineering with the Advanced Sensor Development Team, Samsung Electronics, Hwaseong, South Korea. She has worked on developing a low-power sensor front end. Her current research interest includes the design of a miniaturized ultrasound sensor system.

Kyoung-Rog Lee (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2015 and 2017, respectively, where he is currently pursuing the Ph.D. degree.

His current research interests include low-power biomedical SoC for wearable healthcare systems. He is also interested in low-power sigma–delta analog-to-digital converter (ADC), successive-approximation-register (SAR) ADC circuits, mixed-mode signal processing, and non-volatile memory circuit for biomedical systems.

Benjamin E. Eovino received the B.S. degree in mechanical engineering from the University of California at Santa Barbara, Santa Barbara, CA, USA, in 2013, and the M.S. degree in electrical engineering and the Ph.D. degree in mechanical engineering from the University of California at Berkeley, Berkeley, in 2015 and 2018, respectively.

He is currently with Chirp Microsystems, Berkeley. His graduate work focuses on the design and modeling of high-performance piezoelectric micromachined ultrasonic transducers. His research interests include the development of microelectromechanical systems (MEMS) for consumer devices and medical applications.

Jeong Hoan Park (Member, IEEE) received the B.S. and Ph.D. degrees from the School of Electrical Engineering and Computer Science, Seoul National University, Seoul, South Korea, in 2011 and 2017, respectively.

He has held a research fellow position with the Electrical and Computer Engineering Department, National University of Singapore, Singapore, from 2017 to 2020. He is currently a Staff Engineer with the DRAM Design Team, Samsung Electronics, Hwaseong, South Korea. His main research topic is developing low-power and low-noise multichannel bio-signal acquisition and the neural prosthesis with neuromorphic processing SoC. He is also interested in high bandwidth memory (HBM).

Luna Yue Liang received the B.S. and M.S. degrees in mechanical engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2015 and 2016, respectively, and the Ph.D. degree from the Department of Mechanical Engineering, University of California at Berkeley, Berkeley, CA, USA, in 2020.

She is now with Apple Inc., Shenzhen, Guangdong, China. Her research interests include developing new architectures of PMUTs with higher electro-mechano-acoustical energy efficiency and increased sensitivity while using CMOS-compatible fabrication technology, making them suitable for battery-powered handheld devices.

Liwei Lin (Member, IEEE) received the B.S. degree from the Power Mechanical Engineering Department, National Tsing Hua University, Hsinchu, Taiwan, in 1986, and the M.S. and Ph.D. degrees from the Mechanical Engineering Department, University of California at Berkeley (UC Berkeley), Berkeley, CA, USA, in 1991 and 1993, respectively, all in mechanical engineering.

He is currently the James Marshall Wells Professor with the Department of Mechanical Engineering and the Co-Director of the Berkeley Sensor and Actuator Center, UC Berkeley. He has authored/coauthored more than 300 journal articles. His research interests include microelectromechanical systems (MEMS), nanoelectromechanical systems, nanotechnology, design and manufacturing of microsensors and microactuators, the development of micromachining processes by silicon surface/bulk micromachining, micromolding process, and mechanical issues in MEMS, such as heat transfer, solid/fluid mechanics, and dynamics.

Dr. Lin is a fellow of American Society of Mechanical Engineering (ASME) and a Subject Editor of the IEEE JOURNAL OF MICROELECTROMECHANICAL SYSTEMS.

Hoi-Jun Yoo (Fellow, IEEE) was the VCSEL Pioneer with Bell Communications Research, Red Bank, NJ, USA, and the Manager of the DRAM Design Group, Hyundai Electronics, Icheon, South Korea, during the era of 1M DRAM up to 256M SDRAM. From 2003 to 2005, he has served as the full-time Advisor to the Minister of the Korean Ministry of Information and Communication for SoC and Next Generation Computing. He is currently an ICT Chair Professor with the School of Electrical Engineering and the Director of the System Design Innovation and Application Research Center (SDIA), Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea. He has published more than 400 articles, wrote or edited five books: *DRAM Design* (Hongneung, 1997), *High Performance DRAM* (Hongneung, 1999), *Low Power NoC for High Performance SoC Design* (CRC, 2008), *Mobile 3D Graphics SoC* (Wiley, 2010), and *Bio-Medical CMOS ICs* (co-editing with Chris Van Hoof, Springer, 2010), and co-written chapters in numerous books. His current research interests include bio-inspired artificial intelligence (AI) chip design, multicore AI SoC design, including deep neural network (DNN) accelerators, wearable healthcare systems, network-on-chip, and high-speed low-power memory.

Dr. Yoo is an Executive Committee Member of the Symposium on VLSI and a Steering Committee Member of the Asian Solid-State Circuit Conference (A-SSCC), for which he was nominated as the Steering Committee Chair for the term 2020–2025. He received the Order of Service Merit from the Korean Government in 2011 for his contributions to the Korean Memory Industry, the Scientist/Engineer of the Month Award from the Ministry of Education, Science and Technology of Korea in 2010, and the Kyung-Am Scholar Award in 2014. He also received the Electronic Industrial Association of Korea Award for his contributions to the DRAM technology in 1994, the Hynix Development Award in 1995, the Korea Semiconductor Industry Association Award in 2002, the Best Research of KAIST Award in 2007, the Excellent Scholar of KAIST Award in 2011, and the Best Scholar of KAIST Award in 2019. He was a co-recipient of the ASP-DAC Design Award in 2001, the A-SSCC Outstanding Design Awards in 2005–2007, 2010, 2011, and 2014, the ISSCC/DAC Student Design Contest Awards in 2007, 2008, 2010, and 2011, the ISSCC Demonstration Session Recognition in 2016, 2017, and 2019, and the Best Paper Awards of the IEEE Artificial Intelligence Circuits and Systems (AI-CAS) in 2019. He was the TPC Chair of the 2015 IEEE International Solid-State Circuits Conference (ISSCC), a Plenary Speaker of the ISSCC 2019 entitled Intelligence on Silicon: From Deep Neural Network Accelerators to Brain-Mimicking AI-SoCs, and the Chair of Technology Direction (TD) Subcommittee of the ISSCC 2013. He has served as an Executive Committee Member of the ISSCC, the IEEE SSCS Distinguished Lecturer from 2010 to 2011, and the TPC Chair of the International Symposium on Wearable Computers (ISWC) 2010 and the A-SSCC 2008. He was the Editor-In-Chief (EIC) of the *Journal of Semiconductor Technology and Science* (JSTS) published by the Korean Institute of Electronics and Information Engineers from 2015 to 2019 and a Guest Editor of the IEEE JSSC and the TRANSACTION ON BIOMEDICAL CIRCUIT AND SYSTEM (TBioCAS). He is also an Associate Editor of the IEEE JSSC and the SOLID-STATE CIRCUIT LETTER (SSC-L).

Jerald Yoo (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2002, 2007, and 2010, respectively.

From 2010 to 2016, he was with the Department of Electrical Engineering and Computer Science, Masdar Institute of Science and Technology (now Khalifa University), Abu Dhabi, United Arab Emirates, where he was an Associate Professor. From 2010 to 2011, he was also a Visiting Scholar with the Microsystems Technology Laboratories (MTL), Massachusetts Institute of Technology (MIT), Cambridge, MA, USA. Since 2017, he has been with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, and also with The N.1 Institute for Health, Singapore, where he is currently an Associate Professor. He has pioneered research on low-energy body-area-network (BAN) for communication/powering and wearable body sensor networks using the planar-fashionable circuit board for a continuous health monitoring system. He has authored book chapters in *Biomedical CMOS ICs* (Springer, 2010), *Enabling the Internet of Things—From Circuits to Networks* (Springer, 2017), and *The IoT Physical Layer* (Springer, 2019). His current research interests include low-energy circuit technology for wearable bio-signal sensors, flexible circuit board platform, BAN communication and powering, ASIC for piezoelectric Micromachined Ultrasonic Transducers (pMUTs), and System-on-Chip (SoC) design to system realization for wearable healthcare applications.

Dr. Yoo is a Technical Program Committee Member of the IEEE International Solid-State Circuits Conference (ISSCC), the ISSCC Student Research Preview (Co-Chair), the IEEE Custom Integrated Circuits Conference (CICC, Emerging Technologies, Systems and Applications Subcommittee Chair), and the IEEE Asian Solid-State Circuits Conference (A-SSCC, Emerging Technologies and Applications Subcommittee Chair). He is also an Analog Signal Processing Technical Committee Member of the IEEE Circuits and Systems Society. He was a recipient or co-recipient of several awards, including the IEEE International Symposium on Circuits and Systems (ISCAS) 2015 Best Paper Award (BioCAS Track), the ISCAS 2015 Runner-Up Best Student Paper Award, the Masdar Institute Best Research Award in 2015, and the IEEE Asian Solid-State Circuit Conference (A-SSCC) Outstanding Design Award in 2005. He was the Founding Vice-Chair of the IEEE SSCS United Arab Emirates (UAE) Chapter. He is also the Chair of the IEEE SSCS Singapore Chapter. He has served as the IEEE Solid-State Circuits Society (SSCS) Distinguished Lecturer from 2017 to 2018. He is an IEEE Circuits and Systems Society (CASS) Distinguished Lecturer for the term 2019–2021.