

A Distributed Stubs Technique to Mitigate Flicker Noise Upconversion in a mm-Wave Rotary Traveling-Wave Oscillator

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Abstract—A rotary traveling-wave oscillator (RTWO) has an ability to generate multiple phases at millimeter-wave (mmW) frequencies while achieving low phase noise (PN). Unfortunately, due to the practically unavoidable transmission line (TL) dispersion, which causes the higher-order harmonics to travel faster than the fundamental, RTWOs suffer from flicker noise upconversion. In this article, we propose a “distributed stubs” technique to mitigate this mechanism in which tuning capacitors placed on the TL stubs away from the maintaining amplifiers will slow down the travel speed of higher-order harmonics relative to the fundamental, thus lowering the phase shifts due to the TL dispersion. We further provide a comprehensive analysis of the flicker noise upconversion mechanism due to the TL dispersion. The proposed 26.2–30-GHz RTWO is implemented in 22-nm fully depleted silicon-on-insulator (FD-SOI) CMOS with eight differential phases. At 30 GHz, it achieves PN of -107.6 and -128.9 dBc/Hz at 1- and 10-MHz offsets, respectively. This translates into figures-of-merit (FoMs) of 184.2 and 185.4 dB, respectively, for a single phase. The proposed architecture consumes 20 mW from 0.8-V supply. It achieves a flicker PN corner of 180 kHz, which is an order-of-magnitude better than currently achievable by state-of-the-art mmW RTWOs.

Index Terms—30 GHz, distributed oscillator, fifth generation (5G), flicker noise upconversion, fully depleted silicon-on-insulator (FD-SOI), low phase noise (PN), millimeter-wave (mmW or mm-Wave), phase sensitivity function, rotary traveling-wave oscillator (RTWO), transmission line (TL) dispersion.

I. INTRODUCTION

RECENT years have witnessed increasing demands for high data-rate wireless communications. To meet such demands, the fifth generation (5G) of wireless standards starts to utilize millimeter-wave (mmW) frequencies at 28- and 39-GHz bands, where wider bandwidths are available. This demands more complex modulation schemes, such as 256-QAM, which constraints the maximum error vector

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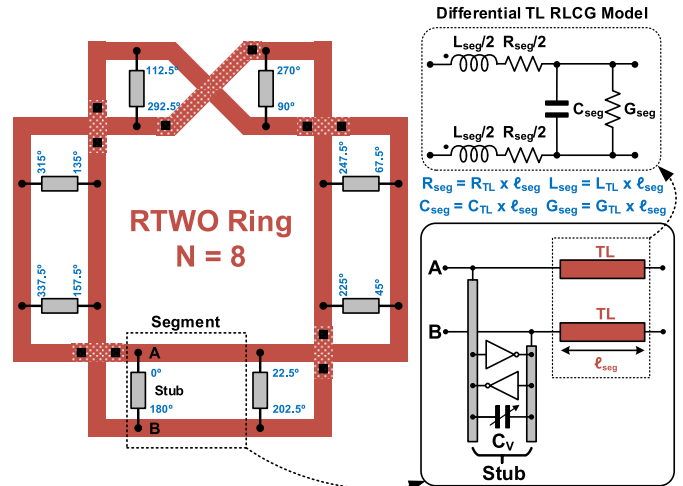


Fig. 1. Basic circuit topology of an RTWO with $N = 8$ segments showing details of its segment's equivalent circuit.

magnitude (EVM_{max}) to better than -30 dB. On the local oscillator (LO) side, this could only be realistically met with an ultralow phase noise (PN) integrated jitter level of sub-100 fs in the 28-GHz band [1]–[4]. Furthermore, multiple phases are highly desired to support direct frequency conversion [5], [6], and to perform frequency multiplication [7]. As one of promising circuit topologies, a rotary traveling-wave oscillator (RTWO) has demonstrated its ability to generate multiple phases at mmW frequencies while achieving low PN [6], [8]–[16]. It is worth mentioning that the ability to generate multiple phases in an RTWO is traded off against a larger occupied area as compared with conventional LC oscillators (LCOs). However, our goal is for an RTWO to consume equivalent or less silicon area than a multi-phase LCO would [17].

A basic RTWO architecture includes a pair of conductors acting as a differential transmission line (TL) that is twisted to form a Möbius ring. The ring is then divided into N segments to provide N differential phases, as shown in Fig. 1 ($N = 8$). Each segment of length l_{seg} is loaded/driven by a single stub which provides layout access for connecting a maintaining amplifier and a tuning varactor or a switched-capacitor (C_V). The traditional maintaining amplifier uses back-to-back inverters acting as negative resistance to compensate for the segment's losses and to ensure differential operation. The differential TL is modeled by its lumped RLCG equivalent

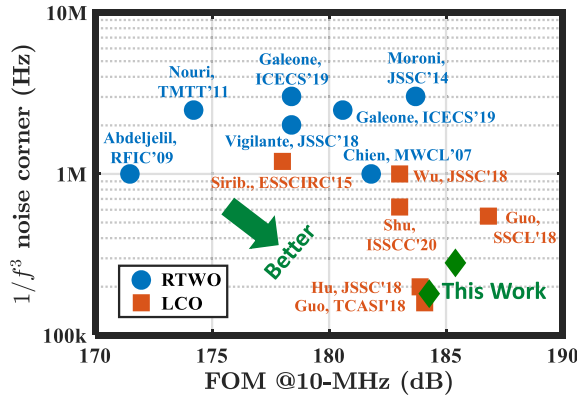


Fig. 2. Survey of $1/f^3$ PN corners of state-of-the-art mmW and sub-mmW oscillators (10–80 GHz) versus thermal noise FOM at 10-MHz offset. (See Table I for the definition of FOM.)

circuit, as illustrated in Fig. 1, where C_{TL} and L_{TL} denote the differential capacitance and inductance per unit length, respectively, and R_{TL} and G_{TL} represent the series resistance and shunt conductance losses per unit length, respectively. To first order, the oscillation frequency is given by [18]:

$$f_1 = \frac{v_{H1}}{2N\ell_{seg}} = \frac{1}{2N\ell_{seg}\sqrt{L_{TL}\left(C_{TL} + \frac{C_V}{\ell_{seg}}\right)}}, \quad (1)$$

where v_{H1} is the phase velocity at the fundamental frequency.

It is well-known that the quality factor (Q) degradation of tuning varactors in mmW RTWOs leads to worse PN in the thermal noise ($1/f^2$) region [9], [14]. Many techniques have been introduced to mitigate such degradation, such as inductive loading [11], using an array of coupled oscillators [6], [9], and combining standing-wave and traveling-wave modes (hybrid RTWO) as devised in [9] and [10]. Despite those PN improvements in the $1/f^2$ region, the flicker PN ($1/f^3$) corner of mmW RTWO appears to always exceed 1 MHz, as surveyed in Fig. 2. This puts a hard limit on the integrated jitter performance, and thus the achievable data rates in mmW transceivers.

Consider an example of a type-II all-digital phase-locked loop (ADPLL) based on a 30-GHz RTWO with $N = 8$, as shown in Fig. 3. The resolution of its phase-to-digital converter (PDC) is determined by the physical distance between RTWO segments, which is equivalent to a step size (time resolution) of $1/2 Nf_0$ [19]. This translates into time resolution as fine as 2.083 ps in this example. According to system simulations using an s-domain linear model, with no $1/f^3$ PN added yet, the loop bandwidth of ADPLL needs to be roughly 300 kHz in order to achieve a minimum integrated jitter of less than 100 fs, as depicted in Fig. 4 (see also [2]). However, due to the $1/f^3$ noise of RTWO, the integrated jitter becomes higher than 150 fs at the same loop bandwidth for the $1/f^3$ noise corners above 1 MHz. It is worth mentioning that the loop bandwidth must still be maintained quite narrow in order to prevent the reference noise from dominating the ADPLL's PN, unless an expensive reference source of high purity could be employed. Consequently, techniques to lower the $1/f^3$ PN of RTWO are highly desired for mmW frequency generation.

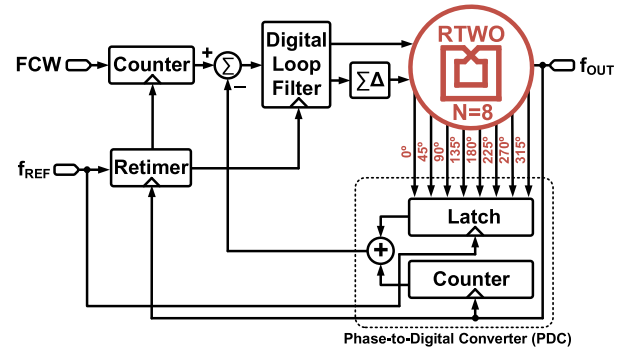


Fig. 3. Example block diagram of ADPLL utilizing the presented RTWO with $N = 8$. The output frequency could further be multiplied by N via an additional edge combiner of the generated N differential phases.

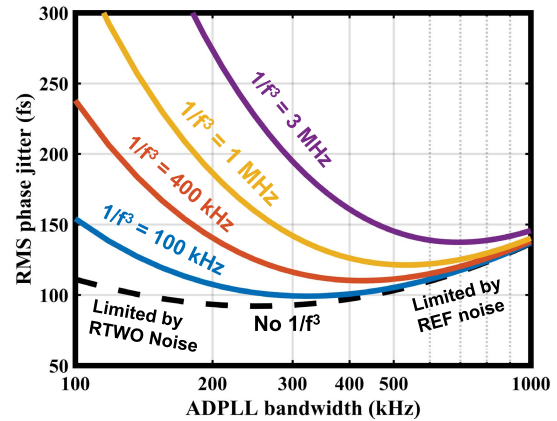


Fig. 4. Simulated rms phase jitter versus loop bandwidth for a type-II 30-GHz RTWO-based ADPLL for various RTWO $1/f^3$ PN corners. Conditions: PN at 10 MHz = -130 dBc/Hz, $f_{REF} = 250$ MHz, $\sigma_{REF} = 1$ ps, and $N = 8$.

It was mentioned in [20] that the flicker noise upconversion in RTWO depends on TL dispersion. As a result, phase shifts among TL modes occur, giving rise to an AM-PM conversion mechanism. One way to mitigate this effect is to intentionally generate a phase difference between the TL modes that cancels out the phase shifts due to the TL dispersion and thus considerably reduces the flicker noise upconversion. In [20], a “gate offset” technique was used to introduce a phase shift between the maintaining amplifier’s input and output. However, that technique is not effective at mmW frequencies due to a large delay introduced by the amplifier’s physical connections to the ring. In this article, we propose a “distributed stubs” technique to reduce the flicker noise upconversion in mmW RTWO [15]. A phase shift is deliberately induced by separating the physical connections of the maintaining amplifier and the tuning capacitors along the RTWO ring. In other words, a dedicated stub is utilized for the maintaining amplifier, whereas one or more stubs are used for connecting the tuning capacitors. By virtue of this technique, the $1/f^3$ PN corner of the proposed 30-GHz RTWO is greatly improved by an order-of-magnitude as compared to state of the art.

This article is organized as follows. In Section II, a detailed mathematical analysis of the flicker noise upconversion mechanism in RTWO is presented. The distributed stubs technique is introduced in Section III, followed by phase sensitivity

analysis to numerically verify its effectiveness. The circuit implementation is described in Section IV, while experimental results are shown and compared with state of the art in Section V.

II. FLICKER NOISE UPCONVERSION IN RTWO

In this section, the effect of TL dispersion on the flicker noise upconversion is studied. First, the effect of TL dispersion on an RTWO waveform is examined, followed by a detailed analysis of the AM-PM conversion mechanism in an RTWO.

A. TL Dispersion

The oscillating square-wave-like voltage waveform in RTWO can be expressed by a Fourier series as follows:

$$v(t) = A_1 \sin(\omega_1 t) + \sum_{k \text{ even}} A_k \cos(k\omega_1 t + \theta_k) + \sum_{k \text{ odd}} A_k \sin(k\omega_1 t + \theta_k), \quad (2)$$

where $\omega_1 = 2\pi f_1$ is the fundamental angular frequency, $k = 2, 3, \dots$, A_k is the harmonic amplitude, and θ_k is the dispersion-induced phase shift between the fundamental and the k th harmonic frequency components at steady state (ideally, $\theta_k = 0$, if no dispersion). In reality, the RTWO suffers from the TL dispersion which arises due to material (conductor and dielectric) losses as well as impedance discontinuities caused by the maintaining amplifier's loading and the shape of different segments, i.e., straight, corner, and crossover. This could result in significant phase shifts between harmonics relative to the ideal phase shifts in the approximating square wave. For simplicity and to reflect the heavy filtering of higher harmonics by the mmW ring resonator, formula (2) is approximated by considering only the fundamental (H1) and second-harmonic (H2) frequency components¹ in determining this phase shift as follows:

$$v(t) = A_1 \sin(\omega_1 t) + A_2 \cos(2\omega_1 t + \theta_2) \quad (3)$$

where A_1 and A_2 are the amplitudes of H1 and H2, respectively, and θ_2 represents the dispersion-induced phase shift between H1 and H2 in a steady state. Note that although the third harmonic is still visible, it does not significantly change the voltage waveform asymmetry between the rising and falling times, hence the little effect on the phase shift and PN, as claimed by Shahmohammadi *et al.* [21]. Pepe *et al.* [22] claim that the flicker noise upconversion is caused by the third harmonic current entering the capacitive path. Recent work [23] has clarified that while both H2 and H3 affect the flicker PN, it is H2 that is more dominant. It will be shown later that the waveform asymmetry in this design causes the flicker noise upconversion, hence it could be used for intuitive explanations. However, this is not the case for all types of oscillators.

¹Note that due to the TL dispersion within the ring structure, the second mode will shift slightly higher than $2\omega_1$ (H2). Our underlying attempt will be to properly slow it down.

The line losses of an RTWO are compensated by means of periodically spaced maintaining amplifiers, which are acting as differential negative resistors. The output current waveform of a maintaining amplifier, considering the lower order terms of its non-linear transconductance, is given as:

$$i(t) = g_1 v(t) + g_2 v^2(t) + g_3 v^3(t) \quad (4)$$

where g_1 , g_2 , and g_3 are the small-signal and higher order transconductance gain coefficients. Substituting (3) into (4), and keeping only the terms at the fundamental frequency reveals:

$$\begin{aligned} i(t) &= I_{\text{osc}} \sin(\omega_1 t) - I_{\text{dis}} \sin(\omega_1 t + \theta_2) \\ &= I_1 \sin(\omega_1 t + \varphi), \end{aligned} \quad (5)$$

where

$$I_{\text{osc}} = g_1 A_1 + \frac{3}{2} g_3 A_1 A_2^2 + \frac{3}{4} g_3 A_1^3, \quad (6)$$

and

$$I_{\text{dis}} = g_2 A_1 A_2. \quad (7)$$

I_{osc} represents the main oscillating current component that is aligned in phase with the H1 voltage component, whereas I_{dis} is the additional current component due to the dispersion-induced phase shift (θ_2) between H1 and H2.

The composite amplitude, I_1 , and phase, φ , of the resulting output current at the fundamental frequency, $i(t)$, is given as:

$$I_1 = \sqrt{I_{\text{osc}}^2 + I_{\text{dis}}^2 + 2 I_{\text{osc}} I_{\text{dis}} \cos \theta_2}, \quad (8)$$

and

$$\begin{aligned} \varphi &= \sin^{-1} \left(\sin \theta_2 \cdot \frac{I_{\text{dis}}}{\sqrt{I_{\text{osc}}^2 + I_{\text{dis}}^2 + 2 I_{\text{osc}} I_{\text{dis}} \cos \theta_2}} \right) \\ &= \sin^{-1} \left(\sin \theta_2 \cdot \frac{g_2 A_1 A_2}{I_1 (g_{1-3}, A_{1-2})} \right). \end{aligned} \quad (9)$$

As revealed by (9), the current's phase φ is sensitive to the maintaining amplifier's characteristics (g_{1-3}) and the harmonic amplitudes (A_{1-2}), both of which can be influenced by the flicker noise-induced variations in the transistors. From this, it is apparent that to reduce the AM-PM conversion gain, the sensitivity of φ to g_{1-3} and A_{1-2} must be minimized. A quick inspection of (9) suggests that the most straightforward solution is to minimize θ_2 .² This can be practically accomplished, as described later, by slowing down the higher harmonics thus ensuring that the TL dispersion is minimized.

B. AM-PM Mechanism

According to the impulse sensitivity function (ISF) theory [24], the flicker noise upconversion to PN can be analyzed in two steps [2]. First, a low-frequency voltage noise $v_{1/f}$ at the input of an RTWO maintaining amplifier, shown in Fig. 5(a),³

²Note that minimizing g_2 is not practical in this RTWO structure because this would require an increase in g_1 , which in turn would lead to a degradation of PN due to operating in the voltage-limited regime, especially at low supplies (~ 0.8 V).

³Only a half-circuit of the maintaining amplifier is shown in Fig. 5(a).

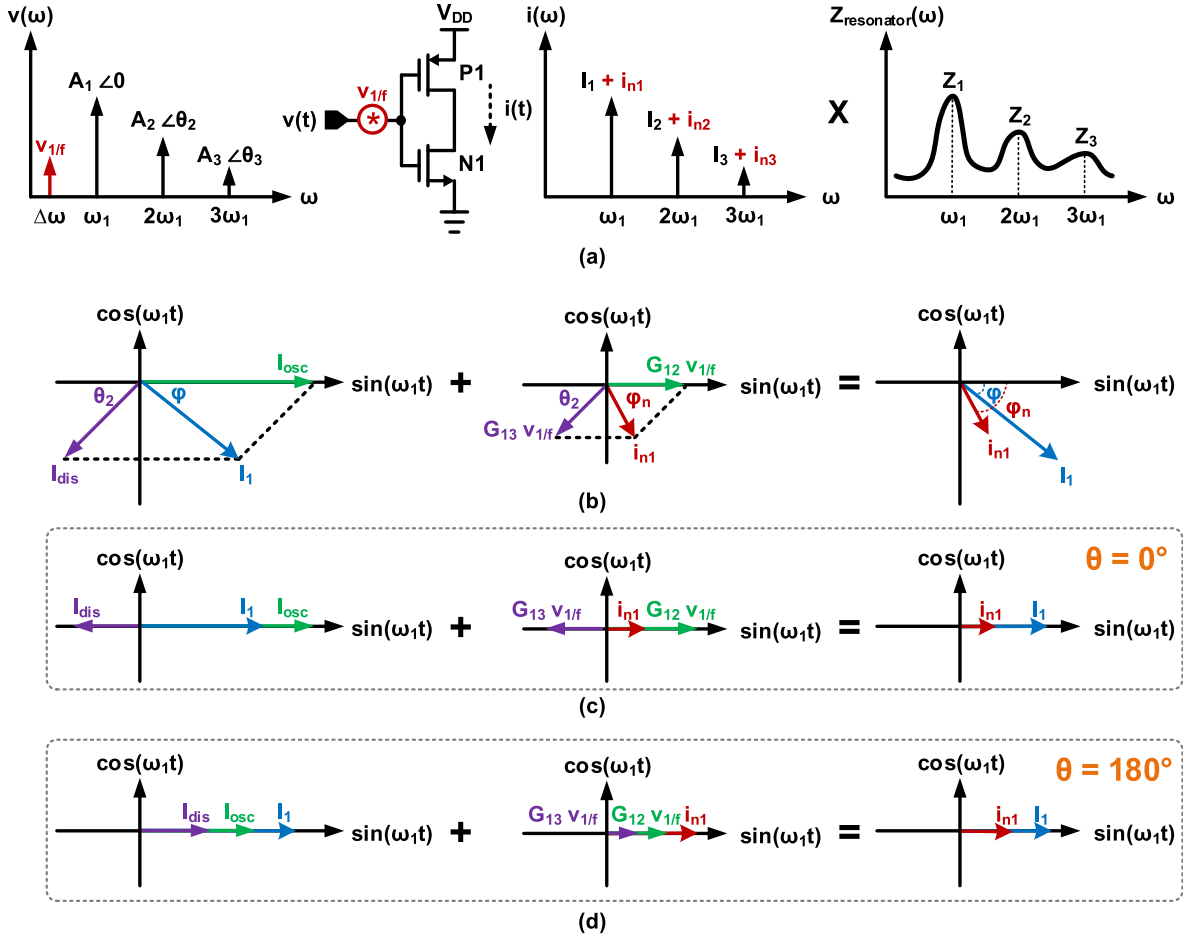


Fig. 5. Flicker noise upconversion mechanism in an RTWO. (a) Flicker noise upconversion to high-frequency current noise in $i(t)$ of its maintaining amplifier. (b) Direct conversion of flicker noise into PN. Suppressing the flicker noise upconversion by forcing: (c) $\theta_2 = 0^\circ$ or (d) $\theta_2 = 180^\circ$.

is modulated into a cyclostationary noise current $i_{n,k}$ around various harmonics $k\omega_1 \pm \Delta\omega$ through a noise modulation mechanism. In the second step, the current noise $i_{n,k}$ turns into PN through its corresponding ISF.

In the first step, assume the input-referred flicker noise voltage, $v_{1/f}(t)$, of the maintaining amplifier's transistors at $\Delta\omega$ (e.g., $2\pi \times 10$ kHz) from the carrier ω_1 is expressed as:

$$v_{1/f}(t) = \sqrt{2} V_{1/f,\text{rms}} \sin(\Delta\omega t + \gamma), \quad (10)$$

where $V_{1/f,\text{rms}}$ is the rms value of flicker noise voltage whose power spectral density (PSD) is $\overline{V_{1/f}^2} [=K_n/(W_n L_n \Delta\omega) + K_p/(W_p L_p \Delta\omega)]$, K_n and K_p are process parameters for nMOS and pMOS transistors, respectively, $W_{n,p}$ and $L_{n,p}$ are nMOS and pMOS transistors' dimensions, respectively, and γ is an initial random phase.

First, the cyclostationary noise current $i_n(t)$ can be calculated as follows. Assume that the RTWO voltage waveform in (3) now includes the input-referred flicker noise voltage $v_{1/f}(t)$, as shown in Fig. 5(a):

$$v(t) = A_1 \sin(\omega_1 t) + A_2 \cos(2\omega_1 t + \theta_2) + v_{1/f}(t). \quad (11)$$

The upconversion of baseband $v_{1/f}(t)$ into high-frequency current components is shown in Fig. 5(b). Substituting (11)

into (4), the upconverted $v_{1/f}(t)$ in $i(t)$ around ω_1 is:

$$\begin{aligned} i_n(t) &= G_{12} \cdot \sin(\omega_1 t) \cdot v_{1/f}(t) - G_{13} \cdot \sin(\omega_1 t + \theta_2) \cdot v_{1/f}(t) \\ &= i_{n1}(t) \cdot \sin(\omega_1 t + \varphi_n), \end{aligned} \quad (12)$$

where $G_{12} = 2g_2 A_1$ and $G_{13} = 3g_3 A_1 A_2$ are the upconversion transconductance gains. The composite amplitude (i_{n1}) and phase (φ_n) of the resulting upconverted noise current at the fundamental frequency, $i_n(t)$, is given as:

$$\begin{aligned} i_{n1}(t) &= \sqrt{G_{12}^2 + G_{13}^2 + 2G_{12}G_{13}\cos\theta_2} \cdot v_{1/f}(t) \\ &= G_n \cdot v_{1/f}(t), \end{aligned} \quad (13)$$

and

$$\begin{aligned} \varphi_n &= \sin^{-1} \left(\sin\theta_2 \cdot \frac{G_{13}}{\sqrt{G_{12}^2 + G_{13}^2 + 2G_{12}G_{13}\cos\theta_2}} \right) \\ &= \sin^{-1} \left(\sin\theta_2 \cdot \frac{3g_3 A_1 A_2}{G_n(g_{2-3}, A_{1-2})} \right). \end{aligned} \quad (14)$$

The first term, G_{12} , in (12) is induced by the second-order non-linearity of the maintaining amplifier. It is in-phase with the fundamental oscillating current and can only create amplitude noise. The second term, G_{13} , in (12) is induced by the third-order non-linearity of the maintaining amplifier. It is

phase-shifted by θ_2 with respect to the fundamental oscillating current and it can directly introduce PN if $\theta_2 \neq 0$ or π . Substituting (10) into (13), (12) can be written as:

$$\begin{aligned} i_n(t) &= \sqrt{2} G_n V_{1/f,\text{rms}} \sin(\omega_1 t + \varphi_n) \sin(\Delta\omega t + \gamma) \\ &= I_{1/f,\text{rms}}(t) \sin(\Delta\omega t + \gamma), \end{aligned} \quad (15)$$

where $I_{1/f,\text{rms}}(t)$ is the periodically modulated rms value of flicker noise current, which is expressed as:

$$I_{1/f,\text{rms}}(t) = \sqrt{2} G_n V_{1/f,\text{rms}} \sin(\omega_1 t + \varphi_n). \quad (16)$$

$I_{1/f,\text{rms}}(t)$ can be readily computed from dc/NOISE simulations using the instantaneous bias conditions of the output voltage waveforms of the maintaining amplifier within one oscillation period. These can be obtained from periodic steady-state (PSS) simulations.

The second step is to calculate the PN from cyclostationary noise current $i_n(t)$ and its non-normalized ISF $[\Gamma(t)]$, defined as (32) in Appendix A. The PN can be evaluated following a general approach outlined in [25] as⁴:

$$\begin{aligned} \Phi(t) &= \int_{-\infty}^t i_n(\tau) \cdot \Gamma(\tau) \cdot d\tau \\ &\approx \frac{\sqrt{2}\Gamma_{\text{eff,dc}}}{\Delta\omega} \sin(\Delta\omega t + \gamma), \end{aligned} \quad (17)$$

where $\Phi(t)$ is mainly dominated by the slow frequency term, and $\Gamma_{\text{eff,dc}}$ is the dc value of non-normalized effective $\Gamma_{\text{eff}}(t)$ [$=\Gamma(t) \times I_{1/f,\text{rms}}(t)$], which is defined as:

$$\Gamma_{\text{eff,dc}} = \frac{1}{T_1} \int_0^{T_1} I_{1/f,\text{rms}}(t) \cdot \Gamma(t) \cdot dt, \quad (18)$$

where T_1 ($=2\pi/\omega_1$) is the oscillation period. Substituting $I_{1/f,\text{rms}}(t)$ in (16) and $\Gamma(t)$ in (32) into (18), $\Gamma_{\text{eff,dc}}$ can take a simpler form if only the fundamental term of $\Gamma(t)$ is considered and assuming $\alpha_1 \approx 0$ as:

$$\Gamma_{\text{eff,dc}} = \frac{\sqrt{2}}{2} 3g_3 A_1 A_2 \cdot c_1 \sin(\theta_2) V_{1/f,\text{rms}}. \quad (19)$$

The terms α_1 and c_1 defined in (32) are the phase and magnitude of the fundamental component of $\Gamma(t)$. Substituting (19) into (36) derived in Appendix A when assuming that all RTWO segments have the same ISF, i.e., $\Gamma_{\text{eff,dc,total}} = N \Gamma_{\text{eff,dc}}$, the derived formula for single-sideband to carrier ratio (SSCR) can be written in a closed-form expression as:

$$\mathcal{L}(\Delta\omega) = \left(\frac{N \cdot 3g_3 A_1 A_2 \cdot c_1 \sin(\theta_2) V_{1/f,\text{rms}}}{2\Delta\omega} \right)^2. \quad (20)$$

Since $V_{1/f,\text{rms}}^2$ is proportional to $1/\Delta\omega$, then $\mathcal{L}(\Delta\omega)$ is ultimately proportional to $1/\Delta\omega^3$.

The flicker noise upconversion mechanism originated by the maintaining amplifier transistors can be practically mitigated in two ways: minimizing the H2 amplitude (A_2) or minimizing the dispersion-induced phase shift of H2 (θ_2). In an LCO, A_2 can be minimized by adding an extra inductor to induce common-mode (CM) resonance at H2 for explicitly defining the CM path to suppress the H2 harmonic current [2], [3]. On the other hand, θ_2 is minimized by tuning the tank's

impedance to be resistive by forcing resonance at H2 for implicitly defining the CM path to align H2 and H1 voltage components in a quadrature manner [21], or by minimizing the delay between primary and secondary transformer windings in transformer-based LCO [3]. Similarly, A_2 can be minimized in an RTWO by adding an extra series LC resonance at H2 in each RTWO maintaining amplifier for explicitly defining the CM path to suppress the H2 harmonic currents [16]. However, this would be a narrow-band solution and consuming a large area. Another solution to minimize the flicker noise upconversion in an RTWO is suggested by tuning θ_2 to 0 or π . This will result in a resistive impedance at H2, as respectively depicted in Fig. 5(c) and (d).

It is worth mentioning that, for simplicity, this analysis is limited only to the phase difference between H1 and H2, even though the dispersion happens between all harmonics. It would not be overly beneficial and practical to include the phase effects between all the harmonics, although in principle they could be analyzed in the same manner as illustrated in this section.

III. DISTRIBUTED STUBS TECHNIQUE

In this section, we propose a method for reducing the flicker noise upconversion, which we call ‘‘distributed stubs’’ [15], and which is facilitated by the inherently distributed nature of RTWO. As discussed earlier in conjunction with (9) and (14), the generation of second harmonic (H2) is unavoidable since g_2 and A_2 are difficult to attenuate below a certain point. Hence, the effort should turn toward reducing θ_2 . We propose to shunt the RTWO differential TLs with capacitive stubs along the way that will naturally introduce a larger phase shift at H2, ψ_{H2} , than at the fundamental (H1), ψ_{H1} , thus bringing θ_2 closer to zero ($\psi_{H2} - \psi_{H1} \rightarrow -\theta_2$).⁵ Adding a capacitance along the differential TL will certainly affect ψ_{H1} , thereby proportionally increasing the oscillating period. To compensate for that, the tuning capacitance C_V in the conventional RTWO of Fig. 6(b) ($M = 0$) is moved to the new capacitive stub ($M = 1$) in Fig. 6(c). Alternatively, C_V can be distributed over two ($M = 2$) capacitive stubs, as shown in Fig. 6(d).

To support our claim of the efficacy of mitigating the flicker noise upconversion using the distributed stubs technique, Fig. 7(a) and (b) shows the simulated level of dispersion (attenuation constant, α , and propagation constant, β) of the implemented RTWO TL structure without ($M = 0$) and with ($M = 1, 2$) the capacitive stubs. The TL models are extracted by the EMX electromagnetic (EM) solver from the actual layout. As indicated in Fig. 7(b), adding the capacitive stubs (with capacitance redistribution to maintain the resonant frequency f_1 at 30 GHz) results in slowing down the second-harmonic ($2f_1 = 60$ GHz). Fig. 7(c) shows the corresponding simulated PN plots, also including a non-dispersive TL that is based on an RLCG model. It is clearly discernible that the non-dispersive TL exhibits the lowest flicker PN corner (only ~ 90 kHz) compared to the implementable (i.e., dispersive) TL with a conventionally single stub ($M = 0$),

⁵Again, for simplicity, we only consider the fundamental and second-harmonic frequency components.

⁴The general formula (17) is adapted for RTWO as (33) in Appendix A.

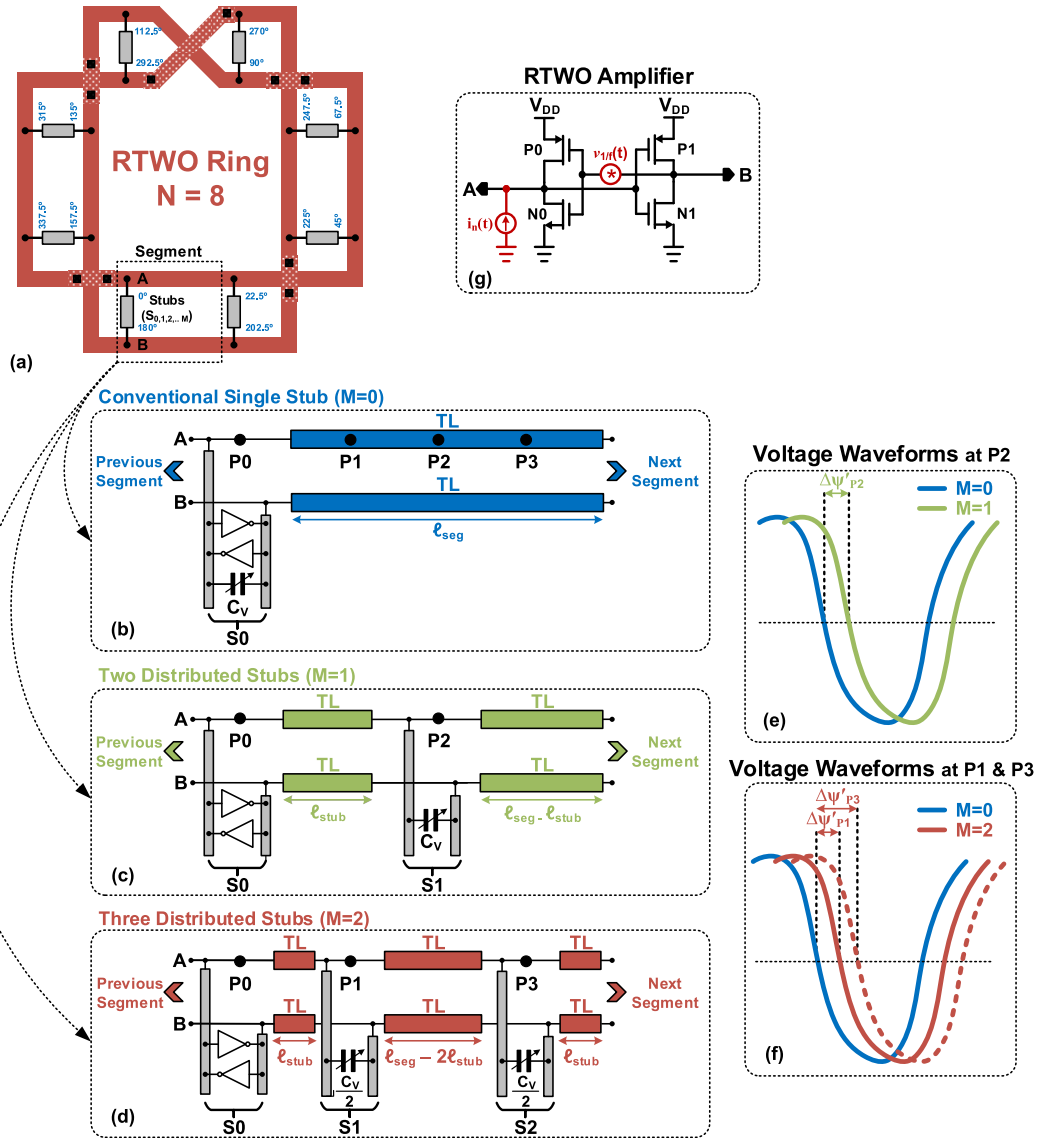


Fig. 6. Distributed stubs technique. (a) RTWO ring with $N = 8$ segments. Details of each segment, and its associated waveforms with: (b) baseline (conventional) $M = 0$, (c) $M = 1$, and (d) $M = 2$ (implemented). Voltage waveforms at: (e) P2 and (f) P1 and P3 points on TL. (g) ISF simulation environment (for simplicity, we exploit the symmetry by injecting the current noise at one of the outputs of the maintaining amplifier, point A).

which shows the $1/f^3$ PN corner as high as ~ 1.5 MHz ($17\times$ higher). When the distributed stubs technique is used with one ($M = 1$) or two capacitive stubs ($M = 2$), the $1/f^3$ PN corner is greatly improved and it is around 500 kHz ($3\times$ lower) and 180 kHz ($9\times$ lower), respectively. Fig. 7(d) shows the steady-state voltage waveforms for the same set of non-dispersive and dispersive TLs. Upon closer inspection, there are no apparent asymmetries between the rising and falling parts of the voltage waveform in the case of non-dispersive TL. In contrast, there are clear asymmetries in the case of dispersive TLs. This concludes that the TL dispersion causes asymmetries between the rising and falling parts of the voltage waveform.

Considering now only a single *isolated* TL segment⁶ for $M = 1$, as shown in Fig. 6(c), the distance ℓ_{stub} between the

⁶This assumption is in order to postpone effects due to the *next* TL segment. To account for it, the prime notation for the phases is used.

maintaining amplifier and the tuning capacitor stubs (S_0 and S_1 , respectively) causes a phase delay for the traveling wave on the TL of $\psi'_{H1} = \psi'_{P2} + \Delta\psi'_{P2}$, where ψ'_{P2} is the purely propagational phase shift at point P2 on the TL, and $\Delta\psi'_{P2}$ is the *induced* excess phase delay due to the placing of the capacitive stub S_1 at P2. Note that the total tuning capacitance does not change. We simply move C_V from the point of low impedance (i.e., maintaining amplifier) to the point of high impedance in the middle of TL where the C_V capacitor is more effective in slowing down the higher harmonics.

Let us assume the shifting distance ℓ_{stub} causes the purely propagational time delays t_{H1} and t_{H2} for H1 and H2, respectively, as:

$$t_{H1} = \frac{\ell_{\text{stub}}}{v_{H1}}, \quad t_{H2} = \frac{\ell_{\text{stub}}}{v_{H2}}, \quad (21)$$

where v_{H1} and v_{H2} are, respectively, the H1 and H2 phase velocities traveling on the TL, which include the effects of

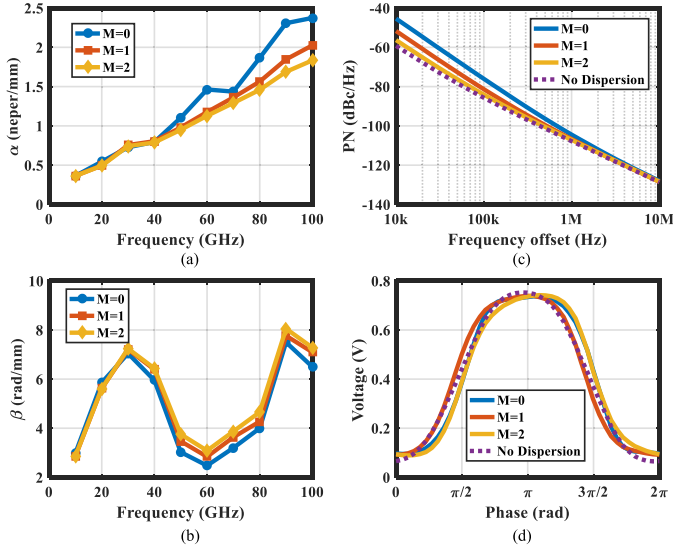


Fig. 7. Simulations of RTWO TLs with $M = 0, 1, 2$. (a) Attenuation constant (α) in neper/mm. (b) Propagation constant (β) in rad/mm. (c) Resulting PN. (d) Voltage waveforms. Conditions: 30-GHz carrier, $N = 8$, and $\ell_{\text{seg}} = 45 \mu\text{m}$. Non-dispersive TLs are included for reference in (c) and (d).

TL dispersion and capacitive stub loading. Because of such effects:

$$v_{H2} = v_{H1} + \Delta v = v_{H1} \left(1 + \frac{\Delta v}{v_{H1}} \right), \quad (22)$$

where Δv is the net increase in H2 phase velocity caused by the TL dispersion and capacitive stub loading. Substituting (22) into (21), t_{H2} can be expressed by its series expansion as follows (assuming $\Delta v \ll v_{H1}$ and ignoring higher-order terms):

$$t_{H2} = \frac{t_{H1}}{1 + \frac{\Delta v}{v_{H1}}} \approx t_{H1} - \frac{t_{H1}^2}{\Delta t}, \quad (23)$$

where $\Delta t = \ell_{\text{stub}}/\Delta v$ is the net decrease in H2 purely propagational delay caused by the TL dispersion and capacitive stub loading.

When properly excited at point P0⁷ in Fig. 6(c), the voltage waveform at P2 in (3) becomes:

$$v_{P2}(t) = A_1 \sin(\omega_1 t + \psi'_{H1}) + A_2 \cos(2\omega_1 t + 2\psi'_{H1} - 2\zeta \psi'^2_{H1} + \theta'_2), \quad (24)$$

where $\psi'_{H1} = \omega_1 t_{H1}$, $\zeta = 1/\omega_1 \Delta t$, and θ'_2 is the previously defined dispersion-induced phase shift between H1 and H2. The phase shift at H2 is constrained by $\psi'_{H2} = 2\psi'_{H1} - 2\zeta \psi'^2_{H1}$.

To be able to continue with the analysis, we now must extrapolate the voltage waveform at stub S1, $v_{P2}(t)$, to the end of the TL, i.e., the beginning of the next segment. By symmetry, this becomes $v_{P0}(t)$ with new phases $\psi_{H1} \leftarrow \psi'_{H1}$, $\psi_{H2} \leftarrow \psi'_{H2}$ and $\theta_2 \leftarrow \theta'_2$. By substituting (24) into (4),

⁷In order to mimic the RTWO environment in this isolated TL case, H2 is shifted from H1 by θ_2 at point P0.

⁸In this case: $\psi_{H1} = \Delta \psi'_{P2}$ because we extrapolate the voltage waveform at stub S1, $v_{P2}(t)$, to the beginning of next segment (*next* P0).

the maintaining amplifier' current waveform at P0 becomes:

$$i(t) = I_{\text{osc}} \sin(\omega_1 t + \psi_{H1}) - I_{\text{dis}} \sin(\omega_1 t + \psi_{H1} - 2\zeta \psi'^2_{H1} + \theta_2). \quad (25)$$

This implies that the *total* phase shift including both the TL dispersion induced and the capacitive stub induced phase shifts should be:

$$\psi_{H1} = \psi_{H1} - 2\zeta \psi'^2_{H1} + \theta_2 \quad (26)$$

$$\psi_{H1} = \sqrt{\frac{\theta_2}{2\zeta}} \quad (27)$$

in order to entirely eliminate the phase separation between the two current components in (25) so that the flicker noise will not be upconverted by the mechanism under consideration. To fully compensate for θ_2 (see Appendix B):

$$\frac{2\pi}{N} \cdot \frac{\Delta v}{v_{H1}} \cdot \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}} \left(1 - \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}} \right) = \theta_2. \quad (28)$$

Its peak value lies at $\ell_{\text{stub}}/\ell_{\text{seg}} = 1/2$ (note, $M = 1$). ψ_{H1} and ζ in (27) can be expressed in terms of ℓ_{stub} and ℓ_{seg} , with taking into account the effect of spatial periodicity of the distributed structure, as captured by (37) and (38) in Appendix B. The ratio $\ell_{\text{stub}}/\ell_{\text{seg}}$ in (28) represents the relative placement of the capacitive stub ($M = 1$) within the segment's length, in order to generate the stub-induced *excess* H2 phase $\psi_{H2} - \psi_{H1}$ that cancels out θ_2 due to the TL dispersion between the fundamental and second harmonic frequency components.

Interestingly, the beneficial phase cancellation in (28) will also force an alignment of the second mode resonant frequency with $2\omega_1$. The ratio $\Delta v/v_{H1}$ cannot be directly ascertained, but it can be calculated from the frequency shift of the second mode slightly away from $2\omega_1$ (i.e., H2) due to the TL dispersion referred to as the fundamental frequency ($\Delta f/f_1$). The latter can be obtained from an open-loop S-parameter simulation of the periodically loaded differential TL. For an RTWO with $N = 8$ and $\ell_{\text{seg}} = 45 \mu\text{m}$, it was found that the ratio $\Delta f/f_1$ is equal to 4% at 30 GHz. Substituting thus obtained $\Delta v/v_{H1}$ into (28), θ_2 and then ultimately ψ_{H1} can be obtained for different $\ell_{\text{stub}}/\ell_{\text{seg}}$, as shown in Fig. 8(a). This plot also superimposes the simulated excess phase shift, $\Delta \psi'_{P2}$ in the associated waveform of Fig. 6(e), of the signal traveling on the differential TL at point P2 when the tuning capacitor stub S1 is added ($M = 0 \rightarrow M = 1$). As expected from the symmetrical geometry constraints, the maximum phase shift occurs at $\ell_{\text{stub}} = \ell_{\text{seg}}/2$, which is also evident from (28). This concludes that the theory and simulations largely match. It is worth mentioning that the flicker noise upconversion is very sensitive to phase delay, and that even a small phase correction ($\leq 0.5^\circ$) can help to significantly reduce the flicker PN corner.

Fig. 8(b) shows the PN improvements at different offset frequencies from the 30-GHz carrier. As expected, the maximum PN improvement (5.6 dB at 10-kHz offset) coincides with the maximum phase shift, i.e., at $\ell_{\text{stub}} = \ell_{\text{seg}}/2$. The improvements are most prominent at low offset frequencies where the flicker noise is dominating. One can note that the PN improvements at higher offset frequencies are diminished. This is due to the fact that the thermal noise ($1/f^2$ region) dominates there. It is

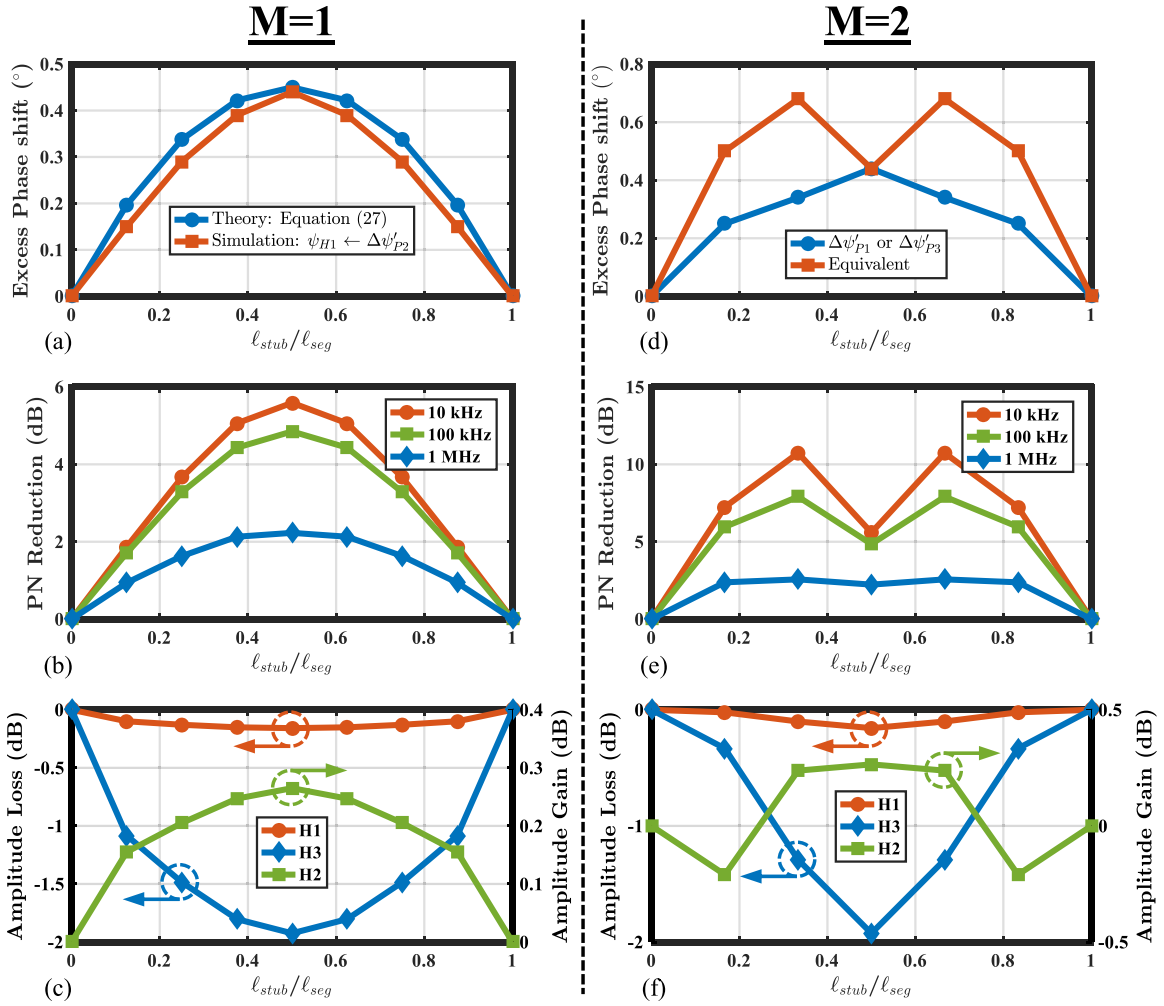


Fig. 8. Simulated parameters versus $l_{\text{stub}}/l_{\text{seg}}$. Excess phase shifts due to adding the capacitor stub(s): (a) $M = 1$ and (d) $M = 2$, relative to the $M = 0$ baseline [$\Delta\psi'_{P1}$, $\Delta\psi'_{P2}$, and $\Delta\psi'_{P3}$ are the induced excess phase delays due to the placing of a capacitive stub at $P1$ – $P3$, respectively (see Fig. 6)]. PN reduction at different offset frequencies when using: (b) $M = 1$ or (e) $M = 2$ compared to $M = 0$. (c) $M = 1$ or (f) $M = 2$ are used compared to $M = 0$. Conditions: 30-GHz carrier, $N = 8$, and $l_{\text{seg}} = 45 \mu\text{m}$.

noted that the addition of capacitive stub lowers the amplitude of the H3 frequency component, as revealed in Fig. 8(c), but the H2 amplitude is slightly increased due to the restorative action of the amplifier [see Fig. 8(c)]. The proposed technique with $M = 1$ can be viewed as inserting a special phase shifter (favoring H2 over H1) between the maintaining amplifier and the tuning capacitor. It is well-known that the phase shifter attenuates while phase-shifting [26], [27]. Therefore, it is expected that maximum losses in H1 and H3 amplitudes happen at $l_{\text{stub}} = l_{\text{seg}}/2$ at which the maximum phase shift is obtained.

Further PN improvement can be attained by adding an extra capacitive stub, as shown in Fig. 6(d), that acquires half of the capacitance C_V from the sole stub in the previous $M = 1$ case. Fig. 8(e) shows that the maximum PN performance boosts (versus the $M = 0$ baseline) are 10.7, 7.9, and 2.6 dB at 10-kHz, 100-kHz, and 1-MHz offsets, respectively, at $l_{\text{stub}} = l_{\text{seg}}/3$ (and, by symmetry, $l_{\text{stub}} = 2l_{\text{seg}}/3$). This happens because the signal is now phase-shifted by $\Delta\psi_{P3}$ at two points $P1$ and $P3$ on the differential TL, as shown

in the associated waveform of Fig. 6(f). This exerts more phase shift at H2, which provides stronger cancellation of the TL dispersion-induced phase shift. The total equivalent phase difference (i.e., the combination of the excess phase shifts from the two stubs) is nearly twice that at $P1$ or $P3$ due to the spatial periodicity of the distributed structure. Again, the proposed technique with $M = 2$ can be viewed as inserting two cascaded special phase shifters (favoring H2 over H1) between the maintaining amplifier. The H1 and H3 amplitudes are attenuated with the same magnitude at two different locations on the TL, i.e., at $l_{\text{stub}} = l_{\text{seg}}/3$ and $l_{\text{stub}} = 2l_{\text{seg}}/3$, respectively, as depicted in Fig. 8(f). This is because the RTWO waveform is firstly phase-shifted at $l_{\text{stub}} = l_{\text{seg}}/3$, then phase shifted again at $l_{\text{stub}} = 2l_{\text{seg}}/3$ with the same phase shift amount.

The proposed technique is verified in Fig. 9 across different carrier frequencies with using a fixed segment length of $l_{\text{seg}} = 45 \mu\text{m}$. Increasing the capacitive loading results in more phase shift because of the higher variation in phase velocity [27], as shown in Fig. 9(a). However, the PN improvements for

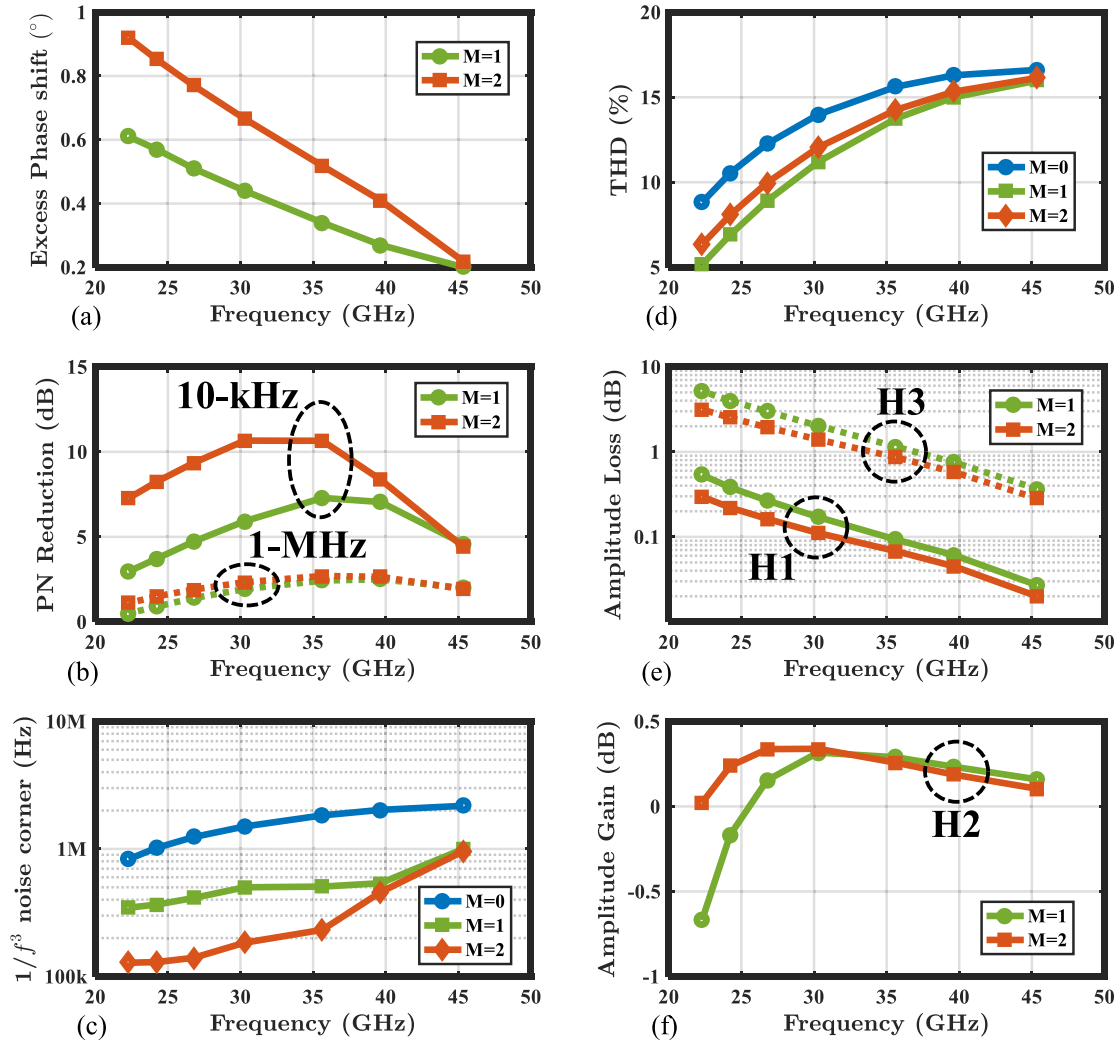


Fig. 9. Simulated parameters versus carrier frequency when using $M = 1$ or $M = 2$ compared to the $M = 0$ baseline. (a) Excess phase shifts due to adding the capacitor stub(s), (b) PN reduction at 10-kHz and 1-MHz frequency offsets, (c) $1/f^3$ PN corner, (d) THD, (e) H1 and H3 amplitude losses, and (f) H2 amplitude gain. Conditions: $N = 8$ and $\ell_{seg} = 45 \mu\text{m}$.

$M = 1$ and 2 relative to the $M = 0$ baseline in Fig. 9(b) do not exhibit a large boost at the highest capacitance loading due to the higher losses in H1 and H3 amplitudes, as depicted in Fig. 9(e). Therefore, a compromise between the maximum phase shift and minimum transmission loss has to be found for a given capacitance range. The $1/f^3$ noise corner is studied in Fig. 9(c) across different carrier frequencies for different stub configurations. At 30 GHz, the $1/f^3$ noise corner for the traditional configuration is around 1.5 MHz whereas it is $3\times$ lower for $M = 1$ and $8\times$ lower for $M = 2$. It is also noted that fewer benefits are achieved at higher frequencies (>40 GHz) due to the reduction in the introduced phase shift that cancels out θ_2 . Fig. 9(d) shows the total harmonic distortion (THD) versus the carrier frequency. Less harmonic distortion is achieved at lower frequencies where higher capacitance loading causes the waveform to look more sinusoidal. The applied technique reduces the harmonic distortion, especially at lower frequencies where heavy filtering in H3 is obtained, as illustrated in Fig. 9(e). In addition,

the H2 amplitude is slightly increased for $M = 1$ and 2 due to the slight improvement of the resonator's impedance at H2, as depicted in Fig. 9(f).

To gain further insight into the proposed technique, the phase sensitivity analysis is now verified. Fig. 10(a) and (b) plots the single-cycle waveforms of voltage $v(t)$ and cyclostationary rms noise current $I_{1/f,rms}(t)$, respectively. The flicker noise currents peak in the regions where the maintaining amplifier's transistors operate in saturation, but are also relatively high in the triode region. The phase sensitivity function, $\Gamma(t)$, is shown in Fig. 10(c) in dashed curves. It can be evaluated based on periodic transfer function (PXF) simulations by injecting a small-signal at one of the outputs of the maintaining amplifier (here, point A) of one of the segments, as depicted in Fig. 6(g), in order to derive the periodic transimpedance [28]. Using the magnitude and phase of this periodic transimpedance and by using the magnitude and initial phase of the fundamental harmonic PSS analysis with a harmonic balance (HB) engine, one can evaluate its

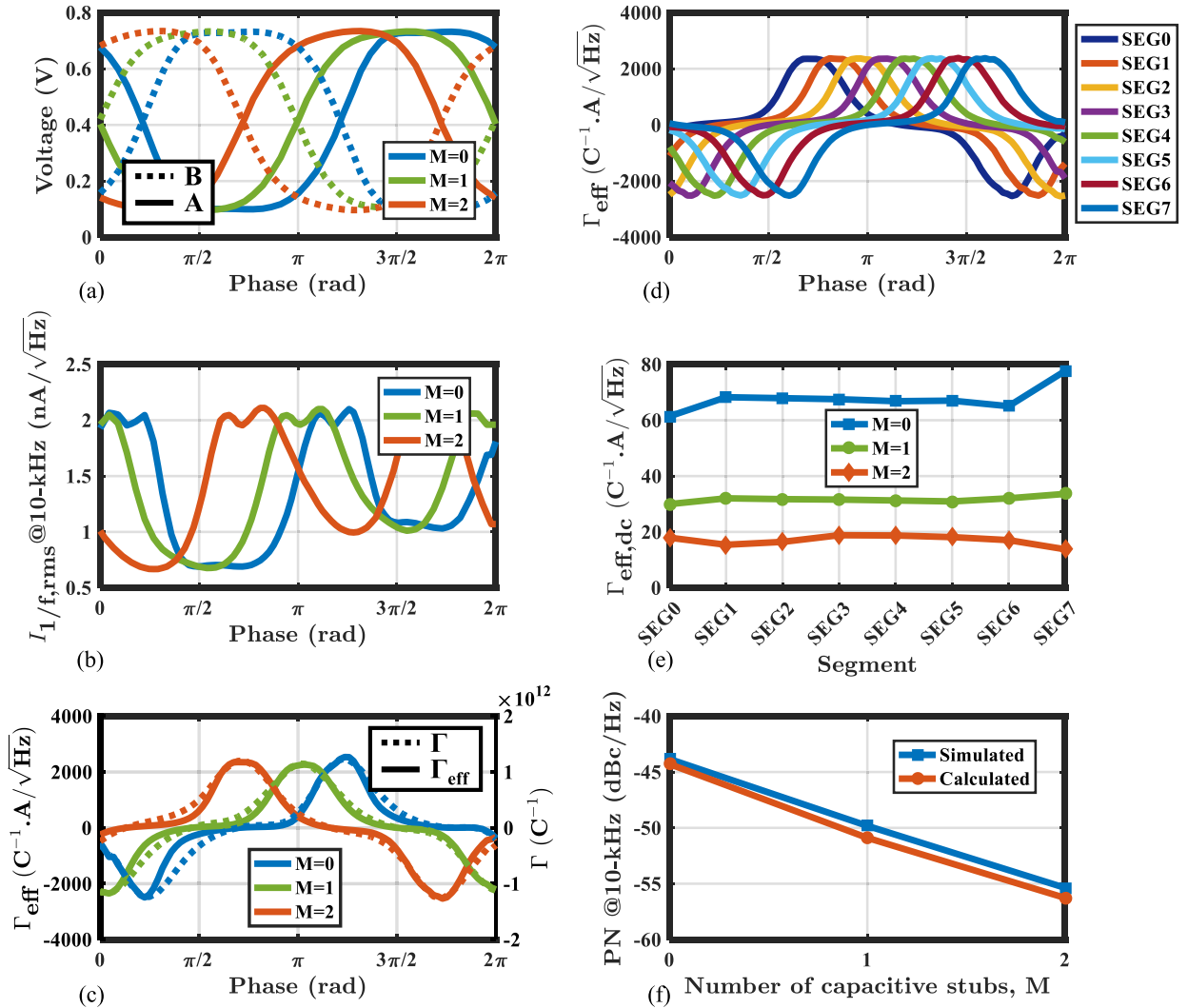


Fig. 10. Comparing simulated waveforms of an RTWO segment when using $M = 0, 1, 2$. (a) Voltages at the amplifiers, (b) rms noise currents, and (c) Γ and effective Γ . For each RTWO segment: (d) effective Γ for $M = 2$, and (e) dc value of effective Γ for $M = 0, 1, 2$. (f) Calculated and simulated PN. Conditions: 30-GHz carrier, $N = 8$, and $\ell_{\text{seg}} = 45 \mu\text{m}$. Spot PN is at 10-kHz offset frequency.

magnitudes c_k and phases (α_k) to calculate $\Gamma(t)$ using (32). The effective phase sensitivity function, $\Gamma_{\text{eff}}(t)$, is calculated as $\Gamma_{\text{eff}} = I_{1/f,rms} \times \Gamma$ of each stub configuration, as depicted in Fig. 10(c) in solid curves. From the Γ_{eff} waveforms, it is obvious that the flicker noise upconversion to PN mainly happens during the two saturation regions that have an opposite influence on the phase change of the voltage waveforms in each region.

In the baseline configuration, the TL dispersion causes asymmetries between the rising and falling parts of $v(t)$, where the positive area of Γ_{eff} is wider than that of the negative. This means that its dc value, $\Gamma_{\text{eff,dc}}$, is not equal to zero. However, with $M = 1$ or 2 , Γ_{eff} can be shaped to be more symmetric, causing the phase change in the two regions to cancel each other within one period, i.e., Γ_{eff} is nearly equal to zero. As per phase sensitivity theory, $\Gamma_{\text{eff,dc}}$ represents the contribution of flicker noise to PN conversion [2]. Ideally, the total $\Gamma_{\text{eff,dc}}$ is calculated by multiplying $\Gamma_{\text{eff,dc}}$ of one segment by the number of segments (N). However, due to

the physical asymmetry between the RTWO segments, Γ_{eff} varies as illustrated in Fig. 10(d). In this case, the total is calculated by summing up $\Gamma_{\text{eff,dc}}$ of each segment according to (34). Fig. 10(e) shows $\Gamma_{\text{eff,dc}}$ of each segment (SEG0–SEG7). The total $\Gamma_{\text{eff,dc}}$ for $M = 1$ and 2 are respectively $2.1\times$ and $4\times$ lower versus the baseline. This is equivalent to 6.2- and 11.3-dB reduction in PN at 10-kHz offset according to (36). The resulting PN at 10-kHz offset shown in Fig. 10(f) versus the number of capacitive stubs shows almost a perfect agreement with the analytical calculations, thus demonstrating the effectiveness of the proposed theory.

IV. CIRCUIT IMPLEMENTATION

The RTWO PN equation in the *thermal* region is expressed as [18]:

$$\mathcal{L}(\Delta f) = \frac{FKT}{2\pi\eta_V^2 V_{\text{DD}}^2} \frac{Z_0}{Q} \left(\frac{f_1}{\Delta f} \right)^2, \quad (29)$$

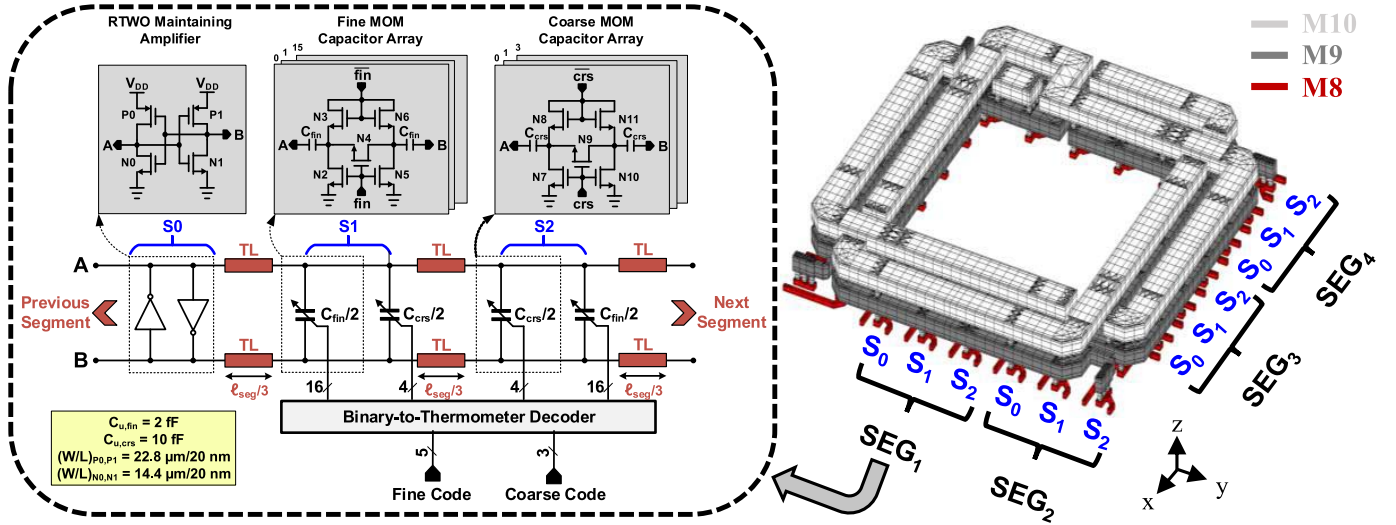


Fig. 11. 3-D view of the implemented RTWO ring with $M = 2$ and $\ell_{\text{seg}} = 45 \mu\text{m}$ with the detailed circuit diagram of one of its segments.

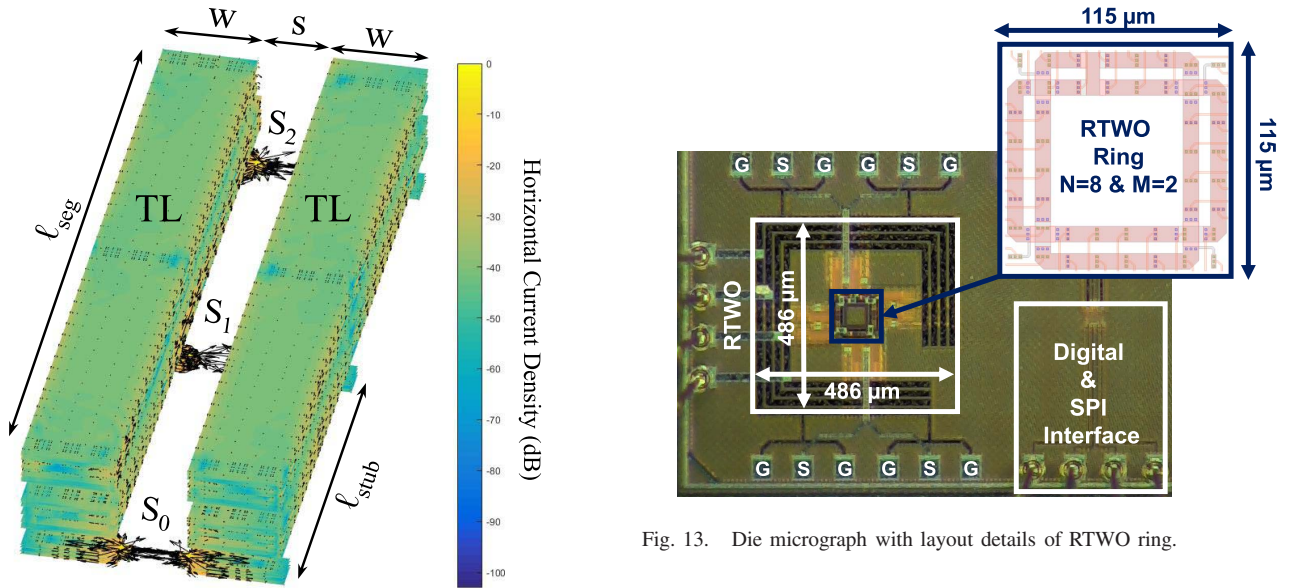


Fig. 12. EM 3-D simulation of the RTWO resonator indicating the horizontal current density in the odd-mode.

and the dc power consumption is given as:

$$P_{\text{dc}} = \frac{\pi \eta_V V_{\text{DD}}^2}{\eta_I} \frac{1}{Z_0 Q}, \quad (30)$$

where $F (=1 + \gamma \omega_1 t_{\text{rise}})$ is the oscillator noise factor, $\gamma [= (\gamma_n + \gamma_p)/2]$ is the total channel noise coefficient, γ_n, γ_p are channel noise coefficients for nMOS and pMOS, respectively, $t_{\text{rise}} [= 1/\omega_1 [(N/\pi) - (1/2)] + 1]$ is the rise time of the voltage waveform [29], K is Boltzmann's constant, T is the absolute temperature, η_I and η_V are the voltage and current efficiencies, V_{DD} is the supply voltage, Z_0 is the differential characteristic impedance of the TL, and Q is the TL resonator's quality factor. For a given Q , (29) and (30), respectively, indicate that the PN is directly proportional to Z_0 , whereas P_{dc} is inversely proportional to it. Thus, with maximizing Q , PN can

be improved by minimizing Z_0 at the expense of higher P_{dc} . The Q is affected by series and shunt losses of the TL resonator while the shunt losses become dominant at mmW frequencies. On the other hand, Z_0 is chosen by setting the differential TL geometries: width (w) and spacing (s). Some iterations are needed to find the optimum Z_0 with loading considerations of the maintaining amplifier and tuning sw-caps. In this design, the optimum geometries for the TL are found to be $w = 8.1 \mu\text{m}$ and $s = 6 \mu\text{m}$ for a given segment length of $\ell_{\text{seg}} = 45 \mu\text{m}$. The resultant RLCG parameters of this TL at 30 GHz are: $R_{\text{TL}} = 353 \text{ m}\Omega/\text{mm}$, $L_{\text{TL}} = 68.4 \text{ pH}/\text{mm}$, $C_{\text{TL}} = 26.3 \text{ fF}/\text{mm}$, and $G_{\text{TL}} = 252 \mu\text{S}/\text{mm}$. This translates to the unloaded Z_0 , Q , and attenuation constant of 52Ω , 12, and $0.9 \text{ dB}/\text{mm}$, respectively. The proposed RTWO ring is realized by stacking the top two $2.88\text{-}\mu\text{m}$ -thick copper metal layers (M9 and M10) in order to minimize the dc resistance and achieve the best possible Q , whereas the stubs use M8 copper layer. The TL length is designed to obtain the resonance condition at the targeted oscillation frequency.

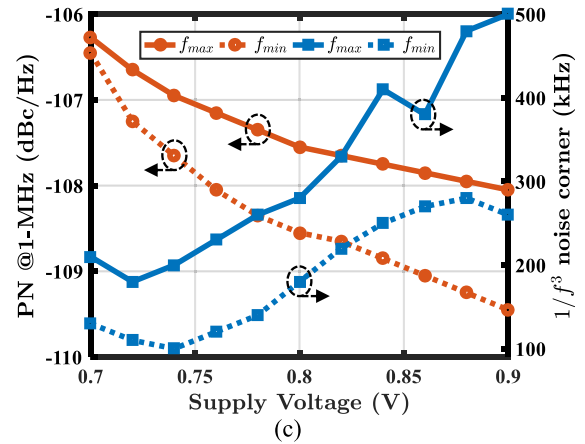
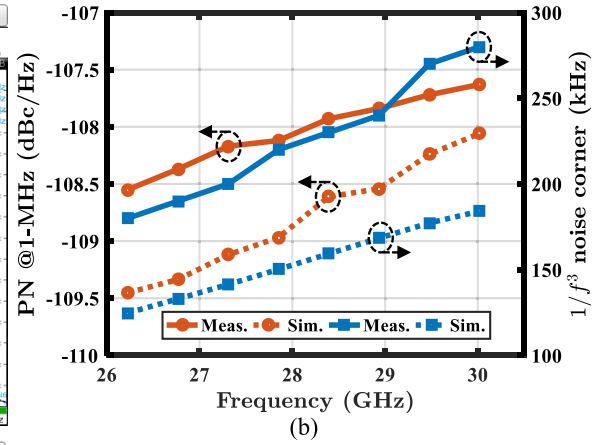
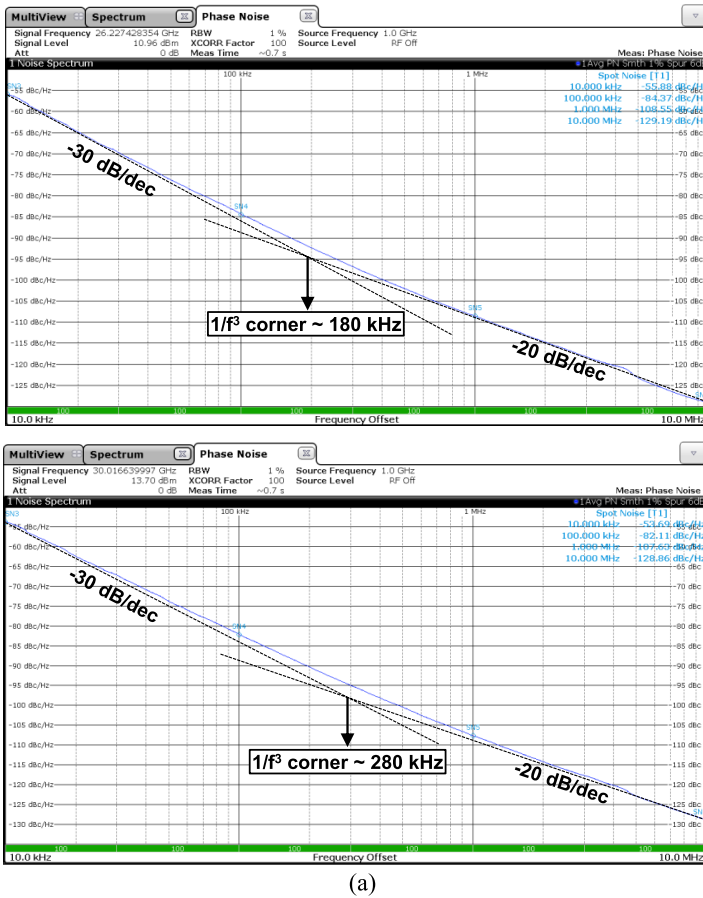


Fig. 14. (a) Measured PN plots at 26.2 and 30 GHz. Measured and simulated PN at 1-MHz offset and $1/f^3$ PN corner: (b) across the TR, (c) versus supply voltage at 26.2 and 30 GHz.

To alleviate the asymmetry in layout design of the proposed RTWO ring, five crossovers are realized by the top two copper metals, as shown in Fig. 11. It ensures that the phase difference between the two laps is as close to 180° as possible. Fig. 12 shows the horizontal current density in the RTWO resonator of Fig. 11. The heat map indicates the ratio in dB of the horizontal current density to its maximum value. As evident, the electric field between the coupled differential TLs is so strong that the penetration into the substrate is negligible.

The ring is divided into eight segments ($N = 8$) by taking into account layout constraints. Each segment is loaded by three distributed stubs ($M = 2$ case), as shown in Fig. 11. The first stub (S_0) is driven by a negative-transconductance amplifier that is based on back-to-back inverters. The nMOS and pMOS transistors are low- V_t devices with widths of 14.4 and 22.8 μm , respectively. All transistors are designed with a minimum channel length of 20 nm. It worth mentioning that the transistors are sized to give a total transconductance of more than twice the inverse of the total TL series loss resistance ($N\ell_{\text{seg}}R_{\text{TL}}$) in order to ensure reliable startup over PVT variations. In addition, there is an optimum W/L aspect ratio between nMOS and pMOS at which the $1/f^3$ PN corner of the oscillator is minimized. This happens when their transconductances are equal. Each S_0 stub is also loaded by a 50- Ω -terminated CMOS buffer to drive its probing pad. Each

of the capacitive stubs (S_1 and S_2) consists of 4-bit coarse- and 16-bit fine-tuning thermometer-coded unary MOM switched-capacitor arrays. The resultant 8-bit coarse and 32-bit fine thermometer codes are then mapped into 3-bit and 5-bit binary codes, respectively, using a binary-to-thermometer decoder. The unit capacitance of coarse and fine arrays are: $C_{\text{crs}} = 10$ fF and $C_{\text{fin}} = 2$ fF, respectively. The simulated on/off capacitance ratio for coarse and fine-tuning arrays are 2.9 and 1.5 with a minimum quality factor at 30 GHz of 22 and 67, respectively. The coarse frequency resolution is 68 MHz/LSB, whereas it is 6 MHz/LSB for the fine one.

With the help of an EMX solver, an EM model was created for all passive structures to capture all significant capacitive and magnetic couplings within the critical layout routing. The EM model includes the RTWO ring, the stubs, and the power supply and ground traces. Therefore, any undesired coupling can be avoided as early as during the layout design. All control signals are routed using the lowest metal layers to minimize their interaction with the mmW signal paths. Symmetrical decoupling capacitors are added between the RTWO power supply and ground traces to reduce supply noise and to satisfy the process metal density requirements. In addition, they are used for tightening the local return path for the even-mode current. Furthermore, the current supply path is kept close to the current return path in order to have

TABLE I
COMPARISON WITH RELEVANT STATE-OF-THE-ART MMW OSCILLATORS

Publication		This Work		JSSC'18 [6]	JSSC'14 [9]	TMTT'11 [10]	JSSC'18 [2]	JSSC'18 [17]	SSCL'18 [30]
Topology		RTWO		Coupled RTWO	Hybrid RTWO	Hybrid RTWO	LCO	Multi-phase LCO	Multi-tank LCO
Process		22 nm FD-SOI		28 nm CMOS	65 nm CMOS	120 nm SiGe	28 nm CMOS	65 nm CMOS	65 nm CMOS
Supply Voltage (Volt)		0.8		1.3	1.2	1.2	1.0	1.0	0.55
Number of Phases (N)		16		16	4	8	2	8	2
Tuning Range (%)		13.5		20.6	8.5	6.5	13.2	5.5	15.7
Frequency (GHz)		26.2	30	19.8	51.9	45	31.2	76.5	28.5
PN (dBc/Hz)	1 MHz	-108.5	-107.6	-101.2	-86	-93	-104	-95.5	-108.7
	10 MHz	-129.2	-128.9	-131.2	-125	-114	-125.2	-116.5	-125.9
Power (mW)		21	20	75	36	19.2	13	13	6.6
$1/f^3$ Corner (MHz)		0.18	0.28	2	3	2.5	0.2	1	0.55
FoM ¹ (dBc/Hz)	1 MHz	183.6	184.2	168.4	164.7	173.2	182.8	182	189.6
	10 MHz	184.3	185.4	178.4	183.7	174.2	183.9	183	186.8
FoM _T ² (dBc/Hz)	1 MHz	186.3	186.8	174.7	163.3	169.5	185.2	176.8	193.5
	10 MHz	187	188.1	184.7	182.3	170.5	186.4	177.8	190.7
FoM _P ³ (dBc/Hz)	1 MHz	195.7	196.2	180.4	170.7	182.2	185.8	191	192.6
	10 MHz	196.4	197.5	190.4	189.8	183.2	187	192.1	189.8
Core Area (mm ²)		0.24		0.38	0.1	0.25	0.15	0.3	0.083

$$^1 \text{FoM}(\Delta f) = -PN(\Delta f) + 20 \log_{10}(f_1/\Delta f) - 10 \log_{10}(P_{\text{DC}}/1\text{mW})$$

$$^2 \text{FoM}_T(\Delta f) = \text{FoM}(\Delta f) + 20 \log_{10}(\text{TR}/10\%) \quad ^3 \text{FoM}_P(\Delta f) = \text{FoM}(\Delta f) + 10 \log_{10}(N)$$

better control of the even-mode. It is worth mentioning that any asymmetries in the layout will cause degradation in the flicker PN. For this reason, it is important to minimize the systematic mismatch by maintaining symmetry in the design and layout of the RTWO. As a result of the careful EM modeling, the RTWO oscillation frequency could be accurately predicted; the difference between the simulated and measured frequencies is merely 460 MHz (1.5%).

V. EXPERIMENTAL RESULTS

The prototype of the proposed 30-GHz RTWO was fabricated in 22 nm fully depleted silicon-on-insulator (FD-SOI) CMOS. The RTWO itself occupies 0.24 mm² utilizing a 115 $\mu\text{m} \times 115 \mu\text{m}$ "ring," as depicted in the die micrograph in Fig. 13. The chip consumes 20 mW from a 0.8-V supply excluding the 50- Ω -terminated CMOS output buffers which consume 25.6 mW. The RTWO signals are probed using ground-signal-ground (GSG) pads. The PN is evaluated using a Rohde & Schwarz FSWP50 PN analyzer. The measured tuning range (TR) is from 26.2 to 30 GHz (13.5%) with 6-MHz/LSB fine frequency resolution. Fig. 14(a) shows the measured PN at 26.2 (f_{\min}) and 30 GHz (f_{\max}) with 0.8-V supply voltage. When tuned to 30 GHz, the measured PN at 100-kHz, 1-MHz, and 10-MHz frequency offsets are -82.1, -107.6, and -128.9 dBc/Hz, respectively. This corresponds to FoM of 178.6, 184.2, and 185.4 dBc/Hz, respectively.

The measured PN at 1-MHz offset across the TR is shown in Fig. 14(b) and varies ~ 1 dB over the entire TR. The measured PN is ~ 1 dB worse than simulated from the extracted EM model, mainly due to the lower Q -factor of the fabricated resonator. Fig. 14(b) also shows the measured

$1/f^3$ PN corner across the TR. It increases almost monotonically from 180 to 280 kHz across the TR. We suspect that the worse measured $1/f^3$ PN corner than predicted through simulations is due to inaccuracies in the $1/f$ noise model of the transistors in the process design kit (PDK). Fig. 14(c) illustrates the measured PN and $1/f^3$ PN corner at different supply voltages at f_{\min} and f_{\max} . The PN is enhanced by ~ 3 and ~ 1.8 dB when varying the supply voltage from 0.7 to 0.9 V at f_{\min} and f_{\max} , respectively, while the $1/f^3$ PN corner increases from 100 to 280 kHz at f_{\min} and from 180 to 500 kHz at f_{\max} . The increase in $1/f^3$ PN corner is due to the high AM-PM conversion gain that happens at higher supply voltages.

The measured supply frequency pushing is 230 and 170 MHz/V at f_{\max} and f_{\min} , respectively, which is in line with other similar state-of-the-art oscillators. This is mainly caused by the non-linear capacitances of the back-to-back inverter transistors (i.e., AM-FM mechanism). The other upconversion mechanisms (e.g., AM-PM) appear nondominant. For example, if (28) is in perfect balance [i.e., θ_2 feeding (20) is vanishing], then theoretically there will be no upconversion to PN from the flicker noise as well as from any small-signal disturbance on V_{DD} . An analysis of (20) based on SPICE simulation data for $\theta_2 = 1^\circ$ indicated only 1.25 dB of PN at 10-kHz degradation when V_{DD} changes from 0.7 to 0.9 V.

Performance comparison of the proposed architecture with state-of-the-art mmW oscillators is given in Table I. The proposed oscillator achieves 180- and 280-kHz flicker noise corners at 26.2- and 30-GHz carriers, respectively, which confirms the efficacy of the proposed technique. This is the lowest $1/f^3$ PN corner ever reached among the mmW RTWOs, which typically report > 1 MHz. The improvement in flicker noise upconversion is prominent when comparing FoM at 1 MHz where the proposed RTWO is 10.5 dB better than

the best report of RTWO's in [10]. When compared with the multi-phase LCO in [17], our PN is 2 dB better assuming that consumes the same power consumption, besides our proposed oscillator generates four more differential phases. Comparing with LCOs, it reaches the best-in-class performance [2], [30] while additionally delivering the benefit of eight differential phases.

A new FoM for multi-phase oscillators was recently proposed in [31] to account for the number of generated output phases, which is given as:

$$\text{FoM}_P = \text{FoM} + 10 \log_{10}(N). \quad (31)$$

To the best of the authors' knowledge, our RTWO achieves the best FoM_P of 197.5 dB at 10 MHz compared to published reports.

VI. CONCLUSION

This article demonstrated a new 30-GHz RTWO for multi-phase clock generation featuring a record low $1/f^3$ PN corner. The proposed architecture uses a new distributed stubs technique to reduce the flicker noise upconversion caused by a TL dispersion. It intentionally generates a phase difference between the fundamental and second harmonics by means of the tuning capacitance redistribution along the TL in order to cancel out the phase shifts due to the phase dispersion. A comprehensive mathematical analysis validates the effectiveness of this technique. The prototype was fabricated in a 22-nm FD-SOI process and achieves the best-in-class performance.

APPENDIX A

The non-normalized ISF $[\Gamma(t)]$ can be expressed as [2]:

$$\Gamma(t) = \frac{1}{2}c_0 \cos(\alpha_0) + \sum_{k=1}^{\infty} c_k \cos(k\omega_1 t + \alpha_k) \quad (32)$$

where c_k and α_k are the magnitude and phase of k th harmonic term, respectively. A fast and accurate simulation technique of ISF based on positive sidebands of a PXF was described in [32]. Note that α_0 is either 0 or π depending on the sign of dc term of $\Gamma(t)$.

Now, suppose that we have different uncorrelated noise sources at all nodes, one at each output of the maintaining amplifier in each RTWO segment. In addition, the ISF waveforms for different nodes will have different shapes. Therefore, the total PN due to all the sources is given by superposition of each node as [25]:

$$\begin{aligned} \Phi(t) &= \sum_{n=0}^{N-1} \int_{-\infty}^t i_n(\tau, n) \cdot \Gamma(\tau, n) \cdot d\tau \\ &\approx \frac{\sqrt{2}\Gamma_{\text{eff,dc,total}}}{\Delta\omega} \sin(\Delta\omega t + \gamma) \end{aligned} \quad (33)$$

where $\Gamma_{\text{eff,dc,total}}$ is given as:

$$\Gamma_{\text{eff,dc,total}} = \sum_{n=0}^{N-1} \Gamma_{\text{eff,dc},n} \quad (34)$$

where $\Gamma_{\text{eff,dc},n}$ is the dc value of effective ISF of segment n . If the noise sources at different nodes and their associated ISF

waveforms are the same (statistically), except for a phase shift, and assuming identical maintaining amplifiers, then $\Gamma_{\text{eff,dc,total}}$ will be N times the value of $\Gamma_{\text{eff,dc}}$ of one of the RTWO segments.

The PN $\Phi(t)$ appears at the output of the maintaining amplifier, showing two correlated terms at $\omega_1 \pm \Delta\omega$:

$$\begin{aligned} v(t) &= A_1 \sin[\omega_1 t + \Phi(t)] \approx A_1 \sin(\omega_1 t) \\ &+ \frac{\sqrt{2}\Gamma_{\text{eff,dc,total}}A_1}{2\Delta\omega} \sin[(\omega_1 + \Delta\omega)t + \gamma] \\ &+ \frac{\sqrt{2}\Gamma_{\text{eff,dc,total}}A_1}{2\Delta\omega} \sin[(\omega_1 - \Delta\omega)t - \gamma]. \end{aligned} \quad (35)$$

The SSCR can be written as:

$$\mathcal{L}(\Delta\omega) = \frac{\frac{1}{2} \left(\frac{\sqrt{2}\Gamma_{\text{eff,dc,total}}A_1}{2\Delta\omega} \right)^2}{\frac{1}{2}A_1^2} = \left(\frac{\sqrt{2}\Gamma_{\text{eff,dc,total}}}{2\Delta\omega} \right)^2. \quad (36)$$

Equation (36) represents the flicker PN caused by a half-circuit of the maintaining amplifiers. The final SSCR caused by the full maintaining amplifiers is $2 \times \mathcal{L}(\Delta\omega)$.

APPENDIX B

ψ_{H1} and ζ in (27) can be expressed in terms of ℓ_{stub} and ℓ_{seg} , while taking into account the effect of the spatial periodicity of the distributed RTWO structure, as:

$$\psi_{H1} = \begin{cases} \frac{\pi}{N} \cdot \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}}, & \ell_{\text{stub}} = 0 \rightarrow \ell_{\text{seg}} \\ \frac{\pi}{N} \cdot \left(1 - \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}}\right), & \ell_{\text{stub}} = \ell_{\text{seg}} \rightarrow 0 \end{cases} \quad (37)$$

$$\zeta = \begin{cases} \frac{N}{\pi} \cdot \frac{\Delta v}{v_{H1}} \cdot \frac{1}{\frac{\ell_{\text{stub}}}{\ell_{\text{seg}}}}, & \ell_{\text{stub}} = 0 \rightarrow \ell_{\text{seg}} \\ \frac{N}{\pi} \cdot \frac{\Delta v}{v_{H1}} \cdot \frac{1}{1 - \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}}}, & \ell_{\text{stub}} = \ell_{\text{seg}} \rightarrow 0 \end{cases}. \quad (38)$$

The equivalent ψ_{H1} can be derived as:

$$\begin{aligned} \frac{1}{\psi_{H1,\text{eq}}} &= \frac{1}{\frac{\pi}{N} \cdot \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}}} + \frac{1}{\frac{\pi}{N} \cdot \left(1 - \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}}\right)} \\ \Rightarrow \psi_{H1,\text{eq}} &= \frac{\pi}{N} \cdot \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}} \left(1 - \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}}\right). \end{aligned} \quad (39)$$

The equivalent ζ can be derived by considering it as presenting a reciprocal quantity to ψ_{H1} as:

$$\begin{aligned} \zeta_{\text{eq}} &= \frac{N}{\pi} \cdot \frac{\Delta v}{v_{H1}} \cdot \frac{1}{\frac{\ell_{\text{stub}}}{\ell_{\text{seg}}}} + \frac{N}{\pi} \cdot \frac{\Delta v}{v_{H1}} \cdot \frac{1}{1 - \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}}} \\ &= \frac{N}{\pi} \cdot \frac{\Delta v}{v_{H1}} \cdot \frac{1}{\frac{\ell_{\text{stub}}}{\ell_{\text{seg}}} \left(1 - \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}}\right)}. \end{aligned} \quad (40)$$

Substituting (39) and (40) into (27), the compensation for θ_2 can be expressed as:

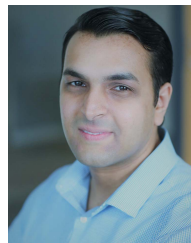
$$\theta_2 \leftarrow 2\zeta \cdot \psi_{H1}^2 = \frac{2\pi}{N} \cdot \frac{\Delta v}{v_{H1}} \cdot \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}} \left(1 - \frac{\ell_{\text{stub}}}{\ell_{\text{seg}}}\right). \quad (41)$$

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REFERENCES

- [1] L. Iotti, A. Mazzanti, and F. Svelto, "Insights into phase-noise scaling in switch-coupled multi-core LC VCOs for E-band adaptive modulation links," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1703–1718, Jul. 2017.
- [2] Y. Hu, T. Siriburanon, and R. B. Staszewski, "A low-flicker-noise 30-GHz class-F23 oscillator in 28-nm CMOS using implicit resonance and explicit common-mode return path," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1977–1987, Jul. 2018.
- [3] Z. Zong, P. Chen, and R. B. Staszewski, "A low-noise fractional- N digital frequency synthesizer with implicit frequency tripling for mm-wave applications," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 755–767, Mar. 2019.
- [4] Y. Hu *et al.*, "A 21.7-to-26.5GHz charge-sharing locking quadrature PLL with implicit digital frequency-tracking loop achieving 75fs jitter and -250dB FoM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 276–278.
- [5] A. Mazzanti, M. Sosio, M. Repposi, and F. Svelto, "A 24GHz sub-harmonic receiver front-end with integrated multi-phase LO generation in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 216–608.
- [6] M. Vigilante and P. Reynaert, "A coupled-RTWO-based subharmonic receiver front end for 5G E-band backhaul links in 28-nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2927–2938, Oct. 2018.
- [7] T. Chi, J. Papapolymerou, and H. Wang, "A +2.3dBm 124-158GHz class-C frequency quadrupler with folded-transformer based multi-phase driving," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2015, pp. 263–266.
- [8] M. Aidoo, G. Ariyak, F. Rabbi, M. D. Kirkman-Bey, N. S. Dogan, and Z. Xie, "A 70 GHz rotary traveling wave oscillator (RTWO) in 65-nm CMOS," in *Proc. SoutheastCon*, Mar. 2017, pp. 1–4.
- [9] A. Moroni, R. Genesi, and D. Manstretta, "Analysis and design of a 54 GHz distributed 'hybrid' wave oscillator array with quadrature outputs," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1158–1172, May 2014.
- [10] N. Nouri and J. F. Buckwalter, "A 45-GHz rotary-wave voltage-controlled oscillator," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 2, pp. 383–392, Feb. 2011.
- [11] J.-C. Chien and L.-H. Lu, "A 32-GHz rotary traveling-wave voltage controlled oscillator in 0.18- μ m CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 10, pp. 724–726, Oct. 2007.
- [12] H. Hsieh, Y. Hsu, and L. Lu, "A 15/30-GHz dual-band multiphase voltage-controlled oscillator in 0.18- μ m CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 3, pp. 474–483, Mar. 2007.
- [13] F. Ben Abdeljelil, W. Tatinian, L. Carpineto, and G. Jacquemod, "Design of a CMOS 12 GHz rotary travelling wave oscillator with switched capacitor tuning," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2009, pp. 579–582.
- [14] A. Devos, M. Vigilante, and P. Reynaert, "Multiphase digitally controlled oscillator for future 5G phased arrays in 90 nm CMOS," in *Proc. IEEE Nordic Circuits Syst. Conf. (NORCAS)*, Nov. 2016, pp. 1–4.
- [15] M. A. Shehata, M. Keaveney, and R. B. Staszewski, "A 184.6-dBc/Hz FoM 100-kHz flicker phase noise corner 30-GHz rotary traveling-wave oscillator using distributed stubs in 22-nm FD-SOI," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 103–106, Sep. 2019.
- [16] S. Galeone, M. P. Kennedy, K. Ahmed, H. Shanani, and M. Keaveney, "An eight-phase 40GHz RTWO in 28nm CMOS with phase noise reduction via head and tail filtering," in *Proc. 26th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Nov. 2019, pp. 306–309.
- [17] L. Wu and Q. Xue, "E-band multi-phase LC oscillators with Rotated-Phase-Tuning using implicit phase shifters," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2560–2571, Sep. 2018.
- [18] J. Wood, T. C. Edwards, and S. Lipa, "Rotary traveling-wave oscillator arrays: A new clock technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1654–1665, Nov. 2001.
- [19] K. Takinami, R. Strandberg, P. C. P. Liang, G. Le Grand de Mercey, T. Wong, and M. Hassibi, "A distributed oscillator based all-digital PLL with a 32-phase embedded Phase-to-Digital converter," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2650–2660, Nov. 2011.
- [20] Y. Chen and K. D. Pedrotti, "Rotary traveling-wave oscillators, analysis and simulation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 1, pp. 77–87, Jan. 2011.
- [21] M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "A $1/f$ noise upconversion reduction technique for voltage-biased RF CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2610–2624, Nov. 2016.
- [22] F. Pepe, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "Suppression of flicker noise up-conversion in a 65-nm CMOS VCO in the 3.0-to-3.6 GHz band," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2375–2389, Oct. 2013.
- [23] X. Chen, Y. Hu, T. Siriburanon, J. Du, R. B. Staszewski, and A. Zhu, "A tiny complementary oscillator with $1/f^3$ noise reduction using a triple-8-shaped transformer," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 162–165, 2020.
- [24] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
- [25] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 1999.
- [26] F. Ellinger, H. Jackel, and W. Bachtold, "Varactor-loaded transmission-line phase shifter at c-band using lumped elements," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 4, pp. 1135–1140, Apr. 2003.
- [27] A. S. Nagra and R. A. York, "Distributed analog phase shifters with low insertion loss," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 9, pp. 1705–1711, Sep. 1999.
- [28] F. Pepe, A. Bonfanti, S. Levantino, P. Maffezzoni, C. Samori, and A. L. Lacaita, "An efficient linear-time variant simulation technique of oscillator phase sensitivity function," in *Proc. Int. Conf. Synth., Modeling, Anal. Simulation Methods Appl. Circuit Design (SMACD)*, Sep. 2012, pp. 17–20.
- [29] K. Takinami, R. Walsworth, S. Osman, and S. Beccue, "Phase-noise analysis in rotary traveling-wave oscillators using simple physical model," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 6, pp. 1465–1474, Jun. 2010.
- [30] H. Guo, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.083-mm² 25.2-to-29.5 GHz multi-LC-tank class-F234 VCO with a 189.6-dBc/Hz FOM," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 4, pp. 86–89, Apr. 2018.
- [31] R. Jiang, H. Noori, and F. F. Dai, "A multi-phase coupled oscillator using inductive resonant coupling and modified dual-tank techniques," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2454–2464, Sep. 2018.
- [32] Y. Hu, T. Siriburanon, and R. B. Staszewski, "Intuitive understanding of flicker noise reduction via narrowing of conduction angle in voltage-biased oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 12, pp. 1962–1966, Dec. 2019.



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