

A 0.02–4.5-GHz LN(T)A in 28-nm CMOS for 5G Exploiting Noise Reduction and Current Reuse

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Abstract—In this article, a new noise reduction/cancellation technique is proposed to improve noise figure (NF) of a broadband low-noise transconductance amplifier (LNTA) for 5G receivers. The LNTA combines a common-gate (CG) stage for wideband input matching and a common-source (CS) stage for canceling the noise and distortion of the CG stage. Yet, another noise reduction is applied to reduce the channel thermal noise of the noise cancellation stage itself. The technique further exploits current reuse and increases transconductance of the CS transistor while keeping its power consumption low. Fabricated in 28-nm CMOS, the proposed LNTA is capable of driving an external 50- Ω load and achieves a NF of 2.09–3.2 dB and input return loss (S_{11}) better than -10 dB over the 3-dB bandwidth of 20 MHz–4.5 GHz while consuming 4.5 mW from a single 1-V power supply. The achieved gain (S_{21}) and IIP3 are 15.2 dB and -4.6 dBm, respectively.

Index Terms—5G, current reuse, low-noise amplifier (LNA), low-noise transconductance amplifier (LNTA), noise cancellation, noise reduction, ultra-wideband.

I. INTRODUCTION

THE usage of various wireless standards, such as Bluetooth, Wi-Fi, GPS, and 2G/3G/4G/5G cellular, has been continually increasing. In order to utilize the frequency bands efficiently and to support more communication standards with lower power consumption, lower occupied volume, and at reduced costs, multimode transceivers, software-defined radios (SDRs), cognitive radios, and so on have been actively investigated [1].

Broadband behavior of a wireless receiver is typically defined by its front-end low-noise amplifier (LNA), whose design must consider tradeoffs between input matching, noise figure (NF), gain, bandwidth, linearity, and voltage headroom in a given process technology. There are several wideband LNA design topologies and techniques, including filter-type amplifiers [2], g_m -enhancement technique [3], common-gate (CG) amplifiers [4], resistive shunt-feedback amplifiers [5]–[7], and distributed amplifiers [8].

A very wide bandwidth LNA can be constructed using a common-source (CS) amplifier topology with several bandpass

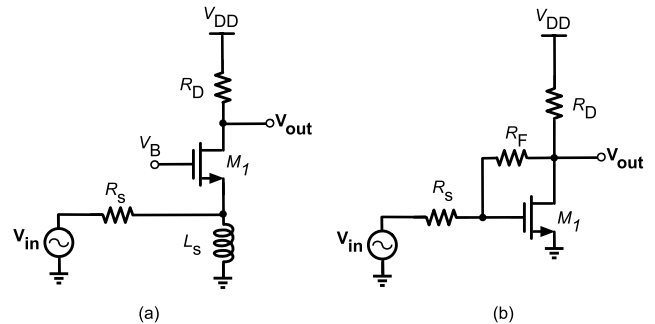


Fig. 1. Common wideband input-matching techniques. (a) CG and (b) shunt-feedback CS amplifiers.

filters for providing wideband input matching. In [2], a three-section bandpass Chebyshev filter is used to resonate the reactive part of the input impedance to provide wideband input matching over the whole band from 3.1 to 10.6 GHz. However, several associated bulky inductors there occupy a large chip area, which makes this technique not suitable for wideband applications below 3 GHz [8]. Moreover, although the CS configuration typically ensures better noise performance than in a CG structure, a low quality factor (Q) of on-chip inductors, especially those at the gate of input stage, deteriorates the noise performance where the minimum achieved NF is limited to 4.2 dB. Distributed amplifiers satisfy the required bandwidth for SDRs and optical communications, but they need several parallel stages to simultaneously provide a sufficiently high bandwidth and gain, thus resulting in high power consumption and large chip area. Moreover, they suffer from high NF due to noise from the gate's line-termination resistors and losses in the inductors [8].

Among popular techniques for designing wideband LNAs, CG and shunt-feedback CS structures, shown in Fig. 1, are of particular interest. The CG stage in Fig. 1(a) can realize a broadband input impedance matching without extra components. Since the parasitic gate–drain capacitor there is ac grounded, the CG amplifier has a better input–output isolation than in a shunt-feedback CS amplifier [4]. The linearity of the CG structure is better than that of the CS amplifier, because in the former, the input source resistance further provides the source degeneration. The input impedance of the CG structure is roughly $1/(g_{mb1} + g_{m1})$ and the noise factor is $F = 1 + (\gamma/\alpha g_{m1} R_S) + (4/g_{m1} R_D)$ [4], where γ is the excess noise factor in short-channel devices and α is the ratio $\alpha = g_m/g_{ds0}$ of the small-signal transistor

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transconductance g_m to the zero-bias drain conductance g_{ds0} . g_{mb} models the transistor's body effect. This structure suffers from poor noise performance since its total g_m should be 20 mA/V so as to satisfy the input-matching condition. A popular method to enhance its noise performance is a noise cancellation technique provided by a successive stage, which removes the channel thermal noise of the main CG transistor [9]. However, the aggregate noise performance is now limited by the channel thermal noise of the cancellation stage. Finally, another architecture in [10] uses current combining as a means to provide noise cancellation in a receiver which not only cancels the noise due to the antenna input resistance, but the baseband noise of a transimpedance amplifier (TIA) is also up-converted to RF and canceled out there.

In this article, we further improve upon the aggregate noise performance of the CG architecture with the successive noise-canceling stage by reducing the channel thermal noise of the cancellation stage itself. The main aim is to lower the NF without increasing the consumed power, which is mainly achieved by employing a current-reuse technique. This article is organized as follows. In Section II, the basic idea of the noise cancellation/reduction scheme is briefly reviewed as an intermediate step in preparation for the introduced noise reduction technique. The proposed wideband LNA is described in Section III, followed by an analysis of input matching, gain, noise, linearity, and stability. In Section IV, the measurement and simulation results are presented.

II. OVERVIEW OF NOISE CANCELLATION AND REDUCTION TECHNIQUES

In this section, we first describe the basic idea of noise cancellation scheme. Then, based on that, we propose a new noise reduction technique. Finally, the two techniques are combined in a manner that saves power.

A. Conventional Noise Cancellation Technique

The most important noise source in CMOS LNAs is the channel thermal noise of MOS transistors. Such noise is modeled as a shunt current source across the transistor's drain and source terminals. The designer's goal is to minimize the generation and propagation of this noise. Among various publications introducing noise cancellation techniques in LNAs, [9], [11]–[13] are noteworthy.

The conventional noise cancellation scheme in the CS shunt-feedback topology is shown in Fig. 2. The noise current of the main, i.e., input-matching transistor, M_1 , flows through the feedback resistor, R_F , toward the M_1 gate and creates two noise voltages at nodes X and Y with the same phase but different amplitudes. On the other hand, the signal voltage at these nodes has opposite polarities and different amplitudes due to the inverting operation of the M_1 amplifier. The signal and noise polarities being opposite at nodes X and Y make it possible to cancel the noise originating from the input-matching transistor while adding the signal contributions constructively. The noise voltage at node X, V_{nX} , is amplified and inverted by M_2 , whereas the noise voltage at node Y, V_{nY} , is passed across M_3 barely changed. At the output node, the

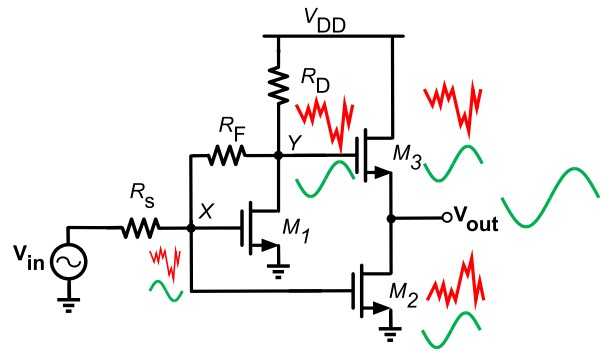


Fig. 2. Conventional noise cancellation of M_1 configured as a CS shunt-feedback amplifier (biasing not shown).

two voltages with opposite phases are canceled. Ultimately, the channel thermal noise of M_1 will be greatly attenuated or altogether canceled, provided that the following condition is satisfied:

$$\begin{aligned} V_{n,out} &= V_{nY} \frac{r_{ds2}}{r_{ds2} + 1/g_{m3}} - V_{nX} \frac{g_{m2}}{g_{m3}} = 0 \\ \frac{R_F + R_s}{R_s} &= \frac{g_{m2}}{g_{m3}} \end{aligned} \quad (1)$$

where $g_m r_{ds} \gg 1$ was assumed.

As mentioned, this kind of noise cancellation is commonly used in LNA structures with the CS input stage. The main drawback here is the need for the extra following stage in order to amplify and invert the voltage noise at node X and add it with the voltage noise at the output. According to (1), since the feedback resistor is much larger than the input source resistor, $R_F \gg R_s$, the transconductance of M_2 , g_{m2} , must be large enough to satisfy the noise cancellation condition, but at a cost of higher power consumption. In the following, we offer a new technique that can be used either as a noise cancellation or as a noise reduction technique without substantially increasing the power consumption.

B. Proposed Noise Reduction Technique

1) *Technique to Cancel the Noise of Main Transistor:* The aforementioned goal of improved noise performance at no extra consumed power can be achieved using a current-reuse technique that was inspired by [14] and [15]. Fig. 3 shows the proposed method. Just as in Fig. 2, the channel noise of the main transistor M_1 develops a noise voltage at node Y, V_{nY} , which appears on its gate at node X as V_{nX} via the resistive divider attenuation $R_s/(R_s + R_F)$. Likewise, it is then amplified and inverted via M_{aux} . Here, however, the M_{aux} 's current is injected right back into node Y via C_3 to subtract the original noise perturbation in the M_1 's channel. In this way, there is no need for an extra branch M_3 used in the conventional noise cancellation of Fig. 2. Furthermore, the source of M_1 is connected to the ground via C_2 . Inductor L_1 provides some ac isolation between the source of M_1 and the drain of M_2 . By stacking M_1 on top of M_2 dc-wise, the dc current is reused, and M_2 is biased by the main transistor current. However, ac-wise, M_{aux} is paralleled with the main transistor M_1 by means of C_1 and C_3 but completes the

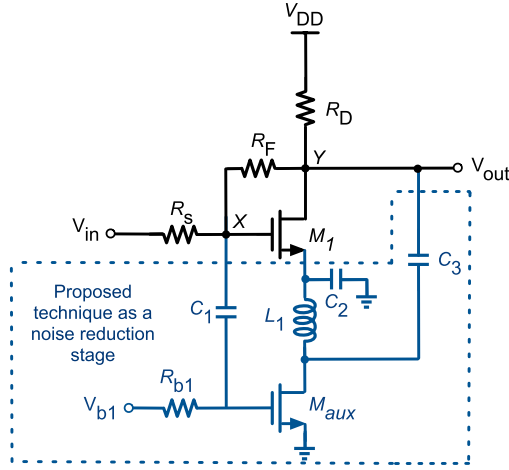


Fig. 3. Proposed noise reduction technique of M_1 's channel noise.

negative feedback around M_1 for its noise. For the proposed technique to cancel the noise of M_1 , the following condition should be met:

$$\begin{aligned} V_{n,\text{out}} &= V_{nY} - V_{nX}g_{m_{\text{aux}}}R_D = 0 \\ \frac{R_F + R_S}{R_S} &= g_{m_{\text{aux}}}R_D. \end{aligned} \quad (2)$$

Equation (2) suggests that the full noise cancellation of M_1 is rather expensive in terms of consumed power since the ratio of R_F/R_D and $g_{m_{\text{aux}}}$ needs to be very high.¹ However, this technique could be beneficially used at low expended power for a partial noise cancellation, i.e., noise reduction, of M_1 .

2) *Proposed Technique as Noise Reduction*: Noise factor excess, F_{M1} , contributed by the M_1 transistor of the shunt-feedback CS amplifier shown in Fig. 1(b) is calculated as

$$\begin{aligned} F_{M1} &= \left| \frac{\overline{V_{n,M1}}/A_v}{\overline{V_{n,R_S}}} \right|^2 = \left| \frac{\overline{I_{n,M1}}Z_{\text{out}}}{\overline{V_{n,R_S}}A_v} \right|^2 \\ &= \frac{4kTg_{m1}|Z_{\text{out}}|^2}{kTR_Sg_{m1}^2|Z_{\text{out}}|^2} \frac{\gamma}{\alpha} = \frac{4}{R_Sg_{m1}} \frac{\gamma}{\alpha} \end{aligned} \quad (3)$$

where Z_{out} is the output impedance of the amplifier as seen by the unloaded output node. In addition, $\overline{I_{n,M1}}^2 = 4kTg_{m1}\gamma$ is the channel thermal noise of M_1 and $|A_v| \simeq g_{m1}Z_{\text{out}} \cdot Z_{\text{in}}/(Z_{\text{in}} + R_S)$ is the voltage gain of M_1 , with $Z_{\text{in}} = R_F/(1 + g_{m1}R_D)|1/sC_{\text{in}}$, and C_{in} is due to parasitics at the gate of M_1 ; for the sake of simplicity, Z_{in} is considered equal to R_S . Hence, the noise factor of the shunt-feedback amplifier shown in Fig. 1(b) is approximately equal to [6]

$$F_{(\text{fig1b})} \geq 1 + \frac{4}{R_Sg_{m1}} \frac{\gamma}{\alpha}. \quad (4)$$

According to (4), the noise factor has a reverse relationship with the transconductance. It means that by increasing the

¹The input matching of the shunt-feedback CS amplifier is defined by R_F and is approximately equal to $R_F/(1 + g_{m1}R_D)$, and for providing the noise cancellation condition, $g_{m_{\text{aux}}}$ should be much larger than g_{m1} , i.e., $g_{m_{\text{aux}}} \simeq (2 + g_{m1}R_D)/R_D$.

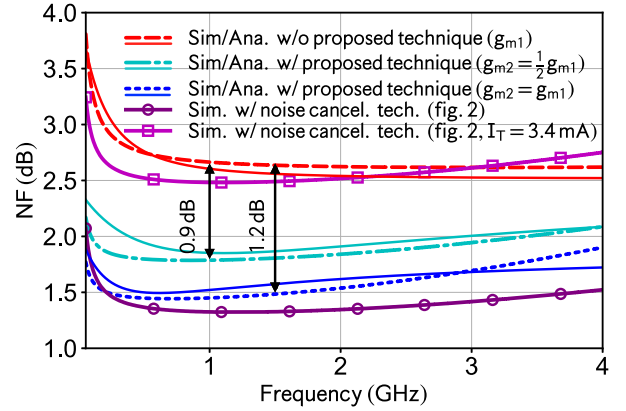


Fig. 4. Comparison of simulated/derived NF of the shunt-feedback CS amplifier of Fig. 1(b), with the same structure but with the noise reduction technique of Fig. 3, while both structures sink the same current, 1.7 mA, from 1-V supply. NF of the conventional noise cancellation configuration (Fig. 2) is included for reference.

transconductance of the main transistor, the circuit's relative noise contribution is decreased. However, this results in a higher power dissipation.

By using the proposed current-reuse technique of Fig. 3, the noise factor is roughly equal to $F_{(\text{fig3})} = 1 + F_{M1} + F_{M_{\text{aux}}}$, where F_{M1} and $F_{M_{\text{aux}}}$ are expressed by

$$\begin{aligned} F_{M1} &= \frac{4kTg_{m1}|Z_{\text{out}}|^2}{kTR_S(g_{m1} + g_{m_{\text{aux}}})^2|Z_{\text{out}}|^2} \frac{\gamma}{\alpha} \\ &= \frac{4g_{m1}}{R_S(g_{m1} + g_{m_{\text{aux}}})^2} \frac{\gamma}{\alpha} \end{aligned} \quad (5)$$

$$\begin{aligned} F_{M_{\text{aux}}} &= \frac{4kTg_{m_{\text{aux}}}|Z_{\text{out}}|^2}{kTR_S(g_{m1} + g_{m_{\text{aux}}})^2|Z_{\text{out}}|^2} \frac{\gamma}{\alpha} \\ &= \frac{4g_{m_{\text{aux}}}}{R_S(g_{m1} + g_{m_{\text{aux}}})^2} \frac{\gamma}{\alpha}. \end{aligned} \quad (6)$$

Finally, the total noise factor of the presented structure, without considering the thermal noise of R_D , is approximately given by

$$F_{(\text{fig3})} \geq 1 + \frac{4\gamma}{\alpha(g_{m1} + g_{m_{\text{aux}}})R_S} + \frac{4}{R_S R_D (g_{m1} + g_{m_{\text{aux}}})^2}. \quad (7)$$

From the standpoint of the received signal, M_{aux} is paralleled with the main transistor M_1 , and hence, according to (7), their transconductances are summed up. This boost in transconductance reduces the NF without increasing the bias current. Without the current-reuse technique, M_{aux} would be paralleled with M_1 in a conventional way as in Fig. 2, and the structure would consume twice the power in order to achieve the same NF. Nonetheless, the main drawback of the new technique is the reduced voltage headroom, leading to some deterioration of linearity.

To demonstrate the benefit of the noise reduction technique introduced in Fig. 3, we now apply it into the CS noise canceling LNA of Fig. 2 for the purpose of reducing the noise of the latter's second stage (i.e., M_2). To have a better

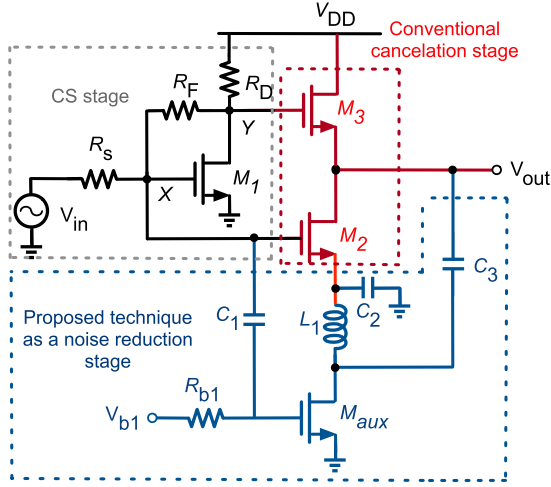


Fig. 5. Conventional noise cancellation along with the proposed noise reduction technique.

comparison between Figs. 2 and 5, their respective simplified noise factors, $F_{(\text{fig}2)}$ and $F_{(\text{fig}5)}$, are calculated as

$$F_{(\text{fig}2)} \geq 1 + \frac{\gamma}{\alpha g_{m2} R_s} + \frac{\gamma g_{m3} + \alpha R_D g_{m3}^2}{\alpha R_s g_{m2}^2} \quad (8)$$

$$F_{(\text{fig}5)} \geq 1 + \frac{\gamma}{\alpha (g_{m2} + g_{m_{\text{aux}}}) R_s} + \frac{\gamma g_{m3} + \alpha R_D g_{m3}^2}{\alpha R_s (g_{m2} + g_{m_{\text{aux}}})^2}. \quad (9)$$

By comparing (8) and (9), it can be seen that for the same value of g_{m2} and g_{m3} in both structures (Figs. 2 and 5), the noise performance in Fig. 5 has improved.

The efficacy of the proposed noise reduction technique of Fig. 3 is illustrated by the NF circuit simulation plots in Fig. 4 with superimposed analytical plots to verify the derived noise equations.² It is compared with the basic shunt-feedback amplifier of Fig. 1(b) consuming the same power of 1.7 mW. The minimum NF of the basic amplifier is 2.65 dB, while the new technique improves it to 1.45 dB. The obtained NF is now within a small fraction of a dB to the straightforward manner of noise cancellation shown in Fig. 2, but which consumes as much as 10 mW. However, when the current is insufficiently high, not only the noise of the first stage cannot be canceled entirely but also it ends up actually adding more noise sources to the circuit, which results in increasing the NF. While we maintain the current of the second stage at 1.7 mA, at the same level as the current of the first stage (the total current of Fig. 2 in this case is 3.4 mA), the current in Fig. 3 can be just 1.7 mA. As shown in Fig. 4, the noise cancellation technique of this case improves the noise performance slightly (i.e., 0.2 dB). The power efficiency advantages could be summarized as follows. According to (1), which describes the conventional noise cancellation technique, the current of the second stage should be increased in order to satisfy the noise cancellation

²We extend (4) and (7) by further considering the thermal noise of R_{D1} , i.e., $F \approx 1 + [(R_D(R_F(1 + (g_{m1} + kg_{m1})R_D))^2/R_s(Z_D + R_F(1 + (g_{m1} + kg_{m1})R_D))^2 Z_D^2 (g_{m1} + kg_{m1})^2 (R_F + R_F Z_{\text{in}} C_{\text{in}}^s + g_{m1} R_D Z_{\text{in}} + Z_{\text{in}})^2) + [\gamma/4(R_s(g_{m1} + kg_{m1}))(R_s/(R_s(1 + R_s C_{\text{in}}^s) + R_s)^2) + (4R_s/R_F)]$, where $k = 0$ gives the result for basic circuit, and also, since R_F is high, its noise effect, $4R_s/R_F$, in the total noise factor is negligible.

condition, resulting in more power drain. Moreover, there are at least two branches in the conventional noise cancellation technique, which means an extra power consumption because, in addition to the main branch, M_1 , the cancellation branch, $M_{2,3}$, drains an extra dc current, whereas in the proposed technique, there is only one branch, which reuses the dc current for M_1 and M_2 .

The salient feature of the proposed noise reduction technique in Fig. 3 is that it consists of a single stage and it saves power by means of the current reuse. This feature allows the structure to be incorporated into the (second) noise cancellation stage of the two-stage amplifier of Fig. 2, as shown in Fig. 5 (another example will be shown Section III). In this way, the channel thermal noise of the noise-canceling device itself (M_2) will be reduced at no extra power. As a net result, the noise cancellation condition is satisfied more effectively. This is given by

$$\begin{aligned} \overline{V}_{n,\text{out}}^2 &= \overline{V}_{nY}^2 \left(\frac{r_{\text{ds}2} || r_{\text{ds}_{\text{aux}}}}{r_{\text{ds}2} || r_{\text{ds}_{\text{aux}}} + 1/g_{m3}} \right)^2 \\ &\quad - \overline{V}_{nX}^2 \left(\frac{g_{m2} + g_{m_{\text{aux}}}}{g_{m3}} \right)^2 \\ V_{n,\text{out}} = 0 &\Rightarrow \frac{R_F + R_s}{R_s} = \frac{g_{m2} + g_{m_{\text{aux}}}}{g_{m3}}. \end{aligned} \quad (10)$$

In (10), $g_{m_{\text{aux}}}$ is added to g_{m2} , and hence, the noise cancellation condition can be satisfied at lower power. Therefore, applying the proposed noise reduction approach in the noise cancellation stage of the conventional noise cancellation scheme reduces the power dissipation without affecting the NF. Moreover, the added new transistor, M_{aux} , also decreases the noise contribution of the cancellation stage, M_2 , without any extra power.

It is worth mentioning that (10) is used just to show the beneficial effect of M_{aux} in the conventional noise cancellation condition, so the parasitic capacitances are not considered. Although, in practice, the condition of (10) is not completely satisfied due to the parasitic capacitances and the limitation of power consumption, the noise will be reasonably attenuated even by meeting this condition partially.

III. PROPOSED LNTA

Section II introduced the noise cancellation and reduction techniques. An example was given in Fig. 5 on how they could be beneficially combined to form a noise-canceling LNA in the CS configuration that saves significant power. The channel thermal noise of the noise cancellation stage (M_2 in the second stage in Fig. 2) was reduced by applying the noise reduction by M_{aux} of Fig. 3.

These techniques are now combined such that the channel thermal noise of the noise cancellation stage, which operates now on the input-matching CG stage, is reduced by applying the same noise reduction technique. Fig. 6 shows the proposed wideband low-noise transconductance amplifier (LNTA). We take advantage of the CG input stage, M_1 , to provide the wideband 50- Ω input matching. M_2 and M_3 of the CS stages are configured to cancel the channel thermal noise of M_1 . To reuse the M_2 current and to improve the IIP3

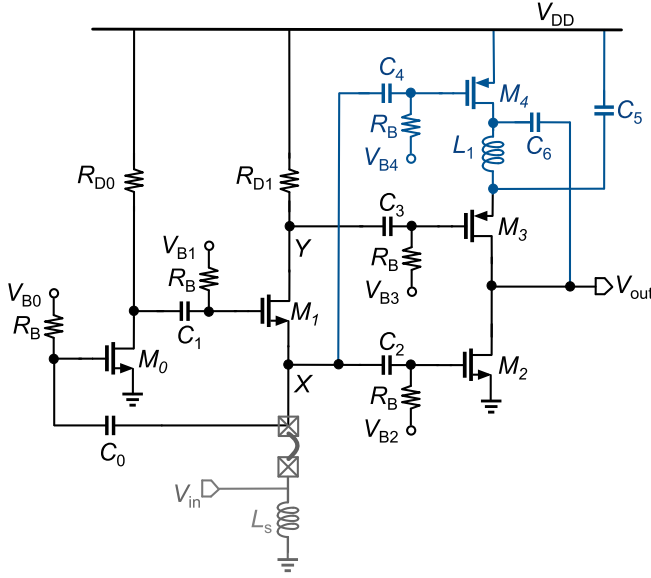


Fig. 6. Proposed wideband LNTA with noise cancellation and reduction techniques (the blue part is the proposed noise reduction technique).

linearity, M_3 is chosen now as a pMOS transistor. The external antenna-port inductor L_s is employed to provide a dc current path to ground and to damp the total parasitic capacitance at the input node. In the proposed noise reduction technique, by exploiting the current-reuse, transistor M_4 is paralleled ac-wise with M_2 , thus boosting its transconductance and hence decreasing its thermal noise effects. The pMOS–nMOS structure and “sweet spot” biasing are applied to improve the linearity. Moreover, the off-chip inductor L_s is on a printed circuit board (PCB), and hence, its value can be fairly large, in the order of a few 100s of nH, which can resonate out all parasitics at the input node at 1.2–1.5 GHz.

A. Input Matching

To consider the body effect of the wideband input-matching CG M_1 transistor and also to simplify the relations, G_{m1} stands for $(1 + R_{D0}g_{m0})(g_{m1} + g_{mb1}) \approx (1 + R_{D0}g_{m0})g_{m1}$. Hence, the input impedance is given by

$$Z_{in} = (R_{Ls} + sL_s) \left\| \frac{1}{sC_X} \right\| \frac{1}{G_{m1}} \\ = \frac{R_{Ls} + sL_s}{C_X L_s s^2 + (R_{Ls} C_X + G_{m1} L_s) s + (G_{m1} R_{Ls} + 1)} \quad (11)$$

where C_X lumps the total parasitic capacitance at node X which is damped by L_s . Since L_s is external and connected to the antenna pin, thus not consuming any extra pads on the chip, it can be fairly large (150 nH); therefore, (11) can be simplified to $Z_{in} = 1/(sC_X + G_{m1})$. This shows that the input matching is mainly defined by M_0 and M_1 . In this case, if the size of L_s changes, for instance, from 150 to 200 nH, there will be just a barely noticeable effect on S_{11} . However, the lower limit of bandwidth (f_L) will be improved. On the other hand, if the size of L_s is decreased, its series resistance, R_{Ls} , will go down (to as low as 5 Ω) due to the limited Q-factor of L_s . This

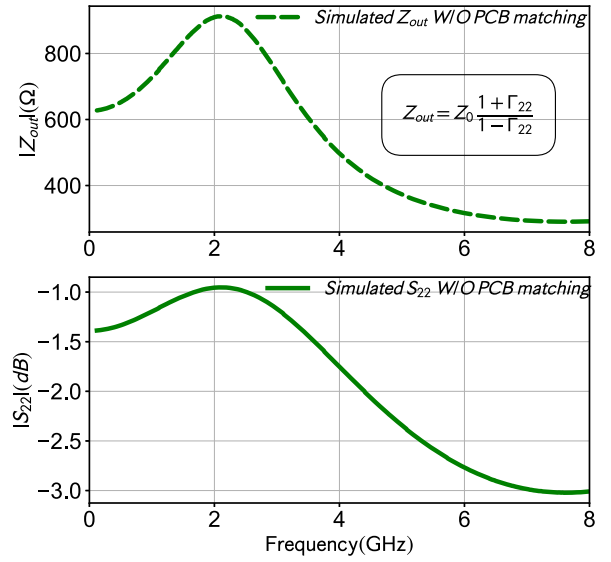


Fig. 7. Simulated output impedance without matching network on PCB.

resistance is paralleled with $1/G_{m1}$, and therefore, it lowers the equivalent input impedance. Although a new technique was described in [16] to extend the bandwidth at lower frequencies without increasing the size of L_s , here, an off-chip inductor in-parallel with the IC antenna input pin is used to realize L_s in order to save the silicon die area. Although the g_m -boost transistor, M_0 , adds a bit more parasitics to the input node, it is of small size, so it does not affect the bandwidth substantially. By increasing its size from $W = 10$ to $20 \mu\text{m}$, the simulated upper cutoff frequency lowers by 450 MHz, from 7.78 to 7.33 GHz.

B. Gain Analysis

The equivalent impedance seen from the drain of M_1 toward the ground is termed Z_Y and is equal to $R_{D1} \parallel [r_{ds1} + (1/sC_X \parallel sL_s)(1 + G_{m1}r_{ds1})] \parallel 1/sC_Y$, where R_{D1} is the load resistance of M_1 and C_Y is the total parasitic capacitance at node Y. Z_{out} determines the output impedance, which is calculated as $r_{ds2} \parallel r_{ds3} \parallel r_{ds4} \parallel 1/sC_{out}$, where C_{out} is the total output parasitic capacitance seen by V_{out} . Therefore, the voltage gain of the proposed LNTA is given by

$$A_v = -\frac{1/G_{m1}}{1/G_{m1} + R_s} (G_{m1}g_{m3}|Z_Y| + g_{m2} + g_{m4})|Z_{out}|. \quad (12)$$

As mentioned earlier, the proposed design can be used either as an LNTA in an integrated current-mode RX or as a stand-alone LNA if it is externally loaded by a 50- Ω termination. In the latter, the amplifier must properly handle the intermediate network of wire-bonding inductance, pad capacitance, package parasitics, and PCB transmission lines (TLs) and components. Fig. 7 shows the simulated output impedance of the proposed LNTA, which confirms that it is suitable for the current-mode application where its output impedance is at least eight times larger than the 50- Ω load impedance [17]. In this matching network, the pad capacitance is in parallel with Z_{out}

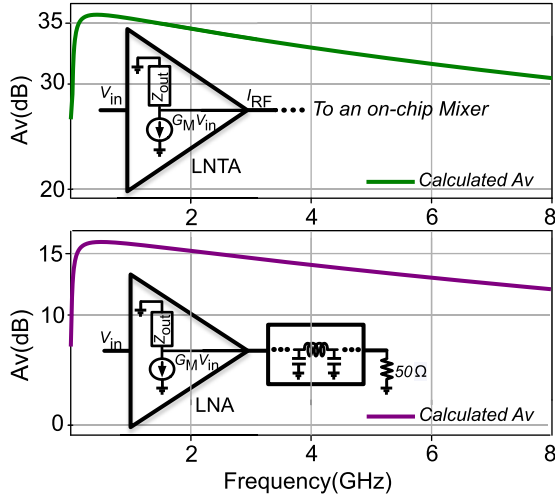


Fig. 8. Calculated A_v from (12) (top) when the amplifier is self-loaded in the LNTA mode and (bottom) when the amplifier is loaded by $50\ \Omega$ through matching network in the LNA mode.

where the equivalent impedance is in series with the wire-bond inductance. The rest of the matching network is provided on the PCB by means of SMD capacitors and TLs, which makes the equivalent output impedance to be compatible with $50\ \Omega$.

To examine the effect of the $50\text{-}\Omega$ load impedance of the external test equipment on the gain of the proposed structure, (12) for A_v is plotted in Fig. 8. As expected, when unloaded, the voltage gain is high since Z_{out} is high.³ When the amplifier is loaded with $50\ \Omega$, the provided gain drops by ~ 20 dB.

Unfortunately, the technology scaling causes r_{ds} to be reduced. Also, by employing the pMOS transistors at the output node, the parasitic capacitances go up, resulting in more variation in Z_{out} at high frequencies. These are the main reasons that limit the LNTA bandwidth at high frequencies. To solve this problem, the inductive shunt- and series-peaking techniques can be used. The shunt inductive peaking causes a resonance at the output of each stage when the gain starts to roll off at higher frequencies [16]. It is worth mentioning that L_1 also helps to dampen the parasitic capacitance at the output node. By increasing L_1 from 240 pH to 1.2 nH, the 3-dB bandwidth can be extended from 7.5 to 9 GHz. The quality factor of L_1 improves the gain only marginally. Increasing it from 5.5 to 10 ($L_1 = 440$ pH), the gain improves only by 0.1 dB.

C. Noise Analysis

As mentioned earlier, the purpose of noise cancellation is to disassociate the input matching from the noise considerations by virtue of canceling the noise from the matching stage at the output node [9]. In the proposed LNTA, the current noise of the input transistor flows into node X, but out of node Y, causing two voltages with opposite phases. These two voltages

³When the LNTA transconductance drives an internal on-chip mixer, its voltage gain will actually be very low, but it can be recovered in the subsequent stages [18].

are converted into currents by M_2 – M_4 (meaning M_2 through M_4) [19]. However, the input signal appears at these two nodes at the same phase. Thus, the input signal is constructively combined at the output. The two noise voltages are calculated as $V_{nX}^2 = Z_{in}^2 I_{n,M1}^2$ and $V_{nY}^2 = Z_Y^2 I_{n,M1}^2$. Therefore, the output current noise due to the thermal noise of M_1 is as follows:

$$\begin{aligned} \overline{I_{n,out}}^2 &= \overline{V_{nX}}^2 (g_{m2} + g_{m4})^2 - \overline{V_{nY}}^2 g_{m3} = 0 \\ &\Rightarrow \frac{g_{m2} + g_{m4}}{g_{m3}} = \frac{Z_Y}{Z_X}. \end{aligned} \quad (13)$$

To reuse the current of M_2 , M_3 is chosen as a pMOS transistor. Also, the noise reduction technique is applied to improve the NF without any additional power cost. In this technique, M_4 is in-parallel with M_2 , and hence, the transconductance of M_4 is added to that of M_2 . Moreover, M_4 is selected as a pMOS transistor in order to be able to reuse the current of M_2 . The consequential increase of M_2 's transconductance reduces the channel thermal noise of the cancellation stage, thus avoiding any need for extra branches. Consequently, the improvement in NF is achieved without burning more current, as explained in Section II.

The most important noise sources in this noise cancellation scheme are the thermal noise of R_{D1} and the channel thermal noise of transistors M_2 – M_4 . The noise factor of the proposed LNA is equal to $F = 1 + F_{R_{D1}} + F_{M2} + F_{M3} + F_{M4}$, where the $F_{R_{D1}}$ term is given by the following relation:

$$\begin{aligned} F_{R_{D1}} &= \frac{4kTR_{D1}(g_{m3}|Z_{out}|)^2(Z_{o1}/(Z_{o1} + R_{D1}))^2}{4kTR_s A_v^2} \\ &\cong \frac{R_s}{R_{D1}} \end{aligned} \quad (14)$$

where, according to Fig. 6, $Z_{o1} = [r_{ds1} + (R_s || 1/sC_X || sL_s)(1 + G_{m1}r_{ds1})]$ and $Z_Y = R_{D1} || Z_{o1}$ when the parasitic capacitance at node Y is not considered for simplicity. A_v is the voltage gain of the LNTA, which is simplified by considering the noise cancellation and input-matching conditions, $(g_{m2} + g_{m4})R_s = g_{m3}R_{D1}$ and $Z_{in} = R_s = 1/G_{m1}$, respectively. The other constituting terms of the noise factor F are

$$\begin{aligned} F_{M2} &= \frac{4kTg_{m2}|Z_{out}|^2 \gamma}{4kTR_s A_v^2 \alpha} = \frac{4g_{m2}}{R_s(Z_Y G_{m1} g_{m3} + g_{m2} + g_{m4})^2 \alpha} \gamma \\ &\cong \frac{g_{m2}}{R_s(g_{m2} + g_{m4})^2 \alpha} \gamma \end{aligned} \quad (15)$$

$$\begin{aligned} F_{M3} &= \frac{4kTg_{m3}|Z_{out}|^2 \gamma}{4kTR_s A_v^2 \alpha} = \frac{4g_{m3}}{R_s(Z_Y G_{m1} g_{m3} + g_{m2} + g_{m4})^2 \alpha} \gamma \\ &\cong \frac{R_s}{|Z_Y|^2 g_{m3}} \frac{\gamma}{\alpha} \end{aligned} \quad (16)$$

$$\begin{aligned} F_{M4} &= \frac{4kTg_{m4}|Z_{out}|^2 \gamma}{4kTR_s A_v^2 \alpha} = \frac{4g_{m4}}{R_s(Z_Y G_{m1} g_{m3} + g_{m2} + g_{m4})^2 \alpha} \gamma \\ &\cong \frac{g_{m4}}{R_s(g_{m2} + g_{m4})^2 \alpha} \gamma. \end{aligned} \quad (17)$$

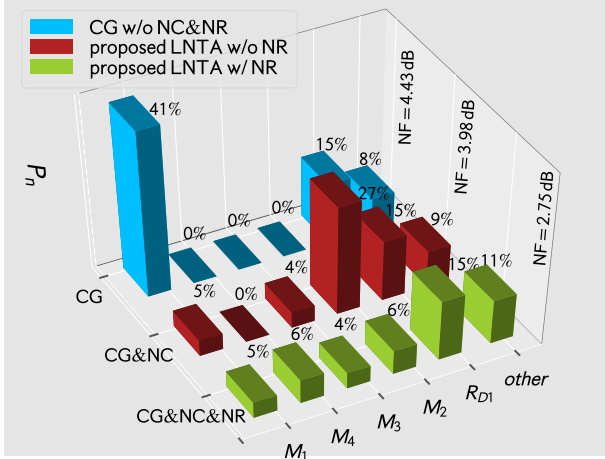


Fig. 9. Relative contributions to the total noise factor F of various circuit components at 800 MHz for CG structure (“CG w/o NC & NR”), the proposed structure without the noise reduction technique (“LNTA w/o NR”), and the proposed LNTA (“LNTA w/ NR”). Note: the complement to 100% is due to the 50- Ω antenna-terminal thermal source.

By considering the noise cancellation condition, (16) can be simplified as

$$F_{M3} = \frac{\gamma R_s}{\alpha |Z_Y|^2 g_{m3}} \cong \frac{\gamma R_s}{R_{D1}(g_{m2} + g_{m4}) R_s \alpha} \cong \frac{\gamma}{\alpha R_{D1}(g_{m2} + g_{m4})}. \quad (18)$$

Finally, the total noise factor of the LNTA is approximately given by

$$F \cong 1 + \frac{R_s}{R_{D1}} + \frac{\gamma}{\alpha R_{D1}(g_{m2} + g_{m4})} + \frac{\gamma}{\alpha R_s(g_{m2} + g_{m4})} \quad (19)$$

where the fourth component is the total noise factor due to M_2 and M_4 transistors. According to (19), to reduce the noise contribution of R_{D1} , its value should be increased, but this is limited by the voltage drop on R_{D1} . In addition, the channel thermal noise of M_3 can be decreased by enhancing g_{m2} . As suggested by (19), the noise factor of M_2 is decreased since g_{m4} is added to g_{m2} without any power penalty.

The simulated relative contributions of noise sources to the total noise factor, F , at 800 MHz are shown in Fig. 9. The proposed LNTA is compared with two other designs: 1) the CG topology shown in Fig. 1(a) without any noise cancellation and reduction techniques and 2) the proposed structure but without M_4 , i.e., without the noise reduction technique. In this comparison, the LNTA with and without M_4 consumes 4.5 mW with the same-size transistors. The size of transistor in the CG structure is the same as the size of CG transistor in the proposed LNTA, and also, its power consumption is exactly like the power consumption of the first stage in the proposed structure, which is about 1.5 mW.

As shown in Fig. 9, the CG structure (top row bars) suffers from high noise. The channel thermal noise of the main transistor, M_1 , is 41% of the total noise factor. By canceling its noise, the next highest contributor is M_2 . The second row

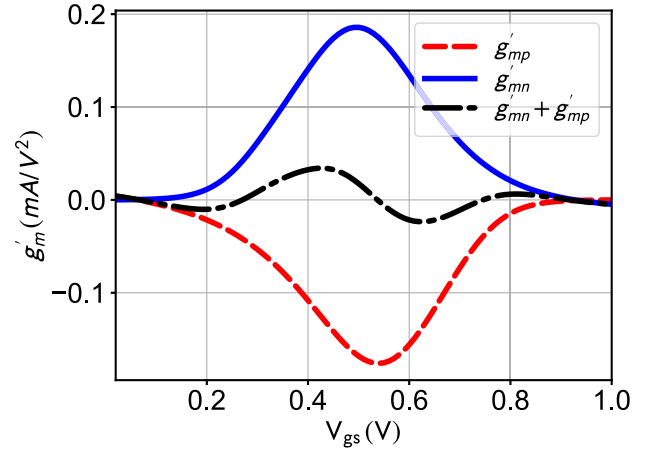


Fig. 10. Second-order nonlinear components of g_m of pMOS and nMOS transistors.

(CG & NC) shows that the thermal noise contribution of the main transistor, M_1 , is reduced to 5%, whereas the thermal noise of the cancellation transistor, M_2 , is added with a contribution of almost 27%. By using both the noise reduction (NR) and noise cancellation (NC) techniques (bottom row bars in Fig. 9), the thermal noise contribution of M_2 is decreased to 6%, thus improving the system noise performance. The thermal noise of R_{D1} is now dominant. According to the second term of (19), to reduce the noise effect of R_{D1} , its value should be increased. However, as mentioned before, the value of R_{D1} is limited by the supply voltage of the first stage, which should be at a certain level in order to provide the input matching. Therefore, to further improve the noise performance, a g_m -boosting technique by using M_0 is introduced. In this way, the amount of current of the first stage decreases as well as the voltage drop on M_1 . Consequently, the value of R_{D1} can be increased, leading to the decrease of NF. The g_m -boosting stage of M_0 boosts g_{m1} of input stage, $G_{m1} = (1 + g_{m0} R_{D0}) g_{m1}$, so the input matching can be provided with less current.

D. Linearity and Stability

Since the nonlinearity of a CS configured transistor is worse than that of the CG, the pMOS–nMOS structure placed at the output stage turns out to also improve the second- and third-order nonlinearities. By using a power series, the total output current of the pMOS and nMOS transistors in the complementary connection is equal to $i_{ds\text{tot}} = i_{dsP} + i_{dsN} = (g_{mN} + g_{mP})(v_g - v_s) + (g'_{mN} - g'_{mP})(v_g - v_s)^2 + (g''_{mN} + g''_{mP})(v_g - v_s)^3$, where g_m , g'_m , and g''_m are the first-, second-, and third-order derivatives of the transistor's composite (large-signal) drain–source current, i_{ds} , with respect to its composite gate–source voltage, v_{gs} . Since the ac input signal for the pMOS and nMOS transistors is out of phase, the total transconductance increases, whereas the total second nonlinear term, $g'_{mN} - g'_{mP}$, decreases [12]. Fig. 10 shows that by applying the noise reduction technique, the pMOS and nMOS transistors, M_2 and M_4 , in fact are like

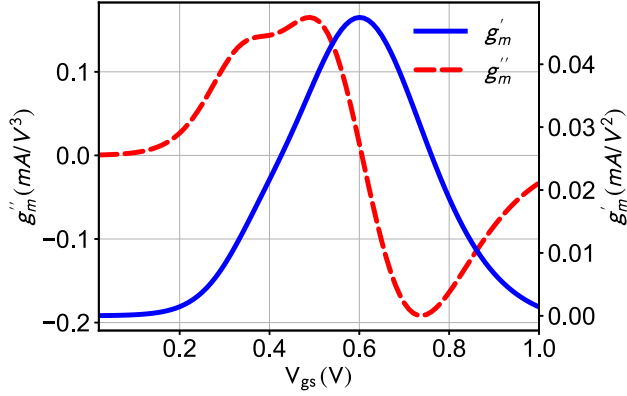


Fig. 11. Second- and third-order derivatives of the drain–source dc current, i_{ds} , with respect to V_{gs} of M_1 .

a complementary circuit in the output stage, which causes the second-order nonlinear components, g'_{mP} and g'_{mN} , to neutralize each other within the range of the bias voltage. As a result, the second-order nonlinear term is attenuated, and since the second-order nonlinear current can be mixed with the input by the feedback path through c_{gd} [12], both IIP2 and IIP3 are significantly improved. However, in this design, the pMOS–nMOS pair is not considered to be biased at the exact point where $g'_{mn} + g'_{mp} = 0$. The measured linearity variation due to different voltage biases of the pMOS–nMOS pair is less than 2 dB. It is worth mentioning that the linearity performance deteriorates a bit (<2 dB) by adding M_4 due to the lowering of the available voltage swing in the output stage.

Consequently, to improve the linearity of the CG transistor, it is biased in a “sweet spot.” According to Fig. 11, at the right bias voltage at which the third-order nonlinear component of the CG transistor, g''_m , is equal to zero, the IIP3 of the CG structure can be improved. It is worth mentioning that by modeling the circuit’s non-linearity via the Volterra series, it can be shown that the parasitic capacitance can also affect the second-/third-order nonlinearity cancellation based on the “sweet spot.” Although the sweet spot could be a bit shifted with frequency, it will be demonstrated in Section IV that the variation of measured IIP3 is within 1 dB across the entire bandwidth. The most important drawback of the sweet-spot technique is its sensitivity to the process corners [20], which might require process calibration. Another option could be a constant- g_m biasing circuit. Once the sweet spot has been calibrated for the process, the LNA is quite insensitive to temperature and voltage variations. The reason is that M_1 , located in the first stage, is mainly used for input matching, so its effective gain is small, and thus, its linearity contribution is not dominant and the signal provided to the second stage is still small. In other words, it is biased mainly to provide the required g_m for the input matching.

To examine the stability of the LNTA with an arbitrary source and load impedances, the Stern stability factor defined in (20) is often utilized [21]

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad (20)$$

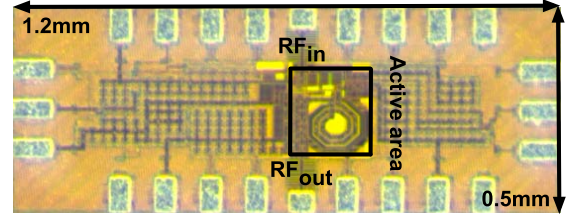


Fig. 12. Microchip photograph.

TABLE I
DEVICE DIMENSIONS

M_0	$(1\ \mu\text{m}/30\ \text{nm}) \times 15$	L_1	450 pH
M_1	$(1\ \mu\text{m}/30\ \text{nm}) \times 14$	R_{D0}	380 Ω
M_2	$(1\ \mu\text{m}/50\ \text{nm}) \times 26 \times 3$	R_{D1}	550 Ω
M_3	$(1\ \mu\text{m}/50\ \text{nm}) \times 32 \times 3$	C_{0-6}	3 pF
M_4	$(1\ \mu\text{m}/50\ \text{nm}) \times 27 \times 3$	–	–

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$ and S_{11} , S_{22} , S_{21} , and S_{12} are the input return loss, output return loss, forward gain, and reverse gain, respectively. If $K > 1$ and $\Delta < 1$, then the circuit is unconditionally stable [21]. According to (20), the stability of the circuit is improved by maximizing the reverse isolation.

IV. MEASUREMENT RESULTS

The proposed wideband LNTA, whose chip micrograph is shown in Fig. 12, is fabricated in TSMC 28-nm bulk LP CMOS. The device dimensions are shown in Table I. Although this amplifier is specifically designed to drive a mainly capacitive load of integrated mixers as a high-impedance transconductor (thus, LNTA), it is also capable of driving heavy external resistive loads. Hence, it can also function as an LNA with 50- Ω input and output ports. To avoid adding an extra test buffer for driving the output port, which would need to be separately characterized, all the performance and power consumption measurements are with the external load of 50 Ω . By carefully sizing the transistors and using the noise cancellation and reduction techniques (with current reuse), this amplifier operates at a 1-V power supply with a power dissipation of 4.5 mW while achieving remarkably high and flat small-signal gain and a very low NF in the whole wide bandwidth.

Measured S-parameters of the LNTA are shown in Fig. 13, which illustrates the best input return loss around 2.7 GHz (i.e., the input impedance is matched at this frequency). Although the input return loss gets worse away from this point, the wideband input-matching feature is well controlled as $S_{11} < -10$ dB in the whole bandwidth. The measurement results are well matched with the simulations. Fig. 14 shows the power gain that varies between 12 and 15.2 dB in the range of 20 MHz–4.5 GHz. By adding transistor M_4 , the second-stage transconductance in the presented LNA increases, resulting in more power gain, which is also expected from (12). Since the drains of three transistors, M_2 – M_4 , are connected to the output node, the total parasitic capacitance at this node increases. Hence, the –3-dB bandwidth of the proposed LNTA

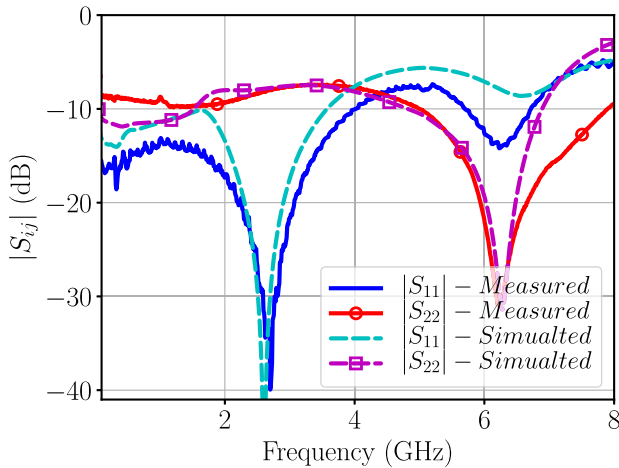


Fig. 13. Measured and simulated input-output return loss.

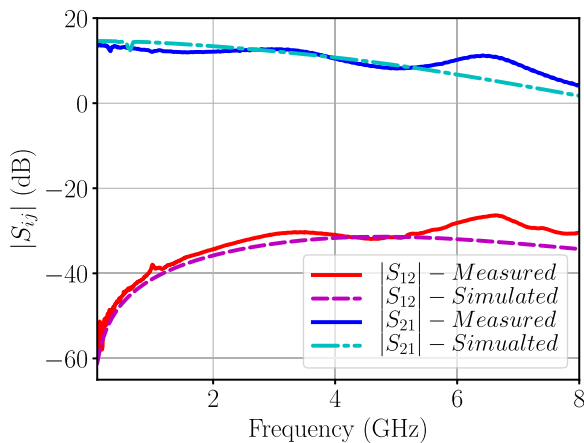


Fig. 14. Measured and simulated gain and isolation.

is partially decreased. However, L_1 helps to dampen the parasitic capacitance at the output node and compensate for the reduction in bandwidth. Unfortunately, the measurement results of the bandwidth fall short mainly because of the larger wire-bonding inductance and parasitic capacitance of the pad and PCB traces affecting the dominant pole at the external output port. It is worth mentioning that this issue is irrelevant in integrated receivers or if the LNA is followed by an integrated mixer on the same die.

The measured NF of the proposed LNTA is superimposed on the simulated NF in Fig. 15. It varies from 2.09 to 3.2 dB in the 4.4-GHz bandwidth. A two-tone RF signal at 500 MHz, 2 GHz, and 4 GHz (i.e., at the beginning, middle, and end of the band, respectively) is used to measure the wideband linearity performance. In order to examine the flatness of linearity, various two-tone spacings of 2.5, 10, 50, and 100 MHz are applied but, as expected, exhibit no difference in performance. As shown in Fig. 16, the measured IIP3 at 500 MHz with 10-MHz spacing, where the maximum gain is achieved, is -4.63 dBm, which is the minimum IIP3 in the entire bandwidth. Fig. 17 shows the measured IIP2 and IIP3 versus frequency. Note that in integrated designs, there is always a dc-blocking capacitor between the LNA and a passive mixer, so the dc will be blocked and low-frequency

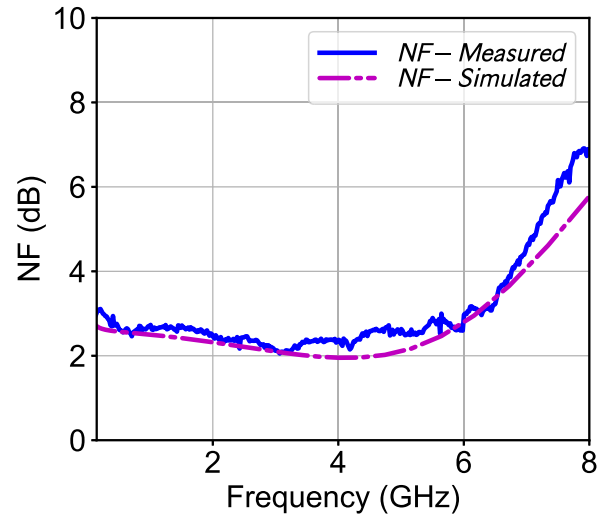


Fig. 15. Measured and simulated NF.

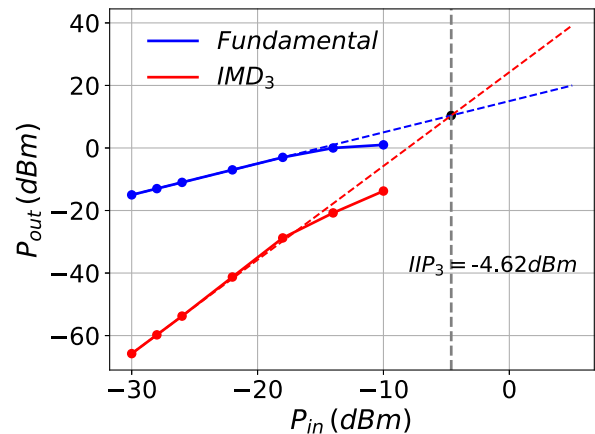


Fig. 16. Measured IIP3 at maximum gain.

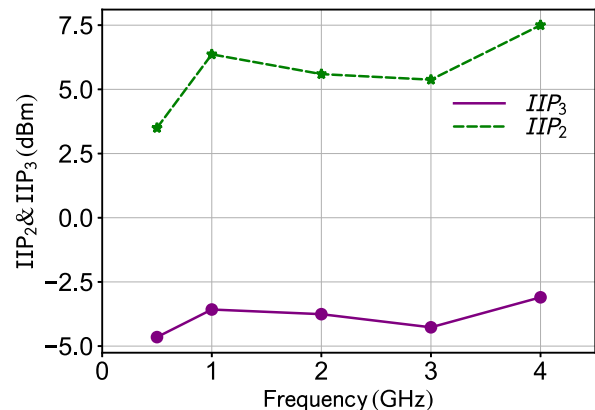


Fig. 17. Measured IIP3 and IIP2 versus frequency.

IM2 products will be heavily attenuated. Without the 50- Ω load, the simulations show the linearity of -8.7 dBm at the gain of 35.2 dB.

Finally, to verify the stability, the Stern stability factor (20), K , with Δ is plotted in Fig. 18 based on the measured data.

TABLE II
SUMMARY AND COMPARISON WITH STATE-OF-THE-ART WIDEBAND LNAs

	CMOS tech. [nm]	BW [GHz]	S_{11} [dB]	S_{21} [dB]	IIP3 [dBm]	NF [dB]	VDD [V]	Power [mW]	Active area [mm ²]	Noise cancel. used?	Can drive extern. 50Ω?	FoM ₁ [-]	FoM ₂ [-]	FoM ₃ [-]
This work	28	0.02~4.5	<-10	15.2	-4.62~-3.53	2.09~3.2[#]	1	4.5	0.03	Yes	Yes	7.76	327	172.6
[22] TCASIF'20	65	0.05~1.3	≤-10	27.5	-4~-1	2.3~3	1	5.7	0.046	Yes	No**	6.18	123.7	6.95
[23] TMTT'20	65	1~20	≤-10	12.8	1~5.8	3.3~5.3	1.6	20.3	0.096	Yes	No**	2.4	2.4	5.28
[24] TCASIF'19	65	0.05~1	≤-10	30	-10~-2.5	2.3~3.3	2.2	19.8	0.0448	Yes	No**	1.6	33.51	26.6
[25] TCASIF'19	65	0.4~2.2	-	16.4	-5	2~2.5	1.2	29	0.16	Yes	Yes	0.6	1.5	0.47
[26] TMTT'19	65	0.3~4.4	-	26.7	-14.2	3~4.4	1	13.7	0.009	No	No**	4.8	16	0.6
[27] TCASIF'19	65	0.5~7	-	16.8	-4.5	2.87~3.77	1.2	11.3	0.044	Yes	No**	3.5	7	2.48
[28] TCASIF'18	65	0.2~2.7	<-5	21.2	-2	3~3.5	1.2	0.96	0.05	Yes	No**	26.85	134.2	84.7
[29] TCASIF'18	180	2~5	-	13	-9.5	6~8	1.8	1.8	0.72	Yes	No**	1.85	0.93	0.1
[30] JSSC'17	180	0.1~2	-	17.5	10.6	2.9~3.5	2.2	21.3	0.63	Yes	Yes*	0.6	6.14	70.5
[31] JSSC'2016	130	0.6~4.2	<-10	14	-10	4~9	0.5	0.25	0.39	No	No**	20.8	34.7	3.46
[32] TMTT'16	130	0.1~2.2	-	12.3	-11.5~-9.5	4.9~6	1	0.4	0.0052	Yes	No**	8.6	86.2	9.68
[33] TCASIF'2014	90	3.5~9.25	≤-8	15	-16.3~-12	2.4	0.8	9.6	0.56	No	-	4.5	1.3	0.0823
[34] MWL'14	180	0.02~1.4	≤-10	16.4	-13.3~-9	3~4.7	1.8	12.8	0.04	No	No***	0.5	24.96	3.1
[35] JSSC'2013	65	0.1~10	≤-11	24	-15~-12	2.59~4.92	1.2	8.64	0.012	No	-	15.29	152.9	9.65
[36] TCASIF'2012	65	0.1~5.1	-	10.7	~6	2.9~5.4	1	6	0.03	Yes	-	1.75	17.52	69.7
[37] JSSC'12	130	0.1~2.7	-	20	-12	4	1.2	1.32	0.007	No	No***	13	130.3	8.2

* Single-ended load is 100 Ω. ** Uses add'l on-chip measurement buffer. *** Needs add'l external measurement buffer.
measured over 100 MHz–6.5 GHz

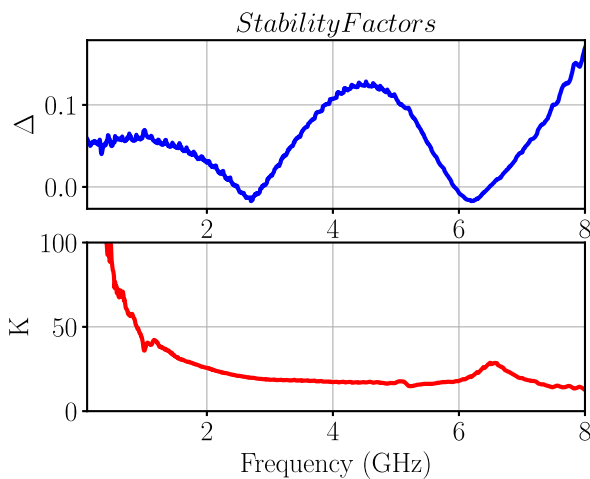


Fig. 18. Measured stability factors K and Δ .

As evident, the LNA is stable over the whole bandwidth, as $K > 1$ and $\Delta < 1$.

To compare the proposed LNTA with prior-art architectures and to emphasize the capabilities of reaching lower frequencies

in this wideband design, the following figures of merit (FoM₂ and FoM₃) are defined based on the original FoM (termed here FoM₁) introduced in [4] and the results are summarized in Table II

$$\text{FoM}_1 = \frac{\text{Gain}_{\text{av}}[\text{abs}] \times (f_H - f_L)[\text{GHz}]}{(F_{\text{av}} - 1) \times P_{\text{dc}}[\text{mW}]} \quad (21)$$

$$\text{FoM}_2 = \frac{\text{Gain}_{\text{av}}[\text{abs}] \times (f_H - f_L)[\text{GHz}]}{(F_{\text{av}} - 1) \times f_L[\text{GHz}] \times P_{\text{dc}}[\text{mW}]} \quad (22)$$

$$\text{FoM}_3 = \frac{\text{Gain}_{\text{av}}[\text{abs}] \times (f_H - f_L)[\text{GHz}] \times \text{IIP3}[\text{mW}]}{(F_{\text{av}} - 1) \times f_L[\text{GHz}] \times P_{\text{dc}}[\text{mW}]} \quad (23)$$

where F_{av} is the average noise factor, Gain_{av} is the average power gain over the 3-dB frequency range f_L to f_H , and P_{dc} is the power consumption. Even without any extra output buffer to mitigate the loading effects of the external 50-Ω termination, the proposed LNTA provides a very low NF and has competitive power consumption for the ultra-wide bandwidth (4.48 GHz), which is achieved by virtue of using both noise reduction and cancellation techniques. Moreover, the circuit has a competitive linearity and quite high power gain versus the other leading designs. As shown in the comparative landscape in Fig. 19, the proposed design achieves the best

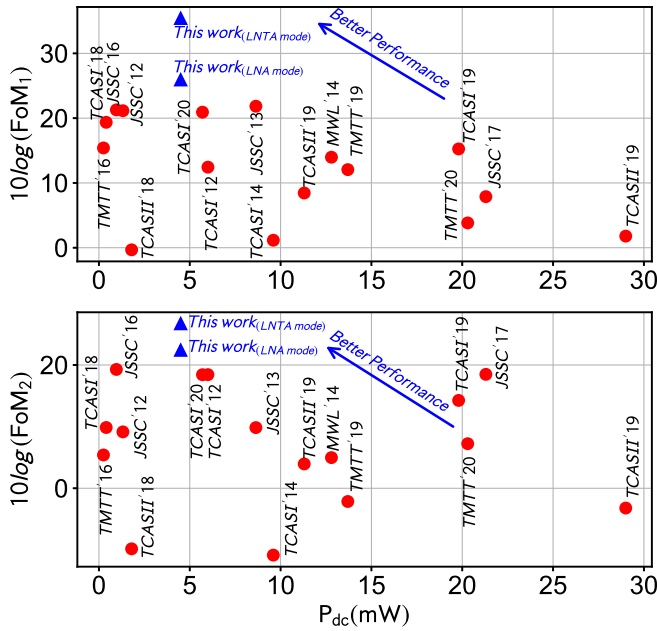


Fig. 19. FoM landscape of high-performance LNAs. Note: $FoM_{2,3}$ of our work in the LNTA mode (assuming a hypothetical test buffer) is based on a combination of measurements and simulations.

FoM among the recent state-of-the-art LNAs. Moreover, one of the main advantages of this architecture compared to prior reports is that it provides a high impedance at its output, which makes it suitable to drive an integrated passive mixer in a modern receiver. Despite the use of the additional on-chip (0.3 nH) inductor, the area still remains very competitive.

V. CONCLUSION

In this article, we present an ultra-wideband LN(T)A for sub-6-GHz 5G applications. A noise reduction technique is proposed that is based on a current-reuse approach and it is applied to the noise cancellation stage of CG to reduce the channel thermal noise of the following CS cancellation stage. By this method, the transconductance of the CS transistor is boosted, thus improving the NF without expending any extra power. The noise reduction technique is utilized, and by increasing g_m of the noise cancellation transistor, the total NF improves. The proposed architecture is designed as an LNTA with an intention to provide high impedance for driving a passive mixer in an integrated receiver. In addition, it can drive a 50- Ω load, which confirms that the proposed design can be used as a stand-alone LNA.

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