# Highly Integrated ZVS Flyback Converter ICs With Pulse Transformer to Optimize USB Power Delivery for Fast-Charging Mobile Devices

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***Abstract*— Flyback converter with USB power delivery is widely used for fast-charging mobile devices. However, conventional solutions have issues such as lower efficiency, higher cost, a large number of external components, and lower loop gain bandwidth. In this article, a high-efficiency zero-voltage switching (ZVS) flyback converter with primary- and secondary-side control ICs is proposed to solve the aforementioned issues with high integration level. The proposed control replaces optocoupler to achieve ZVS and secondary-side-regulation (SSR) by a pulse transformer. The ICs further integrate the USB power delivery (PD) controller and the constant voltage (CV)/constant current (CC) loop compensation to reduce external components. The proposed control and small-signal model are illustrated and verified by the experiment. The control ICs were fabricated in a 180-nm BCD process. The implemented 20-V/3-A/60-W USB PD flyback converter achieved 93.5% maximum efficiency using Si power switches. The feasibility of the proposed converter is verified by a thorough test of programmable power supply (PPS) with various CC/CV levels and load/line transients.**

***Index Terms*— Converter, constant voltage (CV)/constant current (CC), fast-charging, flyback converter, pulse transformer, USB power delivery (PD), zero-voltage switching (ZVS).**

## I. Introduction

USB power delivery (PD) supporting up to 100 W (20 V/5 A) has become a popular standard for mobile devices' fast-charging solution [1]–[3]. An adapter with the USB-PD specification has the advantage of supplying various devices with a single converter. For example, the converter with the input from the grid can provide a 5-V dc output voltage for cellphone load and a 19-V dc output voltage for laptop computer load. Thus, the carrying adaptors and corresponding electronic trash can be reduced. Moreover, the extended specification of USB PD includes a programmable power supply (PPS) which is suitable for fast-charging mobile devices. An adaptor with PPS can dynamically adjust the constant voltage (CV) and constant current (CC) output from 3 to 21 V with 20-mV resolution and 1 to 5 A with 50-mA resolution, respectively. This extended and accurately controlled output voltage and current enables the fast-charging function of mobile devices which greatly reduces charging time and improves user experience.

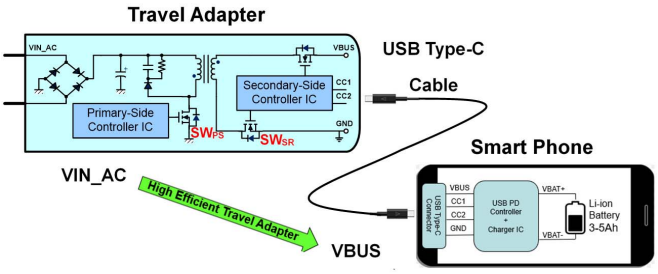


Fig. 1. Power system with USB PD for smart phone fast charging.

Flyback converter with the secondary-side-regulation (SSR) control scheme is often adopted in the USB PD adaptor for fast charging [2]–[7]. Fig. 1 shows the power system for smartphone fast-charging. An adapter with flyback topology converts the universal ac, VIN_AC, with 85–265 $V_{ac}$ to the dc output, VBUS. The flyback converter is widely used in below 100-W adapter applications due to its cost-effectiveness and electrical isolation of power transformer [6], [7]. The output of the adaptor is connected to the mobile device through USB type-C cable. USB PD protocol is implemented both in the adaptor and the mobile device to determine the output voltage and current supplied by the adaptor. Finally, a charger IC within the mobile device converts VBUS voltage to charge Li-ion battery. To meet such a wide range and fine resolution output voltage and current regulation, the flyback converter with the SSR control scheme providing the direct output voltage and current feedback is adopted [4]. Therefore, two ICs including primary-side (PS) and secondary-side (SS) controller ICs are required to control the PS switch $SW_{PS}$ and SS synchronous rectifier (SR) $SW_{SR}$ of flyback converter, respectively.

However, a flyback converter has issues to improve power conversion efficiency. A converter with higher efficiency reduces power loss and temperature rise, which are the keys for mobile charging. To increase the power conversion efficiency, using GaN devices or active clamp circuits is

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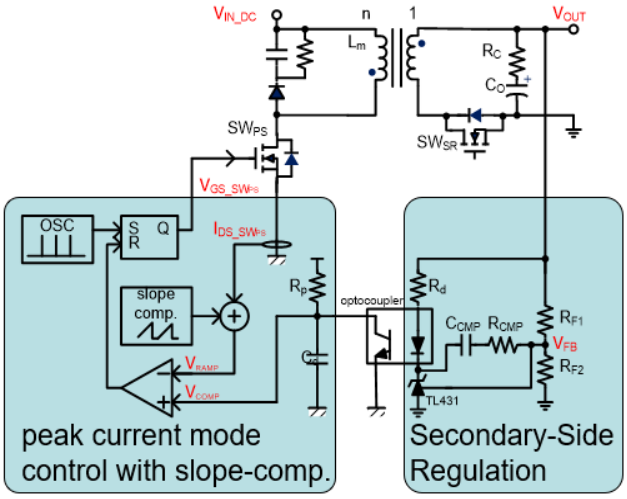


Fig. 2. Conventional flyback converter with SSR control.

possible solutions [7]–[10]. However, the number of external components and the cost is increased. Therefore, a technique to achieve zero-voltage switching (ZVS) at the PS switch by auxiliary turn-on the SR is used in this article [11]. This technique achieves higher efficiency than the quasi-resonance (QR) flyback approach [7], [12], [13]. This article further proposes the switch control method using the pulse transformer to achieve ZVS without extra component and added cost.

Besides, there are two issues for a conventional flyback converter with SSR control for USB PD, as shown in Fig. 2. The detail of Fig. 2 will be explained in Section III-C. First, an optocoupler is used to feedback the compensation signal from the SS to the PS with isolation [2], [5]–[7], [14]. The optocoupler has nonideal effects of current transfer ratio (CTR) variation with temperature/aging and extra low-frequency parasitic pole, resulting in the drawbacks such as lower loop gain bandwidth and possible stability issues of the feedback loop [2]. Second, the commercially available USB PD flyback converter solutions use an external USB PD controller IC and external shunt-regulator-based loop compensation. The loop compensation in the SS requires several external components including TL431, $R_{F1}$, $R_{F2}$, $R_d$, and compensation components $R_{\mathrm{CMP}}$, $C_{\mathrm{CMP}}$. Thus, component cost and board area are increased.

In this article, control ICs with high efficiency, high integration level, and reduced external components are proposed to solve the aforementioned issues of a flyback converter with USB PD. The ZVS/COMP transceiver with pulse transformer achieves both PS switch ZVS and compensation feedback from the SS to the PS. Thus, the converter achieves high efficiency without additional components and cost. Besides, it avoids the drawbacks of the optocoupler with a small pulse transformer, which package size is only 4.6 mm $\times$ 7 mm. To reduce the number of external components and make the adaptor more compact, the proposed ICs further integrate the USB PD controller and the CV/CC loop compensator with the internal programmable proportional–integral compensator (IPPIC).

The system overview of proposed control ICs is introduced in Section II. The concepts, circuit implementation, design, and small-signal model of the proposed ZVS flyback converter

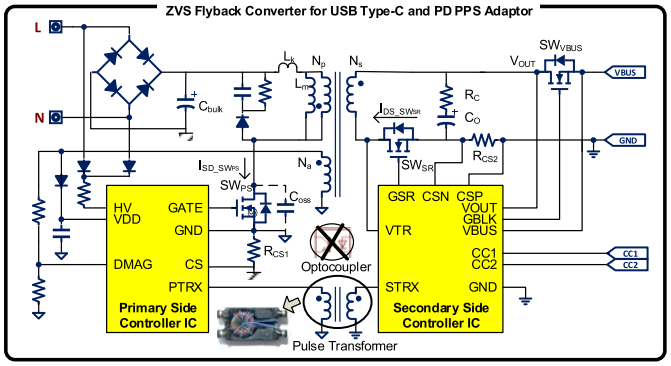


Fig. 3. Simplified circuit diagram of the proposed SSR ZVS flyback converter for the USB PD implemented by the PSC and SSC IC.

are illustrated in Section III. The measurement results are shown in Section IV, and Section V concludes this work.

## II. System Overview

Fig. 3 shows the simplified circuit diagram of the proposed ZVS flyback converter, which includes the two-chip solution for SSR and USB PD. The two chips are the PS controller (PSC) and the SS controller (SSC), respectively. The control ICs achieve high efficiency, high integration level, and reduced external components. The ac power passes through a full bridge diode rectifier, an input capacitor $C_{\mathrm{bulk}}$, and a flyback converter to generate a regulated dc output voltage $V_{\mathrm{OUT}}$. $L_m$ and $L_{\mathrm{K}}$ are the magnetizing inductance and leakage inductance of power transformer, respectively. $N_{\mathrm{p}}$ and $N_{\mathrm{s}}$ represent the turns of the transformer in the PS and SS. $N_a$ stands for the turns of transformer auxiliary winding. PSC IC controls the switching of PS power switch $\mathrm{SW_{PS}}$; SSC IC controls the switching of $\mathrm{SW_{SR}}$ in the SS. $R_{\mathrm{CS1}}$ is used to sense the PS current for the peak current mode control. $R_{\mathrm{CS2}}$ is used to sense the load current for the CC/CV regulation loop control. The output capacitor is represented as $C_{\mathrm{o}}$ in series with the equivalent series resistor (ESR) $R_C$. To get higher efficiency, ZVS control by the auxiliary SR switching is utilized to determine the turn-on timing of $\mathrm{SW_{SR}}$ and optimize efficiency. Besides, a pulse transformer is used to deliver the ZVS control signal and compensation signal. Compared with the conventional solution with TL431 and optocoupler, the integration level would be higher due to largely reduced external components.

Fig. 4 shows the block diagram of the PSC IC. The IC has an HV pin to provide fast startup from the 85- to 265-$\mathrm{V_{ac}}$ ac mains. A 600-V JFET is mounted in the same package with the PSC IC. The JFET is turned on during startup to quickly charge up VDD voltage. Then, the JFET is turned off after the power at the VDD pin is built-up by the auxiliary winding in order to reduce the quiescent current. The GATE pin switches the PS switch, $\mathrm{SW_{PS}}$, to deliver power to the output according to the loading condition. The peak current mode control with the slope compensation is used for the PWM control [5], [6]. The compensated signal comes from the ZVS/COMP transceiver at the PTRX pin. To isolate the ground of the PS and SS, a pulse transformer is used between PTRX and STRX.

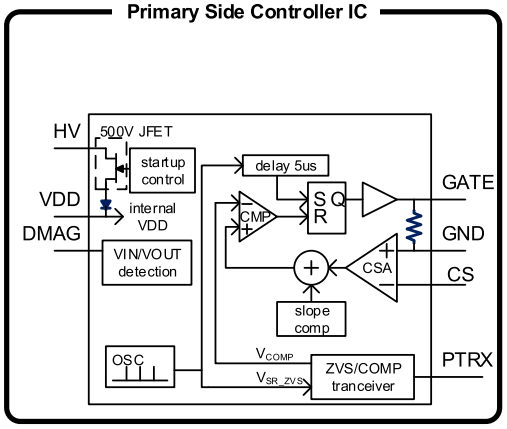


Fig. 4. Block diagram of proposed PSC IC.

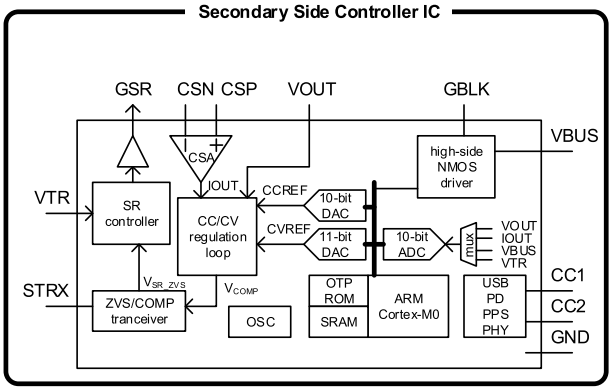


Fig. 5. Block diagram of proposed SSC IC.

There are four major functional blocks in the SSC IC including the SR controller, the internal CV/CC compensator, the ZVS/COMP transceiver, and the embedded Microcontroller Unit (MCU), as shown in Fig. 5. It is common to use the embedded 32-b ARM Cortex-M0 MCU to implement the USB Type-C PD controller IC due to the implementation requirement of the USB PD protocol. In the designed SSC IC, the MCU is not only used to implement the USB PD protocol but also controls and monitors the operating of the flyback converter to respond the smartphone during the fast charging. The MCU sets up the CV/CC compensator's reference DAC through the CC1 and CC2 pins according to the USB PD PPS protocol [1]. Besides, it also sets up various control parameters to optimize the converter's efficiency, stability, and transient response to meet fast-charging requests from the mobile device. By the SR controller, the flyback converter can achieve ZVS control by auxiliary SR switching. The VTR pin is used to sense the zero current in the SS and let the converter operate at DCM.

## III. Proposed ZVS Flyback Converter ICs

In this section, the key proposed concepts, the circuit implementation, the design, and the small-signal model of the proposed ZVS flyback converter ICs are illustrated.

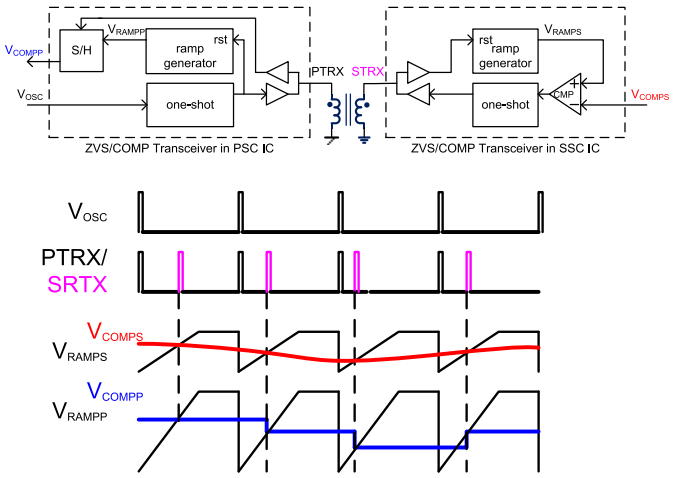


Fig. 6. ZVS/COMP transceiver function block.

### A. ZVS/COMP Transceiver

The top portion of Fig. 6 illustrates the functional block diagram of the ZVS/COMP transceiver in the PSC and SSC. The ZVS/COMP transceiver is used to transmit and receive the ZVS control signal and the compensation signal between the two galvanic isolated ICs from the pulse transformer. The bottom portion of Fig. 6 illustrates the steady-state waveforms of the converter. The inner oscillator generates pulses, $V_{OSC}$. It resets $V_{RAMPP}$ and sends the pulse to PTRX to reset $V_{RAMPS}$ through the pulse transformer. In SSC IC, $V_{COMPS}$, compensation signal from the internal CV/CC loop, crosses $V_{RAMPS}$ and generates one-shot pulse. This pulse sends to STRX through the pulse transformer. In PSC IC, this one-shot pulse is sent to the sample and hold (S/H) block. At this time, $V_{COMPP}$, compensation signal value for the peak current mode control with the slope compensation, is equal to the instant value of $V_{RAMPP}$. As SRTX is close to PTRX, $V_{COMPP}$ would be lower. On the contrary, when SRTX is far from PTRX, $V_{COMPP}$ would be larger. By controlling $V_{COMPP}$, the output voltage of the flyback converter is regulated.

### B. ZVS Control by Auxiliary SR Switching

ZVS operation can improve converter efficiency by reducing switching loss. If the charge stored in the parasitic capacitance $C_{DS}$ does not release before the switch turns on, there would be a voltage VDS across the switch. Thus, the $V_{DS}$ and the channel current IDS would cause some switching loss $P_{switching\_loss} = V_{DS} \times I_{DS}$. Besides, a dead time between the turn-on period of $SW_{PS}$ and $SW_{SS}$ is required to prevent the shoot-through phenomenon. However, long dead time may result in poor efficiency, so the accuracy of the dead-time period must be considered.

Fig. 7 shows the control method of auxiliary SR switching to achieve ZVS. By adding an auxiliary $SW_{SR}$ switching, ZVS of $SW_{PS}$ can be achieved without any extra components like active clamp circuits. After the SR controller receives oscillator signal through the pulse transformer, $SW_{SR}$ makes the auxiliary switching and induces a negative current on SS. When the auxiliary $SW_{SR}$ turns off, PS will generate negative

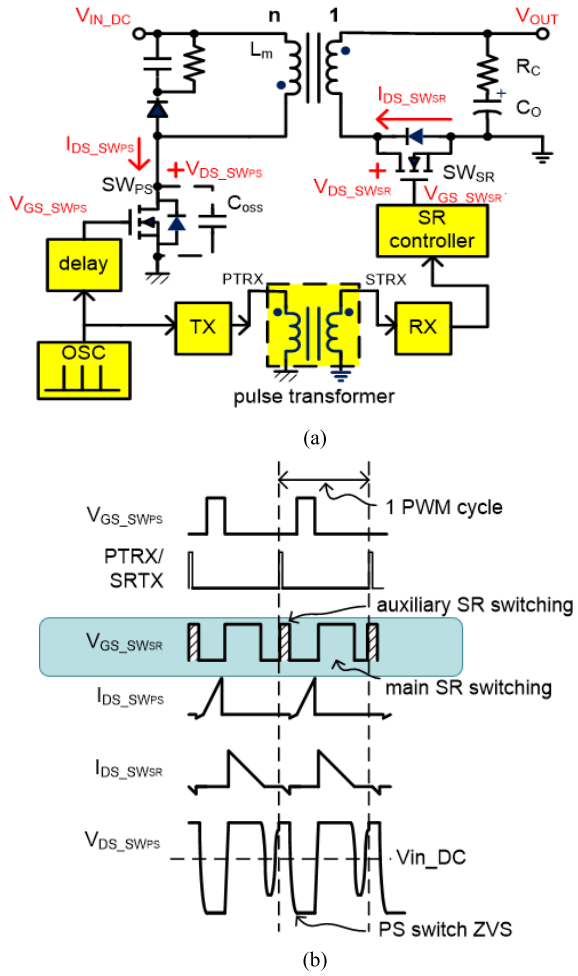


Fig. 7. Auxiliary SR switching control (a) function block and (b) waveform.

current to make the magnetizing inductor current continuously. This negative current will discharge Coss of $SW_{PS}$ and pull down the voltage across $SW_{PS}$. After a delay and low drain voltage is detected, $SW_{PS}$ turns on and achieves ZVS. After that, $SW_{SR}$ turns on to achieve synchronous rectification.

Fig. 8 illustrates the timing diagram of the proposed ZVS flyback converter. The auxiliary SR turn-on signal, $V_{SR\_ZVSP\_tr}$, is triggered by the OSC in the PSC at the predetermined switching frequency and sent out from the PTRX to the STRX pin. After receiving this signal at the STRX pin, the SSC turns on $SW_{SR}$ with the programmable on-time, $T_{ON\_ZVS}$, to create the negative current at the SS of the power transformer, $I_{DS\_SWSR}$, from $t_0$ to $t_1$. The magnitude of $I_{DS\_SWSR}$ is proportional to $T_{ON\_ZVS}$ and is set by the MCU based on the inductance of the power transformer, the parasitic capacitance at $SW_{PS}$'s drain node, $C_{OSS}$, and the input and output voltage. When both $SW_{PS}$ and $SW_{SR}$ are off from $t_1$ to $t_2$, the generated $I_{DS\_SWPS}$ discharges $V_{DS}$ of $SW_{PS}$, $V_{DS\_SWPS}$, which is built by the charge stored in $C_{OSS}$, to achieve ZVS of $SW_{PS}$.

When $V_{DS\_SWPS}$ detected at the DMAG pin of the PSC is lower than the set threshold, $SW_{PS}$ turns on at $t_2$. The on-time of $SW_{PS}$ is determined by the $V_{COMPP}$ signal, which corresponds to $V_{COMPS}$ in the SSC. $SW_{SR}$ turns on, while

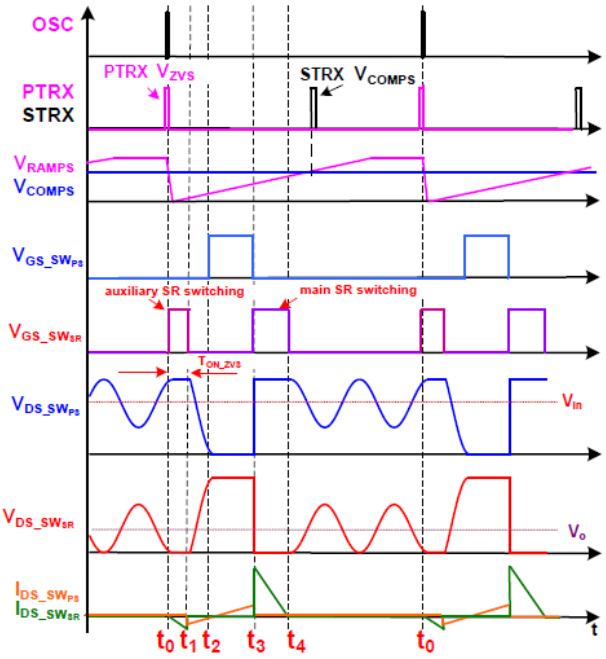


Fig. 8. Timing diagram of the ZVS flyback converter.

$SW_{PS}$ turns off at $t_3$. When zero-current of $SW_{SR}$ is detected at the VTR pin, $SW_{SR}$ turns off at $t_4$.

For the heavy load condition of the power converter, the PSC and SSC enable the ZVS to improve the efficiency; for the light load condition, ZVS is disabled to achieve a standby power of lower than 30 mW.

### C. Peak Current-Mode Control With Slope Compensation

Fig. 2 shows the circuit diagram of a conventional flyback converter with the optocoupler feedback. By the resistive divider comprising of $R_{F1}$ and $R_{F2}$, the output voltage $V_{OUT}$ is fed back to the error amplifier TL431. When $V_{FB}$, the resistive divider's voltage, is larger than the internal reference of TL431, the current of $R_d$ would increase. Through the optocoupler, the current of the optocoupler's transistor would also increase to reduce $V_{COMP}$. By comparing $V_{RAMP}$ and $V_{COMP}$, the duty cycle is determined. However, this method would need external components including TL431, resistors, and capacitors. Moreover, the optocoupler would have a larger delay time to deliver the signal. It would have a control accuracy issue.

The left portion of Fig. 9 illustrates the functional block diagram of the peak current mode control in the PSC. The current mode control is a dual loop control, which includes the outer voltage loop and the inner current loop. The outer voltage loop would sense the output voltage of the power stage and then generates the compensation signal through the ZVS/COMP transceiver and the pulse transformer to regulate the output voltage. The compensation signal from the outer voltage loop is compared with the current sensed by the inner current loop. From [18], a flyback converter with the peak current mode control is a two-pole two-zero system. To compensate the phase drop, an internal type II compensator is proposed to save external component counts. The so-called slope compensation

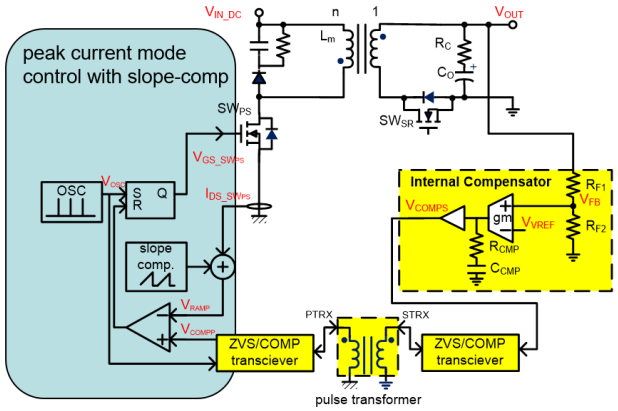


Fig. 9. Peak current mode control with slope compensation.

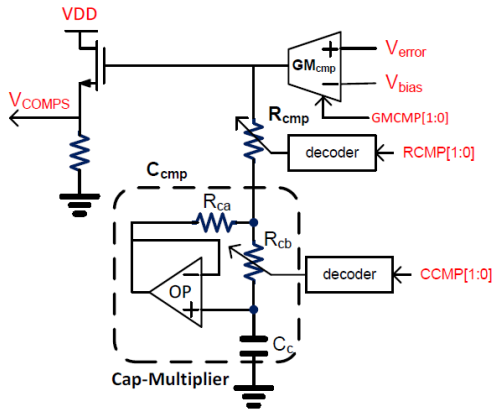


Fig. 10. IPPIC.

is used to improve current loop stability [19]. At the beginning of the $V_{GS\_SWPS}$ duty cycle, $V_{OSC}$ would be sent to the SR latch with a small delay. At this time, $V_{GS\_SWPS}$ will be set to a high level to turn on the switch. Until $V_{CCMPP}$ is larger than $V_{RAMP}$, $V_{GS\_SWPS}$ will be reset to a low level.

### *D. IPPIC for SS Compensation*

Fig. 10 shows the IPPIC circuit. In this IPPIC, the transconductance operational amplifier with $R_{cmp}$ and $C_{cmp}$ series at the output is used as a proportional–integral compensator. In the proposed SSR ZVS flyback converter design, because the PS uses the peak current mode control, the compensator only requires a type II OTA compensator, which provides one pole and one zero into the close loop transfer function of the system. The capacitance-multiplier circuit, which consists of $R_{ca}$, $R_{cb}$, and a two-stage opamp with the common source amplifier, is used to reduce the capacitor's area. $R_{ca}$ is a 50-kΩ resistor, while $R_{cb}$ is a resistor string formed by four resistors and controlled by a 2-bit register. Thus, the equivalent capacitance value, $C_{cmp}$, is expressed as follows:

$$C_{cmp} = \left(1 + \frac{R_{cb}}{R_{ca}}\right) C_C. \tag{1}$$

With the cap-multiplier, the maximum capacitance could be 10 nF by 100 * 100 pF. The parameters $GM_{CMP}$, $R_{CMP}$,

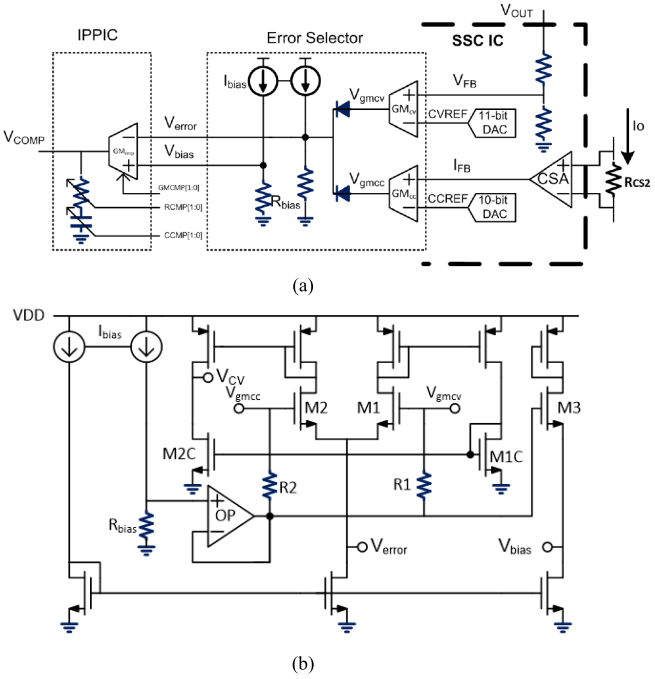


Fig. 11. (a) Internal CV/CC compensator circuit. (b) Error selector circuit.

and $C_{CMP}$ in Fig. 10 could be programed by the MCU based on the different operating conditions of the converter. Therefore, the transfer function of $V_{error}(s)$ to $V_{COMPS}(s)$ in this IPPIC can be derived as

$$\frac{V_{COMPS}(s)}{V_{error}(s)} = \underbrace{gm \cdot R_{cmp}}_{\textbf{Proportional}} + \underbrace{\frac{gm}{C_{cmp}} \cdot \frac{1}{s}}_{\textbf{Integral}}. \tag{2}$$

### *E. Internal CV/CC Regulation Loop*

To achieve accurately controlled output voltage and current for the fast-charging function of mobile devices, an internal CV/CC regulation loop is implemented. The top portion of Fig. 11(a) shows the internal CV/CC compensator circuit in the SSC. Two DACs with 11-bit and 10-bit resolution are used to set the reference voltage of the CV and CC loop, respectively. The feedback signal of the CV loop is sensed through a resistor divider from $V_{OUT}$, while the feedback signal of the CC loop is sensed through $R_{CS2}$ in Fig. 3 to obtain $I_O$ information. The dominated loop is selected by a diode-like circuit, error selector (ES). The IPPIC formed by the active gm-*RC* circuits is used to provide a proportional and an integral controller achieving high dc accuracy. Thus, the output voltage and output current can achieve 3–21 V with 20-mV resolution and 1–5 A with 50-mA resolution, respectively.

Fig. 11(b) shows the implementation of ES. The output currents of $GM_{CV}$ and $GM_{CC}$ flow into R2 and R1 to generate $V_{gmcc}$ and $V_{gmcv}$, respectively. The differential pair composed of M1 and M2 forms a two diode like circuit. The error signal, $V_{error}$, is M1 and M2's source node. Thus, the differential pair compares the input CV and CC error signals, $V_{gmcv}$ and $V_{gmcc}$. The larger one controls the output, $V_{error}$. M1C and M2C in companion with M1 and M2 form the output of the

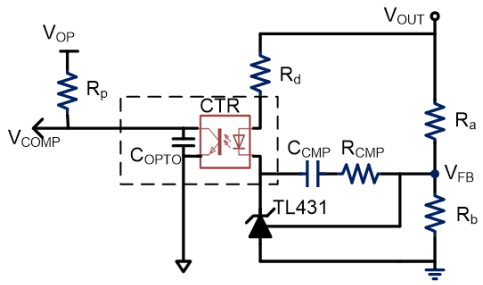


Fig. 12. Conventional CV regulation loop.

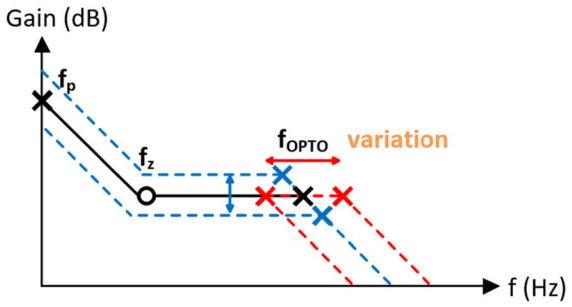


Fig. 13. Bode Plot of conventional type II compensator with optocoupler.

comparator, $V_{\rm CV}$, which indicates the current dominated regulation loop is CV or CC loop.

### *F. Small-Signal Model*

Fig. 12 shows the conventional CV regulation circuit. The optocoupler with the transfer gain, CTR, is usually used in the regulation loop for the isolation.

From the circuit in Fig. 12, the voltage gain from $V_{\rm OUT}$ to $V_{\rm COMP}$ ($G_{C\_OPTO}$) can be derived as

$$\begin{aligned} G_{C\_OPTO}(s) &= \frac{V_{\rm COMP}(s)}{V_{\rm OUT}(s)} \\ &= -\frac{CTR \cdot R_p}{R_a \cdot R_d} \cdot \frac{1}{sC_{\rm CMP}} (1+s(R_a + R_{\rm CMP})C_{\rm CMP}) \\ &\quad \times \frac{1}{1 + sR_pC_{\rm OPTO}}. \end{aligned} \tag{3}$$

In (3), $1/sC_{\rm CMP}$ is the compensator's pole, and $(1 + s(R_a + R_{\rm CMP})C_{\rm CMP})$ is the compensator's zero. Because of the parasitic capacitance $C_{\rm OPTO}$ of the optocoupler, the transfer function adds the extra parasitic pole at $1/(1 + sR_PC_{\rm OPTO})$. Fig. 13 shows the Bode Plot of the conventional type II compensator with the optocoupler. $C_{\rm OPTO}$ increases as the current through the diode increases. Since this current may have some variation, the parasitic pole has a range and may limit the maximum bandwidth of the converter. In some applications, for example, while choosing PC817 as the optocoupler, $C_{\rm OPTO}$ would be up to 5 nF, and $R_P$ might be 20 kΩ [2]. Thus, there would be an extra parasitic pole at 1.59 kHz, which would limit the loop bandwidth seriously. Moreover, the CTR has a large variation that causes the variation of the designed loop dc gain and bandwidth, resulting in possible stability issue as illustrated in (3).

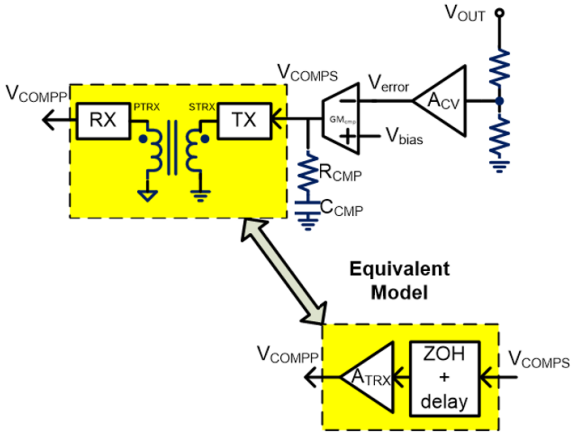


Fig. 14. Proposed CV regulation loop and small-signal model.

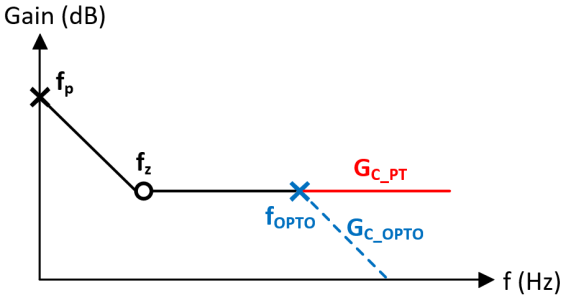


Fig. 15. Comparison of compensator bode plots.

Fig. 14 shows the equivalent circuit model of the proposed CV regulation loop. Since the proposed SSR ZVS flyback converter replaces optocoupler by the pulse transformer, the optocoupler's parasitic pole does not appear in the loop gain. ZVS/COMP transceiver behavior can be modeled by a dc gain $A_{\rm TRX}$ and a zero-order-hold (ZOH) plus delay. Therefore, the transfer function from $V_{\rm OUT}$ to $V_{\rm COMP}$ with the pulse transformer ($G_{C\_PT}$) can be derived as

$$\begin{aligned} G_{C\_PT}(s) &= \frac{V_{\rm COMP}(s)}{V_{\rm OUT}(s)} \\ &= -\frac{R_b}{R_a + R_b} \cdot A_{CV} \cdot GM_{\rm CMP} \cdot A_{\rm TRX} \\ &\quad \cdot \frac{1}{sC_{\rm CMP}} (1 + sR_{\rm CMP}C_{\rm CMP}). \end{aligned} \tag{4}$$

Fig. 15 shows the comparison of the Bode Plot of the proposed compensator gain $G_{C\_PT}$ with $G_{C\_OPTO}$. It can be seen that $G_{C\_OPTO}$ adds an extra parasitic pole at $f_{\rm OPTO}$, which is proportional to $1/(1 + sR_PC_{\rm OPTO})$. It reduces phase margin and the possibility to extend the control bandwidth of the loop gain.

For the proposed peak-current-mode control, the control-to-output voltage gain $G_{\rm vc}(s)$ can be derived as (5) according to the model in [2]

$$G_{vc}(s) = A_{vc} \frac{\left(1 + \frac{s}{\omega_{\rm ESR}}\right)\left(1 - \frac{s}{\omega_{RHP}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)\left(1 + \frac{s}{\omega_{P2}}\right)}. \tag{5}$$

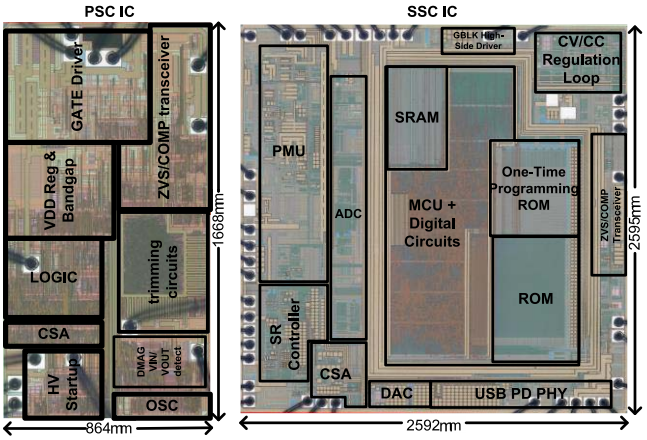


Fig. 16. Fabricated IC photograph of this work.

$G_{vc}(s)$ is a system with two poles and two zeros. There is a dominant pole ($\omega_{P1}$) at low frequency, which relates mainly to load resistance when the other circuit parameters are kept constant. The other pole frequency ($\omega_{P2}$) is determined by the duty cycle and the switching frequency and is located at the high frequency. There is a left-half-plane zero ($\omega_{ESR}$), the location of which is only related to the characteristics of the output capacitor. The right-half-plane zero frequency ($\omega_{RHP}$) is determined by the switching frequency and the duty cycle. The equation of $\omega_{RHP}$ can be derived as $\omega_{RHP} = 2f_S/D$ [2].

The CV loop gain of the system can be expressed as $G_{loop}(s) = G_{vc}(s) \times G_{C\_PT}(s)$. $G_{vc}(s)$ is the transfer function from $V_{comp}$ to $V_{out}$, while $G_{C\_PT}(s)$ is the transfer function from $V_{out}$ to $V_{comp}$. The multiplication of $G_{vc}(s)$ and $G_{C\_PT}(s)$ forms the CV loop gain. The compensator's zero in $G_{C\_PT}(s)$ is used to cancel the power stage's dominant pole $\omega_{P1}$ in $G_{vc}(s)$. By designing loop gain bandwidth smaller than $\omega_{RHP}$, $\omega_{P2}$, and $\omega_{ESR}$, proper phase margin can be achieved [2]. Since $G_{C\_PT}(s)$ does not contain parasitic pole at $f_{OPTO}$, the loop gain bandwidth will not be limited by $f_{OPTO}$. Thus, the output voltage load transient response can be improved [5].

## IV. Experimental Verification

Both the PSC and SSC IC are fabricated in an 0.18-$\mu$m CMOS BCD process. Fig. 16 is the die photograph of these two ICs, and the chip areas are 1.44 and 6.73 mm$^2$, respectively. The marked blocks can be mapped to Figs. 4 and 5.

Fig. 17 is a fabricated adaptor with the proposed SSR ZVS flyback converter. Table I shows the key components value of the fabricated converter. The input voltage $V_{in} = 90 \sim 265$ $V_{ac}$, output voltage $V_{out} = 5 \sim 20$ V, maximum loading current $I_{O\_MAX} = 3$ A, so the maximum power of this converter is 60 W. Because this designed work does not need active-clamp circuits to achieve ZVS switching behavior, the total volume of the converter is only 48.598 cm$^3$. The power density achieves 1.23 W/c.c (20 W/in$^3$). Besides, the external components are muchly reduced as can be seen from the PS and SS printed-circuit-boards.

Fig. 18 shows the experimental result of the ZVS control under heavy load conditions. In STRX waveform,

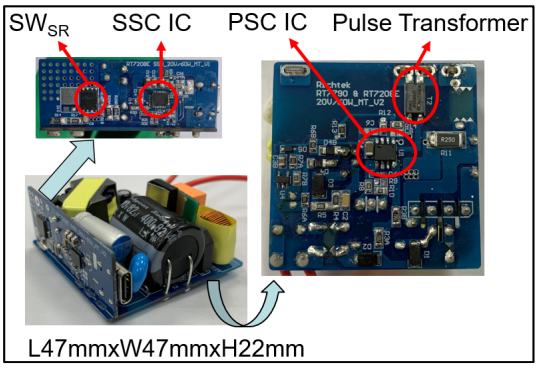


Fig. 17. Fabricated adaptor with the proposed SSR ZVS flyback converter.

TABLE I
KEY COMPONENTS VALUES OF THE FABRICATED CONVERTER

| Transformer | |
|---|---|
| Core Size | RM-8 |
| Material | PC95 |
| Primary Inductor | 210 $\mu$H |
| $N_P$ | 30 |
| $N_S$ | 5 |
| Capacitors | |
| $C_{OUT}$ | 1.15 mF /25V |
| $C_{BULK}$ | 100 µF /400V |
| Resisters | |
| $R_{CS1}$ | 125 mΩ |
| $R_{CS2}$ | 5 mΩ |
| Switches | |
| $SW_{PS}$ | IPA60R180P7, 180mΩ |
| $SW_{SR}$ | BSC050N10NS5, 5mΩ |

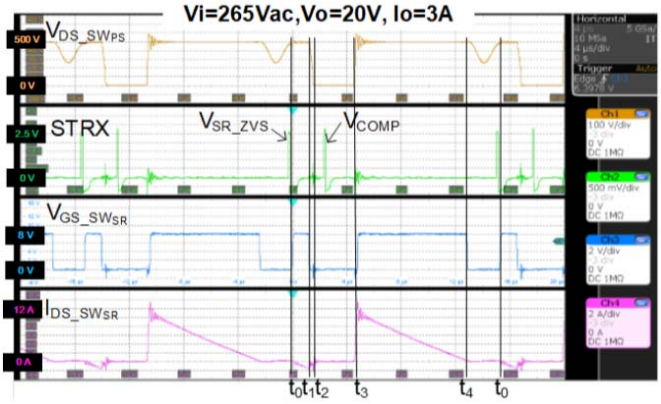


Fig. 18. Waveform of the ZVS control timing diagram (time scale: 4 $\mu$s/div.).

$V_{SR\_ZVS}$ represents the signal from PTRX through the pulse transformer at $t_0$. During $t_0$ to $t_1$, $V_{GS\_SWSR}$ would turn on to generate a negative current, which is shown in $I_{DS\_SWSR}$ waveform. After $V_{GS\_SWSR}$ turns off, the source–drain voltage of PS switch ($V_{DS\_SWPS}$) would drop down to zero at $t_1$ to $t_2$. During $t_2$ to $t_3$, $V_{GS\_SWPS}$ turns on with zero-voltage switching behavior. At this time, the compensation signal is sent to PTRX through the pulse transformer for peak current

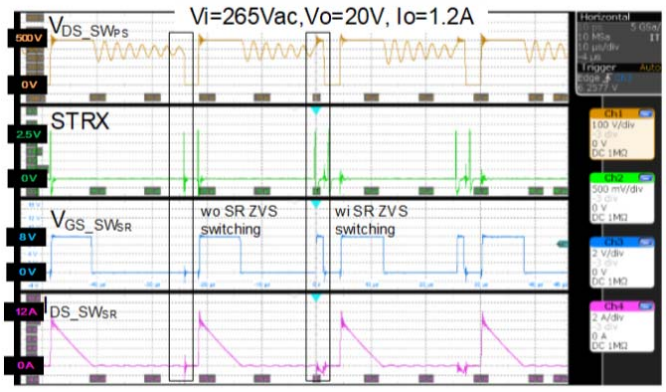


Fig. 19. Waveform ZVS control by auxiliary SR switching disabled at light-load (time scale: 10 $\mu$s/div.).

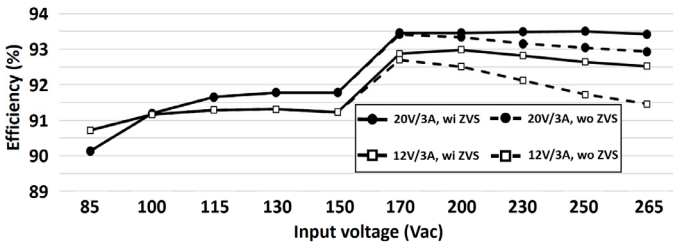


Fig. 20. Efficiency versus the input voltage.

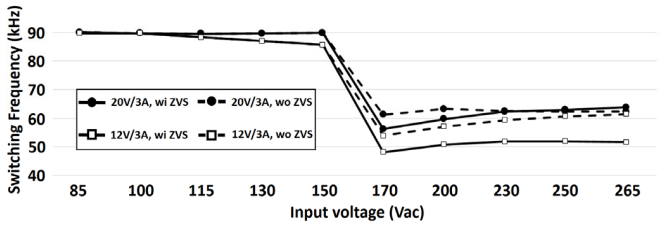


Fig. 21. Switching frequency versus the input voltage

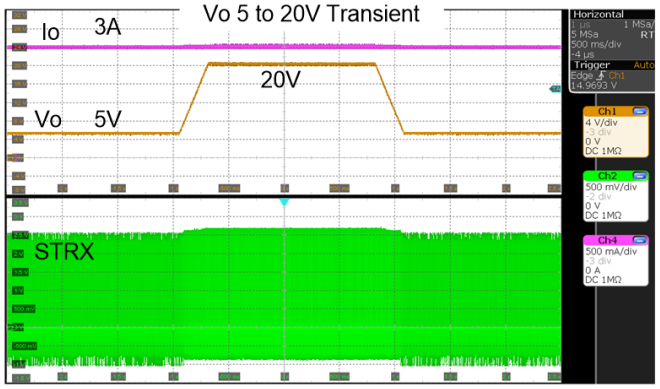


Fig. 22. Reference voltage transient from 5 to 20 V at 3-A load current for USB PD specification (time scale: 500 ms/div.).

mode control. During $t_3$ to $t_4$, $V_{GS\_SWSR}$ turns on for an SR. Finally, $V_{GS\_SWSR}$ turns off at $t_4$ for DCM operation. Under the light load condition, the conduction loss and the switching loss caused by the negative current and auxiliary switching, respectively, for ZVS reduce the efficiency of the converter. Therefore, the ZVS control would be disabled when the output current is lower than 1.2 A. Fig. 19 shows the waveform with ZVS control by auxiliary SR switching disabled at light-load.

The efficiency versus the input voltage at 12- and 20-V full-load 3-A output with ZVS is shown in Fig. 20. The maximum efficiency of 93.5% is reached at 265 $V_{ac}$/20 V. The dotted line shows the efficiency when the proposed ZVS control by auxiliary SR switching is disabled. This indicates that this work provides a feasible way to improve the efficiency of the flyback converter with the Si-based power MOSFET. When the input voltage is higher than 170 $V_{ac}$, the improvement of efficiency is about 1%. This is because PS switching loss increases with input voltage. At high input voltage conditions, ZVS behavior has significant improvement on efficiency. When the input voltage is lower than 170 $V_{ac}$, the ZVS is disabled to reduce the payload of auxiliary SR switching, though the controller works at QR mode and still has high efficiency of more than 90%.

The frequency versus the input voltage at 12- and 20-V full-load 3-A output with ZVS is shown in Fig. 21. Fig. 22 shows reference voltage transient from 5 to 20 V for USB PD specifications. The output voltage can be regulated from 5 to 20 V when the output current is equal to 3 A. Besides, Table II shows the detailed experimental load regulations under

TABLE II

EXPERIMENTAL LOAD REGULATIONS UNDER DIFFERENT LOAD AND OUTPUT VOLTAGE

| Input Voltage | Output Voltage | Measured (V) | | | Load Regulation Specification |
|---|---|---|---|---|---|
| | | 0% | 50% | 100% | |
| 90Vac/60Hz | 5V | 4.932 | 4.927 | 4.922 | $V_{OUT}$ ± 5% |
| 265Vac/50Hz | | 4.932 | 4.927 | 4.922 | |
| 90Vac/60Hz | 9V | 8.953 | 8.947 | 8.941 | |
| 265Vac/50Hz | | 8.953 | 8.946 | 8.940 | |
| 90Vac/60Hz | 15V | 14.948 | 14.938 | 14.934 | |
| 265Vac/50Hz | | 14.947 | 14.936 | 14.927 | |
| 90Vac/60Hz | 20V | 19.961 | 19.944 | 19.942 | |
| 265Vac/50Hz | | 19.960 | 19.939 | 19.928 | |

different load and output voltage. All the load regulations meet the specification of 5% error.

The experimental CV accuracies for various conditions are shown in Table II. With the test conditions of the universal input voltages, 0%/50%/100% of the full load currents, and the output voltage setting from 5 to 20 V, the measured output voltage error is less than 2.12%, which meets the load regulation specification.

Fig. 23(a) shows the transient between CV and CC mode. The CC current threshold, $I_{out\_cc\_set}$, is 3.3 A. As load current is up to 3.3 A, the total system would enter CC mode. On the contrary, the system would enter CV mode when the output load is lower than 3 A. It can be seen that smooth mode

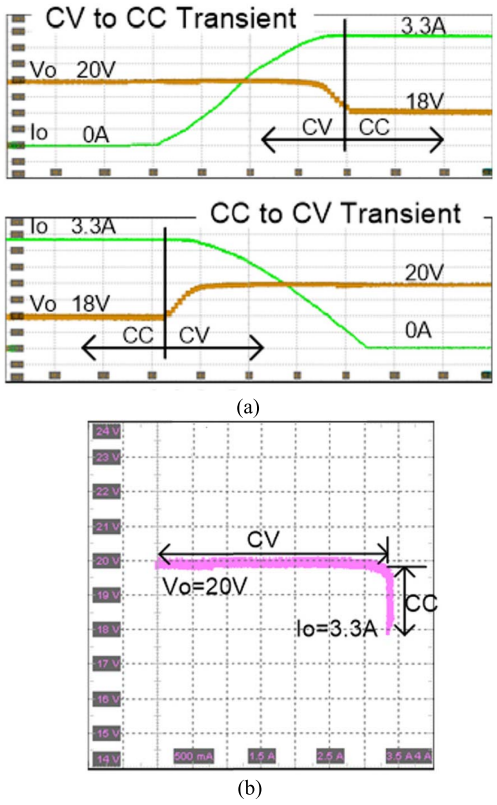


Fig. 23. CC/CV transient waveform. (a) CV-CC. (b) $I$–$V$ curve.

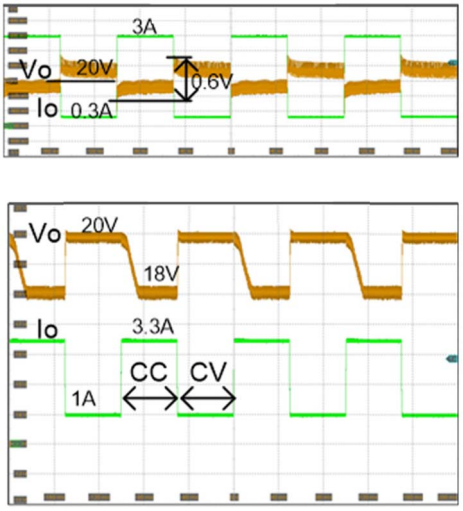


Fig. 24. Dynamic load transient waveform. (a) Io < Iref. (b) Io > Ire.

transitions are achieved. The relationship between CC and CV is discussed in Fig. 23(b). It is obvious that the system would enter CC mode when the output load is closed to 3.3 A. Moreover, Fig. 24(a) illustrates the variation of output voltage when the output load is changed from 0.3 to 3 A. When the output load is changed from 1 to 3.3 A, the system would operate between CC mode and CV mode. As the waveform is shown in Fig. 24(b), the output voltage did not regulate after entering CC mode.

TABLE III
COMPARISON TABLE

| | This work | innoSwitch3 [20] | APEC'18 [8] | TIA'17 [4] | TIE'16 [13] |
|---|---|---|---|---|---|
| Technology | 180nm BCD | NR* | NR | NR | 0.35um BCD |
| Topology | ZVS by SR | QR | ACF | ZVS by SR | QR |
| Power MOSFET | Si | GaN | Si/GaN | Si | Si |
| Number of primary-sideswitch | 1 | 1 | 2 | 1 | 1 |
| Signal Isolation | Magnetic | Magnetic | Optocoupler | Not need | Optocoupler |
| IC Used in Converter | PSC, SSC | INN3379C-H302 | UCC28780, UCC27712, UCC24612 | FPGA, XMC45000 MCU | QR controller |
| USB PD Controller | Integrated | External | External | External | NR |
| Regulation Loops | Internal CV/CC | Internal CV/CC | External CV | External CV | Internal CV |
| Max. Power | 60W | 60W | 30W | 65W | 40W |
| Power Density | 1.132W/c.c | 1.256W/c.c | 1.83W/c.c | 0.885W/c.c | NR |
| Lm | 210uH | 515uH | 85uH | 77uH | 400uH |
| Max. Frequency | 90.01kHz | 77.35kHz | 180kHz | 270kHz | NR |
| Input Voltage | 85-265Vac | 85-265Vac | 70-320Vac | 120-230Vac | 90-264Vac |
| Max. Output V/I | 20V/3A | 20V/3A | 20V/1.5A | 20V/3A | 14V/2.85A |
| Max. Efficiency | 93.5% | 93.8% | Si: 93.5%; GaN:95.8% | 85% | 89.1% |
| Die Size [$mm^2$] | PSC: 1.44, SSC: 6.73 | NR | NR | NR | 2.2 |

NR*: Not reported.

Fig. 25 illustrates the comparison between the small-signal model and the measurement result of CV loop gains. With three different compensator designs, the crossover frequency would vary from 1.7 to 6 kHz. In these cases, the phase margins also vary from 72° to 32°. The small-signal model is almost fit with the experimental result. With this model, the phase margin of the loop gain can be determined precisely.

Table III summarizes the performance of this work and compares it with the prior-art designs. Not like the previous work [7], which integrates the primary power switch in one package [20], our solution uses an external Si power switch to get freedom on the power switch selection for different performance and cost requirements. Moreover, the thermal of the power switch can be better because it has its own package and can be positioned on the PCB freely without bundling the PSC IC. The efficiency of the designed SSR ZVS flyback converter with the proposed two ICs and Si power MOSFET for USB PD PPS applications is competitive with the published works with GaN switch or active clamped flyback (ACF) topology. Thus, the proposed ICs achieve similar high efficiency with lower cost because only one Si MOSFET PS switch is required. Reference [7], [20] uses GaN with the valley switching which does not achieve ZVS. Liu [8] uses

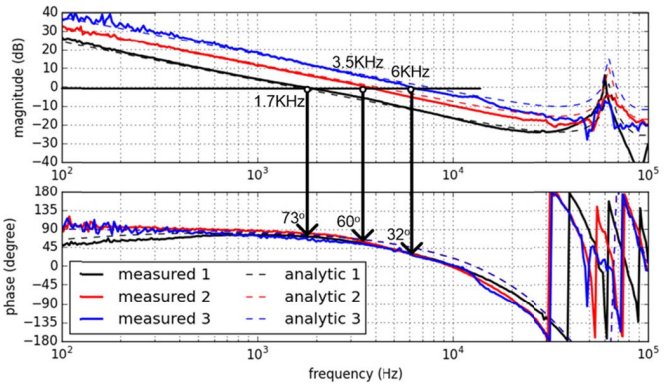


Fig. 25. Loop gain bode plot of CV mode.

ACF to achieve ZVS but with the cost of extra high side driver and GaN switch. The proposed solution is the optimization of cost and power efficiency. Even with lower cost, similar power density can be achieved with the comparison with other work. Furthermore, the proposed converter has fewer external components and a higher integration level by integrating the USB PD controller, internal CC/CV, and compensation components. The optocoupler for isolation is also replaced by a pulse transformer.

## V. Conclusion

A high-efficiency ZVS flyback converter is proposed with two control ICs for USB PD applications. The control replaces the optocoupler with a pulse transformer to transmit the SS-regulation signal to fulfill USB PD PPS for fast-charging mobile devices. ZVS signal for SR is also transmitted through the same pulse transformer to improve efficiency. The proposed two ICs are fabricated in 180-nm BCD process with chip areas of 1.44 and 6.73 $mm^2$, respectively. The highly integrated ICs reduce the external components. The implemented 20-V/3-A/60-W USB PD flyback converter achieved 93.5% maximum efficiency using only Si power switches. The converter power density is 20 $W/in^3$. The proposed ZVS control behavior is verified by the measured time waveform. A thorough test of USB PD specifications proves the feasibility of the proposed solution. The PPS test with various CC/CV levels show accurate SS regulations and smooth transitions between CC and CV modes.

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