

A 15-Channel Orthogonal Code Chopping Instrumentation Amplifier for Area-Efficient, Low-Mismatch Bio-Signal Acquisition

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Abstract—This article presents a 15-channel orthogonal code chopping instrumentation amplifier (OCCIA) for an area-efficient and low gain-mismatch multi-channel bio-signal acquisition. Orthogonal codes directly modulate each channel and merge into a single signal for sharing IA, while performing dynamic offset compensation with low power consumption. Digitization-before-demodulation (DBD) transmits the combined modulated data directly, which alleviates ripple noise, and completely removes the demodulation and TX encoding overhead from the ASIC. The proposed OCCIA in 0.18- μm 1P6M CMOS, when compared with the recent multi-channel instrumentation amplifiers (IAs), shows the smallest area (0.019 mm²/Ch.), low gain mismatch (0.43%), with the lowest power consumption (1.97 μW /Ch.) and low crosstalk (< -51.5 dB) at 490-Hz bandwidth.

Index Terms—Bio-signal acquisition, demodulation-before-digitization (DBD), instrumentation amplifier (IA), low mismatch, orthogonal code chopping (OCC).

I. INTRODUCTION

AS the life span of people increases and lifestyle is changed, there is a rapid increase in patients who suffer from heart diseases and brain diseases such as epilepsy and dementia. Compared with the 1900s, 19 million patients died from heart disease in 2010, which is a 40% increase. The 2.7 million patients passed away with Alzheimer's diseases, which were ranked in the top 10 diseases in 2010 [1]. Many researchers have studied to find the precursor to mitigate such diseases, and electrical bio-signal acquisitions, such

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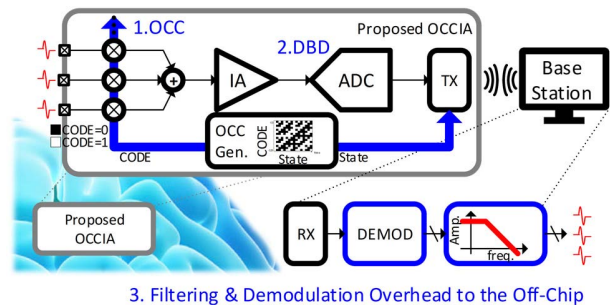


Fig. 1. Proposed OCCIA architecture.

as the electrocardiogram (ECG) and electroencephalogram (EEG), are widely chosen due to its convenience and non-invasiveness [2]–[4]. Their low temporal and spatial resolution, however, cannot offer fully sufficient information about patients' status for the delicate study and accurate monitoring [5]. The brain-machine interface also needs high temporal and spatial resolution bio-signal to send specific commands to the machine [6]. As the demands of more accurate monitoring and machine control are required, the implantable multi-channel bio-signal acquisition system-on-chip (SoC) has been widely developed to achieve higher temporal and spatial resolution [7]–[12]. With increased channel count, the SoC requires aggressive area and power reduction strategies, and especially for power-constrained implantable applications, low-power data encoding and transmission is a must [7]–[12].

To meet the aforementioned requirements, this article proposes an orthogonal code chopping instrumentation amplifier (OCCIA) with digitization-before-demodulation (DBD) scheme (Fig. 1). It exploits the orthogonal codes set that directly modulates and merges the multi-channel input data simultaneously for sharing a single instrumentation amplifier (IA), while reducing dynamic offset noise, power consumption, and inter-channel crosstalk at once. Sharing only a single IA among all channels will fundamentally reduce the gain mismatch while achieving power and area efficiency. DBD performs digitization prior to demodulation between chopping transitions, which leads to intrinsically ripple-free as compared to conventional chopping. As the merged signal is digitized

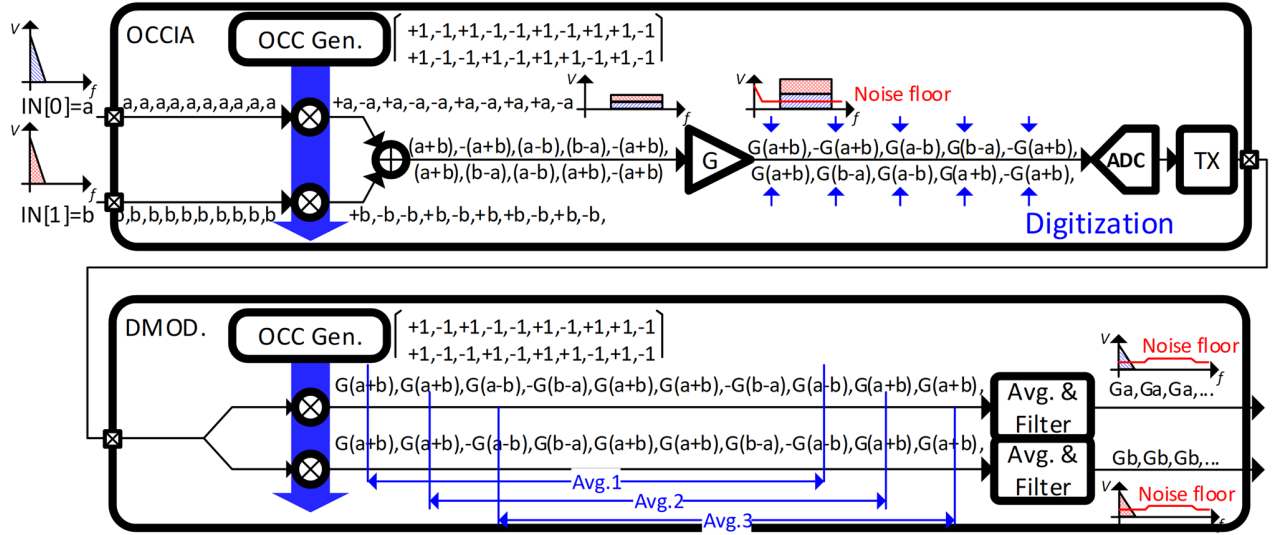


Fig. 2. Orthogonal Code Chopping (OCC) methodology.

and directly transmitted outside, DBD can relieve demodulation and TX encoding overhead from the power-constrained SoC. Such strategies are especially practical to reduce the power and area of multi-channel implantable devices that are suitable in the resource-constrained implantable environment.

This article is organized as follows. Section II illustrates the concepts of the orthogonal code chopping (OCC) and DBD and their benefits compared with other frequency modulations. Section III shows the circuit details in order to implement the proposed concepts. Measurement results and discussions are described in Sections IV and V, respectively. Finally, Section VI provides the conclusion.

II. ORTHOGONAL CODE CHOPPING AND DIGITIZATION BEFORE DEMODULATION

A. Orthogonal Code Chopping (OCC)

Fig. 2 illustrates the operating principle of the proposed OCC method [13]. Orthogonal codes set from the OCC generator (OCC Gen.), used as a chopping input, modulates all inputs into one spread spectrum in the higher frequency range. As the orthogonal codes keep the orthogonality of the modulated input spectrums, all the input signals are merged and capable of sharing a single amplifier. The orthogonal codes set also have the same benefit as chopping stabilizations, as the amplified signal frequency is higher than low-frequency noise such as flicker noise. Moreover, the spread signal is much more immune to frequency-specific interference.

After amplification, ADC digitizes the modulated signal, DBD, and TX transmits the digitized signal to the off-chip demodulator (DMOD) via a single communication channel. As the OCC already merges all the inputs, there are no needs of the additional modulator or serializer, which results in power and area saving. The separation of OCCIA with DMOD has another benefit regarding power reduction in the transmitting node that has more constraint of power and area; this is especially the case for multi-channel implantable sensors. The transmitted signal is multiplied with the orthogonal

codes set and averaged with further noise reduction. The signal orthogonality enables the signals to demodulate back into their respective original signals.

B. Comparison of the OCC With Other Multi-Channel Chopping in Instrumentation Amplifiers (IAs)

To further analyze the advantages of the OCC, Fig. 3 shows the quantitative analysis of the OCC compared with the conventional chopper-stabilization (Conv. Chop) [14]–[16] and the orthogonal frequency chopping (OFC) [17].

In multi-channel (# of Ch = N_{Ch}) Conv. Chop [14]–[16], IA and filter area ($A_{IA+Filter}$) overheads increase proportionally to N_{Ch} as

$$A_{IA+Filter} = N_{Ch} \cdot (A_{OTA} + A_{CIN} + A_{Filter}). \quad (1)$$

If the g_M/I_D ratio and gain are similar, IA power consumption is proportional to bandwidth (BW) as follows:

$$BW = g_M / (A \cdot C_L) \quad (2)$$

where BW is the bandwidth, g_M is the total transconductance of OTA, A is the voltage gain, and C_L is the load capacitance [7]. Assuming that total drain current of OTA (I_D) is proportional to g_M , (2) can be replaced by

$$BW = k \cdot I_D / (A \cdot C_L). \quad (3)$$

Even though OFC shares single IA by using orthogonal frequency modulation to reduce area overhead, the IA BW should cover the fastest chopping frequency as

$$f_{chopping,fast,OFCIA} = 2^{N_{Ch}-1} \cdot f_c \quad (4)$$

where f_c is the slowest (base) chopping frequency [17] and N_{Ch} is the number of channels. Equation (3) shows that chopping frequency increases exponentially with N_{Ch} to avoid harmonic distortion. In contrast, the BW of the OCCIA needs to cover

$$f_{chopping,fast,OCCIA} = (N_{Ch} + 1) \cdot f_c \quad (5)$$

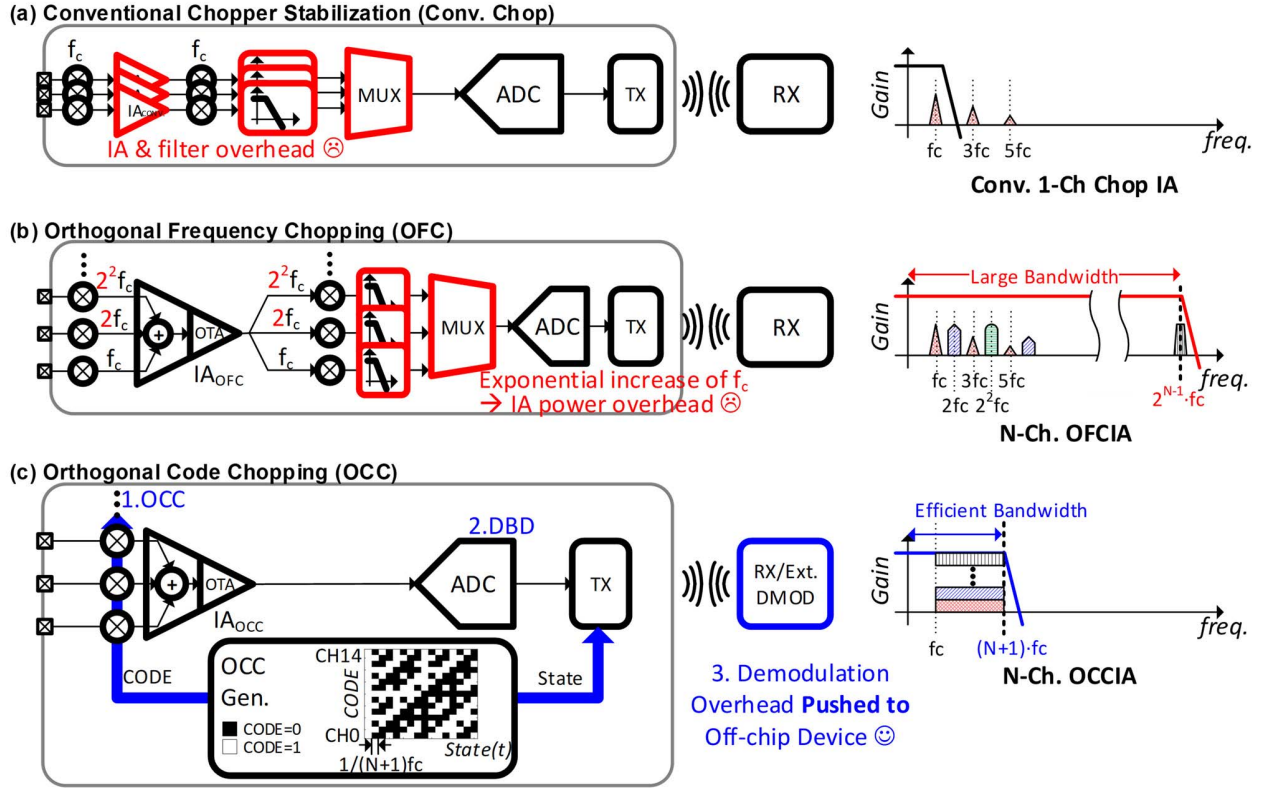


Fig. 3. Comparison between (a) conventional chopping stabilization (Conv. Chop), (b) OFC, and (c) OCC.

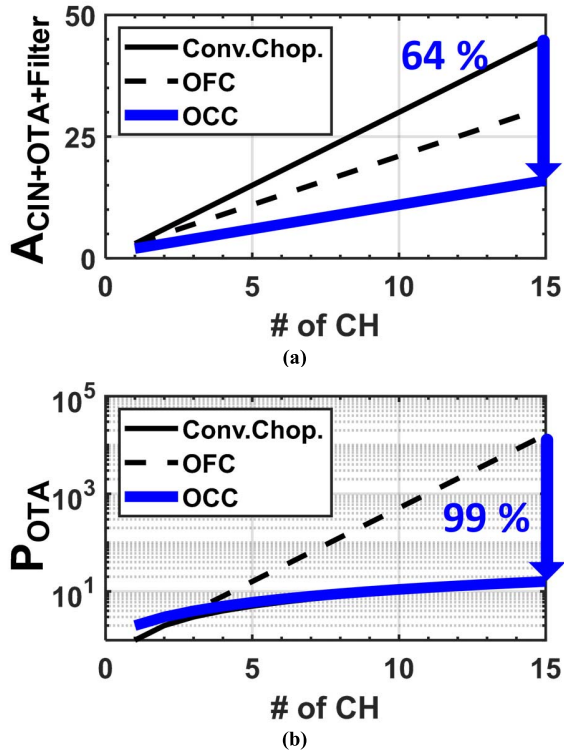


Fig. 4. Normalized (a) area and (b) power comparison of the OTA as increasing the number of channels.

that increases linearly with N_{Ch} , as OCC modulates and spreads the input spectrum while maintaining the orthogonality and dimming harmonic crosstalk. This leads OCC to take only the advantages of the OFC (superior area and gain

TABLE I

SUMMARIZED EQUATIONS OF CONV. CHOP, OFC, AND OCC

	Conventional Chop.	OFC	OCC
^a $A_{IA+Filter}$	$N_{Ch} \cdot (A_{OTA} + A_{CIN} + A_{Filter})$	$N_{Ch} \cdot (A_{CIN} + A_{Filter})$	$N_{Ch} \cdot (A_{CIN})$
^b P_{OTA}	$N_{Ch} \cdot P_{OTA, CONV}$	$2^{(N_{Ch}-1)} \cdot P_{OTA, CONV}$	$(N_{Ch}+1) \cdot P_{OTA, CONV}$

a: $A_{CIN}:A_{OTA}:A_{Filter}=1:1:1$.

b: $P_{OTA, CONV}$ is minimum OTA power of Conv. Chop to cover f_c .

mismatch) and the conventional IA (low power consumption compared to OFC at high N_{Ch}). Carefully considering an input range of the peak amplitude of the brain cortex (0.31 ± 0.07 mV) and low concurrent activation between different regions [18], we choose $N_{Ch} = 15$. Table I summarizes the relationship between power and area of the conventional chopper, OFC, and OCC, assuming that the area ratio of IA, filter, and input capacitor is 1:1:1 and that the most of the power consumption occurs in the IA. As shown in Fig. 4, at $N_{Ch} = 15$, the OCCIA achieves 64% area ($A_{CIN+OTA+Filter}$) reduction than the conventional chopping, as well as a 99% reduction in OTA power compared to OFC.

C. Number of Channels (N_{Ch}) and Its Design Considerations

We also analyze the maximum number of channels allowed by: 1) the dynamic range and sampling rate required from the ADC; 2) TX power/ N_{Ch} ; and 3) OCC generator (OCC Gen.) area/ N_{Ch} , to find the theoretical maximum number of channels for a given BW in OCC. First is the relationship between the number of channels (N_{Ch}) and the ADC bit widths (B_{ADC}). Considering the ADC minimal dynamic range of 45 dB to

TABLE II
RELATIONSHIP BETWEEN N_{Ch} , B_{ADC} , $f_{S,ADC}$, P/N_{Ch} , AND A/N_{Ch}

N_{Ch}	ADC Required		Ideal SAR ADC	
	$B_{ADC,min}$	$f_{S,ADC}$ (kHz)	P/N_{Ch} (nW/Ch.)	A/N_{Ch} (10^{-3} mm ² /Ch.)
1	7.97	1	25.1	0.2383
3	8.47	2	23.6	0.1123
7	8.97	4	28.7	0.0681
15	9.47	8	37.8	0.0449
31	9.97	16	51.8	0.0307
63	10.47	32	72.0	0.0214
127	10.97	64	101.1	0.0150
255	11.47	128	142.4	0.0106
511	11.97	256	201.0	0.0075
1023	12.47	512	283.9	0.0053
2047	12.97	1024	401.4	0.0037
4095	13.47	2048	567.5	0.0026

a. FOM is 100 fJ/Conv.

b. C_{UNIT} is 0.5 fF with 9.5×10^{-7} mm² at the 180 nm CMOS process. [26]

cover bio-signals [16], the minimum B_{ADC} should be 7.47. In OCCIA, the minimum ADC bit widths ($B_{ADC,min}$) is expressed as follows [19]:

$$B_{ADC,min} = 7.47 + \log_2 \sqrt{N_{Ch}}. \quad (6)$$

The sampling rate of the ADC ($f_{S,ADC}$) is determined by the code length (CL) that is determined by N_{Ch} as shown in the following equation:

$$f_{S,ADC} = f_{Nyquist} \cdot CL \approx f_{SAMPLE} \cdot N_{Ch} \quad (7)$$

where $f_{Nyquist}$ is the Nyquist sampling rate of the bio-signal-of-interest. Using (7), we can induce the ideal ADC FOM ($FOM_{ADC,Ideal}$) expressed as [20]

$$FOM_{ADC,Ideal} = P / (f_{S,ADC} \cdot 2^{ENOB}). \quad (8)$$

For the area analysis, an SAR ADC can be classified into a unit capacitor in the DAC (C_{UNIT}), a comparator, and a digital controller. Here, the digital controller size linearly increases with N_{Ch} , and the comparator size is negligible. The total area of C_{UNIT} (ΣC_{UNIT}) can be expressed as

$$\Sigma C_{UNIT} \propto 2^{ENOB}. \quad (9)$$

From (9), most of the area comes from C_{UNIT} . Table II summarizes the relation between N_{Ch} , $N_{ADC,min}$, and $f_{S,ADC}$ using (6) and (7), which corresponds to the power and C_{UNIT} area per channel of the ideal SAR ADC using (8) and (9), respectively. From Table II, we can find that P/N_{Ch} becomes significant at $N_{Ch} > 127$.

Data transmission overhead affects the choice of N_{Ch} . The latest high data rate of bio-medical communication is 12 Mb/s [21], which can cover up to 1023 channels [$f_{S,ADC}$ (512 kHz) \times [Code state (10 b) + B_{ADC} (13 b)] = 11.8 Mb/s]. As a result, the maximum channel can be 1023, and the optimal number is 15–31 in terms of digitization and data transmission.

The orthogonal code set is stored in the lookup table (LUT) in OCC Gen., and the LUT size in OCC Gen. also becomes a significant overhead when it comes to higher N_{Ch} . The area of LUT/ N_{Ch} is linearly proportional to N_{Ch} . Considering the area of D flip-flop cell area of 75 μ m² in 0.18- μ m CMOS process,

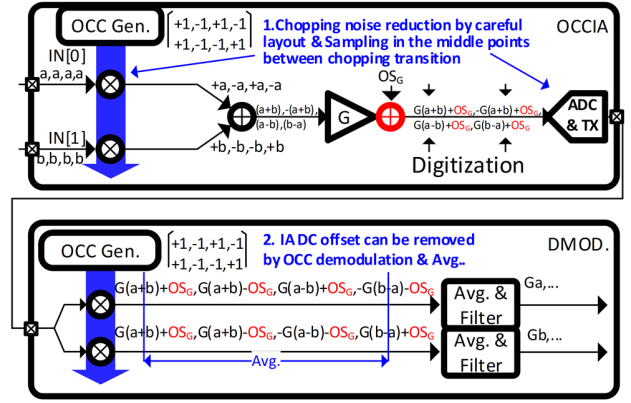


Fig. 5. DC offset (OS) analysis of OCCIA.

N_{Ch} should be less than 26 to occupy 10% of 0.02 mm², which is the state-of-the-art bio-signal SoC area/ N_{Ch} .

Second, we analyze mismatch and the crosstalk depending on N_{Ch} . Fig. 5 shows the OCCIA operation with chopping noise, the mismatch of the chopping switch, and the IA DC offset (OS_G). The common centroid layout and $1.5 \times$ larger than minimum sized chopping switch can minimize process mismatch. The digital sampling in the middle phase between the chopping transition can alleviate the chopping ripple noise; the DC offset from the IA (OS_G) will be reduced by the demodulation and average.

The IA output swing margin also contributes to the crosstalk; if the margin is too small, the output $G(a+b)$ will be distorted, which results in crosstalk. Thus, a sufficient output swing margin should be set up considering OS_G on the top of the output signal $G(a+b)$. From the analyses, we can conclude that N_{Ch} of 15–31 is the optimal value, and we chose 15 in this design.

D. Digitization Before Demodulation (DBD)

In terms of data communication, most bio-medical devices are preferred to have a single data communication channel via RF telemetry, inductive link, or ultrasound due to its area and power restriction [9], [22]–[24]. In order to use single-channel data communication, Conv. Chop and OFC demand channel multiplexer (CH-MUX) or signal encoder, which leads to additional power consumption and the increased chip area. Besides, the additional filter and the ripple reduction loop (RRL) are necessary to reduce ripple and glitch from the chopper that can distort the amplified signal. For example, Fan *et al.* [15] use RRL circuits that have two OTAs and several capacitors that need additional power and area. Chandrakumar and Markovic [16] have passive DC-blocking with 10-pF capacitor for ripple rejection, which results in the increasing area. The proposed DBD is applicable to solve such problems for low-power and area-efficient implantable applications; in conventional signal acquisition chain, digitization of the output signal is done after the analog demodulator and multiplexer for serialization as shown in Fig. 6. In contrast, OCCIA DBD scheme directly digitizes the amplified outputs prior to demodulation, thereby eliminating any need for analog

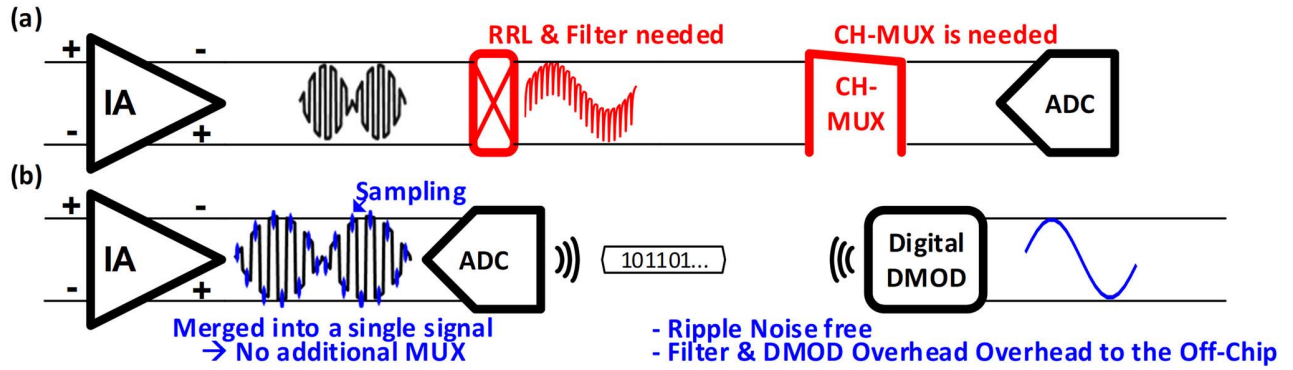


Fig. 6. Illustrations of (a) conventional demodulation system and (b) proposed DBD system.

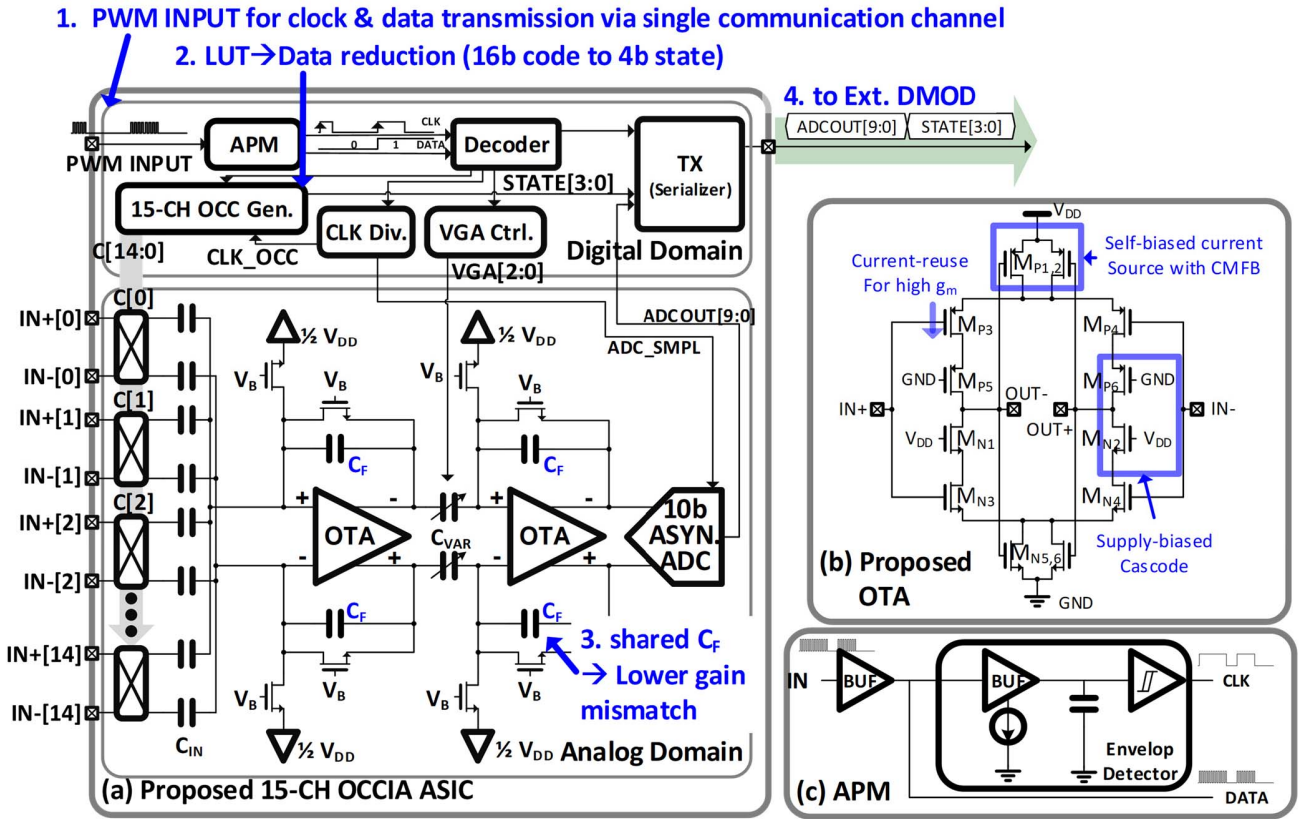


Fig. 7. (a) System block diagram. (b) Schematic of the self-biased fully differential OTA with current-reuse cascode. (c) Schematic of APM.

demodulators nor multiplexers. The ADC samples the outputs between chopping transitions, which significantly reduces the effect of chopping ripples. The direct merged data transmission to external demodulator relieves filter and demodulation overhead inside the chip, which results in power and area reduction.

III. CIRCUIT IMPLEMENTATIONS

Fig. 7 shows the overall system block diagram. As many implantable devices prefer to use a single communication channel such as an inductive link or an ultrasound (see [9], [22]–[24]), the proposed chip extracts the clock and the system parameters from the single incoming pulsewidth

modulated (PWM) programming data. The Decoder recognizes the number of pulses in 16 carrier clocks period to be DATA0, DATA1 as a parameter setting, and end-of-frame (EOF) as a protocol terminator; the distinct range of the number of pulses between DATA0, DATA1, and EOF can alleviate the communication error. PWM encoding has another benefit that it does not need additional clock synchronization circuitry consuming power. The amplifier programming module (APM) extracts the synchronized clock from the first rising edge of every pulse bursts. The current-controlled buffer and the Schmitt trigger enlarge the available carrier frequency by controlling charging speed, as shown in Fig. 7(c).

The orthogonal code generator generates one set of the OCC sequence (Walsh/Hadamard code) for each of the input

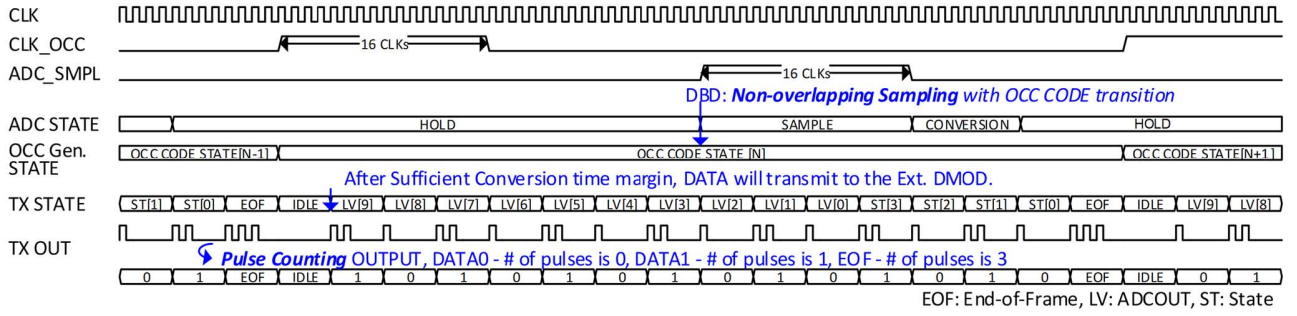


Fig. 8. Time waveform of the OCC Gen., ADC, and TX operations.

chopper switches via C[14:0]. LUT structure, synthesized by the automatically generated HDL, enables to send orthogonal 4-bit code state, instead of the entire 15-Ch. code itself.

The shared capacitive IA drastically reduces gain mismatch by sharing small feedback capacitor ($C_F < 100$ fF) that contributes to the gain due to PVT variation and layout. Depending on the bio-signal range, VGA uses a digitally controlled capacitor array to tune the gain delicately. Fig. 7(b) shows the self-biased fully differential OTA with current-reuse cascode, which achieves high gain and transconductance efficiency. Considering V_{TH} in 0.18- μm process, the lower V_{DD} of 1.2 V leads the proposed OTA to exploit the supply-bias itself, hence do not need any additional bias circuitry. As a result, the proposed design achieves 10% reduction in area and power consumption [25]. The output swing margin becomes smaller with the power-and-area aggressive design. Considering the input voltage range [18], the proposed OTA is acceptable. Single NMOS pseudo-resistor with a bias voltage of V_B is used for control of cut-frequency and fast setup of bias voltage. The thermal input noise of the proposed IA ($V_{N,in}^2$) is expressed as

$$\overline{V_{N,in}^2} = 8KT\gamma / (g_{MN3} + g_{MP3}) \quad (10)$$

where K is Boltzmann's constant, T is the temperature, γ is the coefficient, and g_{MN3}, g_{MP3} are the conductances of MN3 and MP3, respectively. From (3) and (5), integrated input noise ($V_{N,in,total}$) can be calculated as

$$V_{N,in,total} = \sqrt{8KT\gamma / (g_{MN3} + g_{MP3}) \cdot \pi / 2 \cdot BW}. \quad (11)$$

As multiplication of BW and $g_{MN3} + g_{MP3}$ is constant, optimal power consumption and $V_{N,in,total}$ between Conv. Chop. IA and OCCIA would be similar.

The asynchronous ADC modified in [26] samples and digitizes the shared OTA output between chopping clock transitions (DBD) for ripple suppression. The asynchronous scheme does not need a system clock, which can help to reduce power consumption. Also, monotonic digitization is used for efficient power consumption [27]. The TX (serializer) merges the orthogonal 4-bit code state of each channel and the associated ADC output.

Fig. 8 shows the timing waveform of the OCC Gen., ADC, and TX operations. Clock divider (CLK Div.) generates 64x slower the CLK_OCC and ADC_SMPL signals with the

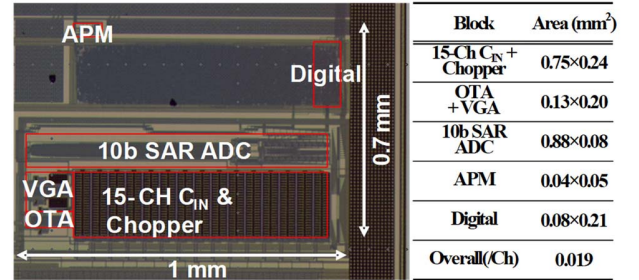


Fig. 9. Chip microphotograph.

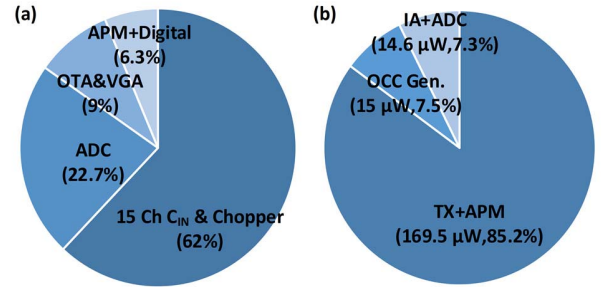


Fig. 10. (a) Area and (b) power breakdown.

synchronous CLK by the external device. OCC Gen. transits the code chopping set in the rising edge of CLK_OCC. After 32 CLKs, ADC starts to sample the output of the IA. This gives a chance that IA has enough time to amplify the signal for the robust DBD. TX output uses pulse counting for the immune of phase noise. Since the external clock is much faster than the TX output, the TX output can be converted with a low error rate.

IV. MEASUREMENT RESULTS

The proposed 15-Ch. OCCIA was fabricated in a 1P6M 0.18- μm CMOS, as shown in Fig. 9. As expected in Section II, 1-Ch. C_{IN}, OTA occupy a similar area of 0.012 and 0.013 mm², respectively [Fig. 10(a)]. Thanks to sharing an IA, VGA, and ADC among all 15 channels, the OCCIA occupies only 0.019 mm²/Ch. OCC Gen., IA, and ADC combined consume 29.6 μW , which translates to 1.97 $\mu\text{W}/\text{Ch}$. [Fig. 10(b)].

The demodulated output with a single-channel input (CH [0]) can be seen in Fig. 11 and Fig. 12. Crosstalk of 51.5 dB was measured when CH [0] inputs sinusoidal signal

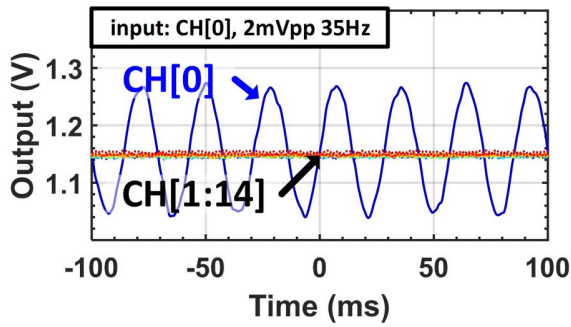


Fig. 11. Transient response of output amplitude.

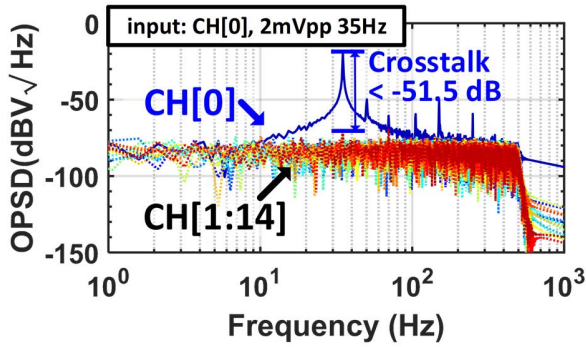


Fig. 12. Output power spectrum density (crosstalk < -51.5 dB).

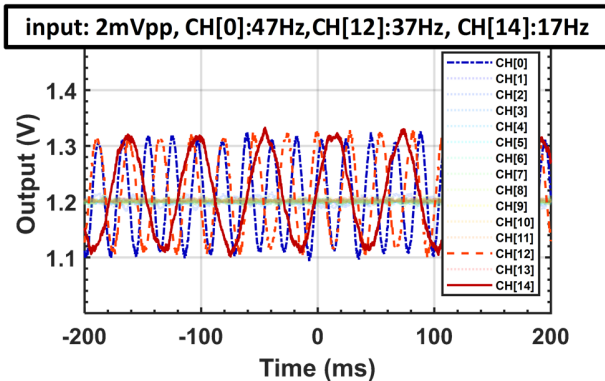


Fig. 13. Transient response of output amplitude with response to 3-Ch inputs.

with a frequency of 35 Hz. To see the crosstalk, the demodulated output was measured with 3-Ch. input, as shown in Figs. 13 and 14. The spectrum shows that no harmonics interference was observed in OCC due to the spread effect. Fig. 15 summarizes the mean amplitude and signal crosstalk of all the channels with each same input stimuli. The GBP curve shows the BW of 490 Hz and its low mismatch (0.43%) with 8th IIR low-pass filter; while the power-aggressive design of the OCCIA with finite linearity leads to limited crosstalk of -51.5 dB, this still satisfies the crosstalk criteria [10] with a sufficient margin at 15 Ch. As the demodulation can be operated in the digital domain, the output noise floor is estimated from the demodulated signals containing ADC and demodulation noise, instead of using the conventional method (e.g., dynamic signal analyzer).

Fig. 16 shows the measured input noise density with ADC and demodulation dynamic offset noise when OCC is

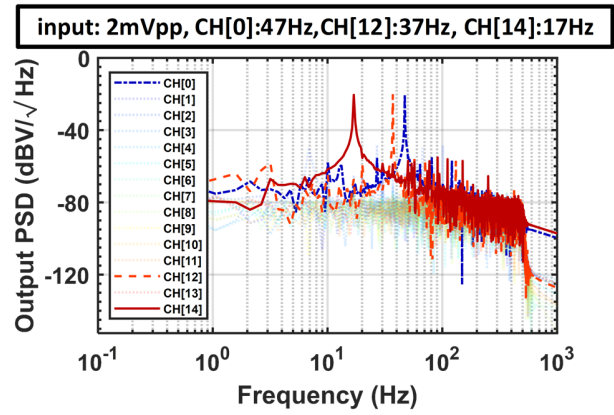


Fig. 14. Output spectrums of 3-Ch inputs.

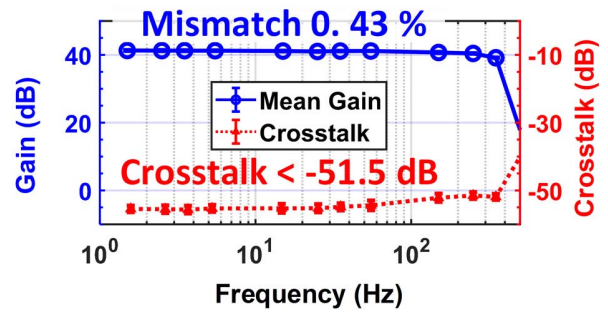


Fig. 15. Mean gain and crosstalk variance of all channels.

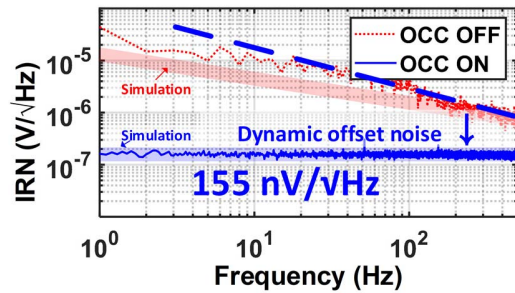


Fig. 16. Input referred noise curve with OCC ON/OFF.

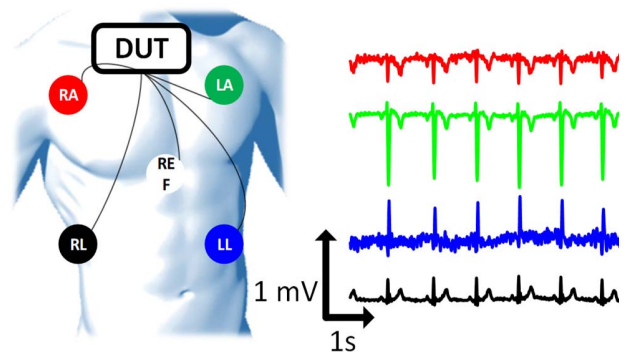


Fig. 17. Multi-channel ECG measurements.

activated. The dynamic offset noise in the low frequency is significantly reduced with the OCC activation. Measured input noise density is 155 nV/√Hz, including ADC and the off-chip OCC demodulator noise. Multi-channel ECG is also measured with OCCIA for an example of bio-signal

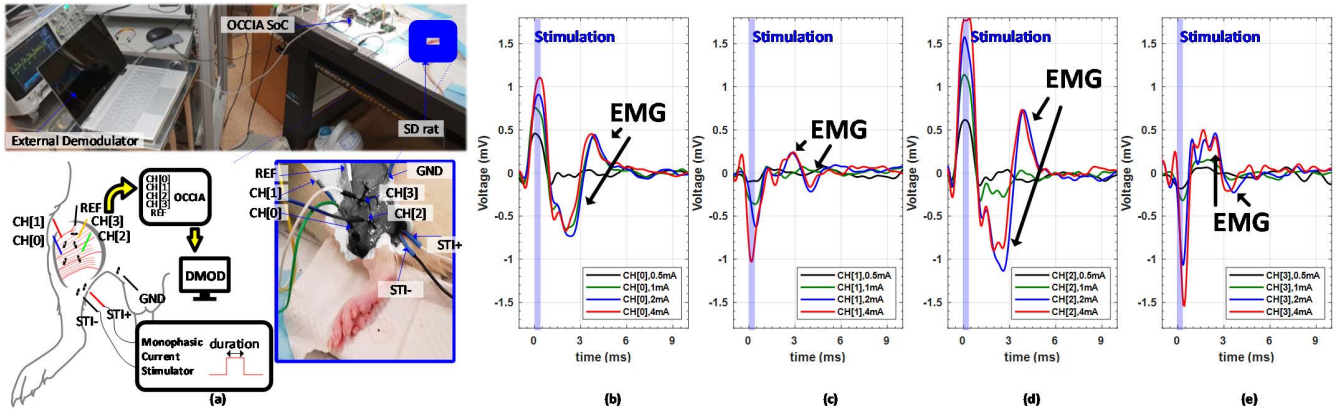


Fig. 18. Multi-channel EMG measurement. (a) Test configuration, and its results depending on the stimulus amplitude of (b) CH [0], (c) CH [1], (d) CH [2], and (e) CH [3].

TABLE III
PERFORMANCE COMPARISON

	This Work	Q. Fan JSSC'11 [15]	Y. Tsai, ISSCC'15 [17]	F. Michel, ISSCC'12 [30]	R. Muller, JSSC'15[9]	C. Lopez, JSSC'14 [8]	V.Majidzadeh, TBCAS'11 [10]
Methodology	OCC	Conv. Chop.	OFC	R-trim feedback	Chop $\Delta\Sigma$ rawData	ACT Electrode AC-couple	Ref. Shared
Area /Ch. (mm ²)	0.019^A	0.1 ^B	0.031 ^B	0.465 ^B	0.025 ^C	0.022 ^D	0.063 ^B
Power/Ch. (μ W)	1.97^A	1.8 ^B	40.5 ^B	25.2 ^B	2.29 ^C	7.02 ^C	7.92 ^B
Max. gain mismatch (%)	0.43(15-Ch.)^E	-	0.55(2-Ch.)	0.70	15.0	-	-
N. of Ch.	15	1	2	1	64	455	4
Crosstalk (dB)	-51.5	-	-83.2	-	-85.0	-44.8	-43.5
Supply (V)	1.2(analog) /1.5(digital)	1	3	1.2	0.5	1.8	1.8
Ch gain (dB)	40-56	40	40	20-60	30	29.5-72	39.4
Bandwidth (BW)	490	0.1-500	1k	1k-100k	500	0.2,6k	7.2k
Noise density (nV/ \sqrt Hz)	155 ^F	60	26.0B	40.0	58.0	41.3 ^G	39.4 ^G
NEF	7.25 ^F	3.3 ^B	3.74 ^B	7.50 ^B	4.76 ^C	3.08 ^B	3.35 ^B
Process (nm)	180	65	350	130	65	180	180

A. IA+ADC+OCC Gen.

B. IA

C. IA+ADC

D. Estimated by merging of IA and Electrode

F. Noise of IA+ADC+Demodulator, current from IA+ADC+OCC Gen.

E. Mismatch includes ADC + Demodulation error.

G. Estimated from IRN and BW with assumption of constant noise density.

acquisition, as shown in Fig. 17. Depending on the electrodes' position, 4-Ch. ECG shows the proper amplitude and its plus and minus sign. Fig. 18 shows the multi-channel electrically evoked subcutaneous EMG measurement from anesthetic SD rat's left leg using isoflurane. Depending on the electrodes' position Fig. 18(a), each channel shows the EMG within 5 ms after an artifact that is proportional to monophasic stimulus current amplitude with a duration of 200 μ s [Fig. 18(b)–(e)]. Chip performances are summarized in Table III, which shows that OCC achieves the smallest area, lowest power, and low gain mismatch among recent multi-channel chopping IAs.

V. DISCUSSION

The measurement results verify the proposed OCC scheme principle. By combining orthogonal code modulator [19] and multi-frequency chopping stabilizations [14], the proposed OCC successfully achieves: 1) low-frequency noise reduction; 2) small area, and low-power consumption by sharing an IA and an ADC; and 3) eliminates the demodulator for data transmission.

The proposed OCCIA modulates 15-Ch. inputs into a single channel, where the output voltage swing margin in the IA must be carefully considered. Hence, Ouh and Johnston [29] propose a current-based CDMA encoding scheme in the optical application to use CDM benefits without the output voltage swing margin issue. However, this results in excessive power consumption as the number of channels increases (to keep the same noise contribution of IA). On the contrary, the OCCIA uses a voltage-based amplifier that has strength in terms of noise and power trade-off. The output voltage swing margin issue is negligible due to the small input bio-signals below 5 mV and the concurrent activation. The VGA solves the output voltage swing margin issue by changing the gain. Also, the VGA compensates for the additional dynamic range loss of $\log_2 \sqrt{N}$ [19] with a combination of the over-sampling and average schemes of the demodulator.

Area of the OCCIA, including IA, OCC Gen., and ADC, is 0.019 mm²/Ch., which is the smallest among recent works shown in Table III. The power consumption is 1.97 μ W/Ch., which is the lowest as well. Also, it shows the lowest gain mismatch of 0.43% among 15 channels, which is superior over

other IA schemes thanks to the shared C_F and the single IA. Capacitive feedback structure enables IA to have flat gain in the OCC operating range, which reduces the gain mismatch from frequency-variant modulation.

VI. CONCLUSION

The proposed OCCIA with DBD shares an IA and an ADC among all the channels with competitive chopping speed, and it also pushes the demodulator overhead from the chip, which further reduces power, area, and noise. This is especially helpful in multi-channel implantable applications. The proposed OCCIA in 1P6M 0.18- μm CMOS, when compared with the recent multi-channel IAs, successfully verifies one of the smallest area (0.019 $\text{mm}^2/\text{Ch.}$) and power consumption (1.97 $\mu\text{W}/\text{Ch.}$), with a low gain mismatch (0.43%) and the crosstalk (< -51.5 dB) at 490-Hz BW.

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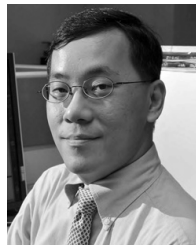
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