A 32 × 128 SPAD-257 TDC Receiver IC for Pulsed TOF Solid-State 3-D Imaging

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Abstract—A single-chip receiver for pulsed laser direct time-of-flight 3-D imaging applications has been realized in a 0.35-μm HV CMOS technology. The chip includes a 32 × 128 single-photon avalanche diode (SPAD) array [35% fill factor (FF)] and 257 time-to-digital converters (TDCs) with a ∼78-ps resolution. Two adjacent rows (2 × 128 SPADs) at a time can be selected for simultaneous measurement, i.e., 16 measurement cycles are needed to cover the whole array. SPADs are capable of operating in a gated mode in order to suppress dark and background light-induced detections. The IC was designed to be used in a solid-state 3-D imaging system with laser illumination concentrated in both time (short sub-ns pulses) and space (targeting only the active rows of the SPAD array). The performance of the receiver IC was characterized in a solid-state 3-D range imager with flood-pulsed illumination from a laser diode (LD)-based transmitter, which produced short [∼150-ps full-width at half-maximum (FWHM)] high-energy (∼3.8-nJ pulse/∼14-W peak power) pulses at a pulsing rate of 250 kHz when operating at a wavelength of 810 nm. Two detector/TDC ICs formed an 8k pixel receiver, targeting a field-of-view of ∼42° × 21° by means of simple optics. Frame rates of up to 20 fps were demonstrated with a centimeter-level precision in the case of Lambertian targets within a range of 3.5 m.

Index Terms—3-D imager, CMOS, direct time-of-flight (dTOF), single-photon avalanche diode (SPAD), solid state, time gating, time-to-digital converter (TDC).

I. INTRODUCTION

OPTICAL 3-D range imagers have recently found many new applications beyond their traditional use in land surveying and geodesy [1]. These include driver assistance systems (even driverless cars), control and guidance of machines (autonomous machines), farming and forestry, and gesture control and face recognition in smartphones and tablets [2]–[4]. The required system-level performance parameters vary considerably, especially with regard to the maximum measurement range, which varies from one meter (face recognition) to a few tens of meters (autonomous machines) and up to ∼200 m in traffic applications. Typically, a measurement speed of >10 frames/s, and in some cases, measurements in bright sunlight, can be required, which is challenging due to the high amount of background noise.

Traditional scanning-based 3-D imagers, in which the laser beam is physically scanned over the target area using rotating components (e.g., mechanical or MEMS), are very accurate systems, but they are also hard to miniaturize, consume a lot of power, and are relatively expensive [5]–[7]. On the other hand, solid-state 3-D imaging (i.e., imaging without any mechanically moving parts) has attracted a lot of attention in recent years [8]–[16] since it tends to offer some relief with regard to the above shortcomings of mechanical 3-D laser range imagers. Integration into hand-held gadgets has been one of the important commercial applications of solid-state 3-D imagers, requiring a relatively short range of a few meters, mm-level precision, a frame rate of tens of fps, a volume of ∼1 cm³, low cost, ∼10-kilopixel spatial resolution, and eye-safety measures. In principle, a solid-state 3-D imager can be implemented with many different approaches, each utilizing unique technologies and techniques, such as stereoscopic vision [17], structured light (and triangulation) [18], and time of flight (TOF) (direct or indirect) [7].

One quite successful approach for the solid-state 3-D range imaging is the indirect TOF technique, in which a continuously modulated optical signal illuminates the target and the measured distance is calculated from the phase shift between the emitted and reflected echo signals (see [10], [19], and references therein). These techniques offer high performance, but at the expense of relatively high average illumination power, typically at a level of hundreds of mWs even in short-range applications if high spatial resolution is required [19].

Another promising solid-state approach for developing miniaturized 3-D imagers is direct TOF (dTOF), in which the transit time of a short laser pulse to the target and back to a 2-D detector array [e.g., single-photon avalanche diode (SPAD)-based] is measured directly, e.g., with time-to-digital converters (TDCs). dTOF has a potential for lower average illumination power, especially under high background noise conditions, since it concentrates the available laser power in short and intensive pulses [20].

The transmitter in a dTOF 3-D imager is usually realized to provide flood illumination covering the field of view (FOV) of the system, and the echo signal is processed from all the pixels in the detector array [6], [9], [11], [13]. The receiver is often constructed in such a way that each of the pixels has processing power for the time-interval measurement (see [21]). The drawback of this method in practice is that only a few of the pixels in the array are triggered by the backscattered
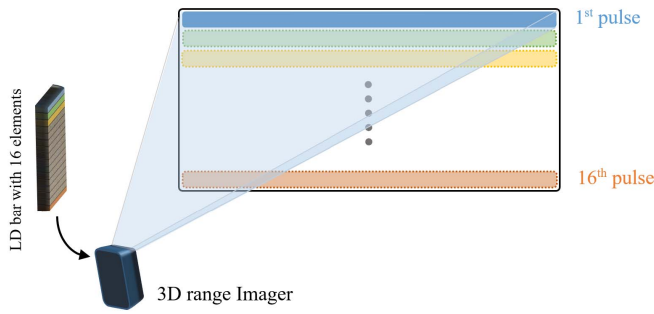
Fig. 1. Block-based illumination scheme using an addressable LD bar as the emitter.

signal photons in each measurement. Thus, most of the time-interval measurement resources are not used effectively. On the other hand, the fill factor (FF) is inevitably lowered due to the in-pixel electronics (e.g., 1% in [21]–[23]), or else, the receiver complexity is highly increased, e.g., if separate IC tiers are used for the detector array and the electronics [13]. Recently, there has been a suggestion that the SPAD and TDC resources should be separated into different chip areas and the reduced TDC resources allocated dynamically to the triggering SPADs [6], [24]. This approach recognizes the limited photon detection probability in flood illumination dTOF and tries to adapt the receiver architecture to it, but at the cost of higher receiver complexity.

Here, we use a dTOF receiver architecture, in which the SPAD and TDC arrays (#SPAD/#TDC = N > 1) are implemented separately on-chip, but the SPAD array is divided into N predefined blocks, and in each measurement, the TDC resources are allocated to only one of the blocks. Due to the ratio of the total number of SPADs to that of TDCs, N measurement cycles are needed in order to fulfill a full scan of the FOV. At first glance, this might appear inefficient since it seems to increase the total measurement time, but while this would really be the case with flood illumination, a major improvement can be achieved using the block-based illumination, in which all the illumination power (typically limited by the available high-speed laser diode (LD) drive current) is concentrated spatially only in the selected active part of the detector array in each measurement.

When N illumination blocks are used (e.g., N = 16 in Fig. 1), the number of on-chip TDCs needed is reduced by a factor of N. However, the measurement time for the total number of signal detections needed remains the same (as with flood illumination and per-pixel TDCs) since the target irradiance within the selected sub-FOV is N times higher during the illumination (assuming the same average illumination powers and bearing in mind that in practical measurement situations, the signal detection probability per pixel per single emitted pulse is ≪1). On the other hand, since the number of laser pulses needed per pixel is N times less (due to the N times higher probability of detecting a signal photon per measurement), the number of random background detections during the "effective detection window" (the number of laser pulses sent multiplied by the width of the laser pulse) is reduced by N, leading to an improvement in the SNR by a factor of $N^{1/2}$. This in turn translates

into an improvement of the frame rate by a factor of N while maintaining the same range (and SNR) or improving the measurement range by $N^{1/4}$, assuming the frame rate is kept constant. An additional advantage of the block-based illumination approach is that it enables adaptive illumination, in the sense that only a few of the illumination blocks within the total system FOV can be used according to the needs of a specific application or measurement situation. It is also important to note that the proposed system is still solid state since the beam steering is realized in the electronic domain.

In practice, block-based illumination can be realized by means of a 1-D array of edge-emitting LDs in a bar or a 2-D vertical surface-emitting LD (VCSEL) array with on-chip addressable element areas, which can be separately chosen and activated to be driven by the LD current driver for a selected number of laser pulses. A simplified presentation of such an architecture is given in Fig. 1.

Based on this approach, this article presents a SPAD/TDC receiver IC that is designed and manufactured in a 0.35-μm HV CMOS technology and supports the abovementioned solid-state 3-D imager architecture with block-based illumination. Another starting point for the design presented here is that in the SPAD-based dTOF 3-D imaging, it is advantageous to concentrate the available average optical illumination power into short (sub-ns), intensive pulses since this would improve the SNR and precision, and also simplify the I/O due to the lower pulsing rate (assuming a constant average illumination power). Thus, a custom-designed LD transmitter running at a moderate pulsing rate of 250 kHz but giving a relatively high pulse energy of ∼3.8 nJ [with a pulselength of ∼150-ps full-width at half-maximum (FWHM)] is used for testing the receiver IC. The performance of the on-chip TDCs and the I/O is designed to match the transmitter parameters.

The design and implementation details of the SPAD-based receiver IC will be explained in detail in Section II, measurement results indicating the performance of the receiver as measured in a 3-D focal-plane imaging system with flood illumination will be presented in Section III, and finally, the results will be discussed and compared with the state-of-the-art solid-state 3-D range imaging receivers and systems in Section IV.

II. RECEIVER IC STRUCTURE

The 6.6 mm × 5.5 mm IC consists of a 4096 SPAD array and a 257-channel TDC array on the same die, realized in a 0.35-μm HV CMOS technology with an operating voltage of 3.3 V. This combination forms a highly integrated receiver for dTOF 3-D imaging applications. A micrograph of the IC and a zoomed version of a sample part of the SPAD matrix are shown in Fig. 2, and a block diagram of the IC is shown in Fig. 3.

A. SPAD Array and Interfacing Logic

The SPADs are placed in 32 rows and 128 columns. Two adjacent rows (2 × 128 SPADs) can be connected to 256 TDCs in each measurement. As a result, a full scan of the whole SPAD array takes 16 measurement cycles (in accordance with the intended block-based illumination scheme). The row
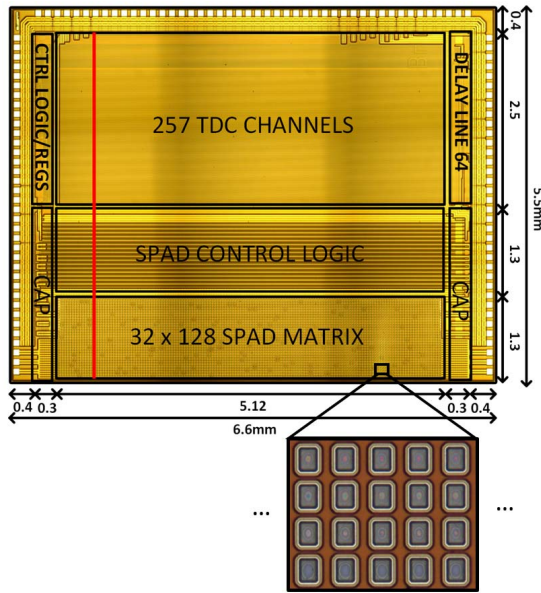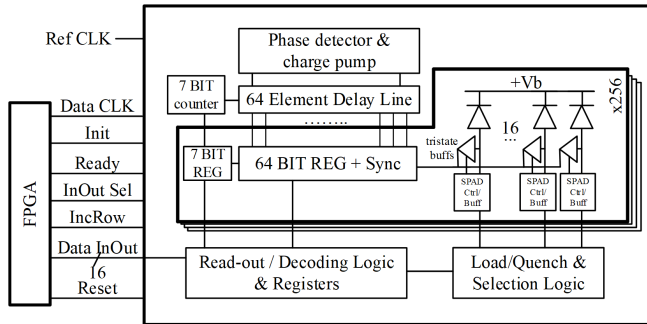
Fig. 2. Die micrograph of the IC.

Fig. 3. Block diagram of the IC.

Fig. 4. (a) Cross section of a single SPAD and (b) SPAD interfacing electronics.

selection for the connection to TDCs is performed before every measurement based on control data received and stored in dedicated registers. Two TDC channels fit within the pitch of each detector column. The I/O pads were removed from the light-sensitive side of the IC (bottom side in Fig. 2), which makes it possible to bond two ICs in close proximity on a PCB and double the imaging resolution, as in [25]. The block diagram of the IC, as shown in Fig. 3, is explained in detail in the following. The main part of the IC layout consists of 256 similar slices, each including 16 SPADs, their interfacing logic, and one TDC interpolator. The red area in Fig. 2 shows the placement of such slices within the IC floorplan.

Each SPAD has a 40 μm $\times$ 40 μm pitch with a rectangular active area of 26 μm $\times$ 21 μm [Fig. 4(a)]. The SPAD matrix was separated from the interfacing electronics, leading to a FF of 35% for the light-sensitive part of the chip. The SPADs have deep-n-well cathode/p+ anode junctions with a lightly doped p-well guard ring and rounded corners (to prevent premature breakdown at the edges). The common deep-n-well cathode is shared among all the SPADs. Each SPAD has its own active quench/load circuit [Fig. 4(b)] located in a separate array besides the SPAD array (see [26] for detail). The activated SPADs are self-quenched if they are triggered
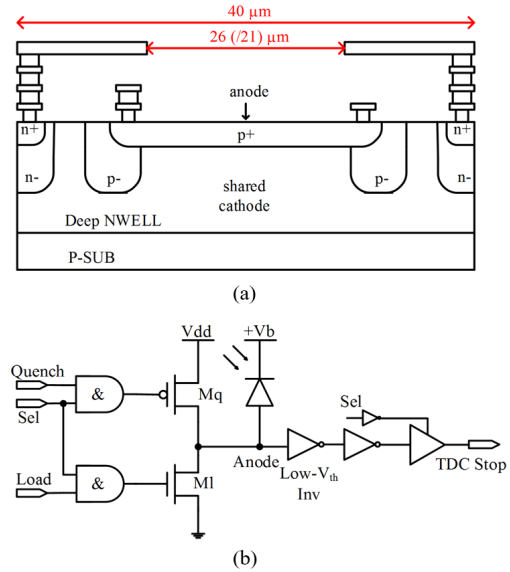
with an avalanche. This structure translates to a nominal excess bias voltage (V_{ex}) of 3.3 V for the detectors while activated. The load, quench, and selection signals are produced by their dedicated logic based on the stored measurement setting and routed to each element of the array.

B. TDC Array

Each TDC measures the arrival time of an electrical signal (1 start and 256 stops). The start signal, taken from the LD-based transmitter, marks the start of the travel time of the pulse ($t_{sharedstart}$), after which it travels to the target and is reflected back to the receiver, generating a stop signal when detected in the optically sensitive active area of a SPAD, marking the end of the laser pulse's flight ($t_{SPADstop}$). Thus, the travel time of the laser pulse is simply $t_{SPADstop} - t_{sharedstart}$. Then, a 257-channel TDC digitizes the travel time (i.e., the distance from the target) for all 256 active SPADs.

The TDC architecture is shown in Fig. 5. The timing core, common to all the 257 measurement channels, is composed of a counter and a delay-locked delay line, which are fed by a 200-MHz external temperature-compensated oscillator (f_{ref}). The delay-adjustable delay line creates time samples for interpolation with τ_{lsb} ~78-ps resolution when the reference clock signal propagates through 64 identical delay elements. The delay element, presented in Fig. 6, consists of two parallel delay-adjustable (current-starved) inverters with outputs that are connected with smaller inverters operating in the opposite direction. This structure provides high resolution for the interpolation even though the resolution is based on the gate-delay principle (τ_{lsb} ~ inverter delay). The differential reference signal propagates through two parallel inverters, which are in the opposite phase, improving the nonlinearity and immunity to noise as compared with a single-ended structure. The two small inverters maintain the phase difference between the two propagating signals throughout the whole delay line.

The phase detector and charge pump adjust the propagation delay of the delay line by regulating the control voltage V_{ctrl}.
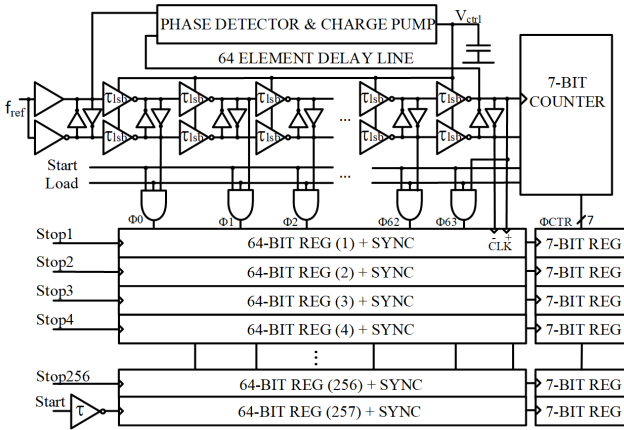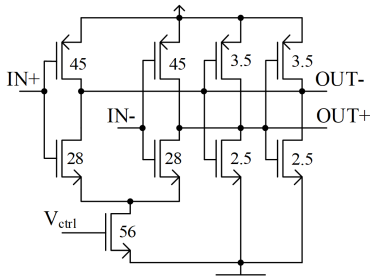
Fig. 5.   TDC architecture.

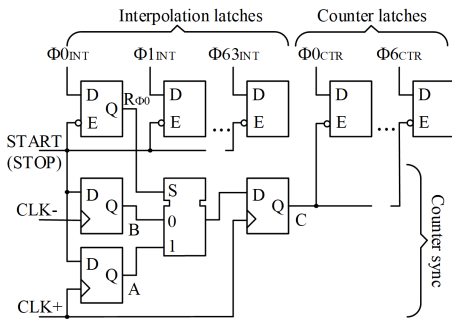Fig. 6.   Delay-element structure with transistor widths (μm). The length is always 0.35 μm.

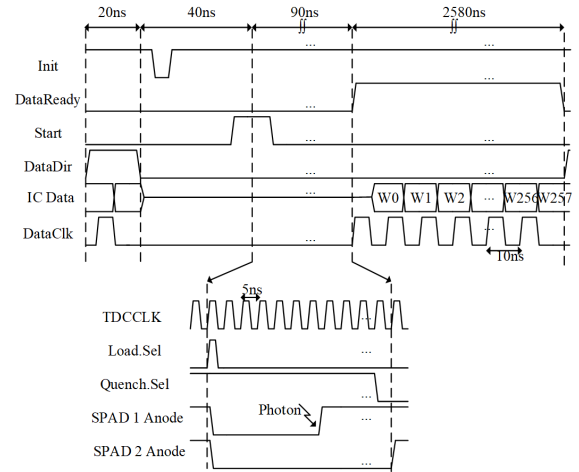Fig. 7.   Measurement channel, including latches and counter synchronization.

Fig. 8.   Measurement cycle for scanning the array and readout.

running DLL. During the active gate window, the outputs of the 64 delay elements simultaneously drive the 257 inter-polation latches through ∼5-mm-long wires, leading to a transient power consumption of ∼1.5 W. The AND gates, placed between the delay elements and long wires, are enabled only during the active gate window to avoid unnecessary power consumption at other times. A delayed version of the start signal is used to register the delay-line state in the start-TDC to make sure that the delay-line signals have settled before the arrival of the registering signal. This translates, for example, into an average power consumption of 175 mW for measuring distances from targets located at up to 10 m at a pulsing rate of 250 kHz operating with a 240-MHz reference frequency.

The high power consumption of the TDC array leads to nearly 10° of temperature increase in the IC, which directly affects the breakdown voltages of the SPADs. As a result, adjustment of the bias voltage of the SPADs [V_b in Fig. 4(b)] according to the IC temperature (e.g., using off-chip voltage regulators) is needed to make sure that they are always operating with the highest possible V_{ex} when active but are not conducting current when deactivated.

C. Operation

A single measurement cycle of the IC is shown in Fig. 8. At the beginning of each measurement, the measurement settings are read to the IC, two adjacent rows are selected for measurement, and the beginning and the end of the gate window are defined (with a 5-ns resolution) with respect to the start signal (the laser pulse). The gate window helps to focus the 3-D measurement to a certain desired distance range and prevents false SPAD triggering in bright ambient conditions (with high background noise) because of unwanted objects. Gate windows with various widths (from 5 up to 640 ns in 5-ns steps) and various delays with respect to the laser pulse (from 5 to 635 ns in 5-ns steps) can be used depending on the measurement conditions.

The measurement setting registers are updated at the falling edge of the Init pulse. After the arrival of the electrical start signal, one TDC measures its arrival time, and the chosen 256 SPADs are biased above the breakdown voltage (V_{br}) for

This delay-locked loop (DLL) keeps the delay-line delay (τ_{ref}), and hence, the delay-element delay ($\tau_{ref}/64$), constant under different process, voltage and temperature (PVT) conditions. The 7-bit counter begins counting the clock cycles when the start signal arrives at the IC. The size of the measurement channels has to be minimized in order to integrate all of them into the same chip. Each of the 257 channels consists of $64 + 7$ registers (latches), as shown in Fig. 7, which store the state of the sampled delay line and the counter value. A synchronization logic between the delay line and counter registers synchronizes the counter sampling, so that the results are compatible [27].

The TDC architecture provides a linear dynamic range of up to 640 ns under varying PVT conditions for all the time-interval digitization between the start and the 256 stops. The power consumption of the TDC array, measured when operating with a 240-MHz reference frequency, is ∼150 mW in its idle state (inactive SPAD array) due to the constantly

the predefined gate window by the load signal (synchronized to the Start and TDCClk). All the other SPADs are biased below V_{br} during the whole measurement cycle. If an active SPAD breaks down, because of either photon detection or detector noise, its respective TDC will measure the breakdown time at the rising edge of the anode voltage (e.g., SPAD 1 in Fig. 8). If no triggering occurs, the SPADs are actively quenched at the end of the gate window (e.g., SPAD 2 in Fig. 8) by the low-active quench signal.

After the measurement window is over, the measured data are transferred out of the chip once the DataReady signal is raised by the IC. The measured data include 258 16-bit words (i.e., the address of the active part of the array, the arrival time of the start signal, and the breakdown time of the 256 active SPADs), which are read out of the IC through a 16-bit bidirectional data path. DataDir determines the direction of data transfer, and DataClk is the data transfer clock in Figs. 3 and 8. The IC supports a maximum DataClk frequency of 100 MHz.

The measurement rate can vary depending on the DataClk frequency, the gate window width (covered range), and whether the settings need to be changed before a measurement cycle or not. With a distance range of ~10 m (70 ns in Fig. 8), if the data are read out of the IC with a DataClk frequency of 100 MHz and the measurement settings are changed after each measurement, loading the new measurement settings (20 ns), the initialization (20 ns), Start signal generation (20 ns), gate window width and DataReady signal generation (70 + 20 ns), and data readout (258 × 10 ns) would make a measurement rate of ~365 kHz possible. Therefore, a frame update rate of ~23 kHz (365/16) can be achieved with a laser pulse frequency of 365 kHz. In practice, the range and frame rate also depend on the average power that the illuminator can provide.

III. PERFORMANCE OF THE RECEIVER IC IN A dTOF FOCAL-PLANE 3-D IMAGER SETUP

A. dTOF Focal-Plane 3-D Imager Setup

The performance of the receiver IC was characterized in a dTOF focal-plane 3-D imager paired with a quantum-well (QW) LD-based transmitter, producing flood illumination over the FOV of interest. In the 3-D imager setup built for this purpose, as shown in Fig. 9, the spatial position of a certain SPAD within the array together with information on the travel time of the laser pulse from the transmitter to that particular SPAD forms an *xyz* location of a point in the observed scene. Two ICs form a combined array of 8k SPADs (128 × 64) and are placed in the focal plane of a lens system with an aperture diameter of 5.6 mm and an effective focal length of 6.67 mm, which is focused on infinity. A narrowband optical filter (FWHM ~20 nm) is combined with the lens to block unwanted ambient light. A zoomed-in view photograph of two bonded ICs with a separation of ~120 μm, which is about three times the pitch of one SPAD, is shown in Fig. 9(c).

A customized QW LD (a 3-mm cavity length and a 90-μm active stripe width) is used to produce high-energy optical pulses with a central wavelength of 810 nm and a spectral
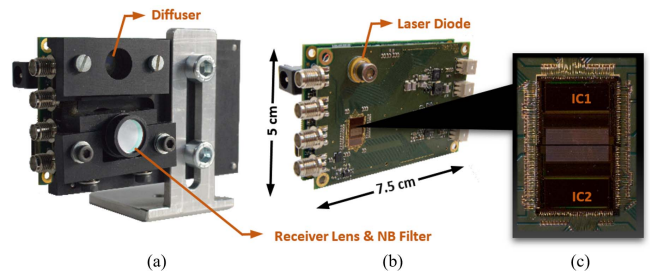

Fig. 9.   (a) dTOF focal-plane 3-D imager. (b) Transmitter–receiver PCB. (c) Zoomed-in view of the receiver.
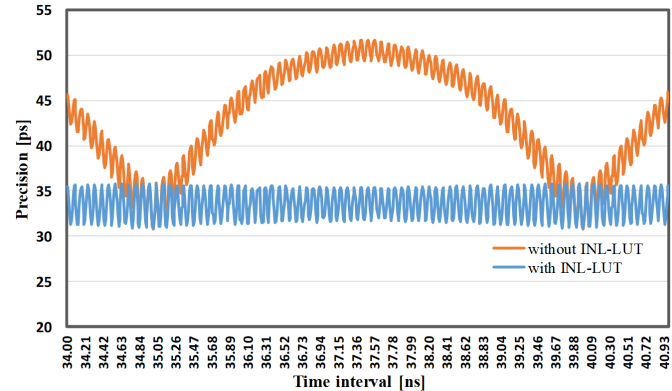

Fig. 10.   Precision variations at different time intervals with and without INL-LUT.

width of 4-nm FWHM. The LD operates in enhanced gain-switching mode as a result of the large equivalent spot size (thickness of the active area/optical confinement factor, $da/\Gamma a \gg 1$) [28] and is driven by a simple MOS-based driver and an *LCR* transient-based pulse-shape control producing current pulses of ~3-ns width and ~10-A peak [29], [30]. With this technique, the LD produces significantly shorter pulses than the width of the drive current pulse. The LD transmitter has a pulsing frequency of 250 kHz, and the laser pulsewidth and energy are ~150 ps (FWHM) and ~3.8 nJ, respectively. A commercially engineered optical diffuser is used to shape the beam into a rectangle illuminating a target FOV of ~42° × 21° (*xy*).

The 3-D camera is connected via a USB 3 field-programmable gate array (FPGA)-based interface to a Qt-based Windows user interface (UI), which is used for real-time measurement control, data collection, data processing, and 2-D (intensity)/3-D (depth) video reconstruction and streaming. The whole system can be powered via the USB 3 connection.

B. Circuit-Level Measurement Results

The precision (standard deviation, σ) of the TDC with different time intervals was evaluated using electrical timing signals by measuring the signal propagation delay in coaxial cables of different lengths. The precision fluctuation when the start channel and one stop channel digitize different time intervals is shown in Fig. 10. The upper precision curve (without the integral nonlinearity lookup table, INL-LUT) repeats itself with a lapse of τ_{ref} due to the identical
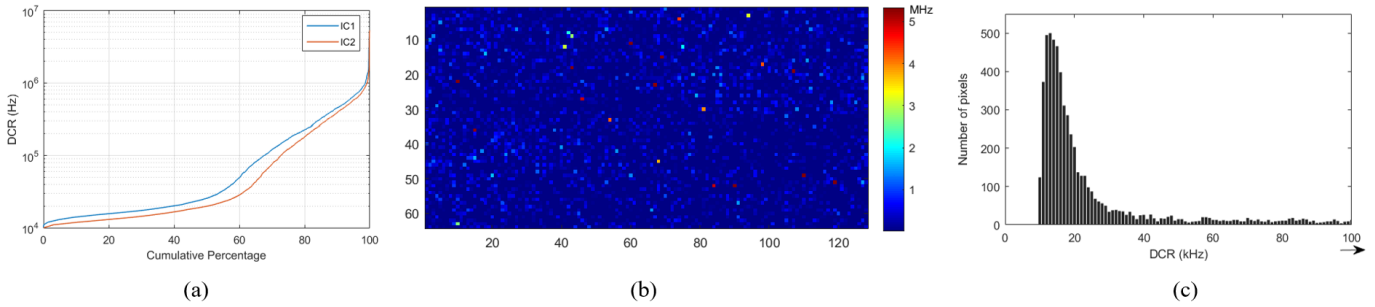
Fig. 11. (a) Cumulative percentage of the DCR. (b) DCR distribution. (c) Uniformity of DCR in the SPAD arrays of two ICs.

interpolation INL after every new reference edge. The lower curve (with INL-LUT) shows the precision when the nonlinearities of the TDC were compensated for by post-processing of the results. The measured rms precision was 45 ps without INL-LUT and 33.6 ps with INL-LUT, which matches well with the precision limitation due to quantization noise $\tau_{lsb}/\sqrt{6}$. However, the INL-LUT was not used in the optical measurements because the TDC precision is not the limiting factor in the system jitter.

The TDC nonlinearity is mainly caused by layout and process parameter variations between the delay elements and registers (latches) storing the signal arrival moment. The measured max and min values for the differential non-linearities (DNLs) of all the 257 TDC channels are 42 and 65 ps, respectively, while the max and min values for the INLs are 97 and 28 ps, respectively. The INL variation, σ_{INL}, which detracts from the measurement precision, fluctuates between measurement channels in the range of 19.5–26.8 ps.

The cumulative dark count rate (DCR) of the SPADs is shown in Fig. 11(a) for each receiver IC separately when measured with a SPAD bias voltage of 22.4 V [V_b in Fig. 4(b)]. As can be seen, there are three trends in the distribution. Nearly 60% of the SPADs have a DCR less than 37 kHz, but the distribution grows exponentially above 60% and 1% of the SPADs have DCRs higher than 1 MHz. There are a few hot pixels in each chip, which are, for practical purposes, too noisy for use even in short-range measurements. The distribution of the DCR with a mean value of 139 kHz and a median of 22.7 kHz is shown in Fig. 11(b), while Fig. 11(c) shows the uniformity of the DCR in the two ICs. As can be seen, the distribution of high DCR pixels in the arrays is quite random.

The value of V_b [see Fig. 4(b)] below which no triggering due to dark noise can be detected is shown for each SPAD of both chips in Fig. 12. A variational range of 550 mV can be seen among the SPADs of both arrays. This non-uniformity may be caused by a combination of reasons. First, although the excess voltage should ideally be 3.3 V throughout the array, this is not usually the case, due to a voltage drop in the high-voltage distribution net, VDD/GND nets (dependent on the switching activity). Second, a breakdown voltage non-uniformity may exist in the array due to imperfections arising in the manufacturing process. It should also be noted that the breakdown voltage of a SPAD has a strong temperature dependence and grows linearly with temperature (∼40 mV/°) [31]. As a result, heating of a section with high current
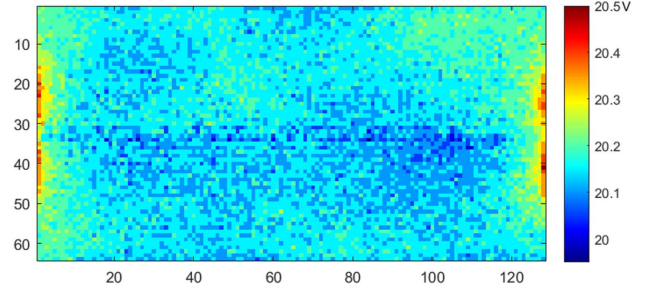

Fig. 12. V_b distribution below which no triggering due to dark noise can be detected.
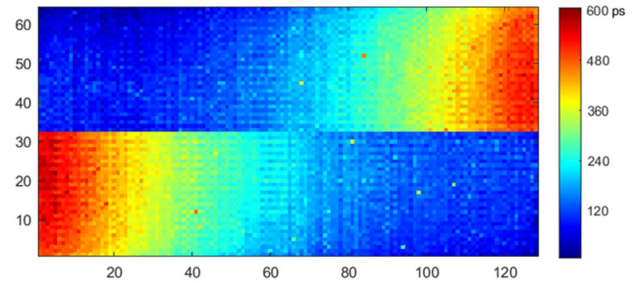

Fig. 13. 2-D on-chip delay distribution color map.

consumption on-chip or other components on the PCB can affect the breakdown voltage distribution in the array. Because of this non-uniformity, most SPADs do not benefit from the highest possible excess voltage (3.3 V).

The distribution of the differences in the measured arrival times recorded by each detector (by means of its respective TDC) when the whole detector array is exposed to the same laser pulse illumination is shown in Fig. 13. This distribution depicts the static delay difference between pixels caused on-chip from photon detection up until the respective TDC's digital result is recorded. In order to obtain the distribution, a multi-mode fiber was used to direct the laser beam to the SPAD arrays. Histograms were formed for each SPAD, and accurate delays were calculated for each pixel by averaging the results of numerous measurements. In order to avoid any unwanted walk error due to multiphoton-triggered avalanches, the detection rate of each SPAD was kept at a few percents by weakening the illumination power using neutral density filters.

Three trends may affect the delay distribution pattern: that, in the horizontal direction, can be explained by the placement of the TDCs with respect to the DLL (as can be seen in Fig. 2),

i.e., the farther the TDC is from the DLL, the more delayed the versions of the DLL transition edges that it gets. The TDC measuring the arrival time of the start signal is located after the farthest TDC from the DLL, and the photon traveling time for each SPAD detection is $t_{\text{SPAD}} - t_{\text{start}}$. Because of this floorplan and TDC architecture, the delay difference pattern in the horizontal direction is mainly affected by the parasitics of the DLL signal distribution. The delay difference pattern in the vertical direction is mainly affected by the routing parasitics from the SPAD anodes to the interfacing electronics and from there to the dedicated TDC channel inputs. This leads to higher delay values for pixels of rows that are located farther from the TDC array. On the other hand, all the SPADs share the same deep-n-well and, hence, the same cathode bias, but as can be deduced from Fig. 12, V_{ex} is not equal for all the SPADs. This can cause weaker avalanches, and as a result longer delay times, for SPADs with lower V_{ex}. The delay map of Fig. 13 may be used as a calibration table in TOF measurements. The maximum measured delay differences among the arrays for the top and bottom ICs were 590 and 600 ps, respectively, which is in good agreement with post-layout simulation results.

C. System-Level Measurement Results

The detection rate of the SPADs measuring distances from a flat target (white paper) located 1.5 m away is shown in Fig. 14(a). Since the measurement was performed with low ambient and low average signal photons, the probability of a SPAD being triggered by noise before signal arrival or a multi-photon-triggered avalanche is negligible. As a result, Fig. 14(a) shows a representation of the distribution of laser illumination power among the pixels of the detector array. Considering the laser radar equation given in (1) [32], [33], we can calculate the average number of photons detected per transmitted laser pulse (N_{det}) for a SPAD located near the optical axis

$$N_{\text{det}} = \frac{E_{\text{tr}} \times \varepsilon_{\text{opt}} \times \rho_{\text{target}} \times A_{\text{rec}}}{\pi \times R^2 \times h\frac{c}{\lambda_{\text{tr}}}} \times \text{PDP} \times \text{FF}. \qquad (1)$$

Here, E_{tr} is the transmitted pulse energy seen by the active area of a SPAD near the optical axis of the imager ($\sim$0.516 pJ). This has been verified using a photodetector (with an active area diameter of 1 cm) at 1.5 m on the optical axis measuring 125 nW. The other parameters are ε_{opt} = optics efficiency (0.8), ρ_{target} = target reflectivity (1), A_{rec} = area of the receiver lens (0.24 cm^2), R = range (1.5 m), hc/λ_{tr} = photon energy (2.3 $\times$ 10^{-19} J), PDP = photon detection probability of the SPAD ($\sim$4% at 810 nm), and FF = fill factor of the SPAD (35%).

The equation with the parameters mentioned here (reflecting the measurement shown in Fig. 14) leads to $\sim$0.08 probability of laser photon detection for central SPADs, which is in agreement with the measured results. The illumination power per pixel active area declines outward from the center as a result of the non-ideal diffuser and light fall-off (proportional to cos^4(θ), where θ is the off-axis field angle).

Time histograms of the hits in Fig. 14(a) measurements for three SPADs located at the center and opposite edges of the array are shown in Fig. 14(b). The histograms have an FWHM
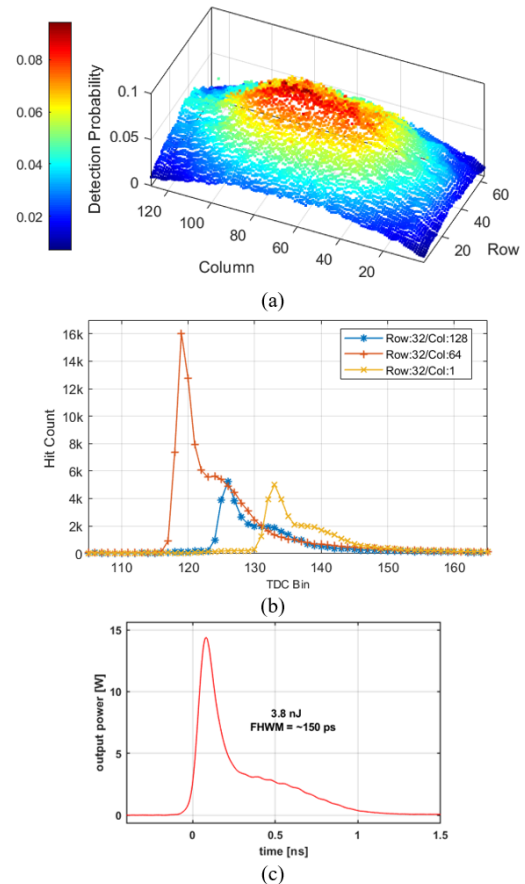

Fig. 14. (a) Detection probability of a pulse targeted at a flat white wall located 1.5 m away from the 3-D imager. (b) Histograms from the center and edges of the detector array. (c) Optical pulse.

of $\sim$250 ps, which is a combined result of the laser pulsewidth ($\sim$150-ps FWHM), SPAD jitter ($\sim$100-ps FWHM), TDC rms single-shot precision ($\sim$100-ps FWHM), and the effects of supply voltage fluctuations due to switching activity. This FWHM confirms that the single-shot precision of the system in distance measurement is better than $\pm$2 cm. Fig. 14(c) shows the laser pulse energy distribution in time. Considering the fact that the probability for a signal detection per single emitted laser pulse is $\ll$1, having such a short pulse envelope of 150 ps with high peak power (compared to ns pulses with the same pulse energy) improves the SNR and the single-shot precision of the measurement. By averaging N consecutive laser photon detection results, it is possible to improve the precision by a factor of $\sqrt{N}$.

There are different sources of static timing differences between pixels, either optical or electrical, such as lens distortion, field curvature, off-axis angle of the target, and static timing offset of the on-chip and off-chip electrical signals. Walk errors due to multi-photon avalanches may also exist, but here, since the illumination is spread over the whole array, the probability of such a walk error occurring can be ignored.

An example of 3-D (point cloud) images taken of a lobby with the farthest point of the scene nearly 6.5 m away from the camera is shown in Fig. 15. A high-resolution photograph is also presented for reference. Cross correlation (sliding dot product) with a filter was used here to translate the histograms
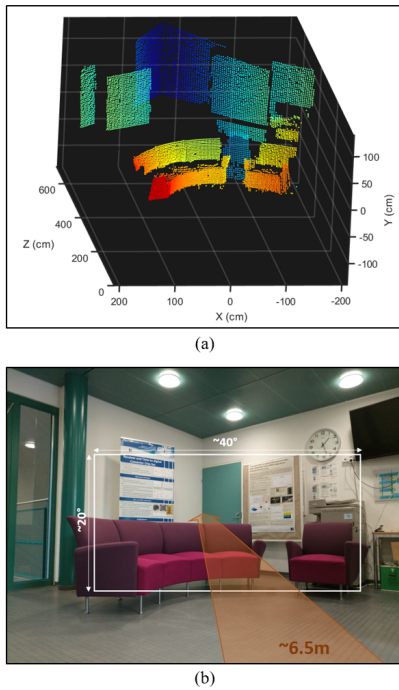
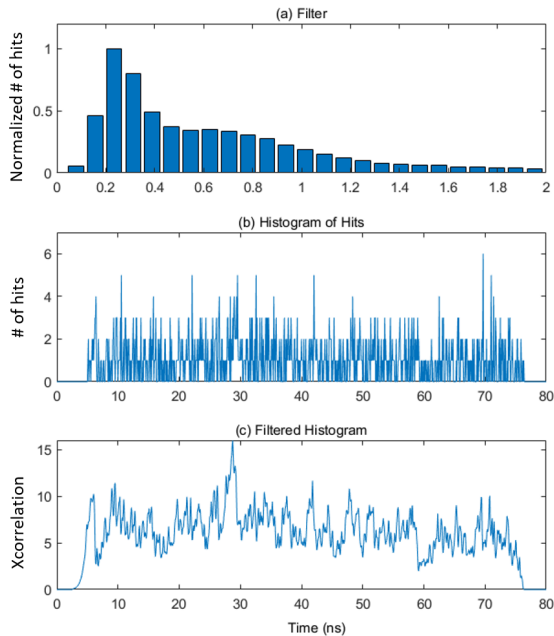Fig. 15.   (a) 3-D point cloud image. (b) Photograph of an indoor area.

Fig. 16.   (a) Filter. Histogram of hits (b) before and (c) after filtering.

into distances. The filter and histogram before and after filtering for a pixel within Fig. 15 (row 13/col 33: armrest of the smaller sofa) are shown in Fig. 16. The filter is a normalized version of a histogram of hits collected by one SPAD in single-photon mode measuring the location of a target placed at a specific distance from the camera. As can be seen in Fig. 16(b) and (c), even in the cases where the photon detection probability is quite low and the signal is almost covered by noise, the signal could be recovered by the abovementioned method. After the filtering, a weighted average of a few points around the maximum of the filtered

time histogram was considered to represent the measured distance.

After resolving the measured distances, calibrations were performed to remove the effect of barrel distortion introduced by the receiver lens and static on-chip (Fig. 13) and off-chip (e.g., start signal delay) electrical signal offsets. The image was taken using a laser pulsing frequency of 250 kHz with a 1-s acquisition time in normal office lighting. It should be noted that no post-processing other than simple noise removal was performed on the point cloud data. A few points, whose measured distances compared to those of all neighboring pixels were higher than a given threshold (e.g., 50 cm), were considered to be noise and removed.

The 3-D point cloud images of a person standing in front of a wall with a ball in the bottom right corner taken at frame rates of 2, 5, 10, 20, and 40 fps are shown in Fig. 17. The wall was located at a distance of ∼3.3 m, and the measurements were performed in normal office lighting. Flood illumination with a total average illumination power of ∼1 mW was used in these measurements, which means that the effective average optical illumination power per block was only ∼65 μW. These results demonstrate the dependence of the recorded 3-D range image quality on the effective frame rate of the measurement.

IV. Conclusion, Future Work, and Discussion

A 32 × 128 SPAD/257 TDC receiver IC (manufactured in a 0.35-μm HV CMOS technology) suitable for dTOF LD-based 3-D range imaging is presented here. Due to the separate SPAD and electronics arrays on the same die, a high FF of 35% was achieved. Each 16 SPADs share one TDC shares one TDC, requiring 16 measurements for producing an image of the whole scene. The TDCs have ∼78-ps resolution (in agreement with the laser pulsewidth), and time gating with a 5-ns resolution can be used to suppress background and dark count noise. A 16-bit I/O with a 100-MHz readout clock makes frame rates up to 23 kHz possible while covering a range of 10 m.

The IC was tested in a 3-D imager setup with flood-pulsed illumination. This system was used to verify the performance of the detectors and the timing measurement circuit. In each measurement, the complete light-sensitive area of the receiver array was illuminated, despite the fact that only one-sixteenth of the SPADs could be activated at any given time. This meant that most of the transmitted optical power was lost and the system efficiency was reduced. As a result, the main improvement at the system level would be to use a matched combination of solid state scan of illumination and SPAD array sections (as explained in the introduction), so that all the optical power could be used in each measurement. However, it should be noted that even with flood illumination, the implemented dTOF 3-D imager utilizing short, intensive laser pulses (∼3.8 nJ and ∼150 ps) produces 3-D range images at a distance of a few meters with a relatively high spatial accuracy (Fig. 17) given an average optical illumination power of only ∼1 mW. Moreover, the transmitter is also miniature in size, consisting of a single custom-designed LD (as shown in Fig. 9) and its own on-board driver.
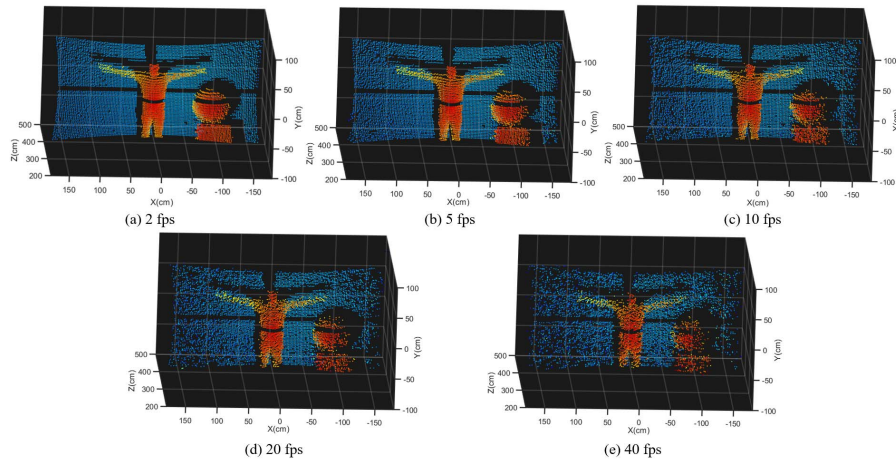
Fig. 17.   3-D images of a scene taken with different frame rates. (a) 2 fps. (b) 5 fps. (c) 10 fps. (d) 20 fps. (e) 40 fps.

TABLE I
COMPARISON OF FLOOD AND BLOCK-BASED ILLUMINATION

System approach	Illumination type	Number of TDCs (64x128 SPADs)	Achievable Performance Optimized for highest range	Achievable Performance Optimized for highest frame rate
This work	flood	4x128 (16 blocks)	5 m @ 5 fps (measured)	
Flash	flood	64x128 (per-pixel TDCs)	10 m @ 5 fps	5 m @ 80 fps
Block-based	16 blocks	4x128 (16 blocks)	20 m @ 5 fps	10 m @ 80 fps

TABLE II
RECENTLY DEVELOPED PULSED TOF RECEIVER ICS AND
SOLID-STATE 3-D IMAGER SYSTEMS

Ref	This work	[11]	[8, 22]	[9, 23]	[6]	[13]
CMOS Tech. (μm)	0.35 HV	0.35 HV	0.35HV	0.35	0.18	0.04/0.09[c]
Pixel size	40 μm (pitch)	50x100 μm^2	20 μm (diam.)	30 μm (diam.)	28.5 μm (pitch)	38.4 μm (pitch)
2D resolution	128x32	80x25	32x32	32x32	32x32	256x256[g]
Array FF%	35	32	3[b]	3	28	51
Chip size (mm^2)	5.5x6.6	5x5.7	3.5x3.5	9x9	2x5	~2.5x2.5
IC Power (mW)	180	66	-	-	-	77.6
single-shot prec.	<2cm	2cm	27cm	1cm	<1cm	<2cm
FOV (degrees)	21x42	18x28	40x40	6.9x6.9	40x40	1.2x1.2
Range@ Fr. rate	3.5m @20fps[e]	3.5m @9fps	14m @25fps	8m @6fps	0.7m @<1fps	50m @30fps[f]
λ(nm)	810	870	808	750	637	671
Illum. P. (mW)	1	0.1	~200	90	2	1.8
Pulse width	150ps	110ps	150 ns	100 ps	40 ps	100 ps
Pulsing rate	250kHz	100kHz	1.7 MHz	40 MHz	40 MHz	1.9 MHz
TOF technique	direct	gate scan	indirect	direct	direct	direct
Background noise	200 lux	200 lux	NK	<50 lux	dark	1 klux
System size (cm^3)	5x7x4	NK[d]	6x5x8[a]	6x6x8[a]	NK	NK

[a] excluding the transmitter, [b] microlens array used to make up for low FF, [c] 3D stacked, [d] Not Known, [e] 14m @ 20fps (if block-based illumination is used), receiver aperture not specified, [g] 64x64 in LIDAR measurements.

A comparison between the performances of two hypothetical examples of transmitter/receiver architectures based on the results acquired by measuring the prototype presented in this article is shown in Table I. It is assumed that a spatial resolution (128 × 64 SPADs), LD illumination power, and the optics are kept the same as in the above prototype, and the achievable performance with different transmitter architectures and receiver complexities (i.e., the number of TDCs) are compared. The first row of Table I presents the performance of the system for which the measured results were presented in this article. A frame rate of 5 fr/s was achieved when covering a 5-m range, which serves as a basis for calculating the performance of the other rows while maintaining the same frame point cloud quality (SNR, noise dominated by background illumination).

The second row depicts the case of a flash-type receiver (all the SPADs can be measured in one measurement, i.e., for each laser pulse) combined with flood illumination in the transmitter. Since there is always a tradeoff between achieving a higher frame rate or a longer range, both extremes of the tradeoff are shown in the row, i.e., a higher frame rate of 80 fr/s with a maximum range of 5 m or a longer range of 10 m while keeping the frame rate at 5 fr/s. The third row presents the calculated performance of a system using the block-based receiver architecture when paired with the same block-based architecture in the transmitter.

As can be seen in Table I (and based on the explanations presented in the introduction), the block-based transmit-ter/receiver solution reduces the complexity of the receiver IC drastically and simultaneously offers better performance than a flood illumination/flash detector architecture, but at the cost of a more complex transmitter.

On the other hand, although the major improvement to the system of this article is the matching block-based illumination, there are a few other possibilities for achieving better performance. Diffusers can be grown on top of the LDs to make the system even more compact, and the laser pulse energy can be increased further to ~10 nJ by using a multi-

junction structure, for example. Since the IC can support laser pulsing frequencies up to 365 kHz (while covering a 10-m range), the average transmitted power could also be increased by using higher LD pulsing rates. As a result of having a TDC depth (640 ns) that is nearly five times larger than the practical range, a train of multiple laser pulses (e.g., 100 ns apart) can be used instead of a single laser pulse in one measurement under low ambient light conditions to improve the exposure time per frame. It should be noted that the 3-D image results presented here are based on simple data processing. Further advanced computational imaging approaches can be used for both distance approximation and point cloud data processing.

A thorough comparison of state-of-the-art solid-state 3-D imagers (even when using pulsed TOF) is a difficult task since each of them is aimed at specific applications and is designed with the specific circuit- and system-level performance requirements in mind (e.g., FOV, 2-D resolution, frame rate, and range). Table II shows the comparison of a few recently developed state-of-the-art pulsed TOF solid-state 3-D imagers and the corresponding receiver ICs, the emphasis being on ones with a system-level realization (i.e., both transmitter and receiver) and aimed at small-size/short-range (up to tens of meters) applications. Of the 3-D imager designs presented in Table II, that described in [13] has excellent receiver features, but the realization uses separate IC tiers for the SPAD array and the electronics, which complicates the receiver considerably. However, the system-level measurements are performed in a much smaller system FOV, which makes a meaningful comparison of the 3-D results difficult.

In [34], a SPAD-based receiver is presented that has an overall functionality resembling that discussed here. On the other hand, the receiver presented in [34] has quite different circuit-level parameters (e.g., FF = 13.9%, TDC resolution = 208 ps, and the number of TDCs = 64) and is designed and optimized for an illuminator based on a micro-mechanical scanner leading to a non-solid-state implementation (and as a result not presented in Table II).

The main distinction between this work and other recently realized systems is the optimization of the overall receiver architecture and circuit realization to support the idea of block-based illumination. This approach may be used to improve the performance of the 3-D range imager relative to systems with flood illumination while operating at the same average illumination power. The selected receiver architecture has resulted in a simple, straightforward receiver IC structure and a high FF of the sensor area of the chip, even in a standard nonaggressive CMOS technology. The receiver IC has proved to be fully operative when evaluated in a fully realized solid-state 3-D range imager of small size but with a performance that compares favorably with state-of-the-art pulsed TOF range imagers.

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