A 39-GHz 64-Element Phased-Array Transceiver With Built-In Phase and Amplitude Calibrations for Large-Array 5G NR in 65-nm CMOS

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***Abstract*— This article presents the first 39-GHz phased-array transceiver (TRX) chipset for fifth-generation new radio (5G NR). The proposed transceiver chipset consists of 4 sub-array TRX elements with local-oscillator (LO) phase-shifting architecture and built-in calibration on phase and amplitude. The calibration scheme is proposed to alleviate phase and amplitude mismatch between each sub-array TRX element, especially for a large-array transceiver system in the base station (BS). Based on LO phase-shifting architecture, the transceiver has a 0.04-dB maximum gain variation over the 360° full tuning range, allowing constant-gain characteristic during phase calibration. A phase-to-digital converter (PDC) and a high-resolution phase-detection mechanism are proposed for highly accurate phase calibration. The built-in calibration has a measured accuracy of 0.08° rms phase error and 0.01-dB rms amplitude error. Moreover, a pseudo-single-balanced mixer is proposed for LO-feedthrough (LOFT) cancellation and sub-array TRX LO-to-LO isolation. The transceiver is fabricated in standard 65-nm CMOS technology with flip-chip packaging. The 8TX–8RX phased-array transceiver module 1-m OTA measurement supports 5G NR 400-MHz 256-QAM OFDMA modulation with −30.0-dB EVM. The 64-element transceiver has a $EIRP_{MAX}$ of 53 dBm. The four-element chip consumes a power of 1.5 W in the TX mode and 0.5 W in the RX mode.**

***Index Terms*— 39 GHz, 5G cellular network, 5G new radio (5G NR), CMOS, fifth generation (5G), large array, local-oscillator (LO) phase shifting, LO feedthrough (LOFT), millimeter-wave, patch antenna, phase calibration, phase quantization, phase shifter, phased-array, power amplifier (PA), sliding IF, transceiver, TRX switch.**

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I. Introduction

THE cellular network technology evolution has reached the fifth generation (5G) driven by the enormous growth of mobile data. The 5G technology has three sets of use cases defined as enhanced mobile broadband (eMBB), ultra-reliable and low latency communication (URLLC), and massive machine type communication (mMTC). At 3GPP release 15, the eMBB can be referred to as the first phase of 5G technology due to the evermore bandwidth demanding by applications, such as streaming video, playing 3-D games, and immersive virtual reality (VR) and augmented reality (AR) [1]. The second phase will then go beyond eMBB to URLLC and mMTC in 3GPP release [2], [3]. In order to greatly enhance user data rate and area traffic capacity for the eMBB usage scenario, the new spectrum will be used. 3GPP defines the 5G new radio (5G NR) bands at millimeter-wave frequency range (FR2) from 24.25 to 52.6 GHz as an extension of the sub-6-GHz frequency range (FR1) [1]. Operating in the time-division duplex (TDD) mode, NR band n260 allocated at 39 GHz specifies a 3-GHz available spectrum covering from 37 to 40 GHz with a maximum channel bandwidth of 400 MHz. Multi-Gb/s data rate user experience can be provided by 5G NR employing millimeter wave.

Silicon-based millimeter-wave transceiver with a high integration level and large throughput has been widely studied due to its wide bandwidth [4]–[15]. The smaller wavelength at millimeter-wave frequency leads to higher free-space path loss (FSPL); however, it also facilitates small-size high-gain antenna design, which can be used to compensate for the loss. Phased-array beamforming directive communication is one of the distinguishing features of 5G NR; it enables enhanced signal strength and spatial efficiency [4], [11], [16]–[39]. There are several approaches for phased-array beamforming:

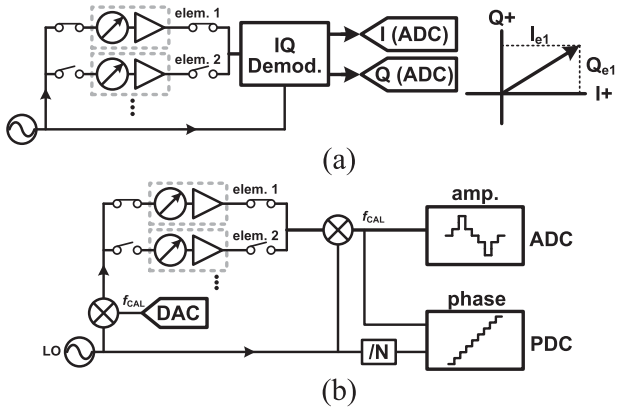


Fig. 1. Phased-array element calibration. (a) Conventional. (b) Proposed.

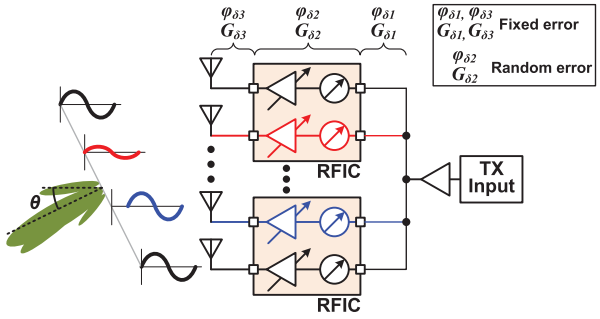


Fig. 2. Phased-array transceiver with the error effect.

phase shifting in the radio frequency (RF) stage, in the local-oscillator (LO) stage, and in the digital baseband stage. The RF phase-shifting architecture has the advantages of small area and low power consumption by phase shifting and signal combining at the RF path and sharing the other RF blocks. However, the RF phase shifting usually suffers from gain variation versus phase-shifting issue, which deteriorates the beamforming quality [40]. The digital phase shifting enables the highest beamforming flexibility by digitizing the delay and executing beamforming and signal combining in the digital domain. However, the system complexity and dc power consumption will increase extensively with the array size increases.

Recent years, the millimeter-wave phased-array transceivers based on LO phase-shifting architecture have been demonstrated [16]–[20], [32]. This architecture is attractive because the insertion loss, non-linearity of a phase shifter will not be directly applied to the transceiver front-end performance. In addition, by saturating the LO drive power of the mixer, the LO phase-shifting-based transceiver can achieve very fine beamsteering resolution and gain-invariant phase tuning. As a result of the gain-invariant phase-tuning characteristic, a simplified array element calibration procedure can be designed by first calibrating the amplitude of each element and then calibrating their phases. By using the phase and amplitude calibrations, the phased-array beamforming accuracy can be enhanced to minimize amplitude and phase mismatch, especially for a large-scale antenna array used in the base station (BS). As shown in Fig. 1(a), the conventional phased-array calibration methods [37]–[39] are mainly in the analog domain using IQ demodulator or phase detector. Both the phase and amplitude can be calculated and quantized using the demodulated IQ signal. However, the analog phase detection is either lack of sufficient accuracy or limited by quantization steps. To overcome these issues, as shown in Fig. 1(b), this article proposes a calibration scheme using independent phased and amplitude detector. This scheme avoids inaccuracy and limited resolution in the conventional analog methods.

This article introduces a 39-GHz phased-array transceiver with LO phase-shifting architecture and proposed a highly accurate built-in phase–amplitude digital calibration. The calibration scheme reuses a pair of sub-array TX and RX; the phase and amplitude information at the TX or RX RF stage can be down-converted to the IF stage and further quantized in the calibration block. A phase quantization technique is also proposed by using a phase-to-digital converter (PDC). The built-in calibration has a measured accuracy of 0.08° rms phase error and 0.01-dB rms amplitude error. The 39-GHz phased-array transceiver supports 5G NR 400-MHz 256-QAM OFDMA in 1-m link over-the-air (OTA) measurement at band n260.

This article is an extension of [41], and it is organized as follows. Section II discusses the proposed calibration scheme. Section III provides a detailed explanation of transceiver design and phased-array module implementation. Section IV introduces the measurement setup and results. Section V concludes this article.

II. Proposed Calibration Scheme

A. Effect of Phased-Array Element Error

By using low-cost CMOS technology, the digital-intensive high-EIRP millimeter-wave phased-array beamforming transceiver for BS can be realized with large-scale antenna elements [42]. However, the element error of a phased-array system will degrade the beamforming quality and link data rate, especially in the case of large array elements with a narrow beamwidth. As shown in Fig. 2, the element error has mainly three contribution sources: signal distribution path, IC characteristic, and antenna feeding. The distribution errors between ICs and PCBs are fixed errors due to fabrication and implementation mismatch. The IC characteristics due to the process variation, nonlinearity, and AM/PM AM/AM effects will create a variable error during operation. The antenna feeding path also creates significant error at millimeter-wave frequency. The wave velocity in the substrate will be decreased by a factor of $1/\sqrt{\varepsilon_r}$, where ε_r is the relative permittivity of the dielectric. A 1-mm implementation error will lead to 90° phase error using a low-permittivity ($\varepsilon_r = 3$) material substrate.

The effect of element error is modeled to illustrate the corresponding degradation of beamforming quality. The linear isotropic antenna array is shown in Fig. 3, and the total array element is N with an element space of d. The distance between a far-field point and the nth element is r_n. The excitation current on the nth element with phase and amplitude error

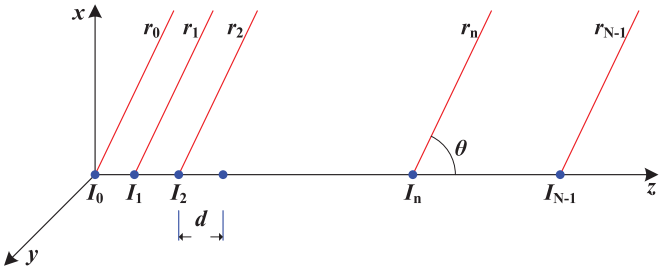


Fig. 3. Linear isotropic antenna array.

is given by

$$I_n = I_0 10^{G_{\delta n}/20} e^{-j(n\alpha+\varphi_{\delta n})}, \quad (n = 0, 1, 2, \ldots, N-1) \tag{1}$$

where I_0 is the first antenna element excitation current, α is the phase offset of two adjacent elements, and $G_{\delta n}$ and $\varphi_{\delta n}$ are random amplitude error and phase error. Therefore, the nth antenna element far-field radiation field is

$$E_n = j\frac{60I_n}{r_n} e^{-j\beta r_n}, \quad (n = 0, 1, 2, \ldots, N-1) \tag{2}$$

where $\beta = 2\pi/\lambda$ is known as the propagation constant. The total radiated field is summed as

$$E_{\mathrm{T}} = \sum E_n = j\frac{60I_0}{r_0} e^{-j\beta r_0} \sum 10^{G_{\delta n}/20} e^{-j\beta(r_n - r_0)} e^{-j(n\alpha+\varphi_{\delta n})} \tag{3}$$

$$= E_0 \cdot \sum 10^{G_{\delta n}/20} e^{-j(n(\beta d\cos\theta - \alpha)+\varphi_{\delta n})} = E_0 \cdot f(\theta) \tag{4}$$

where E_0 is the normalization coefficient, which is independent with phase offset α, space d, and direction θ. The normalized total radiation pattern $f(\theta)$ with different random error factors is modeled to demonstrate the effect of element error. Fig. 4 shows the calculated radiation pattern of a 16-element linear array with different random error efforts at the space of $d = 0.5\lambda$. The simulation shows a minimum phase error of 10° and an amplitude error of 1.5 dB are required for maintaining less than 3-dB sidelobe degradation while steering the beam direction angle. A phased-array transceiver without calibration is introduced in [36] with an error range of $G_\delta = \pm 2$ dB in gain and $\varphi_\delta = \pm 20°$ in phase. As shown in Fig. 4, the phase and gain error may lead to 10-dB degradation in sidelobe. A potential sidelobe suppression is required for mass production.

B. Phase and Amplitude Calibrations

At first, the conventional phase calibration methods are analyzed. In [37], the calibration employs an IQ demodulator to quantize the phase and amplitude for TX and RX through a coupling network. By comparing the phase and amplitude of the low-frequency IQ output signals from different paths, the path error can be calibrated. However, the phase is calculated from IQ signal amplitude in ADC, and the accuracy is limited to ±7° as reported. More accurate phase calibration methods are reported in [38] and [39]. The key technique is to utilize the characteristic of phase detector at a fixed 90° phase offset. When the phase offset of two input signals has a 90° phase offset, the phase detector can achieve the highest accuracy, which are ±0.6° and ±1° in [38] and [39],

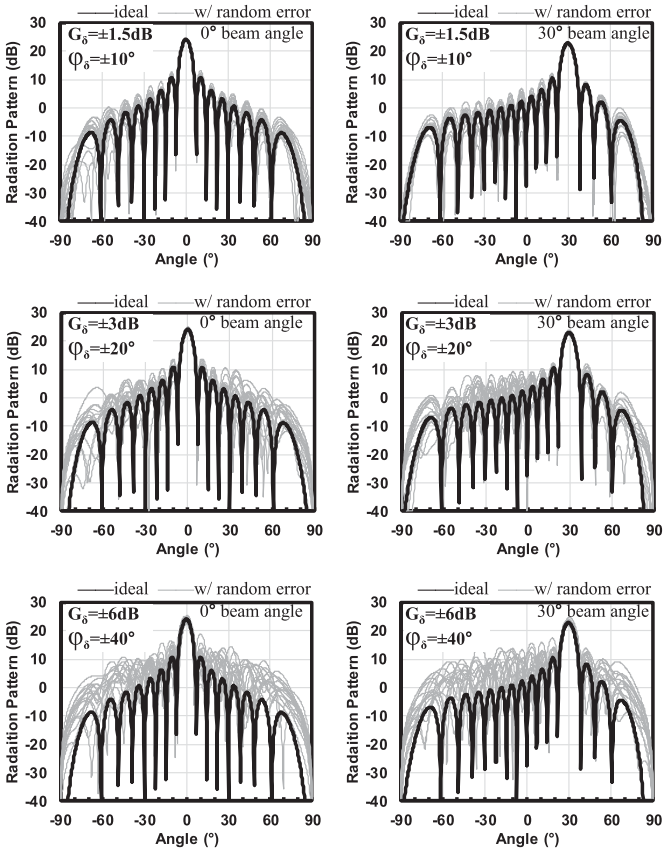


Fig. 4. Calculated radiation pattern with the random error effect.

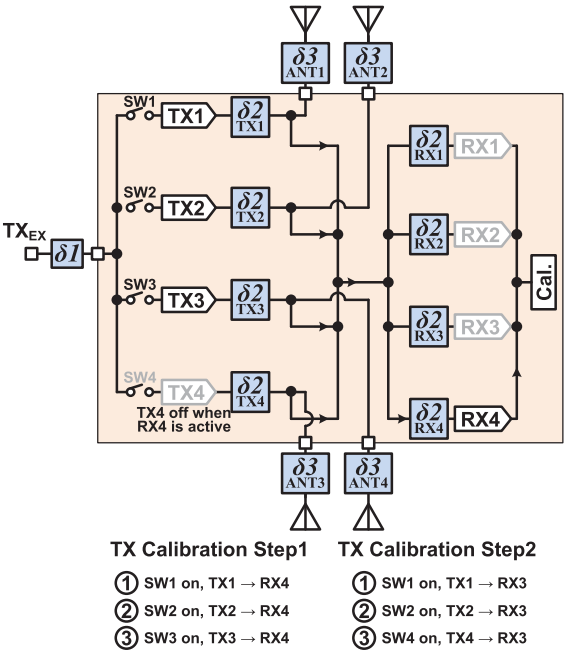


Fig. 5. TX error calibration using a fixed RX.

respectively. However, this method limits the calibration step to 90° in [38] and an improved step of 22.5° in [39].

In order to overcome these issues, this article proposes a highly accurate on-chip calibration scheme for eliminating the variable errors $\delta 2$ among sub-array TRXs, as shown in Fig. 5.

The fixed errors $\delta 1$ and $\delta 3$ in Fig. 5 can be calibrated one time. For TX calibration, the sub-array TX RF outputs are connected to a fixed RX. It can be proven that the phase and amplitude differences in the RF node between the TXs will keep the same when they are down-converted to a low frequency. In the first step, the phase and amplitude differences between TX1, TX2, and TX3 can be calibrated using RX4. In the second step, the remaining TX4 phase and amplitude differences can be calibrated using RX3. Based on this concept, this article implements a phased-array transceiver with a built-in calibration block, which can be used for on-chip sub-array TRX calibration and high-accurate phase–amplitude tuning. The large array calibration can be automatically performed using a far-field antenna or near-field algorithm in [43]. Fig. 6(a) shows a simplified block diagram of the four-element phased-array transceiver IC; sub-array TRX RF nodes are connected to each other symmetrically. The external LO frequency and IF frequency are set to 1/10 of the RF frequency; a $\times 9$ frequency multiplier is used to provide $\times 9$ LO for frequency conversion at the RF stage. In the calibration mode, a very low-frequency offset f_{CAL} (*e.g.*, $f_{\mathrm{CAL}} = 120$ kHz) is set between f_{IF} and f_{LO}, defined as $f_{\mathrm{IF}} = f_{\mathrm{LO}} + f_{\mathrm{CAL}}$. In the calibration process, the phase and amplitude information in the RF node of TX output or RX input is down-converted to IF frequency f_{IF} and further quantized in the calibration block. For the case of TX calibration, the RX is fixed to guarantee the quantized phase, or the amplitude difference is entirely from TX tuning, and vice versa for the RX calibration. The signal contains phase or amplitude information at IF frequency is further down-converted to a low-frequency f_{CAL} in the calibration block. The phase and amplitude adjustments can be quantized at a different frequency due to the phase linear-combination characteristic and amplitude multiplication characteristic of the mixer. For a given initial RF signal with an expression of $A_{\mathrm{RF}} \cos(\omega_{\mathrm{RF}} t + \varphi_{\mathrm{RF}})$, the output signal down-converted by a mixer in sub-array RX is

$$V_{\mathrm{IF\_out}} = A_{\mathrm{RF}} \cos(\omega_{\mathrm{RF}} t + \varphi_{\mathrm{RF}}) \times A_{\mathrm{LO}} \cos(9\omega_{\mathrm{LO}} t + \varphi_{\mathrm{LO}}) \quad (5)$$

$$= \frac{1}{2} A_{\mathrm{RF}} A_{\mathrm{LO}} \cos((\omega_{\mathrm{RF}} - 9\omega_{\mathrm{LO}})t + (\varphi_{\mathrm{RF}} - \varphi_{\mathrm{LO}})) + \frac{1}{2} A_{\mathrm{RF}} A_{\mathrm{LO}} \cos((\omega_{\mathrm{RF}} + 9\omega_{\mathrm{LO}})t + (\varphi_{\mathrm{RF}} + \varphi_{\mathrm{LO}})). \quad (6)$$

Filtering using a low-pass filter (LPF) and assuming that $\varphi_{\mathrm{LO}} = 0$ and $A_{\mathrm{LO}} = 1$, the output is then

$$V_{\mathrm{IF\_out}} = \frac{1}{2} A_{\mathrm{RF}} \cos(\omega_{\mathrm{IF}} t + \varphi_{\mathrm{RF}}) \quad (7)$$

where A_{RF} is the RF input signal amplitude, and ω_{RF}, φ_{RF}, ω_{LO}, and φ_{LO} are RF input signal and LO signal frequency and phase, respectively. The mixer is treated as an ideal signal multiplier for simplicity. It can be seen in (7) that the down-converted output signal has amplitude proportional to the RF input signal and a phase linear to the RF input signal.

In order to realize highly accurate beamsteering, the initial phase or amplitude value before tuning and the target value after tuning are calibrated digitally. A simplified calibration block is shown in Fig. 6(a). The calibration block mainly consists of an IF mixer, an LPF, an ADC for amplitude quantization, and a PDC for phase quantization. The IF mixer in the calibration block further down-converts (7) to low-frequency f_{CAL}; again, assuming the mixer as an ideal signal multiplier, the output signal for quantization in calibration block is

$$V_{\mathrm{CAL\_out}} = \frac{1}{4} A_{\mathrm{RF}} \cos(\omega_{\mathrm{CAL}} t + \varphi_{\mathrm{RF}}). \quad (8)$$

It can be seen in (8) that the phase and amplitude information from RF can be indicated at low frequency effectively. As shown in Fig. 6(b), the RF signal with phase tuning has an expression of $A_{\mathrm{RF}} \cos(\omega_{\mathrm{RF}} t + \varphi_{\mathrm{RF}} + \Delta\varphi)$; after down-conversion, the phase difference $\Delta\varphi$ at f_{CAL} corresponds to a longer timing difference than at f_{RF}. A PDC is designed for converting analog phase value to digital, which will be explained in detail in Section III.

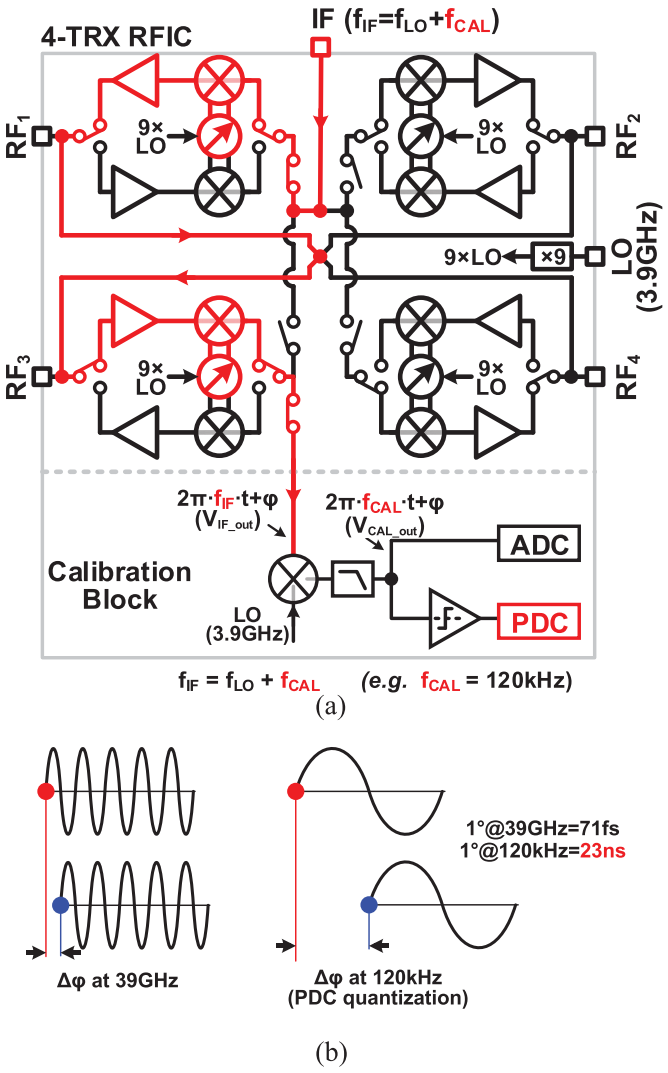


Fig. 6. (a) Block diagram of the four-element phased-array transceiver IC with simplified calibration block for amplitude and phase calibration. (b) Phase-tuning calibration at low-frequency f_{CAL}.

C. LOFT Calibration

Since, in this work, the phased-array transceiver is based on LO phase-shifting architecture, the LO feedthrough (LOFT) will also be radiated from the antenna array, which will

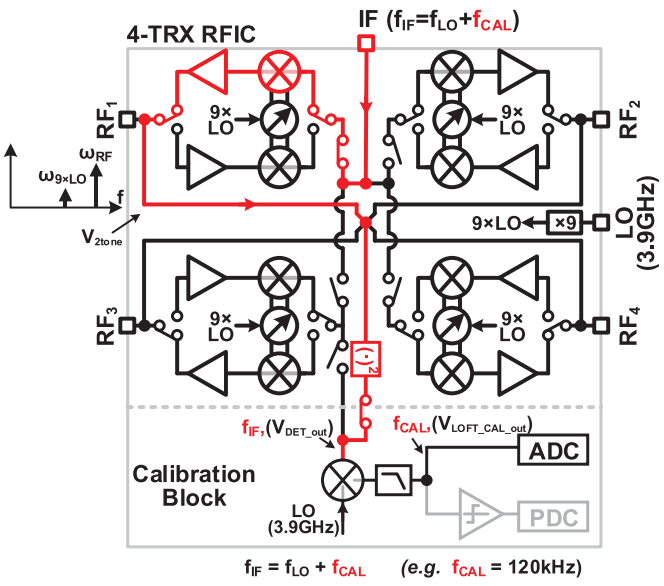


Fig. 7. LOFT calibration scheme.

become a great interference to other wireless receivers. Theoretically, a balanced mixer can suppress the LOFT using a pair of switches driven by differential LO. However, due to the mismatch on switch transistor layout and fabrication, the differential LOFT signal at the RF path cannot exactly cancel each other and, therefore, lead to potential LOFT issues. Prior work [44] presents a power-efficient LOFT calibration method, which can be easily extended to this phased-array transceiver with a shared calibration block for phase and amplitude.

The LOFT calibration scheme is illustrated in Fig. 7. Instead of detecting LO power level directly at the transmitter output using a transmitter signal strength indicator (TSSI), which requires a down-conversion block with additional LO, the proposed method employs a square-law detector with two-tone signal input. The sinusoid IF input is up-converted to RF, and it is combined with LO to create the two-tone signal for the square-law detector. The IF input for LOFT calibration has the same frequency offset with LO as before. Given the two-tone signal LO and RF as in the following expression:

$$V_{2\text{tone}} = A_{\text{RF}}\cos(\omega_{\text{RF}}t) + A_{\text{LOFT}}\cos(9\omega_{\text{LO}}t). \tag{9}$$

where A_{LOFT} is the LOFT amplitude. The output of the square-law detector is

$$\begin{aligned} V_{\text{det\_out}} &= (V_{2\text{tone}})^2 && (10)\\ &= (A_{\text{RF}}\cos(\omega_{\text{RF}}t) + A_{\text{LOFT}}\cos(9\omega_{\text{LO}}t))^2 && (11)\\ &= A_{\text{RF}}A_{\text{LOFT}}\cos((\omega_{\text{RF}} - 9\omega_{\text{LO}})t)\\ &\quad + A_{\text{RF}}A_{\text{LOFT}}\cos((\omega_{\text{RF}} + 9\omega_{\text{LO}})t)\\ &\quad + (A_{\text{RF}}\cos(\omega_{\text{RF}}t))^2 + (A_{\text{LOFT}}\cos(9\omega_{\text{LO}}t))^2. && (12)\end{aligned}$$

The high-frequency and dc components in (12) can be filtered, and the detector remaining output is

$$V_{\text{det\_out}} = A_{\text{RF}}A_{\text{LOFT}}\cos(\omega_{\text{IF}}t). \tag{13}$$

Since the LOFT detector output signal (13) has the same frequency with output signal (7) in the amplitude calibration, the LOFT amplitude quantization can reuse the same calibration block introduced in Section II-B. Assuming an ideal IF mixer, the detector IF output is down-converted to f_{CAL} for the calibration using ADC, and it can be expressed as

$$V_{\text{LOFT\_CAL\_out}} = \frac{1}{2}A_{\text{RF}}A_{\text{LOFT}}\cos(\omega_{\text{CAL}}t). \tag{14}$$

In the LOFT calibration process, the IF input amplitude and the TX/RX gain characteristic are fixed; thereby, the RF amplitude f_{RF} is also fixed in (14). The amplitude of $V_{\text{LOFT\_CAL\_out}}$ is dependent only on LOFT level A_{LOFT}. The automatic LOFT calibration can be realized by adjusting the TX mixer dc offset and gate bias to search minimum $V_{\text{LOFT\_CAL\_out}}$, which corresponds to the best LOFT cancellation. The detailed circuit design and consideration are introduced in Section III.

III. Transceiver Implementation

A. Transceiver Architecture

Fig. 8 shows the proposed 39-GHz phased-array transceiver detailed system architecture. The transceiver chip is composed of four sub-array transceivers, an LO phase-shifting chain, and a calibration block. The transceiver is based on the LO-phase-shifting architecture since it can achieve very fine beamsteering resolution and gain-invariant phase tuning. Both the IF and LO frequency are chosen as 3.9 GHz to minimize the number of LO synthesizers. The external 3.9-GHz LO is distributed to the ×9 frequency multiplier and the calibration block. The sub-array transceiver single-ended IF port can switch to external IF path or internal calibration path through the switch depending on the operation mode. The calibration block has two signal input paths: one is for phase and amplitude calibrations, and another is for LOFT calibration. A quarter-wavelength transmission line (TL)-based coupling network is used to connect four sub-array transceiver RF ports for calibration. Besides the RF path, the IF and LO paths are also connected using a coplanar waveguide with a lower ground plane (CPWG) TL, as shown in Fig. 9(a). Including T-junction, L-junction, and cross-line, the TL is measured and modeled up to 110 GHz using multi-line de-embedding method introduced in [15] and [45]–[47]. Fig. 9(b)–(d) shows the cross TL structure. A metal–insulator–metal TL (MIMTL) is used for the VDD supply. The MIMTL consists of a TL and large shunt MIM decoupling capacitors for filtering supply noise [15], [45]. A bias and logic block for phase tuning, gain setting, mode setting, and digital readout are integrated. A Raspberry Pi computer is used to control the transceiver chips through a serial peripheral interface (SPI).

In order to realize a fully symmetric network for calibration, the layout design of the calibration RF path, the IF path, and the calibration IF path is illustrated in Fig. 10. The TLs with the same labels have the same physical lengths in the layout. The single-ended IF is chosen for less layout complexity, which also leads to the use of a pseudo-single-balanced mixer. With the same TL length, the calibration RF path, the IF path, and the calibration IF path are kept identical to all the sub-array TXs and RXs. The consistency is checked by using

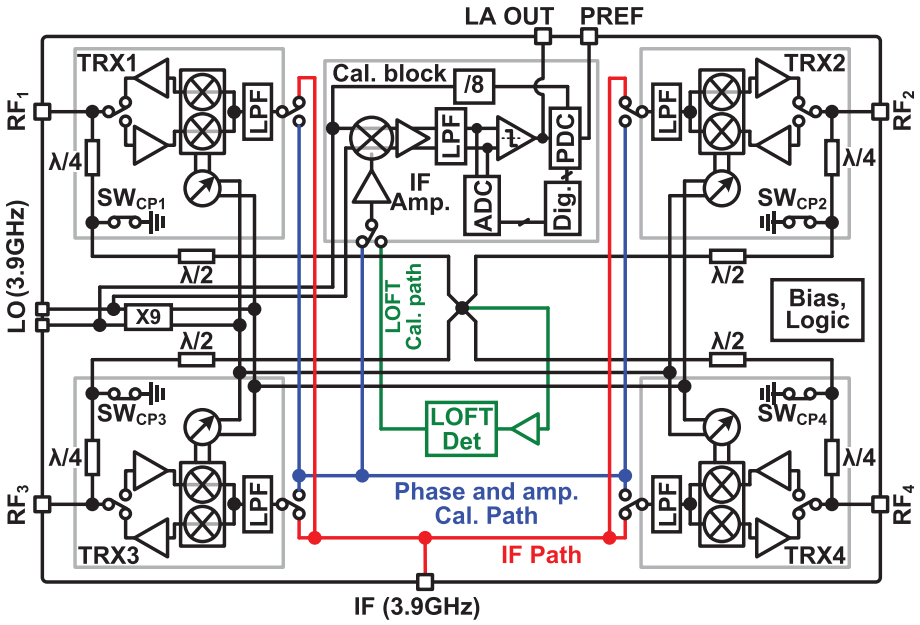


Fig. 8. Detailed block diagram of the proposed phased-array transceiver with built-in calibration.

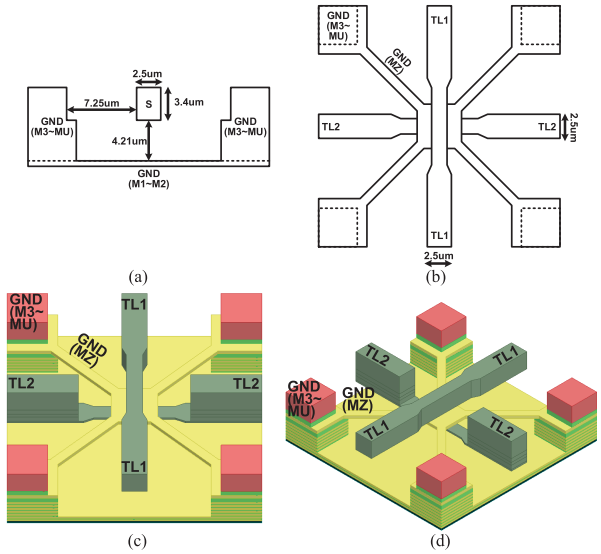


Fig. 9. (a) CPWG TL. (b) CPWG TL cross structure. (c) CPWG TL cross side view. (d) CPWG TL cross rotated side view.

the measurement-based TL model; the maximum phase and gain difference of calibration RF paths between any pair of sub-array TX and RX are 0.8° and 0.02 dB, respectively. Furthermore, considering the load impedance effect, a 20% mismatch is introduced in the load impedance of the antenna. With the load impedance mismatch effect, the maximum phase and amplitude differences of calibration RF paths between any pair of sub-array TX and RX are less than 2.0° and 0.5 dB, respectively.

The switches shown in Fig. 9 have two operation modes. In the transmitting mode or the receiving mode, the SW-IF switches are all turned on, and the SW-CAL switches are all turned off. The simulated IF splitter gains in the transmitting mode and the receiving mode are −12 and −14 dB,

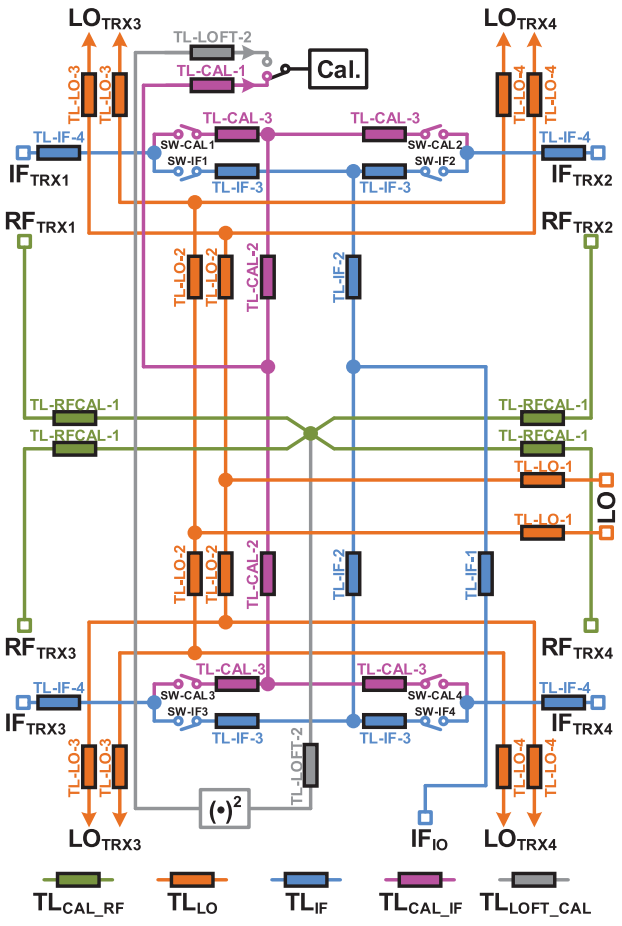
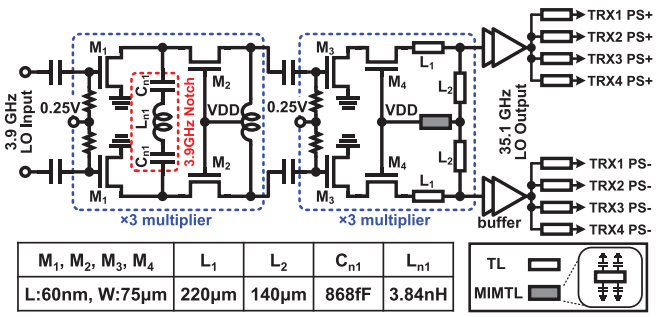


Fig. 10. Symmetric signal distribution layout using TL.

respectively. In the phase or gain calibration mode, a pair of sub-array TX and RX are turned on for calibration; the sub-array TX and RX corresponding SW-IF switch and



M_1, M_2, M_3, M_4	L_1	L_2	C_{n1}	L_{n1}
L:60nm, W:75μm	220μm	140μm	868fF	3.84nH

Fig. 11. Circuit schematic of the ×9 frequency multiplier.

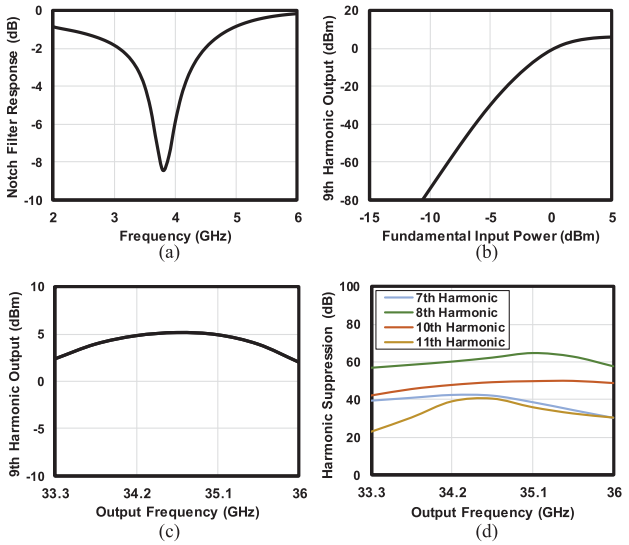


Fig. 12. ×9 frequency multiplier simulated performance. (a) 3.9-GHz notch filter insertion loss. (b) Ninth-harmonic signal output power against 3.9-GHz fundamental input power. (c) Ninth-harmonic output bandwidth with 3-dBm input power. (d) Output harmonic suppression with 3-dBm input power.

SW-CAL switch are turned on, while the other SW-IF switches and SW-CAL switches are turned off. It can be seen that no matter which pair of sub-array TX and RX is chosen, the calibration paths are identical. The simulated IF path gain in the calibration mode is −7 dB; CAL_IF splitter gain in the calibration mode is −8 dB.

B. LO

The LO chain consists of a ×9 frequency multiplier and a phase-shifting block. Fig. 11 shows the detailed circuit schematic of the ×9 frequency multiplier. The ×9 frequency multiplication is realized by cascading two stages of ×3 multiplier. Both multipliers are with a differential topology for intrinsic even harmonic suppression [32], [48]. The 3.9-GHz LO fundamental signal is further suppressed by using a differential *LC* notch filter with a peak frequency at 3.9 GHz. The differential *LC* notch filter consists of two 8.68-fF capacitors and a 3.84-nH inductor. With the notch filter, low impedance to the ground will be created at 3.9 GHz. Fig. 12(a) shows the simulated notch filter insertion loss, a 8.2 dB suppression at 3.9 GHz is realized. The multiplier transistor is biased in the sub-threshold region to enhance non-linearity for third-harmonic generation. Fig. 12(b) shows the simulated 9th LO harmonic signal has a saturated power of 5 dBm with fundamental frequency at 3.9 GHz. The 9th LO harmonic signal output power flatness and harmonic suppression are shown in Fig. 12(c) and (d), respectively. The ×9 frequency multiplier has a 3 dB output power flatness and higher than 22 dB harmonic suppression over 33.3 GHz to 36 GHz. The multiplier output is distributed to phase shifters in each sub-array transceivers.

Fig. 13(a) shows the detailed block diagram of the proposed LO phase-shifting chain. Different from the RF phase-shifting architecture, in which the phase shifter is required with a wide-bandwidth high-linearity characteristic, the LO phase-shifting architecture only handle the continuous wave (CW) signal. As a result, there are more flexible choices on the LO phase shifter topology. In this work, the 35.1 GHz differential LO signal is first converted to a quad-phase signal by using a poly-phase filter (PPF). The PPF is then followed by a 3-bit phase selector, which further divides the phase-shifting step from 90° to 45°. The fine phase shifting is realized by utilizing an *LC*-resonator-based phase shifter with voltage-controlled varactor, as shown in Fig. 13(b). In order to minimize the load impedance variation on phase selector during the fine phase tuning, this article proposes a cascode switching array topology with an additional buffer to provide the required isolation between the PPF and the fine phase shifter. There are four switch controls in the phase selector, which are SW0, SW1, SW2, and SW3 corresponding to 180°, 0°, 270°, and 90° phase selection. In addition, as shown in the phase mapping chart, the phase selection step is further divided by vector summing the quadrature phase [20]. In the case of only one switch is turned on, for instance, SW1 or SW3 is set from "0" to "1," the phase selector has an output phase of 0° or 90°, respectively. Once a pair of switches with 90° phase offset are turned on simultaneously, for instance, SW1 and SW3 are both on with the switch status of "0101," and 45° can be generated from the phase selector. Fig. 13(c) shows the phase mapping of the 3-bit phase selector with corresponding switch codes. Compared with the 90° quadrant phase selector, the proposed phase selector has a smaller phase step; consequently, the fine phase shifter can be designed with a relaxed phase coverage, which improves the gain consistency over the varactor tuning range. The fine phase shifter is based on *LC*-resonator topology following the design in [32]. In this work, due to the reduced phase step, the capacitance tuning range can be realized by using the only varactor instead of employing additional switching capacitor banks; therefore, the gain variance resulting from the fine phase tuning is minimized. The MOS varactor in fine phase shifter has a fixed bias V_B on bulk contact and a 10-bit DAC controlled bias voltage V_C on the gate. Fig. 13(d) illustrates the phase-shifting range of the *LC* resonator-based fine phase shifter. Fig. 14(a) shows the simulated phase-shifting value with controlling V_C. The bulk bias V_B is set as 0.5 V to prevent the MOS varactor from over accumulation or over the inversion. Fig. 14(b) shows the measured phase map with all eight phase-selector modes. Due to the LO phase-shifting architecture as well as the

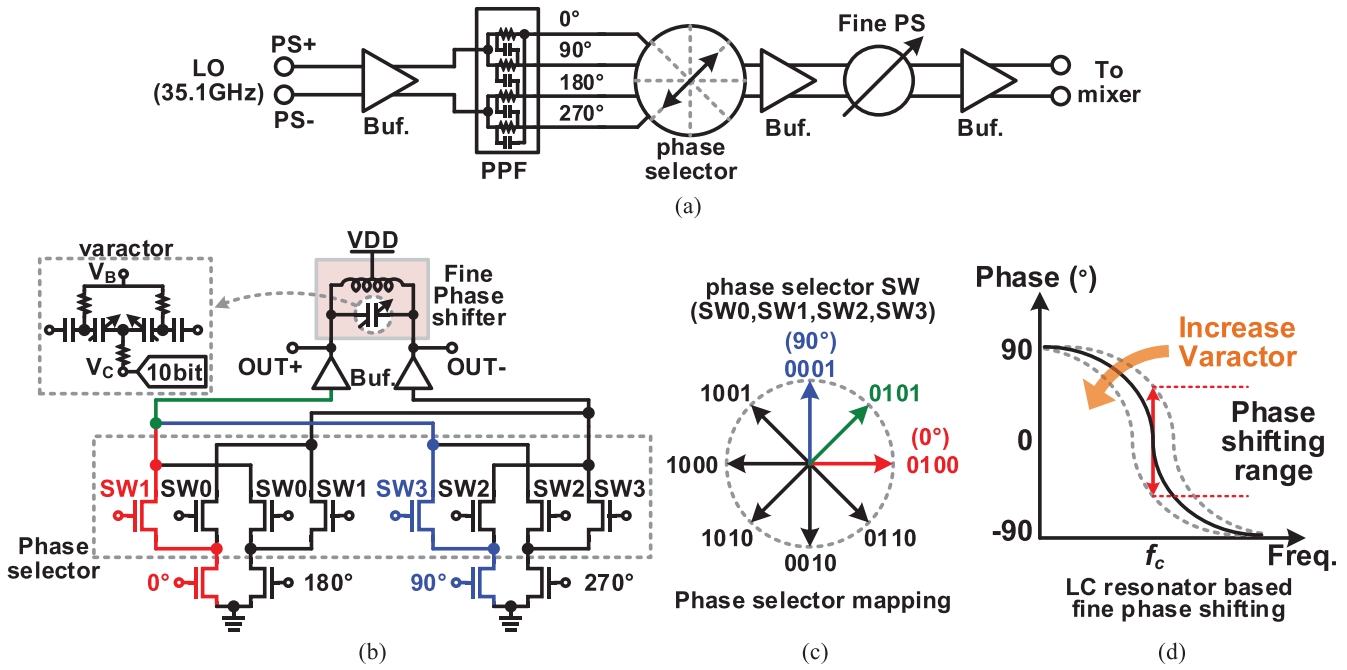


Fig. 13. LO phase shifter chain. (a) Detailed block diagram of LO phase-shifting chain. (b) Circuit schematic of phase selector and phase shifter. (c) Phase mapping of 3-bit phase selector. (d) *LC* resonator-based fine phase shifting.

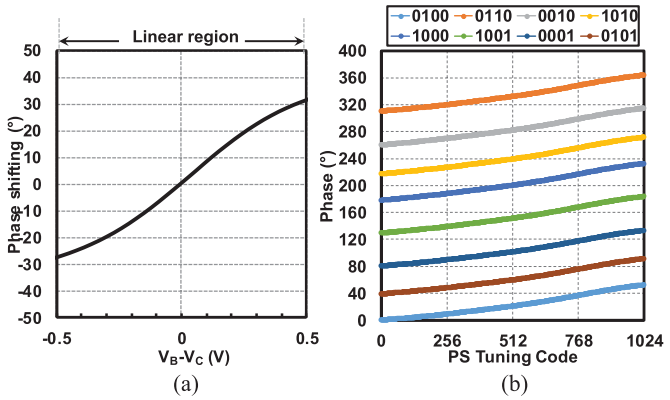


Fig. 14. LO phase shifter. (a) Varactor bias for linear phase-tuning region. (b) Measured 360° phase mapping.

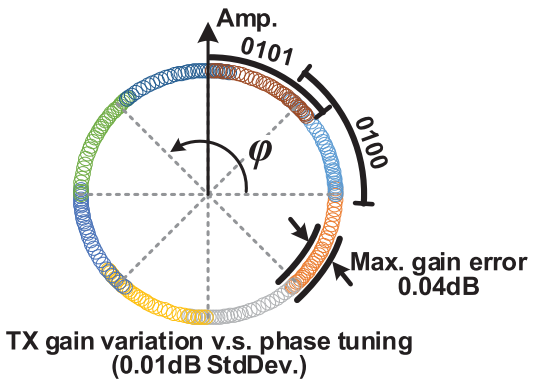


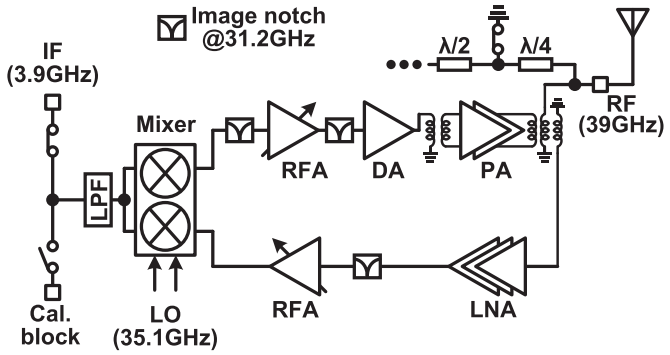
Fig. 15. Measured TX gain variation against 360° phase tuning.

reduced phase-selector step, the proposed transceiver realizes a gain-invariant phase-tuning characteristic. The LO chain, including output buffer, has realized a simulated output power of more than 5 dBm to drive the mixer. Fig. 15 shows the measured TX gain variation over the entire 360° phase-shifting range. The gain variation over phase shifting is measured by observing the TX output power in power meter while tuning the TX phase shifter. The measured gain has a maximum variance of 0.04 dB and a standard deviation of 0.01 dB over the entire phase-shifting range.

C. Front-End Design

The detailed block diagram and gain contribution of the sub-array transceiver RF front end are shown in Fig. 16. The sub-array transceiver consists of a pseudo-single-balanced mixer with LPF for both TX and RX frequency conversions, a series of TX gain stages, including a two-stage differential power amplifier (PA), and a three-stage low-noise amplifier (LNA) followed by an RF amplifier. The *LC*-based notch filters are inserted in both TX and RX for image signal suppression. A pair of single-pole–single-throw (SPST) IF switch are used to select the signal path from IF or calibration block. A switched quarter-wavelength TL is used to control the signal coupling from the RF path for calibration. The insertion loss on PA and LNA is 0.6 dB.

The single-ended IF interface is used to facilitate the phased-array transceiver system implementation as well as the chip layout. Usually, in superheterodyne TX, the single-ended IF up-converting to RF will lead to LOFT leakage, which will be emitted through the antenna and become an undesired interference signal for other wireless devices. To address



	TX				RX		
Blocks	IF Splitter	Mixer	RFA+DA	PA	LNA+RFA	Mixer	IF Splitter
Gain (dB)	-12	-14	17	15	33	-15	-14
OIP3 (dBm)	∞	6	9	23	19	5	∞

Fig. 16. Sub-array TRX front-end block diagram.

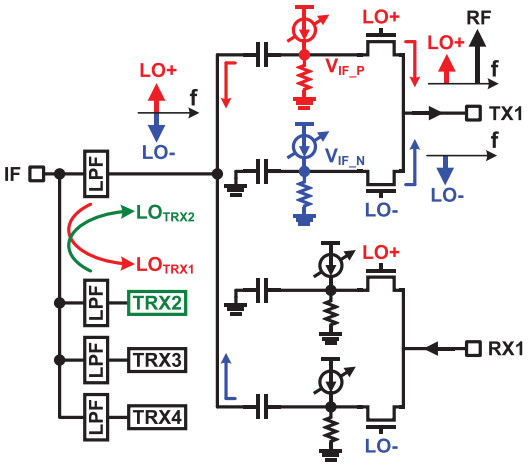


Fig. 17. Pseudo-single-balanced mixer circuit schematic with LOFT cancellation and LO isolation.

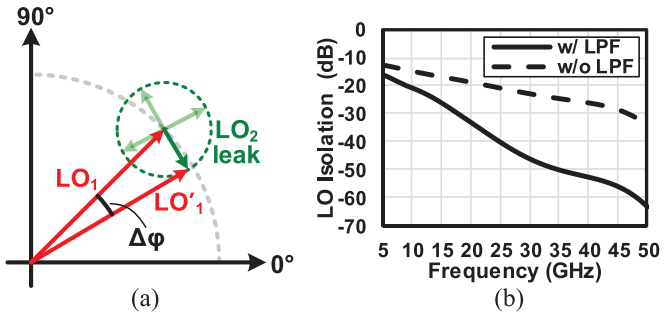


Fig. 18. (a) LO phase dependence on leakage from other LOs. (b) Simulated LO isolation.

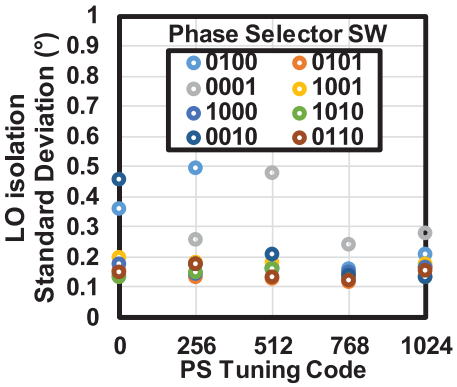


Fig. 19. Measured LO isolation over 360° phase tuning.

this issue, a pseudo-single-balanced mixer is proposed by associating with a dummy path. Fig. 17 shows the proposed mixer circuit schematic. In TX, the proposed mixer combines the signal path (LO+) and a dummy path (LO−) for LOFT cancellation. However, due to the layout and fabrication mismatch between the signal path and the dummy path, the LOFT cancellation requires additional calibration on dc offset [13], [44]. The current sources at the TX IF input are used for LOFT calibration. By adjusting the current source, the mixer dc-offset voltage at the IF node ($V_{\mathrm{IF\_P}}$ and $V_{\mathrm{IF\_N}}$) can compensate for the LOFT mismatch between the signal path and dummy path. In addition, associating with the RX path, the proposed mixer mitigates the issue of LO leakage to the IF path, which causes LO phase shifters affecting each other when tuning the phase. As shown in Fig. 17, when the TX1 path is ON, the LO leakage from the TX1 mixer will be leaked through the IF path to LOs in the other TRXs. The phase dependence on leakage from other LO is illustrated in Fig. 18(a). For simplicity, only LO_1 and LO_2 are shown in Fig. 18(a), and the LO_1 initial phase is fixed while changing the LO_2 phase. It can be observed that the LO_1 phase will also be shifted to LO'_1 due to vector summing with LO_2 leak signal, while LO_2 phase is changing. Assume that the amplitudes of LO_1 and LO_2 leak are A and $k \cdot A$, respectively. The maximum phase difference $\Delta\varphi_{\max}$ between LO_1 and LO'_1 can be expressed as

$$\sin(\Delta\varphi_{\mathrm{MAX}}) = (k \cdot A)/A = k. \tag{15}$$

Since LO_2 is the leakage signal, which usually has a much smaller amplitude than LO_1, we have $k \approx \sin(k)$, and $\Delta\varphi_{\mathrm{MAX}}$ can be further simplified as

$$\Delta\varphi_{\mathrm{MAX}} = k. \tag{16}$$

It indicates that LO_1 phase variance affected by LO_2 is proportional to LO_2 leakage signal level, which should be suppressed as small as possible. The mitigation of the LO leakage to the IF path is realized by summing the LO signals in the antithetical phase. The mixer for TX and RX is turned on simultaneously; moreover, the LO for RX mixer is connected to anti-phase (LO−) for cancellation. An *RC* LPF at the mixer IF port is added to further enhance the LO isolation. Fig. 18(b) shows the simulated LO isolation. It can be seen at the LO frequency of 35.1 GHz, the LO isolation is improved by 25 dB, which means that the phase dependence on phase tuning in other LOs is 17.8 times improved with a low-pass filter. The measured phase variation of one TX path at different phase control code is shown in Fig. 19, which shows a maximum standard deviation of 0.5°. The phase variation is measured by sweeping the phase of other TXs over 360° with 100 iterations.

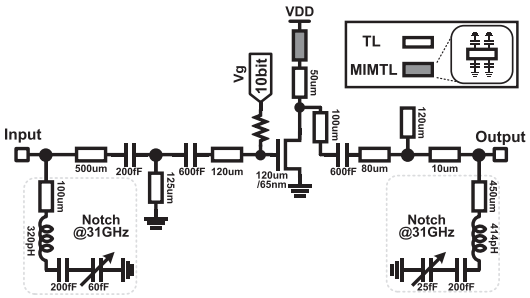


Fig. 20. TX RF amplifier with 31-GHz notch filters.

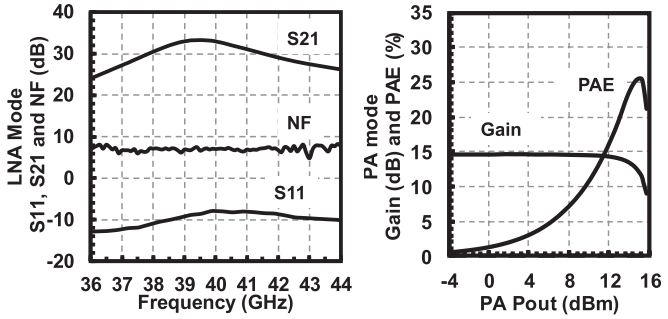
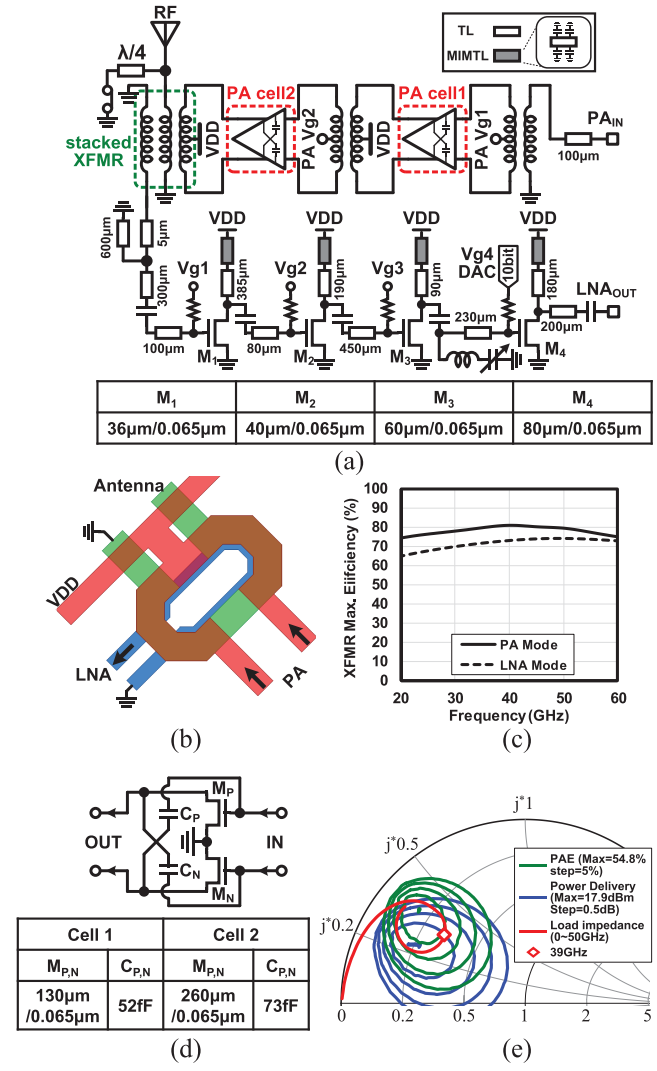


Fig. 22. PA/LNA measured results.



M_1	M_2	M_3	M_4
36μm/0.065μm	40μm/0.065μm	60μm/0.065μm	80μm/0.065μm

(a) (b) (c)

Cell 1		Cell 2	
$M_{P,N}$	$C_{P,N}$	$M_{P,N}$	$C_{P,N}$
130μm /0.065μm	52fF	260μm /0.065μm	73fF

(d) (e)

Fig. 21. (a) PA/LNA detailed circuit schematic. (b) Stacked transformer for the shared antenna. (c) Simulated transformer efficiency. (d) Differential PA cell. (e) Simulated PA load impedance.

The TX RF amplifier circuit schematic is shown in Fig. 20. The RF amplifier employs common source topology with an adjustable bias in a range from 400 to 600 mV. The total gain range of RF amplifier and driver amplifier is from 8 to 17 dB. In TX, two notch filters with 15-dB insertion loss at an image frequency of 31 GHz are added for satisfying the out-of-band emission (OOBE) EIRP regulation [49].

The PA/LNA with shared antenna, as shown in Fig. 21(a), employs the proposed stacked transformer to switch between the PA mode and the LNA mode. The transformer middle layer is designed to couple PA output power when PA is ON and couple to LNA input when LNA is ON. The PA employs differential architecture for achieving 3-dB higher power than single-ended PA. The capacitive neutralization technique is used in the PA core cell for gain enhancement at the millimeter-wave frequency. The differential PA final stage impedance is decided by load-pull result; the transformer design is to convert the 50-Ω load impedance to optimal PA load impedance extracted by load-pull. The LNA has a single-ended architecture, the matching of the first two stages is optimized for low-noise figures; the following stages are optimized for linearity with increased transistor sizes. Fig. 21(b) shows the top view of the three-stacked transformer for the shared antenna. The red color metal layer is shown at the top; it is connected to the PA output. The PA VDD supply is also at the top layer through a center tap. The blue bottom metal layer has a single-ended output connected to LNA. The green middle layer is connected to 50-Ω impedance antenna; it converts PA differential output to single-ended in the TX mode and couples RF input to LNA. Fig. 21(c) shows the EM simulation result. When LNA is OFF, the transformer maximum efficiency from PA output to antenna input is 80% at 39 GHz; when PA is OFF, the transformer maximum efficiency from the antenna to the LNA input is 73% at 39 GHz. The efficiency of the transformer is calculated from the transformer simulated maximum available gain by $\eta_{\mathrm{MAX}} = 10^{(\mathrm{MAG}/10)}$. By comparing with the optimal individual PA and LNA design without T/R switch, the three-stacked transformer additional insertion losses are 0.7 dB in the PA mode and 1.6 dB in the LNA mode, respectively. The differential PA cell and the load-pull result are shown in Fig. 21(d) and (e). The identical standalone PA/LNA circuit is fabricated for characterization. As shown in Fig. 22, the measured LNA gain and noise figure are 33 and 7.0 dB, respectively. The measured PA achieves P_{SAT} of 15.5 dBm, $P_{1\mathrm{dB}}$ of 13.5 dBm, and peak PAE of 25.5% under deep class-AB bias.

D. Calibration Block Design

As introduced in Section II, the calibration block is designed to quantize the sub-array phase/amplitude value as well as the TX LOFT amplitude. The detailed block diagram of the calibration block is shown in Fig. 23. There is a low-frequency offset f_{CAL} (e.g., $f_{\mathrm{CAL}} = 120$ kHz) between the calibration IF

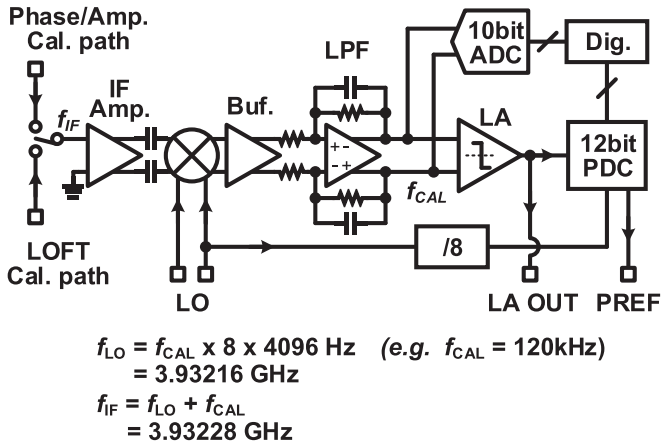


Fig. 23. Detailed block diagram of the calibration circuit.

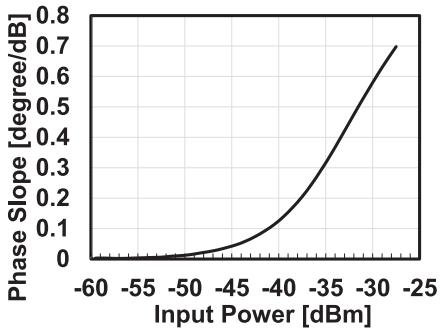


Fig. 24. Calibration block AM-PM characteristic.

input frequency and LO frequency. The calibration IF input signal comes from two paths depending on calibration modes: phase/amplitude calibration path and LOFT calibration path. In the calibration block, the IF input signal is first amplified by an IF LNA to maintain a good noise performance required by the IF demodulator. The IF amplifier is designed based on [50] for area saving. The gain of the IF amplifier has about a 10-dB tuning range to widen the detection dynamic range. The amplified signal is then down-converted to f_{CAL} for further quantization at low frequency using ADC or PDC. The down-conversion double-balanced mixer occupies a small area due to the passive architecture. An LPF with a cutoff frequency $f_{3\mathrm{dB}}$ of 320 kHz is used to suppress IF and LO leakage from the mixer. A baseband buffer that adopts a fully differential single-stage topology is inserted between the mixer and LPF for impedance matching. The signal at LPF differential output is a 120-kHz sinusoid wave with its phase and amplitude defined in (8). Thus, the amplitude can be quantized accurately by using an ADC. The readout logic realizes the mean-square function for the output of the ADC. Conventionally, the phase information can also be quantized in an ADC by mapping the detected sinusoid wave voltage to phase. However, the sinusoid waveform is not a linear waveform; the waveform slope has a great variation against the phase, which decreases the phase mapping accuracy, especially at the wave crest and trough. This article proposes a phase quantization method in the digital

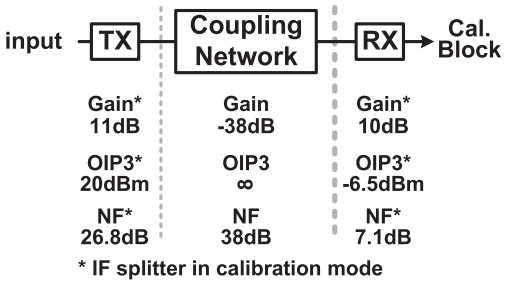


Fig. 25. TRX and coupling network characteristic in the calibration mode.

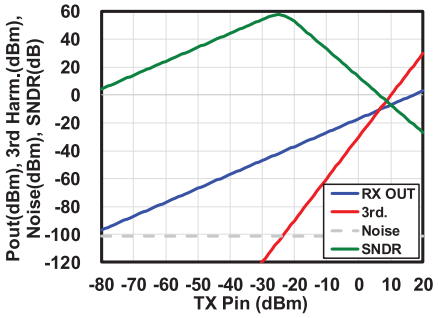


Fig. 26. Calculated calibration signal SNDR.

domain in association with a PDC. The differential sinusoid wave is converted to single-ended through a differential pair with an active current mirror circuit. An inverter-based limiting amplifier amplifies the sinusoid signal to rail-to-rail for digital operation.

In this design, we target a fine phase and gain calibration resolution of 0.1° and 0.1 dB. In order to detect 0.1° phase offset, a 12-bit PDC is used with a theoretical resolution of $360°/2^{12} = 0.088°$. The 0.1-dB gain offset detection is determined by the linearity of the calibration block. The linearity and AM-PM characteristics of the calibration block have been checked. The simulated IP1dB is −30 dBm; the simulated AM-PM is shown in Fig. 24. In order to detect phase and gain in the linear region, the calibration block uses an input power of −45 dBm, which is 15-dB back off from IP1dB. The phase change along the input power change is less than 0.05 °/dB. In the calibration block, the −45-dBm input signal is amplified to −5 dBm for the ADC differential input. The −5-dBm ADC input signal has a peak-to-peak voltage of $V_{\mathrm{pp}} = 355$ mV. Considering 0.1-dB calibration resolution, the 0.1-dB voltage offset at −5 dBm is 4.1 mV. A 9-bit ADC (LSB = 4 mV) is required, and for design margin, a 10-bit 61.44 MS/s successive approximation (SAR) ADC is used.

As shown in Fig. 25, the SNR of the calibration block quantization signal is calculated based on TRX characteristics. Fig. 26 shows the calculated link budget. At −28-dBm TX input power, the output power from RX is −45 dBm, which is also the calibration block input signal. The SNR of the −45-dBm calibration block input signal is 57 dB; it corresponds to ENOB = 9.2 bit and satisfies the gain calibration resolution.

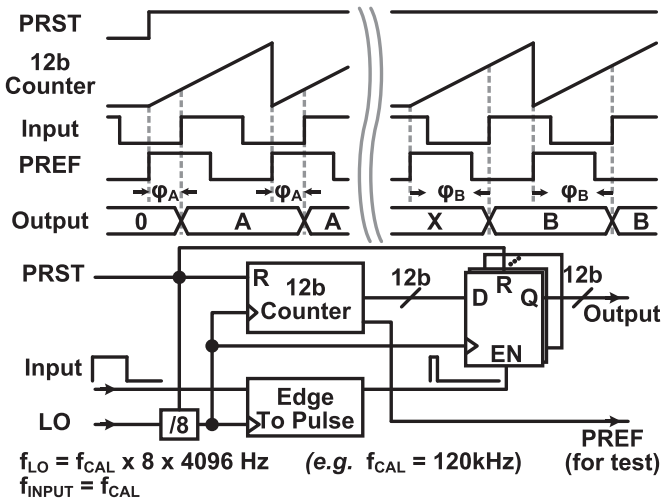


Fig. 27. Proposed PDC circuit schematic and timing diagram.

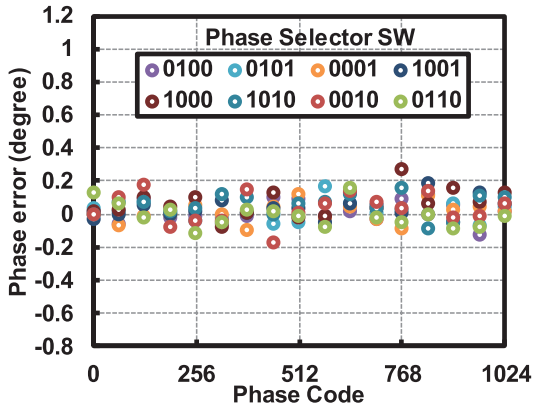


Fig. 28. Measurement results of PDC quantization error over 360° phase-shifting range.

Fig. 27 shows the PDC detailed circuit schematic and timing diagram. In Fig. 27, PRST denotes the PDC reset control signal, INPUT denotes the PDC input signal from limiting amplifier, and PREF denotes the PDC 120-kHz reference clock. The PDC is turned on when PRST is set high; the 12-bit counter keeps counting from 0° to 360°. The PDC input signal is reshaped to a pulse, which samples the instant phase in the 12-bit counter as the digital output of the PDC. The proposed on-chip phase quantization technique achieves a very high resolution at the millimeter-wave frequency, and it is tens of times improved compared with the analog solution in [51].

Fig. 28 shows the measurement results of the PDC quantization error over 360° phase-shifting range. In order to measure the PDC quantization error correctly, the reference phase is first required. As shown in Fig. 23, PREF is a reserved output of the 120-kHz square-wave reference clock; LA OUT is a reserved output of 120-kHz square-wave signal with actual phase information. The LA OUT phase can be measured in an external oscilloscope by comparing it with PREF. The quantization error is defined as the difference between the PDC readout and the external oscilloscope. The measured rms phase quantization error between PDC readout value and external oscilloscope readout value is 0.08°.

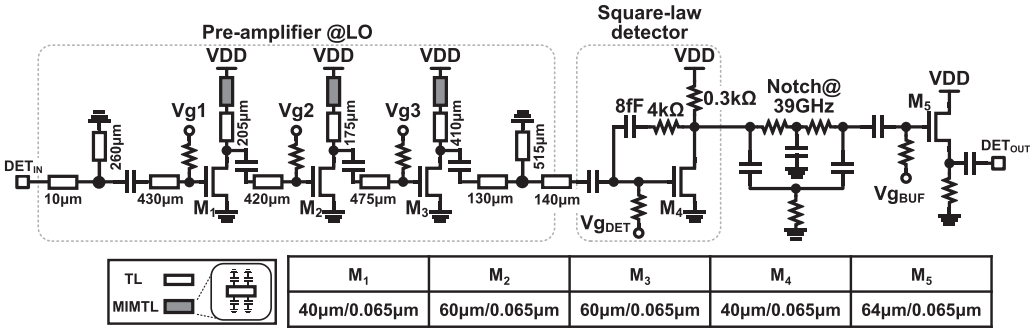
The LOFT calibration employs an additional square-law detector circuit other than the abovementioned calibration block. To improve the LOFT detection sensitivity, a pre-amplifier optimized at the LO frequency is placed before the square-law detector. Fig. 29 shows the detailed circuit schematic of the LOFT detector with a three-stage pre-amplifier. The square-law detector bias is optimized with maximum second-order harmonic output. The LOFT calibration uses the two-tone signal containing 35.1-GHz LO and 39-GHz RF. Since the 35.1-GHz LO can be canceled much lower than the 39-GHz RF signal, an *RC*-based RF notch filter at 39 GHz is inserted between the detector and the output buffer.

IV. Transceiver Measurement Results

The 39-GHz four-element phased-array transceiver is fabricated in standard 65-nm CMOS technology.

The fabricated chip micrograph is shown in Fig. 30; the transceiver occupies a chip area of 3 mm × 4 mm. The four sub-array TRX elements are placed symmetrically; each TRX contains an LO phase-shifting chain and an RF front end. The RF coupling network is connected to the center of the chip for calibration. The IF and LO signal paths are distributed to each TRXs from the chip center. The LOFT square-law detector and the calibration block are located at the lower and upper sides of the center distribution network. The external 3.9-GHz LO input and the ×9 multiplier are on the right-hand side of the chip, while the SPI control is located on the left-hand side.

A four-chip 16-element transceiver unit PCB module is fabricated for characterization and data communication. A 64-element transceiver can be realized by extending with four-unit PCB modules. The PCB layer stack up is shown in Fig. 31; it consists of six substrate layers using low-relative-permittivity Megtron-6 material and seven metal layers for signal, ground, and antenna. The chip is flip-chip mounted using Au bumping technology in the PCB front side; the RF IOs are connected to backside antenna through vias. Fig. 32 shows the fabricated PCB module with mounted chips. For massive production and flexible antenna scale, the PCB module has a periodic layout with a fixed antenna distance. The chip control and digital IOs are on the top of PCB; the VDD supplies are from both the upper and lower sides of the chips. The LO and IF ports employ the compact and easy-integration U.FL connectors for signal feeding at 3.9 GHz. The PCB back side shows the antenna array; in this work, there are 16 chips and 64 patch-antenna elements are implemented. To eliminate the element mismatch, dummy antennas are also placed near the border of the array with the same element distance. The patch antenna is designed in an electromagnetic (EM) simulator, including PCB layers and excitation. Fig. 33(a) shows the 39-GHz circular patch antenna structure; the single-element antenna has a diameter of 2.25 mm. The patch antenna employs the type of coaxial probe feed technique since it is easy to fabricate and has low spurious radiation. The antenna element-to-element distance is 4.5 mm. Fig. 33(b) shows the simulated input reflection



M_1	M_2	M_3	M_4	M_5
40μm/0.065μm	60μm/0.065μm	60μm/0.065μm	40μm/0.065μm	64μm/0.065μm

Fig. 29. Detailed circuit schematic of LOFT square-law detector with a three-stage pre-amplifier.

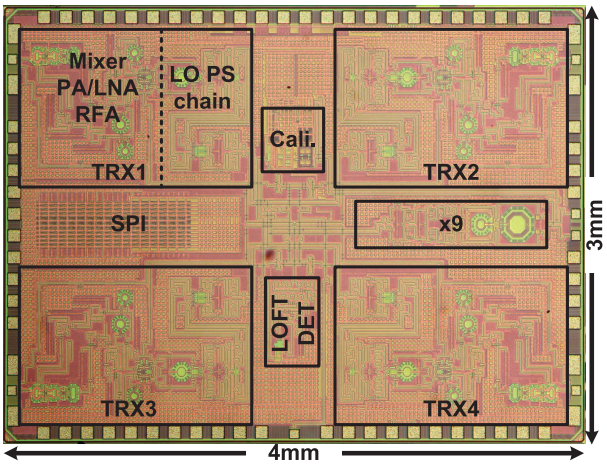


Fig. 30. Chip micrograph.

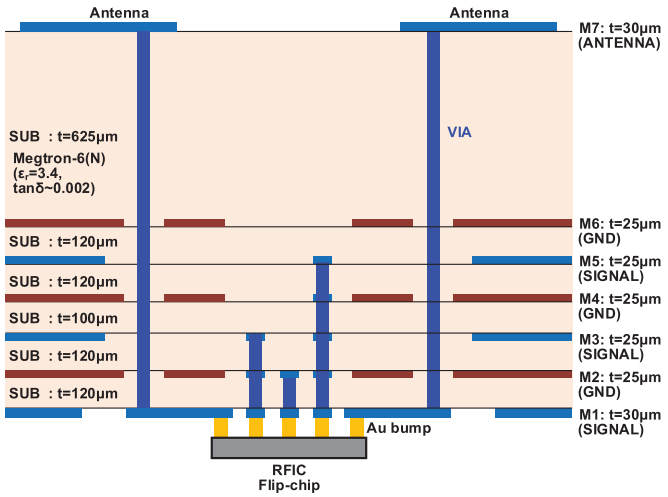


Fig. 31. Flip-chip packaging with seven-layer PCB stack up.

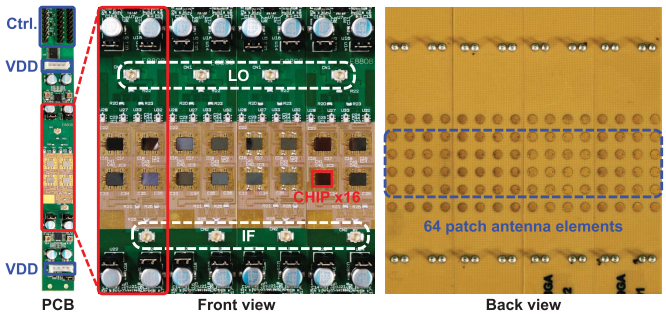


Fig. 32. Implemented PCB with patch antenna on the back side.

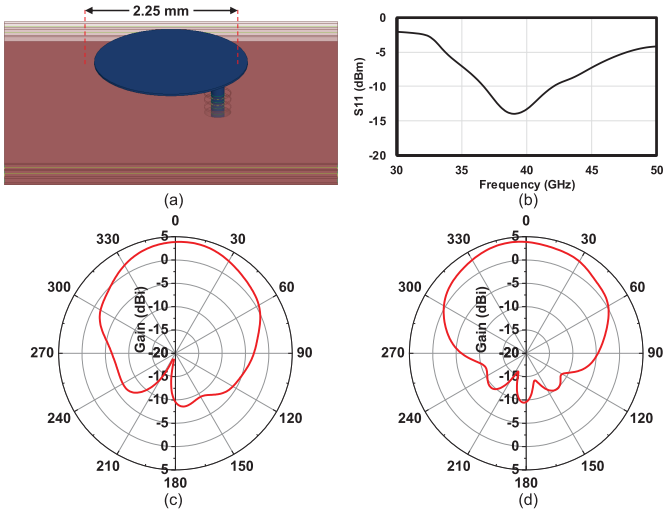


Fig. 33. (a) Structure of 39-GHz patch antenna. (b) Simulated S_{11}. (c) Simulated E-plane radiation pattern. (d) Simulated H-plane radiation pattern.

coefficient (S_{11}), terminated using 50-Ω impedance load; the antenna has a 4.4-GHz bandwidth from 36.7 to 41.4 GHz with S_{11} below −10 dB. The patch antenna achieves a maximum realized gain of 3.9 dBi; Fig. 33(c) and (d) shows the simulated radiation pattern in the E-plane and H-plane.

The phased-array transceiver chip single-channel TX/RX characteristics are first measured with an on-wafer probing setup. The transceiver conversion gain, linearity, and noise figure are measured by Keysight N5247A PNA-X with a fixed LO frequency at 3.9 GHz. Fig. 34(a) shows the single-channel TX-mode up-conversion gain; the converted image signal is measured as well. The single-channel TX achieves a conversion gain of 7 dB at 39 GHz and an image suppression of 50 dBc at 31 GHz. Fig. 34(b) shows the single-channel TX linearity measurement at 39 GHz, the measured output P_{1dB} is 9.0 dBm, and the third-order output intercept point (OIP3)

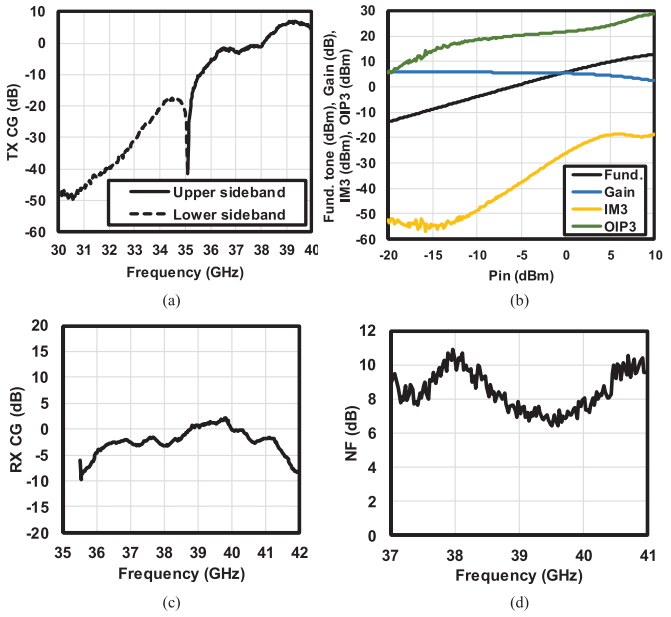


Fig. 34. Measured single-channel TX/RX characteristics at fixed f_{LO} = 3.9 GHz. (a) TX conversion gain. (b) TX linearity performance. (c) RX conversion gain. (d) RX noise figure.

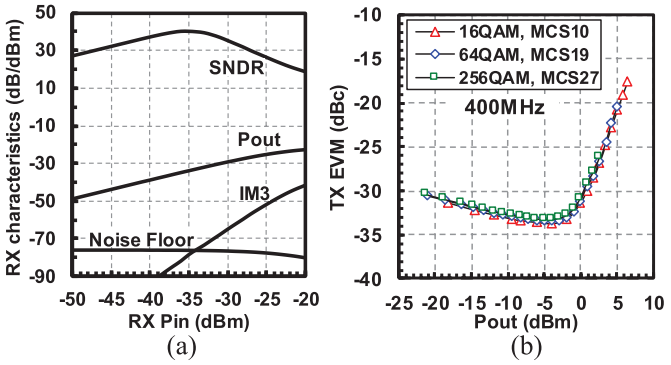


Fig. 35. Measured single-channel (a) RX SNDR and (b) TX EVM.

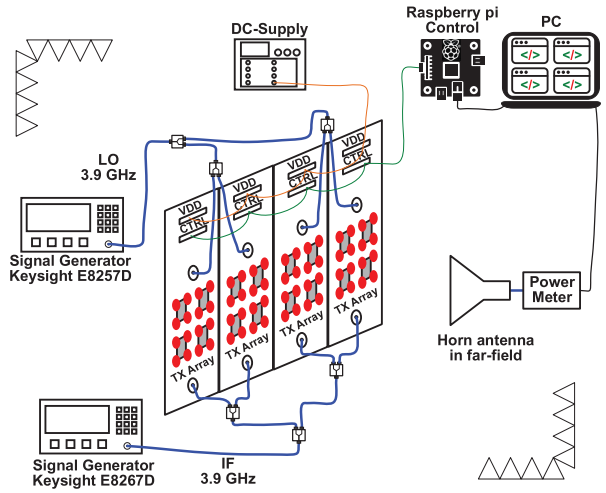


Fig. 36. Radiation pattern and EIRP measurement setup.

is 20 dBm. The measured TX OIP3 is 3.5 dB lower than the standalone PA due to the limited drive ability of DA. The single-channel RX has a measured peak conversion gain of 3 dB and a 6-dB gain flatness from 37 to 40 GHz,

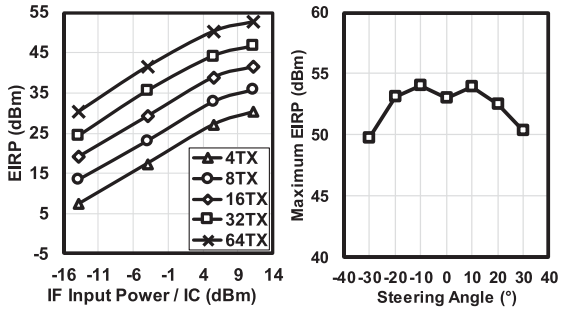


Fig. 37. Measured EIRP against array scale and steering angle.

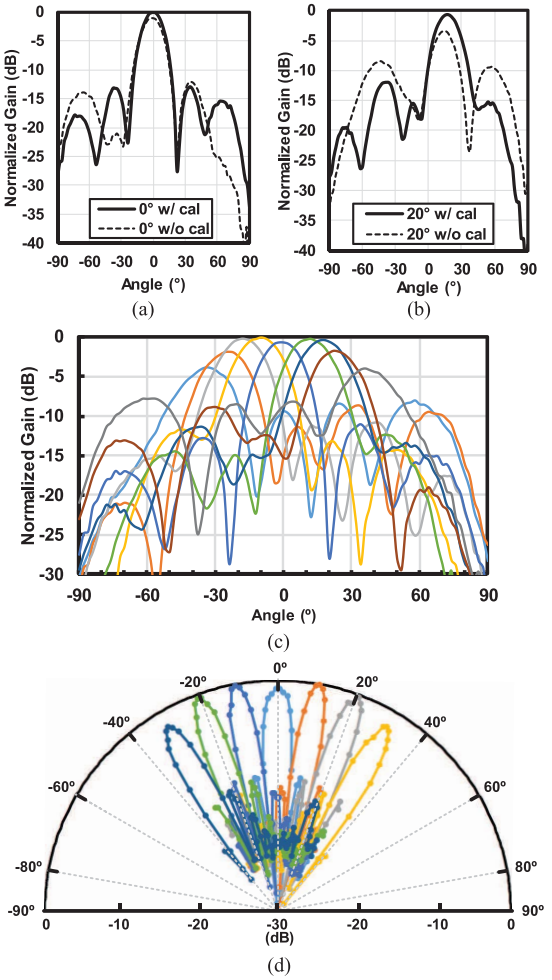


Fig. 38. Measured radiation patterns. (a) 4 × 1 antenna element at 0°. (b) 4 × 1 antenna element at 20°. (c) 4 × 1 antenna element with steering angle in ±40°. (d) 16 × 1 antenna element with steering angle in ±30°.

as shown in Fig. 34(c). The measured RX noise figure is shown in Fig. 34(d). Fig. 35(a) shows the measured single-channel RX linearity; the RX achieves a third-order input intercept point (IIP3) of −12 dBm. The RX signal-to-noise and distortion ratio (SNDR) can be calculated from the measured RX gain, intermodulation distortion (IM3), and noise figure, Fig. 35(a) shows that the RX achieves a peak SNDR of 40 dB at −35-dBm input power with a 400-MHz signal bandwidth. The single-channel TX is evaluated using 5G NR 400-MHz

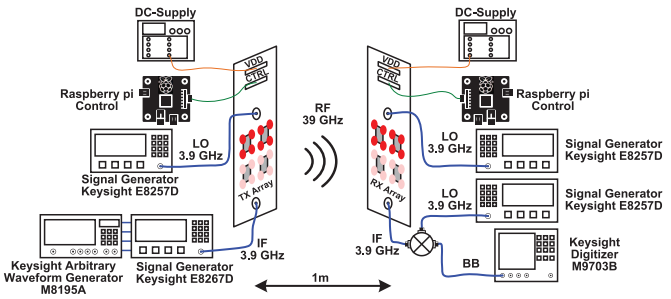


Fig. 39. Measurement setup for 1-m OTA link.

TABLE I
POWER CONSUMPTION OF BLOCKS

Power breakdown / IC With 1-V DC supply	
Blocks	P_{DC} (W)
TX PA	0.65
TX RFA+DA	0.39
RX LNA+RFA	0.13
X9 Multiplier	0.14
Phase Shifter	0.24
Cal. Blocks	0.03
LOFT Det.	0.05
SPI	0.01

bandwidth OFDMA MCS10/19/27 (16, 64, and 256 QAM) modulated signal. As shown in Fig. 35(b), the TX achieves a peak EVM in 64 QAM of −33.2 dB and an average output power of 3.6 dBm at −24.6-dB EVM while transmitting 64-QAM modulation signal.

The large-array transmitter radiation performance is characterized using 64-element transceiver module shown in Fig. 32. The radiation measurement setup is shown in Fig. 36; two 25-dBm maximum P_{OUT} signal generators (Keysight E8267D) are used for the LO input and IF input. The LO and IF are distributed to each board through power dividers. The transceiver arrays are controlled through a Raspberry Pi. A far-field horn antenna with the same linear polarization plane receives radiated 39-GHz RF signal and measured using a power meter. Fig. 37(a) shows the measured EIRP against input power at 0° steering angle with increasing TX elements. For the largest antenna scale in our case, the 64-element TX achieves a maximum EIRP of 53 dBm. The 64-element TX maximum EIRP at steering angle of ±30° is measured, as shown in Fig. 37(b). The phased-array transmitter beam patterns in the azimuth plane are measured employing 4×1 elements and 16×1 elements. For 4×1 elements, the normalized radiation patterns with and without calibration at 0° and 20° beamsteering angles are shown in Fig. 38(a) and (b). The initial errors in Fig. 38(a) and (b) result from the different initial phase and gain characteristics of each sub-array TXs as well as the antenna mismatches. The one-time chip-to-chip calibration is accomplished by using the setup shown in Fig. 36. The TXs are turned on alternatively with their output power calibrated using a horn antenna in far-field. After setting the TXs with the same output power level, a pair of TXs are turned on simultaneously. One TX is set as 0° phase reference and sweeping another TX phase to find the minimum received power. The minimum receiving power corresponded phase value has a 180° phase difference with the reference. The automatic angle steering and amplitude tuning are realized by a built-in calibration block. A similar offline calibration can be done as in [52] by establishing an OTA link between TX and RX instead of an on-chip coupling network. It can be seen at 20° angle, the main lobe strength is improved by 3 dB after calibration, and the sidelobe is suppressed by more than 5 dB. After calibration, the 4×1 elements' radiation pattern with beamsteering angle in ± 40° is demonstrated in Fig. 38(c). For achieving high antenna gain and beam directivity, the 16×1 elements' radiation pattern with ±30° steering angle is measured and shown in Fig. 38(d). The measured radiation pattern shows that the proposed transceiver has accurate directivity and enhanced beamforming quality.

The phased-array transceiver is also evaluated using 5G NR modulated signal. Fig. 39 shows the measurement setup for establishing the OTA link. Due to the limitation of the linear output power range of SG with vector modulation, the OTA link distance is set to 1 m, and each TX module and RX module employs eight (4×2) antenna elements. The 5G NR OFDMA modulated signals in QPSK, 16 QAM, 64 QAM, and 265 QAM are tested with modulation and coding scheme 4 (MCS4), MCS10, MCS19, and MCS27, respectively. The 5G NR IQ baseband signal is generated by an arbitrary waveform generator (AWG) (Keysight E8195A); the IQ baseband is then up-converted to 3.9-GHz IF by a signal generator (Keysight E8267D) with vector modulation. The RX-received 3.9-GHz IF signal is down-converted to baseband and demodulated using a digitizer (Keysight M9703B). Both TX and RX are controlled through Raspberry Pi with the same master PC. Fig. 40 summarizes the measured OTA constellation, spectrum, and EVM performance. The measurement results show that the proposed transceiver supports a 400-MHz 256-QAM 5G NR modulation signal with a TX-to-RX error vector magnitude (EVM) of −30.0 dB, which is capable of the requirement for less than 10^{-3} bit error rate [32]. The minimum TX-to-RX EVM of −30.7 dB is measured in QPSK modulation. The measured TX-to-RX EVMs at 20° and 40° beam direction with 64-QAM modulation are −30.1 and −28.6 dB, respectively.

In addition, LOFT calibration and image suppression are also measured and presented in Fig. 41. After automatic LOFT calibration, the LOFT signal is canceled to less than −70 dBm, which is 33 dB lower than before calibration. Due to the two stages of image notch filters in TX, the image is suppressed by 50 dBc compared with the 39-GHz RF signal, which matches the TX CG measurement result using PNA-X shown in Fig. 34(a).

The transceiver consumes a dc power of 1.5 W/chip in the TX mode and 0.5 W/chip in the RX mode both from a 1-V supply. The detailed power consumption breakdown is shown in Table I. For achieving high emission performance at 39 GHz, this transceiver consumes more power than prior arts working at 28 GHz. The higher loss of the IF

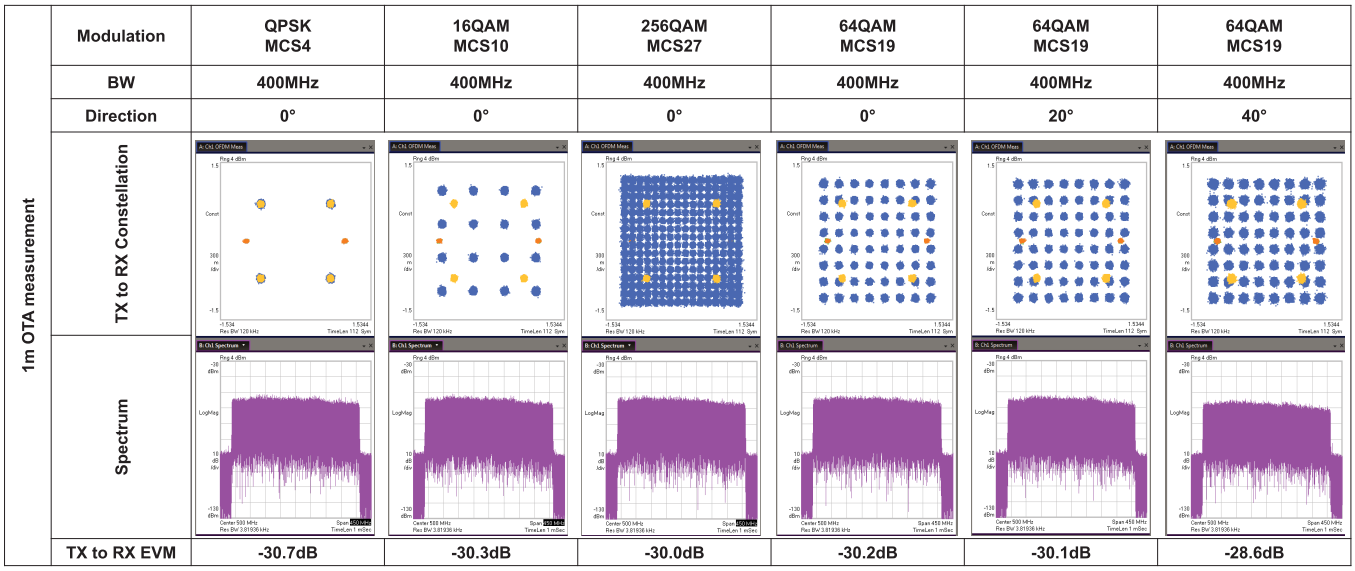


Fig. 40. Measured 1-m OTA constellation, spectrum and EVM performance using eight-TX module and eight-RX module with −7-dBm IF input power per chip.

TABLE II

PERFORMANCE COMPARISON OF mm-WAVE PHASED ARRAY TRANSCEIVERS FOR 5G AND BEYOND

	This work	[30] Qualcomm	[31] Broadcom	[32] TokyoTech	[21] UCSD	[25] IBM	[33] TokyoTech	[34] Intel
Frequency (GHz)	39 (n260)	28 (n257)	60	28	29	28	28 (n257)	39
Process	65nm CMOS	28nm CMOS LP	28/40nm CMOS	65nm CMOS	180nm SiGe	130nm SiGe	65nm CMOS	28nm CMOS
Architecture	LOPS	RFPS	RFPS	LOPS	RFPS	RFPS	RFPS	RFPS
Element/Chip	4 TRX	4 TRX	24 TRX	4 TRX	4 TRX	32 TRX	8 TRX	8 TRX
Array size	64	24	288	8	32	128	64	16
Polarization	Single	Dual	Single	Single	Single	Dual	Dual	Dual
PS resolution	3+10 bit / 0.05°	3 bit -	6bit / 6°	2+3+10 / 0.04°	6 bit / 5.6°	1+5 bit / 5°	5+10 bit -	5 bit -
TX Psat / path (dBm)	15.5	14	6.5	18**	12.5	16.4	15.1	-
TX P_{1dB} / path (dBm)	9.0	12	0	15.7**	10.5	13.5	11.3	11
RX NF / path (dB)	7.7	4.4	7	4.1**	4.6	3.7	4.2	6
RX IP1dB (dBm)	-22	-	-	-	-22	-22.5	-	-36
$EIRP_{MAX}$ (dBm)	53	35 (8TX)	51	39.8	45	57	45.6	-
Power dissipation (W)	1.5 / 4TX 0.5 / 4RX	0.36 / 4TX 0.17 / 4RX	8.4 / 144TX 6.6 / 144RX	1.2 / 4TX 0.6 / 4RX	0.8 / 4TX 0.5 / 4RX	4.6 / 16TX 3.3 / 16RX	2.0 / 8TX 0.9 / 8RX	0.34 / 1TX 0.08 / 1RX
Calibration	phase, amp., LOFT	-	amp., IQ LOFT	-	-	-	phase, amp.,	-
Phase shifter RMS gain variation (dB)	0.01	-	1.5 (Max.)	0.03	0.8 (Max.)	1.5 (Max.)	0.2	2 (Max.)
RMS phase error (°)	0.08	-	-	0.28	6	1	0.4	-
TX LOFT (dBm)	< -70	-	-	-	-	-	-	-
OTA Distance (m)	1	-	-	5	5	-	1	-
OTA Array Elem.	8TX 8RX	-	-	8TX 8RX	32TX 32RX	-	16TX 16RX	-
OTA Link BW	400 MHz	100 MHz	1760 MHz	800 MS/s	500 MHz	-	400MHz	-
OTA TX to RX EVM (dB)	-30.2 64QAM	-41 (TX) 64QAM	-24 (TX) 16QAM	-35 64QAM	-27 64QAM	-	-34.6 64QAM	-
Chip area (mm^2)	12	28	22	12	12	166	12	17.2
5G NR evaluated	Yes	Yes	-	-	-	-	Yes	-

*estimated from figure ** w/o TRX switch

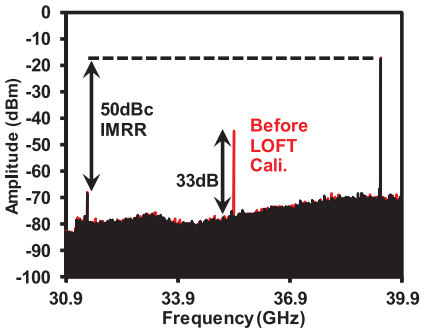


Fig. 41. Measurement results of LOFT cancellation and image suppression.

distribution network also causes additional power consumption for more gain stages. The performance comparison of millimeter-wave phased-array transceivers for 5G and beyond is listed in Table II. This article demonstrates a 39-GHz phased-array transceiver with built-in phase, gain, and LOFT calibration, which can ease the deployment of the large array. The on-chip phase and amplitude calibrations' rms error are 0.08° and 0.01 dB, respectively. A 1-m OTA link is established with −30.2-dB EVM using 5G NR 400-MHz bandwidth MCS19 64-QAM modulation signal. EIRP_{MAX} of 53 dBm is achieved, the LOFT is auto-calibrated to −70 dBm, and the image signal is suppressed by 50 dBc.

V. Conclusion

This article first presents a CMOS 39-GHz four-element phased-array transceiver for 5G NR with built-in phase–amplitude and LOFT calibration. Due to the LO phase-shifting architecture, the maximum gain variation while phase tuning is less than 0.04 dB. To achieve high-resolution and highly accurate phase detection, a 14-bit PDC is proposed with quantization resolution less than 0.1° and quantization rms error of 0.08°. The LOFT calibration and image notch filter are integrated; the LOFT and image signal are −70 dBm and 50 dBc suppressed, respectively. A 64-element transceiver module is implemented, and the measured maximum EIRP achieves 53 dBm. The 8TX–8RX 1-m OTA measurement shows that the transceiver supports 5G NR 400-MHz 256-QAM OFDMA modulation with −30-dB EVM.

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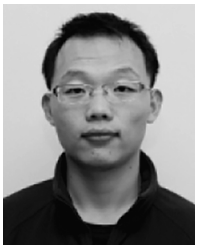

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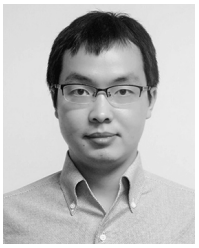

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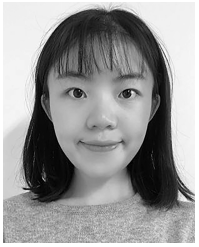

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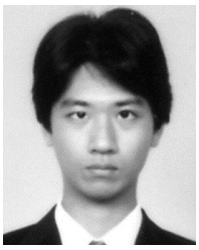

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