An Event-Driven Quasi-Level-Crossing Delta Modulator Based on Residue Quantization

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***Abstract*— This article introduces a digitally intensive event-driven quasi-level-crossing (quasi-LC) delta-modulator analog-to-digital converter (ADC) with adaptive resolution (AR) for Internet of Things (IoT) wireless networks, in which minimizing the average sampling rate for sparse input signals can significantly reduce the power consumed in data transmission, processing, and storage. The proposed AR quasi-LC delta modulator quantizes the residue voltage signal with a 4-bit asynchronous successive-approximation-register (SAR) sub-ADC, which enables a straightforward implementation of LC and AR algorithms in the digital domain. The proposed modulator achieves data compression by means of a globally signal-dependent average sampling rate and achieves AR through a digital multi-level comparison window that overcomes the tradeoff between the dynamic range and the input bandwidth in the conventional LC ADCs. Engaging the AR algorithm reduces the average sampling rate by a factor of 3 at the edge of the modulator's signal bandwidth. The proposed modulator is fabricated in 28-nm CMOS and achieves a peak SNDR of 53 dB over a signal bandwidth of 1.42 MHz while consuming 205 μW and an active area of 0.0126 mm^2.**

***Index Terms*— Adaptive resolution (AR), analog-to-digital converter (ADC), asynchronous successive-approximation-register (SAR) ADC, compressed sensing, event-based signal processing, Internet of Things (IoT), level crossing (LC).**

I. Introduction

WIRELESS sensor devices underpin the broad ecosystem of the Internet of Things (IoT), in which the RF transmitter (TX) and digital signal processor (DSP) dominate the power consumption budget. By adopting the nanoscale CMOS technology, wireless sensor nodes in the large-scale sensor array can achieve inexpensive integration with excellent digital power efficiency. Considering the relatively slow development in the energy storage technology and the need for extending the stand-by time of battery-powered wireless sensor nodes, the high power efficiency needs to be emphasized and pursued at the analog front-end, analog-to-digital converter (ADC), RF TX, and DSP levels. An emergent way of improving the system power efficiency is to adaptively reduce the average sampling rate of communicated data, thus reducing the power consumed by the RF TX and DSP for the data transmission and processing, respectively.

The adaptive-Nyquist and adaptive-oversampling ADCs were, respectively, exploited in [1] and [2] for bio-potential signal acquisition, which adopt an adaptive sampling mechanism by adjusting the ADC sampling frequency f_s based on the slew rate of the input signals. However, the adjustment of f_s is between only two frequencies, thus limiting the effectiveness of the average sampling rate reduction. An alternative architecture applies the compressed sensing algorithm to the analog front-end circuitry, and then, the sub-Nyquist-rate ADCs digitize the compressively sampled data [3]. This requires, however, complex hardware in the front end, including a pipelined Nyquist-rate programmable switched-capacitor (sw-cap) multiplying DAC/integrators and the sub-Nyquist-rate ADCs. This also results in a complex and more power-hungry signal recovery at the receiver side.

Level-crossing sampling (LCS) is an attractive alternative to the aforementioned techniques. The input signal there is sampled and converted into the continuous-time (CT) domain only when it crosses specific threshold levels [4]. Therefore, the average sampling rate of LC ADCs is signal-dependent, which is in contrast with uniform sampling ADCs. The delta-modulator-based [5], [6] and the flash-based [7], [8] [respectively, shown in Fig. 1(a) and (b)] are two common LC ADC topologies. Both of them generally use high-performance CT comparators to be the threshold-crossing detectors. It is rather challenging to implement them in deep nanoscale CMOS given the low intrinsic gain of transistors and, more importantly, the propagation delay dispersion that is signal-dependent in most cases, ultimately impairing the ADC linearity. Moreover, a purely CT approach cannot directly interface to the conventional discrete-time (DT) DSPs, demanding the time-domain quantization that would lead to the quantization noise. Otherwise, a custom-designed CT DSP [9] would be needed to process the CT digitized data. To take advantage of the technological scaling, [10] and [11] propose VCO-based topologies so as to avoid the use of high-performance CT comparators. However, the phase of VCO keeps on increasing with time and this causes a continual triggering of level-crossing (LC) events. As a consequence, the approach appears less suitable for compressed sensing applications. Alternative sampling techniques based on LCS have been proposed, such as the

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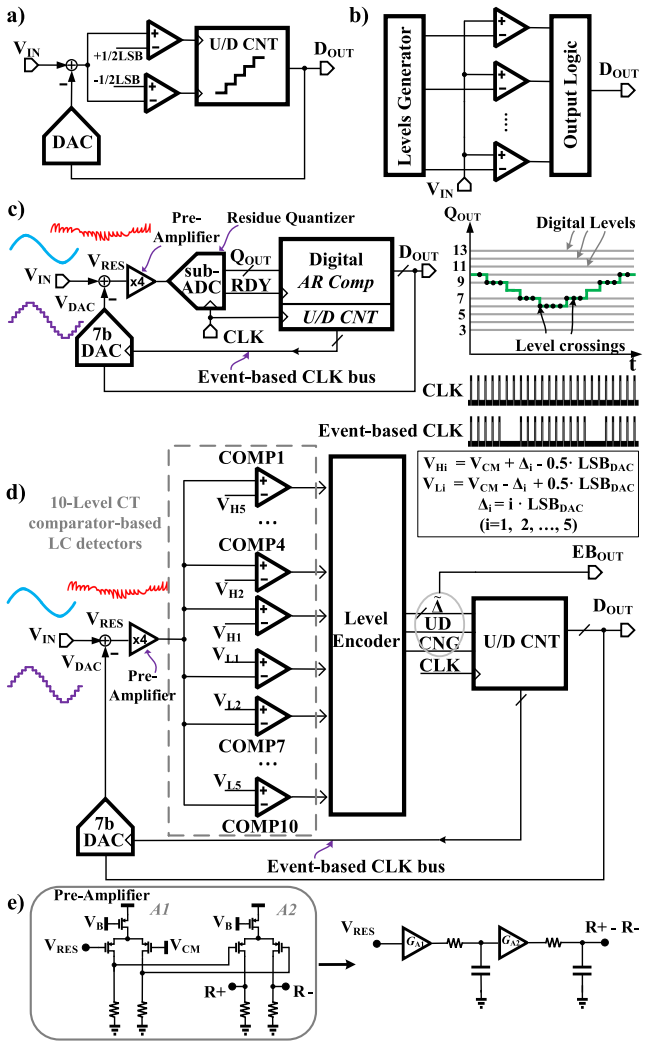

Fig. 1. (a) Conventional delta-modulator-based and (b) flash-based LC ADCs. (c) Proposed LC delta modulator topology and (d) its equivalent circuit with CT analog comparators. (e) Simplified schematic of pre-amplifier and its corresponding linear model.

derivative LCS [12] and the adaptive resolution LCS (AR LCS) [13].

AR LCS can further reduce the average sampling rate of an LC ADC by adaptively tuning the ADC resolution (LSB step) depending on the input signal derivative while avoiding the degradation of its in-band performance [13]. A fast-changing input can be tracked and converted without a slew-rate overload, which means that the signal bandwidth can be extended by the AR technique. The delta-modulator-based architecture in [5] implements the AR algorithm with a time-varying comparison window that is reduced gradually (from 7 to 1 LSB) using control signals generated by delay cells and two DACs that can generate the variable comparison intervals. However, all of them lead to a significant hardware overhead. A method in [6] attempts to verify the AR algorithm in an field-programmable gate array (FPGA). However, it uses a 16-bit counter in the FPGA operating at a frequency with an OSR of 500, which is not a practical solution for an IoT node.

In this article, which is an extension of [14], we propose an AR delta modulator that quantizes its voltage residue V_{RES} by means of a low-resolution sub-ADC (hereafter also referred to as "residue quantizer"). This allows a straightforward implementation of LC and AR algorithms in the digital domain, which can be realized as readily synthesizable logic. Differently from conventional LC ADCs, the proposed delta modulator exploits the LC algorithm in the sampled digital domain, which is the reason for adopting the "quasi-LC" terminology. The developing trend for highly integrated wireless sensor devices is to implement the analog front-end, RF TX, and DSPs in the nanoscale CMOS technologies [15], [16]. The proposed quasi-LC delta modulator is in line with this aim and enables a simple implementation of the compressed sensing. Section II introduces the proposed topology, compares it to conventional LC ADCs, and presents system-level analysis, AR algorithm implementation, and dynamic range (DR). Section III discusses the circuit implementation. Section IV discloses the measurement results, and Section V concludes this article.

II. Proposed Residue-Quantizing Delta Modulator

The proposed AR delta modulator is shown in Fig. 1(c). The modulator consists of an analog part, which comprises the 7-bit sw-cap feedback DAC, subtractor (here, event-based sampled DT, but generally it could be CT), pre-amplifier, and the 4-bit residue quantizer; and a digital part, comprising synthesized logic and a custom digital section. After the subtraction node, the pre-amplifier, which consists of two cascaded low-gain amplifiers [shown in Fig. 1(e)], is used to amplify the residue V_{RES} signal by $4\times$ to compensate for the gain loss of the passive subtractor and to drive the 4-bit residue quantizer. The synthesized logic serves the purpose of multi-threshold comparison (thus, the name AR Comp) of the quantized residue signal, moreover exploiting the LC and AR algorithms and performing up/down counting (U/D CNT) to generate the binary digital control for the sw-cap feedback DAC. The sw-cap feedback DAC and subtractor are triggered by an event-based CLK bus, generated by gating off the system CLK with the LC events generated in the AR Comp. The AR Comp compares the digitized V_{RES} with multiple digital threshold levels (i.e., 10 in the proposed work). When the residue voltage V_{RES} is within the range of $V_{\mathrm{CM}} \pm \mathrm{LSB}_{\mathrm{DAC}}/4$, where V_{CM} is the common-mode voltage of the subtractor and $\mathrm{LSB}_{\mathrm{DAC}}$ is the LSB of the sw-cap DAC, the output of the residue quantizer Q_{OUT} stays at 8, and no level crossings are detected by the AR Comp. When V_{RES} exceeds this range, it indicates that one among the ten digital levels (3, 4, ... 7 and 9, 10, ... 13) is crossed. This will trigger the event and will enable the event-based CLK bus.

Unlike in the conventional LC delta modulator, the proposed modulator digitizes the delta-modulator residue V_{RES} using a low-resolution sub-ADC, thus enabling the AR-LC algorithm to be carried out in the digital domain. Therefore, the realization of AR is nearly costless in terms of hardware resources. The equivalent topology of the proposed modulator using CT comparators is shown in Fig. 1(d). It exploits ten high-performance CT comparators to compare

V_{RES} versus ten different threshold levels (i.e., resembling the operation of a ten-level LC flash ADC), thus performing AR LC detection without the need of a slope detector. The subsequent CT digital circuitry [marked as level encoder in Fig. 1(d)] controls the U/D counter based on the highest (or lowest) level that is crossed. In contrast, the proposed modulator completely avoids multiple high-performance CT comparators and multi-level reference voltages by instead adopting a successive-approximation-register (SAR) sub-ADC, which digitizes the V_{RES} signal, and by then performing the multi-threshold comparison in the digital domain.

A. Comparison to Conventional LC ADCs

The conventional LC ADCs shown in Fig. 1(a) and (b) are generally clockless, with the following digital block triggered by events from the CT comparators. The well-known advantages of conventional LC ADCs are being fast in terms of output updates to respond to input changes, input-dependent output bit rate and dynamic power consumption, a lower in-band quantization error, and ideally an aliasing-free nature [17].

The first two of these advantages are due to their inherent input-dependent oversampling behavior. Indeed, in the example of a sinusoidal signal converted at a fixed resolution, the oversampling ratio of a CT LC ADC can be expressed as

$$\mathrm{OSR}_{\mathrm{CT-LC}} = \frac{f_{\mathrm{out}}}{2 \cdot f_{\mathrm{in}}} = \frac{A_{\mathrm{in,pp}}}{\mathrm{FS}} \cdot N_{\mathrm{level}} \tag{1}$$

where f_{out} is the average sampling rate, f_{in} is the frequency of the sinusoidal input, $A_{\mathrm{in,pp}}$ is the input peak-to-peak amplitude, FS is the ADC full-scale range, and N_{level} is the number of quantization levels of the LC ADC, corresponding to 2^N for a delta modulator with an N-bit feedback DAC, and to the number of comparators for the flash topology. For the proposed quasi-LC delta modulator, it is worth observing that from a black-box perspective, it resembles the operation of a conventional CT LC ADC as it also oversamples the input signals with an input-dependent oversampling ratio, thus responding to input changes almost immediately, achieving signal-dependent output bit rate and dynamic power consumption.

In terms of in-band error, the proposed modulator has different dominant contributors compared to the conventional LC ADCs, whose main sources of inaccuracy are amplitude and timing errors. The amplitude errors arise from the uncertainty in the position of the threshold levels due to mismatches in reference generator and to the offset of CT comparators, while the timing errors arise from the finite time resolution of the time quantizer [18]. Neglecting the amplitude errors, which can be calibrated, the SNR of a conventional CT LC ADC can be expressed as a function of time quantization as in [19]

$$\mathrm{SNR}_{\Delta t,\mathrm{dB}} = 20\log_{10}(R) - 14.2 \tag{2}$$

where R is the timing resolution ratio, defined as $(f_{\mathrm{in}} \cdot \Delta t_e)^{-1}$, in which f_{in} is the input signal frequency and Δt_e is the absolute timing error, represented by the loop delay variation (Δt_L) in the delta-modulator topology. Such an error is mainly due to the propagation delay dispersion of the CT comparators that are sensitive to the input voltage derivative, and thus, it ultimately represents the main nonlinearity impairment of CT LC ADCs. The proposed modulator exploits an alternative method of performing LC sampling, which is reasonably insensitive to the effects of absolute timing errors, here represented by the absolute time jitter of the sub-ADC clock, which is reasonably lower than Δt_L and furthermore not signal-dependent. Differently from conventional CT LC ADCs, the amplitude quantization noise from the residue quantizer does contribute to the quasi-LC delta modulator SNR (i.e., noise floor). However, such contribution is mitigated by the oversampling in the sub-ADC, and hence, the proposed modulator can also achieve a lower in-band error.

In terms of aliasing, unlike the conventional LC ADCs that are clockless and alias-free, the proposed quasi-LC modulator locally performs the uniform sampling of the amplified V_{RES} right at the sub-ADC. Similar to uniform sampling ADCs, if large interferers are expected at the input signal, then the use of an input anti-aliasing pre-filter in front of the modulator might be unavoidable. Due to the heavy oversampling in the sub-ADC, however, the specifications of such pre-filter can be relaxed.

Despite losing the ideal aliasing-free characteristic inherent with the conventional LC ADCs, the proposed modulator introduces two alternative advantages. The first is the digitally intensive nature of the AR-LC algorithm, exploited with the aid of the residue quantization. This relieves the design from the sensitivity to the propagation delay dispersion of comparators and also ensures amenability with nanoscale CMOS technology nodes. The other advantage is the modulator digital output being updated synchronously to the local clock, therefore allowing the proposed quasi-LC delta modulator to directly interface with the DT DSPs.

B. System-Level Analysis

The two cascaded low-gain amplifiers in the pre-amplifier function as a second-order RC low-pass filter (LPF) as shown in Fig. 1(e), whose z-domain transfer function can be expressed as

$$H_{\mathrm{LPF}}(z) = \frac{G_A \cdot (1-p_1) \cdot (1-p_2)}{(1-p_1 z^{-1}) \cdot (1-p_2 z^{-1})} \tag{3}$$

where G_A is the overall dc gain of the pre-amplifier, while p_1 and p_2 are the dominant poles, generated by the two cascaded low-gain amplifiers. By defining α as the ratio between the LSB of the sw-cap DAC ($\mathrm{LSB}_{\mathrm{DAC}}$) and the LSB of the residue-quantizer sub-ADC ($\mathrm{LSB}_{\mathrm{sub\text{-}ADC}}$), nominally unity, the z-domain transfer functions to the system output D_{OUT} of the quantization noise E_Q of the residue quantizer (NTF) and of the input signal V_{IN} (STF) can be expressed as

$$\mathrm{NTF(z)} = \frac{D_{\mathrm{OUT}}}{E_Q} = \frac{1}{1 - z^{-1} + z^{-1} \cdot \alpha \cdot G_S \cdot H_{\mathrm{LPF}}(z)} \tag{4}$$

$$\mathrm{STF}(z) = \frac{D_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{\alpha \cdot G_S \cdot H_{\mathrm{LPF}}(z)}{1 - z^{-1} + z^{-1} \cdot \alpha \cdot G_S \cdot H_{\mathrm{LPF}}(z)} \tag{5}$$

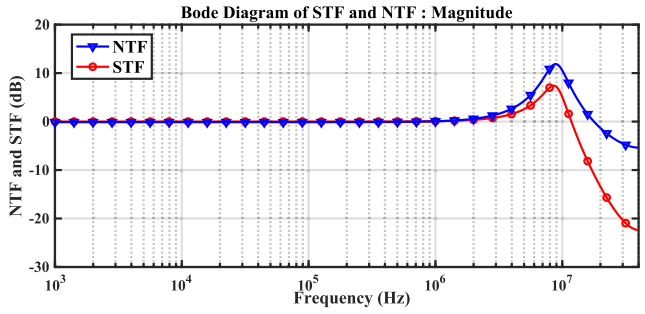

Fig. 2. STF and NTF of the proposed quasi-LC delta modulator.

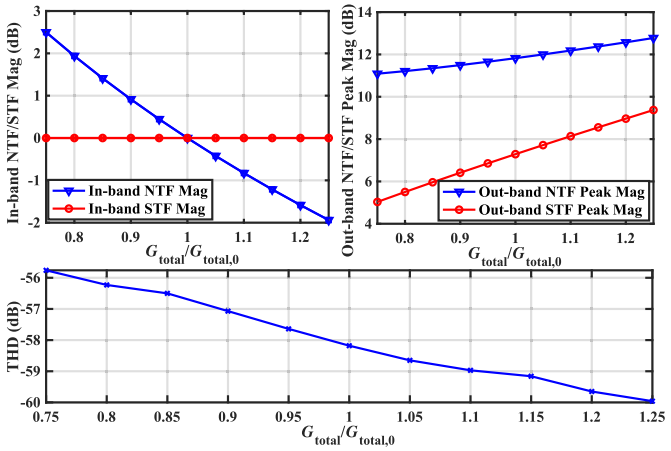

Fig. 3. In-band magnitude (top left) and out-band peaking (top right) of the STF and NTF of the proposed modulator versus the signal path gain variation. THD versus the signal path gain variation (bottom).

where G_S is the gain of the subtractor that immediately precedes the amplifier (equal to (1/4) in this design). Any mismatch between LSB_{DAC} and $\text{LSB}_{\text{sub-ADC}}$ can be treated as a gain error, described by a value of α different than 1. The poles of the LPF are located at a nominal frequency p_0 of 10 MHz, which is considerably higher than the signal bandwidth of 1.42 MHz, and almost an order of magnitude lower than the frequency of CLK (f_{CLK}). The magnitude of NTF and STF versus frequency is shown in Fig. 2, assuming that the gain of the signal path, defined as $G_{\text{total}} = \alpha \cdot G_S \cdot G_A$, is unity. As the in-band NTF is equal to 0 dB, the in-band noise floor of the modulator output spectrum only depends on $\text{LSB}_{\text{sub-ADC}}$ and on the chosen oversampling ratio (given that the in-band quantization noise power from the residue quantizer is inversely proportional to it).

From (4) and (5), it is possible to quantify the effects that variations in the values of G_{total}, p_1, and p_2 have on the magnitude of STF and NTF. The top-left part of Fig. 3 shows that a $\pm 25\%$ variation of G_{total} relative to its nominal value does not impact the in-band STF magnitude, while it causes approximately a ∓ 2.5-dB variation in the in-band quantization noise power. Another parameter of interest in the modulator transfer function plots in Fig. 2 is the magnitude of the peak at around 10 MHz, since the signal harmonics, potential interferers, and the quantization noise around that frequency experience a 5–10-dB amplification (although not impairing the modulator performance, since it is substantially

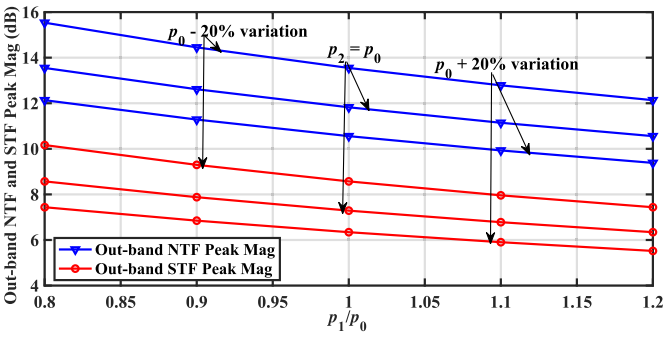

Fig. 4. Out-band peak of STF and NTF of the delta modulator versus one of the LPF pole position variation.

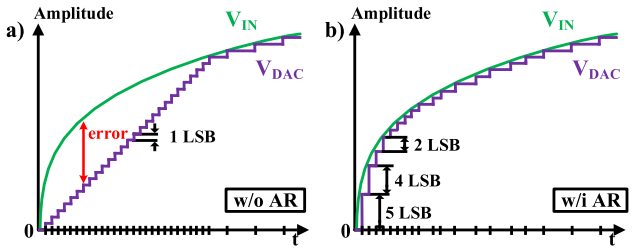

Fig. 5. Example of a logarithmic signal sampled and converted with the proposed modulator, (a) without and (b) with the AR algorithm.

above the signal bandwidth of the modulator). In face of a G_{total} variation of $\pm 25\%$, as shown in the top-right part of Fig. 3, the out-of-band peak magnitude of the STF and NTF will vary by approximately ± 2.5 and ± 1 dB, respectively, without incurring any appreciable phase margin deterioration. This out-of-band peak can also be reduced by pushing p_1 and p_2 to higher frequencies, but this will degrade the low-pass filtering performance. As shown in Fig. 4, a $\pm 20\%$ variation of p_1 and p_2 from the nominal frequency $p_0 = 10$ MHz results in about $-1.5/+2$ and $-1/+1.5$ dB variation in the out-band peak magnitude of the NTF and STF, respectively. In terms of distortion [i.e., total harmonic distortion (THD)], system-level behavioral modeling simulations of the proposed modulator without considering circuit-level non-idealities (e.g., parasitics, mismatches, and leakage) show that the THD degrades gradually when G_{total} decreases, and a 25% decrease of G_{total} relative to its nominal value can lead to a 2.5-dB THD degradation, as shown in the plot at the bottom of Fig. 3. PVT variations also produce uncertainty in the pole frequencies and signal path gain, introducing the need for tunability within the pre-amplifier.

C. AR Algorithm

The AR algorithm accomplishes the purpose of further reducing the average sampling rate so as to lower the power consumed for processing and wirelessly transmitting the data from the IoT node. It is exploited by adjusting the threshold intervals based on the input signal activity (i.e., derivative) without sacrificing the ADC in-band performance [13]. A slowly varying input signal is converted with the finest resolution (Δ_{min}), while a fast varying signal is converted with the coarsest resolution (Δ_{max}), which can be observed from the example shown in Fig. 5(b). For the conventional

LC delta modulators without the AR algorithm, the delay introduced by the loop must be kept shorter than the time needed for a −3-dBFS sinusoidal input (amplitude indicated as $A_{-3\,\mathrm{dB}}$) at the edge of the signal bandwidth (BW) to cross two consecutive threshold levels, whose distance is $\Delta_{\min}$. In other words, the loop must react fast enough to track quick variations of the input signal; otherwise, the signal V_{DAC} would entail a large voltage error during the fast-varying part of the input signal, as shown in Fig. 5(a).

Therefore, a specification on the maximum allowed loop delay $t_{L,\max}$ of an LC delta modulator without the AR algorithm, which therefore has a fixed resolution Δ (equal to $\Delta_{\min}$), can be derived

$$t_{L,\max} = \frac{\Delta}{2\pi \cdot \mathrm{BW} \cdot A_{-3\,\mathrm{dB}}}. \tag{6}$$

Consequently, the signal bandwidth is upper bounded at

$$\mathrm{BW}_{\max} = \frac{\Delta}{2\pi \cdot t_{L,\max} \cdot A_{-3\,\mathrm{dB}}}. \tag{7}$$

The direct proportionality to the LC ADC resolution indicates that by exploiting the AR up to the coarsest value $\Delta_{\max}$, $\mathrm{BW}_{\max}$ and the maximum slew rate that can be tracked can extend by a factor $L = \Delta_{\max}/\Delta_{\min}$ (hereinafter referred to as AR factor).

A way of implementing the AR in a conventional CT LC delta modulator is to adaptively tune, in a time-varying fashion, the comparison interval (i.e., the difference between the upper and lower comparison thresholds of the two comparators that sense the residue voltage, V_H and V_L), based on the input signal derivative [5], [6]. This leads, however, to hardware overhead. Logically, the proposed quasi-LC delta modulator replaces the two comparators of the CT delta modulator, each with time-varying thresholds, with $2L$ comparators each with a fixed threshold, with reference to Fig. 1(d). In the proposed work, the multi-threshold comparison is performed in the digital domain by the AR Comp, implemented as readily synthesizable logic. The highest number $\tilde{\Delta}$[1] of comparison thresholds that are crossed within a certain time window T_{W} determines the magnitude of the shift that D_{OUT} needs to undertake. As a consequence, the residue voltage V_{RES} needs to be first digitized, which is the task of the residue quantizer, the 4-bit SAR sub-ADC. The use of a local clock signal is then unavoidable, and its period sets both the above-mentioned value of T_W and the loop delay t_L, which now becomes fixed and independent of the input signal. It is worth noting that although a uniformly sampled sub-ADC is adopted here for residue quantization, the proposed solution proves to be among the best in class in AR LC ADCs, both in terms of loop delay dispersion and power efficiency. Indeed, for nanoscale CMOS technologies, the use of CT high-performance comparators, which commonly adopt a multi-stage topology to achieve sufficient gain, likely results in a higher static power consumption, which needs to be traded off with the bandwidth and therefore the loop delay dispersion.

[1]The symbol tilde indicates an integer value (or the name of an associated digital bus), and it is used here to differentiate it from Δ, $\Delta_{\max}$, and $\Delta_{\min}$, which are instead analog variables expressed in volt.

As CLK is applied to the residue quantizer, the signal bandwidth of the proposed quasi-LC delta modulator is constrained by the fact that the maximum voltage shift that the feedback DAC is able to provide within T_{CLK} corresponds to the coarsest resolution allowed by the AR scheme, $\Delta_{\max}$. This means that the product $\Delta_{\max} \cdot f_{\mathrm{CLK}}$ represents the maximum absolute value of the signal derivative that the ADC is able to handle without introducing obvious distortion. By considering a −3-dBFS input sinusoidal signal with a frequency equal to BW, the ADC bandwidth can be calculated as

$$\Delta_{\max} \cdot f_{\mathrm{CLK}} = \max\left\{\frac{\delta}{\delta t}[A_{-3\,\mathrm{dB}} \cdot \sin(2\pi \cdot \mathrm{BW} \cdot t)]\right\} \tag{8}$$

and therefore

$$\mathrm{BW} = \frac{\Delta_{\max} \cdot f_{\mathrm{CLK}}}{2\pi \cdot A_{-3\,\mathrm{dB}}} = \frac{L \cdot \Delta_{\min} \cdot f_{\mathrm{CLK}}}{2\pi \cdot A_{-3\,\mathrm{dB}}} \tag{9}$$

where L is set to 5 in this design. Similar to the CT counterparts, as outlined by (7), the AR algorithm enables a bandwidth extension by a factor L compared to a fixed-resolution topology. It is also worth noting that given the minimum resolution, AR factor, input full scale, and clock frequency, the bandwidth of the proposed quasi-LC delta modulator can be calculated rather precisely, which is in contrast to CT LC delta modulators, where the loop delay is instead a nonlinear function of the input signal derivative, and thus not constant.

The impact of AR in terms of ADC accuracy is reasonably negligible since it mainly entails higher harmonic distortion in a frequency range outside the signal bandwidth [13]. In addition, the aforementioned low-pass filtering of the pre-amplifier helps in further attenuating the out-band high-frequency harmonics. It is interesting to observe that larger $\Delta_{\max}$ chosen at the design stage would result in both a wider signal bandwidth and a lower average sampling rate (as discussed in Section IV), but it would in turn demand a pre-amplifier with a faster slew rate and wider output voltage range.

D. Response Speed Comparison With SAR ADCs

In general, the aforementioned signal-dependent oversampling behavior of LC ADCs allows to respond "quickly" to any change in the input voltage that is larger than or equal to the distance Δ between the neighboring levels [17], thus enabling real-time monitoring of the signals to sense. For the conventional CT LC delta modulators, the response time (t_R) can be as short as the minimum loop delay ($t_{L,\min}$), while for the proposed quasi-LC delta modulator, it corresponds to T_{CLK}. For both the former and latter, Δ corresponds instead to the voltage shift at the feedback DAC output, which spans from $1\times$ to $L\times$ of $\mathrm{LSB}_{\mathrm{DAC}}$. In the framework of real-time monitoring sensing applications, a quantitative comparison between the proposed quasi-LC ADC and uniform Nyquist sampling converters (i.e., SAR ADCs, given their state-of-the-art power efficiency) can be carried out under the constraint of identical t_R (in both cases equal to $T_{\mathrm{CLK}} = f_{\mathrm{CLK}}^{-1}$) in response to the same input voltage shift $\Delta_{\max}$ (which is the maximum allowed for the proposed quasi-LC ADC). In such condition, the SAR ADCs would also need to be oversampled, thus dissipating more power, which would furthermore not

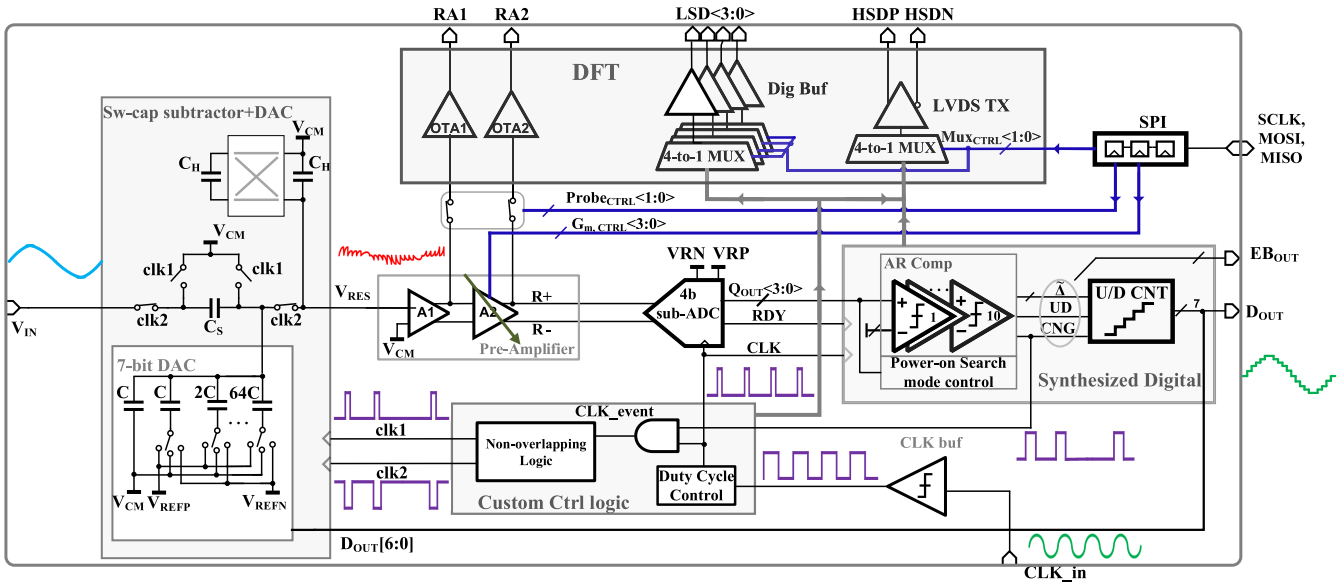

Fig. 6. Block diagram of the proposed AR quasi-LC delta-modulator ADC.

depend on the input signal activity (to the first order) in most cases, except for the design like [20]. In contrast, LC ADCs feature power scalability versus the input signal activity, which is especially beneficial when sensing sparse signals. The OSR of the uniform-sampling ADC counterparts would, therefore, be equal to

$$\mathrm{OSR_{SAR}} = \frac{f_{\mathrm{CLK}}}{2 \cdot \mathrm{BW}} = \frac{\pi \cdot A_{-3\,\mathrm{dB}}}{\Delta_{\max}}. \tag{10}$$

Given that in the proposed quasi-LC ADC, $\Delta_{\max} = 5 \cdot \Delta_{\min}$ and $A_{-3\,\mathrm{dB}} \approx 45 \cdot \Delta_{\min}$ (since the feedback DAC nominal resolution is 7 bits), the equivalent SAR design should have an OSR of ~28. Under the assumption that the SNDR of SAR ADCs is mainly limited by quantization noise, operating with an OSR of 28 (and scaling the BW accordingly) can lead to an increase of 14.5 dB in SNDR. As a consequence, the SAR ADC power efficiency would reduce approximately by a factor ~5.27 ($28/2^{14.5/6.02}$). By considering, for the sake of comparison, only SAR ADCs with similar speed and resolution, such as those presented in [21]–[23], their corresponding power efficiency would degrade, under these circumstances, down to 23.2, 38.5, and 89.6 fJ/c-s, respectively. In addition to this, the proposed estimation does not consider the fact that the following digital block, which would be needed to perform the compressed sensing algorithm on the SAR ADC output, also consumes power. Therefore, for compressed sensing applications, the proposed modulator can be a viable alternative to SAR ADCs. It is furthermore worth observing that for the targeted applications and in virtue of the operating principle of LC ADCs, the widely adopted Walden FoM ($\mathrm{FoM_W}$) does not represent a faithful performance metric, since power scalability and average sampling rate compression, which are the peculiar features of LC ADCs, are not appropriately embedded into its expression.

E. Dynamic Range (DR)

DR of the conventional CT LC delta modulators is upper bounded by the resolution of the feedback DAC (e.g., 8-bit in [5]). In flash LC ADCs, DR depends instead on the ratio between the largest $\Delta_{\max}$ and smallest $\Delta_{\min}$ threshold intervals of the voltage quantizer. If the consecutive threshold levels in the flash-based topology are equally spaced, then the DR is limited by the number of the comparators employed (e.g., 15 in [24]). In the proposed quasi-LC delta modulator, the smallest peak-to-peak signal amplitude ($V_{\mathrm{IN,min}}$), which can be detected, is in the range of $[\Delta_{\min}, \Delta_{\min+1}]$, i.e., between 1 and 2 $\mathrm{LSB_{DAC}}$, depending on the signal common-mode voltage ($V_{\mathrm{IN,CM}}$). Indeed, if $V_{\mathrm{IN,CM}}$ lies right in the middle of two consecutive levels of the feedback DAC ($V_{\mathrm{DAC},i}$ and $V_{\mathrm{DAC},i+1}$), then $V_{\mathrm{IN,min}}$ equals $\Delta_{\min}$, whereas if $V_{\mathrm{IN,CM}}$ is not equally spaced at $V_{\mathrm{DAC},i}$ and $V_{\mathrm{DAC},i+1}$, then $V_{\mathrm{IN,min}}$ increases linearly as the distance between $V_{\mathrm{IN,CM}}$ and one of the two thresholds decreases; therefore, it is upper bounded by $2\Delta_{\min}$. Consequently, similar to the conventional CT LC ADCs, the proposed quasi-LC delta modulator exhibits a 6-dB DR variation, subject to $V_{\mathrm{IN,CM}}$ of input signal. However, even in this regard, AR can be seen as a means of improving the DR of an LC ADC. Indeed, as it can be seen from (9), if the ADC BW and the residue-quantizer clock frequency are fixed, then the DR can be extended (i.e., smaller $\Delta_{\min}$) by increasing the AR factor L. Therefore, the AR scheme helps to overcome the tradeoff between the DR and the signal bandwidth [6].

III. Circuit Implementation

The block diagram of the proposed quasi-LC delta modulator is shown in Fig. 6. The residue quantizer is implemented as a 4-bit asynchronous top-plate-sampling SAR sub-ADC ("4b sub-ADC"). Apart from the feedback DAC's digital control code (D_{OUT}), AR Comp also generates an "event-based" output signal $\mathrm{EB_{OUT}}$ comprising the trigger CNG going high if a level is crossed, signal UD indicating a positive or negative input derivative, and $\tilde{\Delta}$ indicating the magnitude of the shift that D_{OUT} experienced during the CLK period. A custom digital control block (Custom Ctrl logic) is used

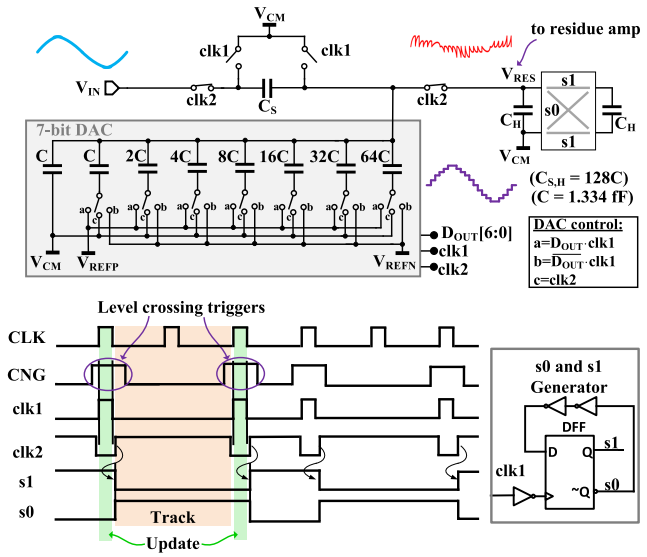

Fig. 7. Binary-weighted 7-bit DAC with sw-cap subtractor (top) and timing of control signals (bottom).

to generate the 12.5% duty cycle clock signal for the residue quantizer (CLK), to gate off CLK with the CNG event trigger from AR Comp, thus generating CLK_event, and to finally produce the non-overlapping replicas of CLK_event (clk1 and clk2) responsible for controlling the sw-cap feedback DAC and subtractor. Design for testability circuitry (marked as DFT in Fig. 6) consists of two operational amplifiers (OTA1 and OTA2) to probe the amplified residue voltages, an low-voltage differential signalling (LVDS) transmitter (TX) to probe "low-duty-cycle" digital signals, such as CLK and clk1, as well as four digital output buffers (Dig Buf) to probe the other digital signals, such as $\tilde{\Delta}$ and CNG. An serial peripheral interface (SPI) interface provides the static digital control signals to allow for programmability of different blocks, such as $\text{Mux}_{\text{CTRL}}\langle 1{:}0\rangle$, used to control the 4-to-1 output MUXes for both the LVDS TX and Dig Buf, $\text{Probe}_{\text{CTRL}}\langle 1{:}0\rangle$ to enable OTA1 and OTA2, and $\text{G}_{m,\text{CTRL}}\langle 3{:}0\rangle$, which is used to control the gain and pole frequency of the pre-amplifier (as described later in this section).

A. Switched-Capacitor Feedback DAC and Subtractor

The charge-redistribution sw-cap feedback DAC and subtractor, inspired by [5], are shown in Fig. 7. The digital control signals, including clk1, clk2, s0, and s1, are all derived from the LC trigger CNG and system clock CLK. There are two operational phases: track and update. When a digital threshold level in the AR Comp is crossed, CNG is asserted, thus generating clk1 as a gated version of CLK. Likewise, clk2 is a non-overlapping inverted replica of clk1. The rising edge of clk1 asserts the update phase of the DAC. During this phase, depending on the digital binary output D_{OUT} of *U/D CNT*, the bottom plates of the DAC capacitors are connected to V_{REFP} or V_{REFN}, while the input capacitor C_S is shorted to V_{CM}. Moreover, the hold capacitor C_H maintains the value that node V_{RES} captured right before the end of the previous track phase. At the rising edge of clk2, the subtraction between V_{IN} and the sw-cap DAC output V_{DAC} is performed, which

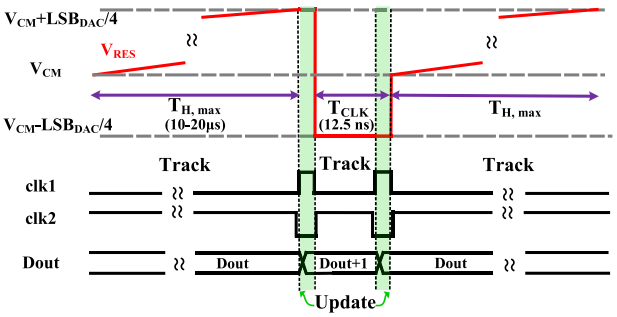

Fig. 8. Voltage pattern at node V_{RES} considering the sole effect of the switches leakage currents.

marks the beginning of the track phase. Synchronously to this, the control signals s0 and s1 also change state, inducing the flipping of the right-most C_H capacitor, thus removing the memory charge. During the track phase, V_{RES} is a CT signal and is equal to

$$V_{\text{RES}}(t) = G_S \cdot [V_{\text{IN}}(t) - V_{\text{DAC}}] + V_{\text{CM}} \tag{11}$$

where V_{DAC} is equal to $\text{LSB}_{\text{DAC}} \cdot \sum_{i=0}^{6}(D_{\text{OUT}}[i] \cdot 2^i)$ and G_S is 1/4.

The unit capacitance C is equal to 1.334 fF, and it is implemented as an M4-to-M6 MOM-cap from the PDK. The value of the two hold capacitors C_H is 170.7 fF (i.e., 128 C), which ensures that the standard deviation of mismatch between the two C_H's is only 0.1%, meaning the voltage error at V_{RES} due to the memory charge after the flipping of the second C_H (the right-most C_H in Fig. 7) is $\leq$30 μV (considering a 3σ variation) and can therefore be ignored. However, as the bulk CMOS technology scales, the drain(source)-to-gate ($I_{\text{gd,leak}}$), drain(source)-to-bulk ($I_{\text{bd,leak}}$), and subthreshold (off) drain-to-source (I_{off}) leakage current densities of the CMOS switches increase. Although the impact of the latter is negligible, since the residue voltage V_{RES} is in a small range around V_{CM} during the track phase, both the former leakage components (reasonably signal-independent) from all the switches asserting to V_{RES} lead to the loss of the charge information stored on C_H.

1) Maximum Voltage Error: It is worth noting that the maximum voltage error of V_{RES} caused by the sum of all these accumulating spurious leakage currents (I_{leakage}) is upper bounded by $\Delta V_{\text{err,max}} = \text{LSB}_{\text{DAC}}/4$ (or equivalently, $\Delta_{\text{min}}/4$, where the factor 4 stems from $\alpha \cdot G_A$). To understand this, let us consider the sole effect of leakage on node V_{RES}, and assume, without loss of generality, that the sign of I_{leakage} is such that V_{RES} is linearly increasing, and that the track phase has just been asserted. Therefore, the subsequent update phase will only be asserted when the residue-quantizer sub-ADC will "sense" a positive voltage shift of its input (i.e., the amplified residue voltage, $G_A \cdot V_{\text{RES}}$) equal to $\text{LSB}_{\text{sub-ADC}}$, implying $\alpha \cdot G_{\text{A}} \cdot V_{\text{RES}} = \alpha \cdot \text{LSB}_{\text{sub-ADC}} = \text{LSB}_{\text{DAC}}$ (where $\alpha \cdot G_A$ is nominally equal to 4). As a consequence, the loop reacts by increasing by 1 the feedback DAC digital input D_{OUT}, thus causing a negative voltage shift of V_{RES}. Such a shift would trigger another LC event, with D_{OUT} being decremented by 1 and consequently V_{RES} restored back to its initial correct value of V_{CM}. This mechanism produces a sawtooth voltage

pattern at node V_{RES}, as shown in Fig. 8, which acts as a dithering signal for the slowly varying input signal, ultimately resulting in a small increase in power consumption.

2) Maximum Hold Time: The above-mentioned effect of leakage current is particularly harmful at the turning point of a low-frequency input signal, as analyzed in [25], since the rate of change of V_{RES} caused by the linear charge (discharge) due to I_{leakage} can be comparable, or even considerably higher, than that caused by the slow ADC input signal. With reference to Fig. 8, we can therefore define with $T_{H,\max}$ the maximum hold time allowed for node V_{RES} before the accumulated leakage current would trigger an LC event (i.e., the time needed for I_{leakage} to make V_{RES} vary by an amount equal to $\Delta V_{\mathrm{err,max}}$) and expressed it as

$$T_{H,\max} = \frac{\Delta V_{\mathrm{err,max}} \cdot C_{H,\mathrm{total}}}{I_{\mathrm{leakage}}} = \frac{\Delta_{\min} \cdot C_{H,\mathrm{total}}}{4 \cdot I_{\mathrm{leakage}}} \tag{12}$$

where $C_{H,\mathrm{total}}$ is the total hold capacitor at node V_{RES}, which includes C_S, both the C_H capacitors, the total DAC capacitance, and any routing/parasitic capacitance, for an overall value of ~680 fF.

3) Input-Referred Voltage Error: The input-referred voltage error caused by the above-mentioned leakage current increases linearly with time. When the track-phase hold time reaches its maximum ($T_{H,\max}$), such error has an rms value of $\mathrm{LSB_{DAC}}/\sqrt{3}$. A first-order approximation of this voltage error at the modulator output can be derived by considering the average hold time $T_{H,\mathrm{avg,in}}$ between two consecutive level crossing events in the absence of current leakage, i.e., only due to the input signal. Its power can be expressed as

$$P(\delta_{\mathrm{leakage}}) = \left(\frac{T_{H,\mathrm{avg,in}}}{T_{H,\max}} \cdot \frac{\mathrm{LSB_{DAC}}}{\sqrt{3}} \right)^2. \tag{13}$$

This power is distributed over a frequency range that can span up to a frequency $\mathrm{BW_{leak}}$ (hereinafter referred to as leakage bandwidth) equal to the inverse of the minimum time between the consecutive level crossing events, $T^{-1}_{H,\mathrm{min,in}}$, whose maximum value corresponds to the clock frequency. This is because, according to the pseudo-CT operation of the proposed quasi-LC ADC, $T_{H,\mathrm{min,in}}$ cannot be lower than T_{CLK}. For a sinusoidal input signal with peak-to-peak amplitude $A_{\mathrm{in,pp}}$ and frequency f_{in}, $T_{H,\mathrm{avg,in}}$ and $T_{H,\mathrm{min,in}}$ can be expressed as

$$T_{H,\mathrm{avg,in}} = \frac{\mathrm{FS}}{f_{\mathrm{in}} \cdot A_{\mathrm{in,pp}} \cdot 2^{N+1}} \tag{14}$$

$$T_{H,\mathrm{min,in}} = \frac{\Delta_{\min}}{\pi \cdot f_{\mathrm{in}} \cdot A_{\mathrm{in,pp}}} \tag{15}$$

where FS is the modulator full-scale range and N is the resolution of the feedback DAC, equal to 7 in this design. Note that in (14) and (15) and for the sake of simplicity, we have assumed that f_{in} is such that the AR is not asserted, which justifies the use of the factor 2^{N+1} in the denominator of (14) (i.e., the number of levels crossed in one period of a full-scale input sinewave) and $\Delta_{\min}$ in that of (15). It is therefore evident that the leakage bandwidth depends on the input signal characteristics (e.g., frequency and amplitude) and, in the example of a −3-dBFS input sinewave, it equals to the signal bandwidth BW for $f_{\mathrm{in}} = 5$ kHz, meaning that all the leakage error power falls in-band when $f_{\mathrm{in}} \leq 5$ kHz. By substituting (12) and (15) into (13), $P(\delta_{\mathrm{leakage}})$ can be rewritten in the form

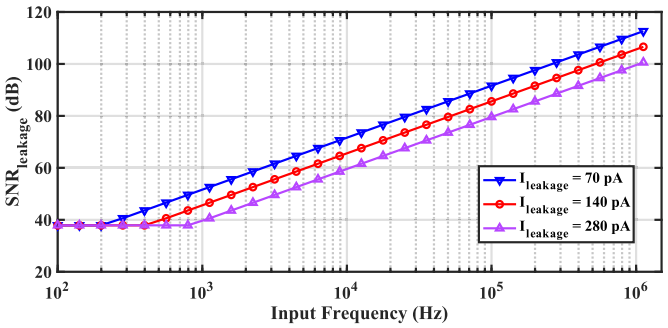

Fig. 9. ADC SNR caused by the sw-cap feedback DAC and subtractor leakage current versus input sinewave frequency.

$$P(\delta_{\mathrm{leakage}}) = \left(\frac{4 \cdot I_{\mathrm{leakage}} \cdot \mathrm{FS}}{2^{N+1} \cdot A_{\mathrm{in,pp}} \cdot C_{H,\mathrm{total}} \cdot f_{\mathrm{in}} \cdot \sqrt{3}} \right)^2 \tag{16}$$

which once again supports the intuition that for a given design of the sw-cap feedback DAC and subtractor, which implies certain I_{leakage}, N, $C_{H,\mathrm{total}}$, and FS, the error power caused by the leakage current of the switches only depends on the input signal characteristics (e.g., frequency and amplitude), suggesting that the SNR of the proposed quasi-LC delta modulator degrades at low signal frequencies. However, (16) also seems to suggest that $P(\delta_{\mathrm{leakage}})$ grows infinitely as f_{in} goes to zero. In reality, as stated earlier, the maximum voltage error at node V_{RES} due to the leakage is bounded by $\mathrm{LSB_{DAC}}/4$, and the maximum of $T_{H,\mathrm{avg,in}}$ is $T_{H,\max}$. Based on (13), the maximum power of voltage error at the modulator output caused by the leakage is $1/3 \cdot \mathrm{LSB^2_{DAC}}$, which falls completely within the signal bandwidth of the modulator, thus resulting in a lower bounded SNR caused by leakage ($\mathrm{SNR_{leakage}}$) of about 38 dB.

Circuit simulations indicate a nominal value of I_{leakage} of approximately 70 pA, which leads to a nominal $T_{H,\max}$ of about 19 μs. The degradation of the $\mathrm{SNR_{leakage}}$ is plotted in Fig. 9 for I_{leakage} equal to 70, 140, and 280 pA (i.e., the expected best, nominal, and worst case leakage) in which, for the sake of illustration, all the leakage power is considered to be in-band (even for input signal frequencies above the aforementioned 5 kHz). By increasing $C_{H,\mathrm{total}}$ (whose size is tied to the unit cap C) and by reducing the size of the switches so as to decrease I_{leakage}, the implemented sw-cap feedback DAC and subtractor can support even lower signal bandwidths (i.e., biomedical implantable devices). The size of the switches and of the unit cap C determines the tradeoff between the leakage error power at low signal frequency and the modulator distortion arising from the incomplete settling of the sw-cap DAC and subtractor.

Although the above-mentioned analysis focuses on the low-frequency impairments of the proposed quasi-LC ADC, the SNDR in the mid-band region of the spectrum is also a function of the signal path gain G_{total}, and it is moreover affected not only by the resolution of the sw-cap feedback DAC, which directly relates to the odd harmonics of the modulator, but also by the nonlinearity of the sw-cap feedback

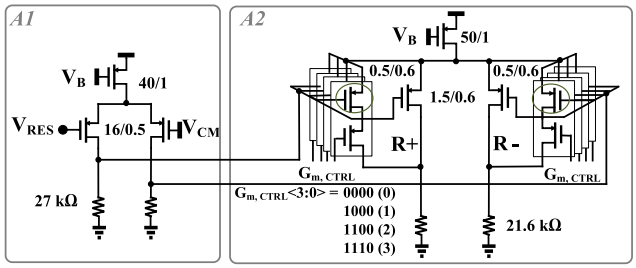

Fig. 10. Pre-amplifier implementation (MOS dimensions are in μm).

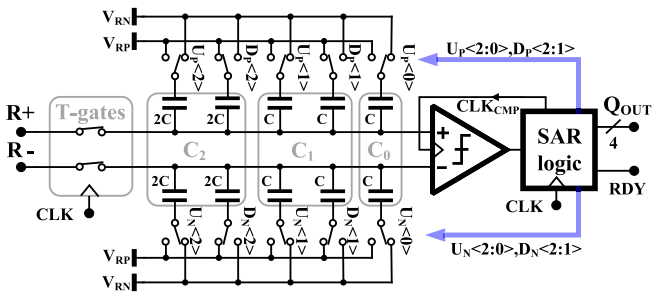

Fig. 11. Residue quantizer.

DAC and subtractor, whose harmonic distortion (i.e., SFDR of about 60 dB) directly impacts the delta modulator output.

B. Pre-Amplifier

The pre-amplifier serves the purpose of amplifying the residue voltage V_{RES}, converting the single-ended residue voltage to differential and driving the input capacitance of the differential asynchronous SAR residue quantizer behaving as an LPF in front of residue quantizer. As shown in Fig. 6, the pre-amplifier consists of two stages (A1 and A2), each with a nominal dc gain of 2, and whose detailed implementation is shown in Fig. 10. As discussed earlier, the gain and pole frequencies of the pre-amplifier determine the NTF and STF characteristics of the delta modulator. A PVT-induced deviation of the signal path gain G_{total} from its nominal value can be accommodated by adjusting the amplitude of $\mathrm{LSB}_{\mathrm{sub\text{-}ADC}}$ (tuning V_{RP} and V_{RN}, with reference to Fig. 6), as well as by tuning the aspect ratio of the input differential pair transistors of A2 (therefore the transconductance) for the situation that V_{RP} and V_{RN} need to be fixed, which allows to restore $\alpha \cdot G_A \cdot G_S$ to unity. This is implemented using a bank of five parallel PMOS transistors, three of which can be disconnected from the output node of A2 with PMOS switches in series to their drains, controlled by the digital code $G_{m,CTRL}$ (active low). This tuning scheme is only implemented in A2, as the parasitic capacitor at V_{RES} would lead to gain deviation of G_S and memory charge on capacitor C_H. Besides, such tuning scheme is also effective in compensating for variations in the frequency of dominant poles, since increasing the number of PMOS transistors connected in parallel also increases the load capacitance of A1. Indeed, from $G_{m,\mathrm{CTRL}} = 0$ to $G_{m,\mathrm{CTRL}} = 3$, G_{A2} drops by 50%, while the load capacitor of A1 decreases by approximately 20% (neglecting the parasitic capacitance). For the conventional LC ADCs, the offsets of CT comparators cause shifts of the threshold levels, ultimately leading to nonlinearity. Therefore, an offset calibration protocol is needed, such as in [5] and [24]. In the proposed modulator, the offset of pre-amplifier and residue quantizer can be treated as an input dc voltage shift, which only leads to an offset in the digital binary output code of *U/D CNT* (D_{OUT}) and which has no impact on linearity. From the value $G_{m,\mathrm{CTRL}} = 0$ to $G_{m,\mathrm{CTRL}} = 3$, the input-referred in-band noise of the pre-amplifier increases by 16%, from 20.94 $\mu\mathrm{V}_{\mathrm{rms}}$ to 24.3 $\mu\mathrm{V}_{\mathrm{rms}}$, respectively, mainly contributed by flicker noise, as the effective size of the input MOS transistors of the stage A2 decreases (less transistors connected in parallel). However, considering that the power of this noise is much smaller than that of the in-band quantization noise contributed by the residue quantizer, its effect on the system SNR can be neglected.

C. SAR-Based Residue Quantizer

In the proposed quasi-LC ADC, the residue quantizer converts the amplified residue voltage into a 4-bit digital information (Q_{out}). The choice of 4 bits relies on the chosen AR factor ($L = 5$) demanding ten threshold levels [according to the equivalent model presented in Fig. 1(d)]. The clock frequency of 80 MHz is chosen to allow all the 4 bits to be resolved (i.e., ensuring that the conversion-ready output trigger, RDY, is always asserted within a clock period), and accounting for a reasonable time margin to cope with process variations. The residue quantizer is implemented as a top-plate sampling asynchronous SAR ADC with split binary-weighted capacitive DAC (apart from the LSB capacitors C_0, which are not split), as shown in Fig. 11. The choice of the successive approximation topology relies on its simplicity, amenability to process scaling and state-of-the-art power efficiency.

The unit capacitor of the residue-quantizer capacitive DAC is a 4.5-fF MOM-cap from the PDK, while the sampling switches are simple transmission gates. Given the low resolution of sub-ADC, as well as the low amplitude of the amplified V_{RES} (well below the ADC's full-scale range), switch bootstrapping is not necessary. The comparator is implemented as a simple latch stage, while the SAR logic consists of only TSPC flip-flops and logic gates. Because of oversampling (f_{CLK} is about 56 $\times$ BW), the contribution of the residue-quantizer quantization noise power to the proposed LC ADC's SNR is

$$\mathrm{SNR}_{\mathrm{SAR,dB}} = 6.02N + 1.76 + 10\log\left(\frac{f_{\mathrm{CLK}}}{2 \cdot \mathrm{BW}}\right) \quad (17)$$

where N is the resolution of the sw-cap feedback DAC. For BW = 1.42 MHz, $\mathrm{SNR}_{\mathrm{SAR}} = 58$ dB, which is indeed the upper bound of the SNR of the proposed quasi-LC ADC. With reference to (2), a conventional LC ADC with equal bandwidth would demand a loop delay dispersion Δt_e lower than 173 ps to achieve the same SNR, which is rather difficult to obtain with a multi-stage comparator topology, and would need to be traded off with the comparators' bandwidth and power consumption. For example, the four-stage comparator in the LC ADC presented in [24] could achieve a delay dispersion of

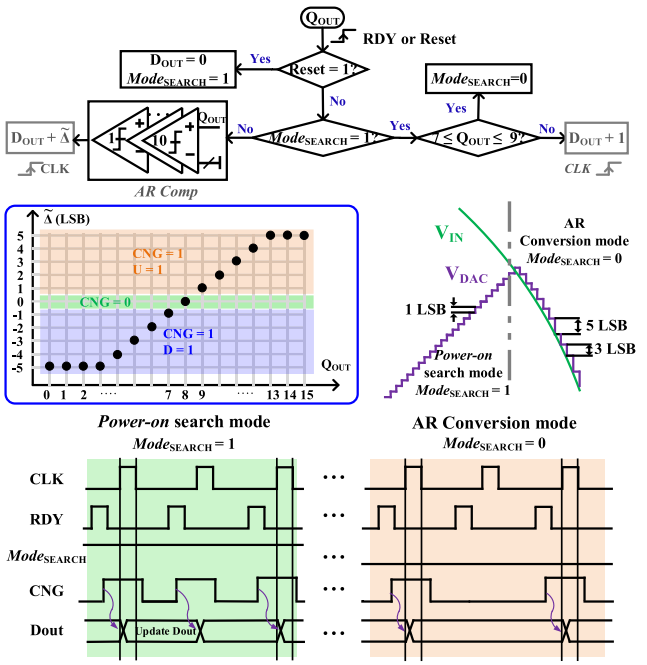

Fig. 12. Logic flow of the synthesized digital block and the corresponding timing diagram.

around 150 ps with a bandwidth of 200 MHz when the ADC converts a 20-MHz full-scale input sinewave. In the proposed modulator, the quantization noise of the residue quantizer dominates the SNR at signal frequencies in the upper range of the signal bandwidth of the modulator, while for low input frequencies, the ADC SNR is instead dominated by the voltage error caused by the current leakage of the switches within the sw-cap subtractor, as discussed earlier.

D. AR Comparator and Up/Down Counter

Fig. 12 shows the flow diagram of the synthesized digital logic. At the system reset (Reset, e.g., power-ON reset or user interrupt), a power-ON search mode is asserted by setting $\text{Mode}_{\text{SEARCH}}$ to 1 at the rising edge of Reset. The U/D counter then increments at each rising edge of CLK until the feedback DAC output "locks" within 1 LSB_{DAC} away from V_{IN} or, alternatively, until $|V_{\text{RES}} - V_{\text{CM}}| \leqslant \Delta_{\text{min}}/4$. This ends the power-ON search mode and asserts the normal AR conversion mode ($\text{Mode}_{\text{SEARCH}} = 0$). In this operational phase, when RDY $= 1$ is asserted, the digital comparison is performed between Q_{OUT} and the ten thresholds of the AR Comp (9, 10, ... 13 and 3, 4, ... 7; see Fig. 12), which are the digital equivalents of the "levels" of an LC ADC [with reference to Fig. 1(d)]. This will end in generating the event-based digital output signal EB_{OUT}. This whole sequence of operations must be completed before the next rising edge of CLK, which triggers the update of the U/D counter output D_{OUT}, according to EB_{OUT}.

IV. Measurement Results

The proposed quasi-LC delta modulator is implemented in TSMC 28-nm LP CMOS and occupies an area of 0.0126 mm^2.

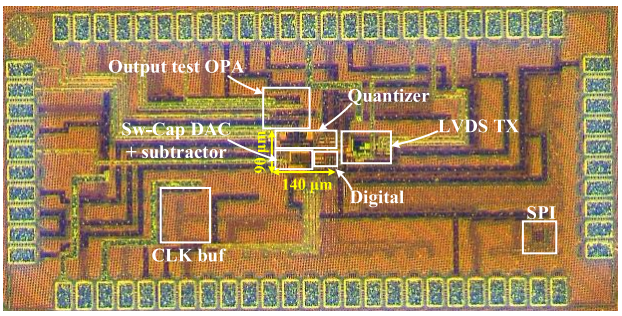

Fig. 13. Chip micrograph of the proposed AR quasi-LC delta modulator.

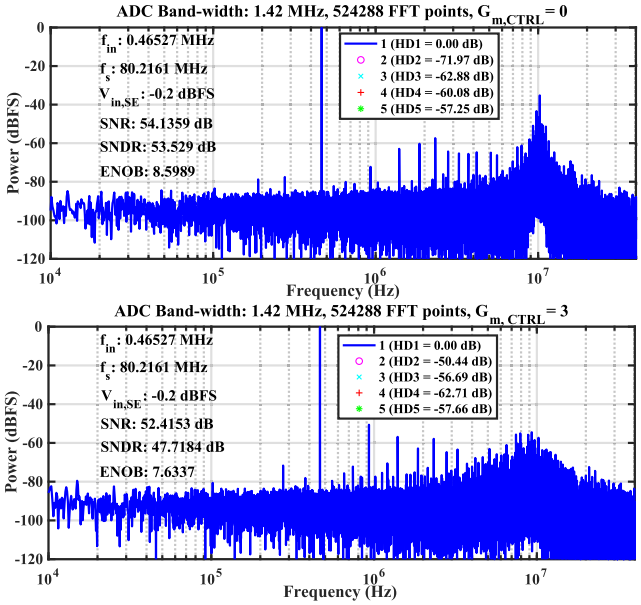

Fig. 14. Measured spectrum with a 465-kHz −0.2-dBFS sinusoidal input with different $G_{m,\text{CTRL}}$ settings.

The chip micrograph is shown in Fig. 13. The core modulator consists of the sw-cap subtractor, pre-amplifier, residue quantizer, and synthesized logic. Supporting circuitry includes the input clock buffer, SPI interface, output test OTAs, and LVDS TX.

Fig. 14 shows the measured spectra of the modulator at the two extreme signal path gain settings (maximum and minimum for $G_{m,\text{CTRL}}$ equal to 0 and 3, respectively) with a 465-kHz −0.2-dBFS sinusoidal input signal. The SAR sub-ADC voltage references $V_{\text{RP}}/V_{\text{RN}}$ are fixed. From $G_{m,\text{CTRL}} = 0$ to $G_{m,\text{CTRL}} = 3$, the signal path gain G_{total} decreases by 50%, while the dominant pole introduced by the pre-amplifier increases by 20%. Based on the comparison, a 50% drop in G_{total} causes a 1.7-dB increase in SNR, as well as about 10-dB reduction in the out-band peaking of both STF and NTF, which matches the outcome of the system-level analysis introduced in Section II-B. For the spectrum with $G_{m,\text{CTRL}} = 3$, the harmonic power is higher, which is in agreement with system behavioral modeling results, outlining indeed that THD degrades as G_{total} decreases. The quantization noise generated by the residue quantizer is the dominant contributor to the ADC noise power although the oversampling enables the

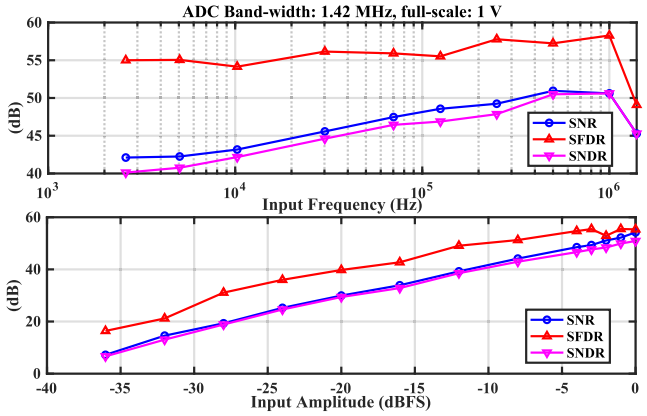

Fig. 15. Measured SNR/SFDR/SNDR versus frequency at −3-dBFS amplitude (top) and versus amplitude at 250-kHz frequency (bottom) for a sinusoidal input.

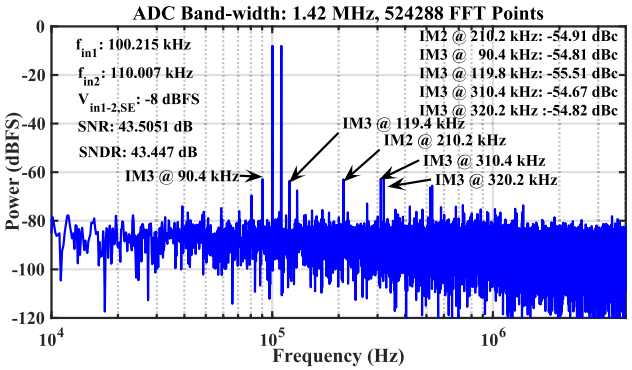

Fig. 16. Two-tone test with input sinewaves at 100.21 and 110.01 kHz.

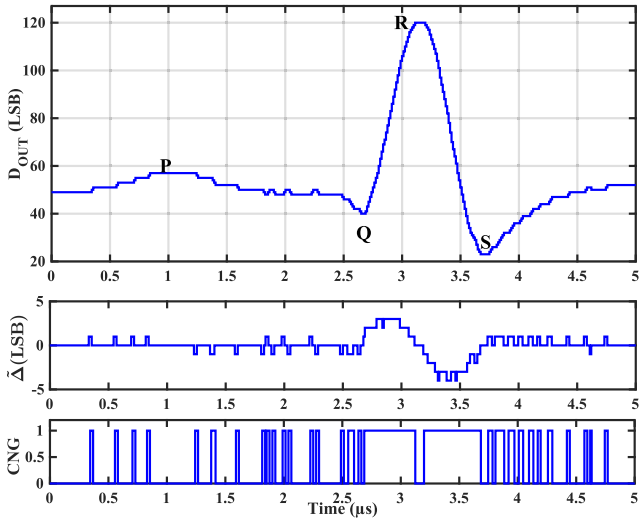

Fig. 17. Measured digital output (D_{OUT}) and event-based output signals ($\tilde{\Delta}$ and CNG) in the example of an ECG signal pattern generated with an arbitrary waveform generator (note: the signal frequency has been purposely increased so as to visualize the operation of the AR algorithm in the regions of high signal derivative).

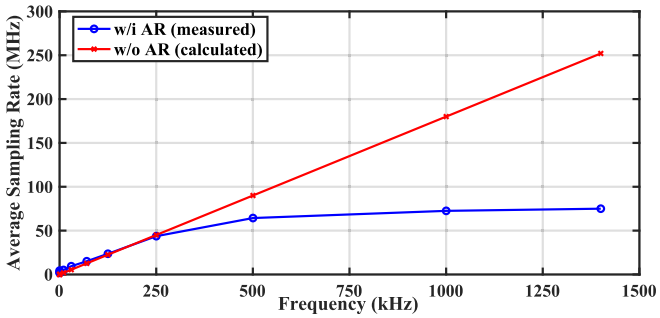

Fig. 18. Measured average sampling rate (with AR algorithm) and theoretical average sampling rate without AR versus input sinewave frequency.

system to achieve an effective resolution of about 1.5 bits higher than the 7-bit nominal resolution of the feedback DAC.

Fig. 15 shows the measured SNR, SFDR, and SNDR versus the frequency of a −3-dBFS sinusoidal input, and versus the amplitude of a 250-kHz input sinewave, for the setting of signal path gain $G_{m,\mathrm{CTRL}} = 0$. The gradual drop of SNDR at low frequencies is caused by more harmonics falling into the signal bandwidth, as well as by the voltage error at node V_{RES} induced by leakage current of the switches within the sw-cap subtractor, as discussed in Section III-A. The measured SNDR versus input amplitude demonstrates that the DR of the proposed quasi-LC ADC is higher than 36 dB, suggesting that the main limiting factor is the resolution of the sw-cap feedback DAC. Therefore, the smallest signal peak-to-peak amplitude that can be detected is ≤15.6 mV ($V_{\mathrm{DD}}/2^6$, where $V_{\mathrm{DD}} = 1$ V in this design), which is located in between 1 and 2 $\mathrm{LSB}_{\mathrm{DAC}}$. The two-tone ADC output spectrum is shown in Fig. 16, using two −8-dBFS input sinewaves at 100.21 and 110.01 kHz. Compared to the single-tone output spectrum in Fig. 14, the input signals around 100 kHz entail a higher voltage error caused by the leakage current at node V_{RES}, thus resulting in a higher noise floor.

Given the intended use of the proposed quasi-LC ADC for digitizing signals that are sparse in time and with a low-to-medium accuracy, it is illustrative to show its behavior with relevant signals, e.g., an electrocardiographic (ECG)-like shape generated via an arbitrary waveform generator. The measured 7-bit digital binary output D_{OUT} and the event-based output $\mathrm{EB}_{\mathrm{OUT}}$ are shown in Fig. 17, demonstrating that the AR algorithm is enabled only when the input signal changes rapidly, as visible when $\tilde{\Delta}$ (the direction information is included in UD) becomes higher than 1 or lower than −1 (e.g., between the Q and R and between the R and S intervals). Moreover, the event trigger CNG is kept low when no level crossing occurs.

In order to highlight the advantages of AR, the measured average sampling rate of the $\mathrm{EB}_{\mathrm{OUT}}$ signal bus is shown in Fig. 18 for a −3-dBFS sinusoidal input and compared to that without the AR algorithm, whose estimation $f_{\mathrm{EB,out}}$ is well approximated by (1)

$$f_{\mathrm{EB,out}} = 2 \cdot f_{\mathrm{in}} \cdot \frac{A_{\mathrm{in,pp}}}{\mathrm{FS}} \cdot 2^N \tag{18}$$

where N is the resolution of the sw-cap feedback DAC, which is equal to 7. It can be observed from Fig. 18 that the AR algorithm starts engaging when the input signal frequency is >280 kHz. It can reduce the average sampling rate by as much

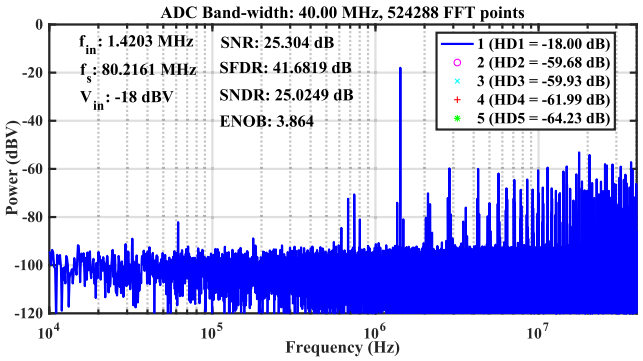

Fig. 19. 4-bit SAR sub-ADC measured output spectrum at 80 MS/s and with a differential 176-mV 1.42-MHz input sinewave.

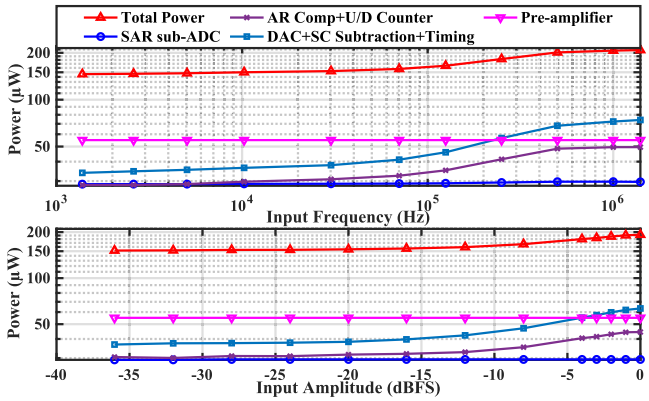

Fig. 20. Measured power consumption versus frequency of a −3-dBFS sinusoidal input and versus amplitude of a 250-kHz sinusoidal input.

as 3× at the edge of the bandwidth (∼1.4 MHz). On the other hand, for input frequencies <100 kHz, the measured average sampling rate is slightly higher than its theoretical value (i.e., the two curves in Fig. 18 are not overlapped) due, again, to the leakage current at node V_{RES} which, in addition to slightly impairing the ADC performance, also causes "spurious" level crossing events. It must be reminded that apart from the clear advantage in terms of average sampling rate reduction, the exploitation of the AR algorithm enables a wider signal bandwidth, which would otherwise be limited to only 280 kHz.

For the sake of completeness, the 4-bit SAR sub-ADC has also been separately characterized. The additional DFT circuitry allows to disconnect its stage A1 from A2 and to provide a differential sinewave to the input of A2, thus using it as a driving amplifier. The residue-quantizer output Q_{OUT} is read out through a logic analyzer, showing a maximum DNL and INL of 0.17 and 0.13 LSB, respectively. The output spectrum with an 88-mV 1.42-MHz differential input sinewave is shown in Fig. 19. Considering that the dc gain of A2 is equal to 2, the differential signal amplitude at the sub-ADC input is 176 mV (−18 dBV), which will trigger a full-scale "swing" of the digital output of the SAR sub-ADC without yet causing any clipping.

The measured power consumption of the proposed quasi-LC modulator versus frequency for a −3-dBFS sinusoidal input and versus amplitude for a 250-kHz sinusoidal input is shown in Fig. 20. Only the low-gain pre-amplifier consumes static power. The proposed modulator exhibits the scalable power consumption versus the input signal frequency and amplitude, as mainly contributed by the sw-cap feedback DAC, subtractor, and AR Comp, which are dynamic circuits driven by the on-demand event-based CLK. Although the uniform sampling occurs at the residue quantizer, the proposed modulator is comparable to most CT LC ADCs in terms of both power consumption and power scalability over input frequency and amplitude and, in most cases, superior to uniform-sampling ADCs in terms of power scalability over input frequency and amplitude.

The modulator performance has been characterized over multiple dies, and the measured SNDR versus frequency of a −3-dBFS input sinewave and versus amplitude of a 250-kHz sinewave is shown in Fig. 21 for six different ICs. The maximum SNDR variation for the same input frequency between different dies is upper bounded to 2 dB, whereas the maximum SNDR variation between different dies is around 6 dB when the sinusoidal input signal amplitude is −36 dBFS, in agreement with the discussion on the DR in Section II-E. Fig. 22 shows the measured SNDR versus ±10% supply voltage variation, demonstrating a gradual drop toward lower supply voltages. The minimum value of 47.5 dB is mainly

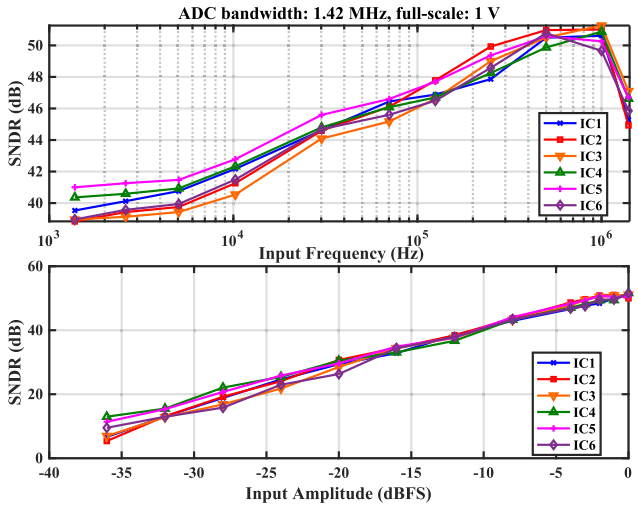

Fig. 21. Measured SNDR versus frequency of a −3-dBFS sinusoidal input and versus amplitude of a 250-kHz sinusoidal input for six measured ICs.

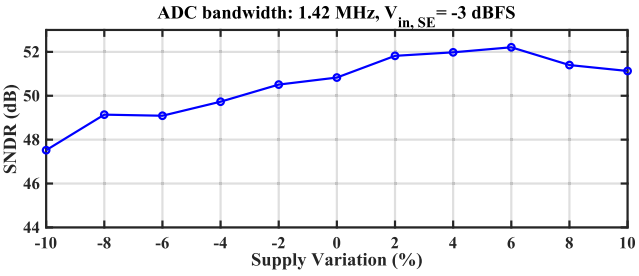

Fig. 22. Measured SNDR versus supply variation of a −3-dBFS 465-kHz sinusoidal input.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART IN ADCS FOR COMPRESSED SENSING APPLICATIONS

	[5] Wu JSSC 2013	[6] Trakimas TCASI 2011	[8] Kurchuk JSSC 2012	[9] Schell JSSC 2008	[24] Wu JSSC 2017	[26] Tang TCASI 2013	**This Work**		
							$\mathbf{G_{m,CTRL}}$		**worst case**
							0	**3**	**@slow-varying signal**
Topology	AR LCS	AR LCS	LCS	LCS	LCS	LCS	**AR LCS**		
Need CT Comparator	Yes	Yes	Yes	Yes	Yes	Yes	**No**		
Process (nm)	130	180	65	90	65	500	**28**		
Area (mm^2)	0.3575	0.96	0.0036	0.06	0.3	0.06	**0.0126**		
BW	20 kHz	1 kHz	2.4 GHz	10 kHz	20 MHz	5 kHz	**1.42 MHz**		
Power	3-9 μW	25 μW	2.3 mW	1.23 mW	30 mW	106 μW	**205 μW**		**146 μW**
SNDR (dB)	47-54	52.2	25.3	47-62	59.9	31	**53.53**	**47.72**	**43.12**
$\mathbf{FoM_W}$(fJ/c-s)	230-888	37,600	32	59783	929	365,700	**186.1**	**363.2**	**439.4**

impaired by a 40% gain reduction in G_A, which results in a 40% gain reduction in G_{total}, thus degrading the system THD as per discussion in Section II-B.

Finally, Table I summarizes the performance of the proposed quasi-LC delta modulator and compares it with state-of-the-art ADCs for compressed sensing applications. It shows that our ADC can achieve the best FoM and smallest area among the listed ADCs with >6-bit resolution. The worst case current leakage scenario, represented by the conversion of a slowly varying input signal, is listed in the last column.

V. CONCLUSION

A quasi-LC delta modulator featuring AR and exploiting voltage residue quantization using a 4-bit asynchronous SAR sub-ADC was presented. This promotes shifting the LC detection into the digital domain where the AR and LC algorithms can be straightforwardly implemented as synthesizable logic. By avoiding the use of high-performance analog comparators, the timing errors no longer contribute to the ADC SNR, while amplitude quantization does not impair the performance due to the oversampling nature in the residue quantizer of the proposed delta modulator. Its synchronous DT digital output allows to directly interface to conventional DT DSPs. Finally, thanks to the AR algorithm, the average sampling rate is reduced by a factor of 3 at the edge of the modulator's signal bandwidth.

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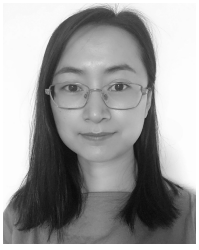

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