A 265-μW Fractional-N Digital PLL With Seamless Automatic Switching Sub-Sampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65-nm CMOS

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***Abstract*— This article proposes a fractional-N digital phase-locked loop (DPLL) that achieves a 265-μW ultra-low-power operation. The proposed switching feedback can seamlessly change the DPLL from sampling operation to sub-sampling operation without disturbing the phase-locked state of the DPLL to reduce the number of building blocks that works at the oscillator frequency, leading to significant power reduction. With the reduced number of high-frequency circuits, scaling the reference frequency is fully used to reduce the power consumption of the DPLL. Together with an out-of-dead-zone detector and a duty-cycled frequency-locked loop running in the background, the switching feedback achieves robust frequency and phase acquisition at start-up and helps the sub-sampling PLL recover when large phase and frequency disturbances occur. A transformer-based stacked-g_m oscillator is proposed to minimize the power consumption while providing the sufficient swing to drive the subsequent stages. A truncated constant-slope digital-to-time converter is proposed to improve the power efficiency while retaining good linearity. The proposed fractional-N DPLL consumes only 265 μW while achieving an integrated jitter of 2.8 ps and a worst case fractional spur of −52 dBc, which corresponds to a figure of merit (FOM) of −237 dB.**

***Index Terms*— Constant slope, digital phase-locked loop (DPLL), digital-to-time converter (DTC), duty-cycled frequency-locked loop (DC-FLL), FLL, fractional-N, low power, out-of-dead zone (ODZ), PLL, sampling, sub-sampling, switching feedback, transformer, truncated, ultra-low-power (ULP), ULP VCO, voltage-controlled oscillator.**

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I. Introduction

THE demand for ultra-low-power (ULP) circuits and systems has exponentially increased with the growth of today's system-on-chip (SoC) devices. SoC power reduction greatly benefits battery-driven applications, such as the Internet-of-Things devices, sensor networks, and cellular networks. Phase-locked loops (PLLs), one of the most important building blocks in the SoC devices, have recently drawn much research attention, as they account for a significant portion of device power consumption. For example, the PLL in [1] consumes nearly 48% of the total power of the receiver. The output of the fractional-N PLL has a much finer frequency resolution than that of an integer-N PLL and is thus used in a variety of applications. However, it consumes additional power to minimize the jitter-spur degradation caused by the fractional-N operation. Reducing the power consumption of a fractional-N PLL while maintaining good jitter and spur performance is very challenging.

Digital PLLs (DPLLs) [2]–[16] are gaining more attention over traditional analog PLLs due to their scalability in advanced CMOS technology and design portability across technologies. Another advantage of the DPLLs is their digital input–output that enables self-calibration, such as that of the bandwidth and the oscillator gain.

Fig. 1 shows two low-power fractional-N DPLL architectures. They demonstrate a significant power reduction from the time-to-digital converter (TDC) because of the digital-to-time converter (DTC) [2]–[7]. Fig. 1(a) shows the so-called divider-based architecture [2]–[4]. It mimics the conventional charge-pump (CP) PLL operation by replacing the phase-frequency detector (PFD) and the CP with a TDC. Because the DTC reduces the quantization noise from the multi-modulus divider (MMD), a narrow-range TDC (NR-TDC) [2], [4] or even a bang-bang phase detector (BBPD) [3] can be used for the phase-quantizing operation to lower

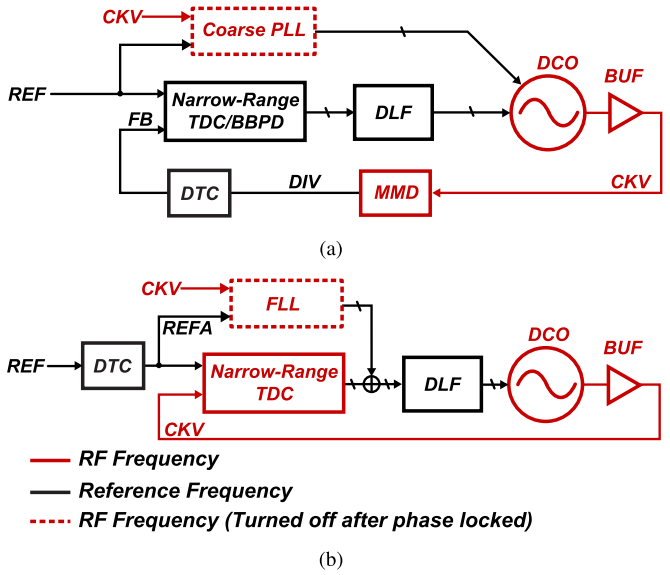


Fig. 1. (a) Divider-based fractional-*N* low-power DPLL. (b) Dividerless fractional-*N* low-power DPLL.

the overall power consumption. The fractional-*N* DPLL in [2] achieves an unprecedented low power consumption of 0.65 mW with a jitter of 1.0 ps and a worst case fractional spur of −52 dBc. One of the simplest methods to further lower the power consumption is to lower the reference frequency to reduce the power consumption of the TDC, DTC, and digital circuits. However, the power consumption of some building blocks does not scale with the reference clock, such as the digitally controlled oscillator (DCO), the DCO buffer, and MMD. The DCO alone consumes 0.29 mW [2] to maintain a sufficiently high-output amplitude to drive further stages. Further lowering the DCO bias current will result in the oscillation or the divider failure. Fig. 1(b) shows another popular architecture for low-power design, namely the dividerless architecture [5]–[7]. It directly samples and compares the DCO clock (CKV) with the reference clock. A DTC is used to shrink the required TDC range to lower power consumption. The operation of this architecture is very similar to that of the analog sub-sampling PLL, which uses a reference to directly sample the oscillator output [17]–[20]. The dividerless architecture removes the power consumption of the divider. However, the TDC still consumes significant power during the sub-sampling operation and is affected by frequency disturbances due to the multiple narrow-frequency lock-in ranges when the frequency-locked loop (FLL) is turned off. A DPLL [21] based on this architecture achieved a very low power consumption of 0.67 mW with a jitter of 1.98 ps and an in-band fractional spur of −56 dBc.

The key challenges for furthering reducing power consumption are: 1) reducing the power consumption of the building blocks operating at the oscillator frequency and 2) reducing the power consumption from the DCO while maintaining a large output swing and a low phase noise. This article proposes a ULP fractional-*N* DPLL fabricated in the TSMC 65-nm CMOS technology. The proposed seamless switching feedback works in conjunction with the out-of-dead zone (ODZ) detector and the duty-cycled FLL (DC-FLL) to remove the power consumption of the MMD while achieving robust frequency acquisition characteristics when frequency disturbances occur. The switching feedback leads to a 48% power consumption reduction from the DPLL, excluding the DCO power consumption. A transformer-based stacked-g_m ULP DCO is proposed that consumes only 107 μW and gives −107 dBc/Hz at a 1-MHz offset frequency. A truncated constant-slope DTC (CS DTC) is proposed to improve the power efficiency of the conventional architecture while retaining excellent linearity to achieve low fractional spurs. Thanks to these techniques, the presented fractional-*N* DPLL consumes only 265 μW while achieving a jitter of 2.8 ps and a worst case in-band fractional spur of −52 dBc. The obtained power consumption is nearly 2.5 times smaller than that of a state-of-the-art low-power fractional-*N* DPLL [2].

TABLE I
POWER BUDGET BREAKDOWN FOR 10-MHz REFERENCE CLOCK

Blocks	Specification	Jitter Contribution	Power Consumption
DCO	-107 dBc/Hz@1MHz	49.8%	107 µW
TDC	10 ps/LSB	27.0%	22 µW
DTC	2 ps/LSB	23.2%	23 µW
Digital Circuits[1]	-	0.0%	45 µW
BUF and MMD	9-bit Freq. Control	**∼0.0%**	**218 µW**

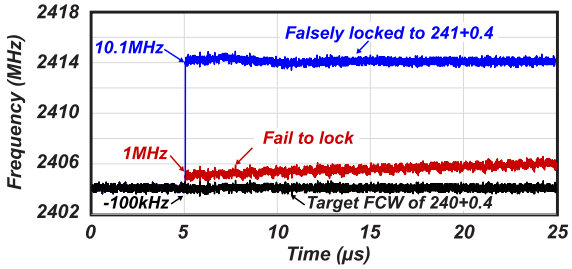
[1] DLF, DC-FLL, DSM-based controller, DTC-gain cal., state machine.

II. PROPOSED ULP FRACTIONAL-*N* DPLL

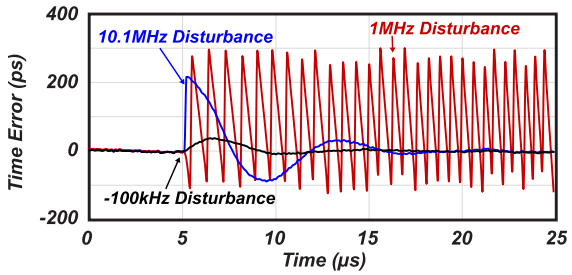
A. Proposed Seamless Switching Feedback Path

Scaling the reference frequency can effectively lower the power consumption of the TDC, DTC, and digital circuits [22]. However, power consumption is dominated by the building blocks operating at radio frequency (RF), as shown in Fig. 1. Table I shows the power breakdown based on a low reference clock of 10 MHz for the architecture in Fig. 1(a). The total power consumption can be separated into the power consumption from the loop and that from the DCO. To achieve the best jitter-power tradeoff [23], the jitter from the oscillator and that from the loop should be equal, so are the power consumption. As shown in Table I, the DCO contributes 50% of the jitter in the DPLL output. However, due to the high power consumption by the MMD and the DCO buffer, the loop (TDC, DTC, MMD, DCO buffer, and digital circuits) consumes almost three times the power of the DCO, resulting in a poor power-jitter tradeoff.

As mentioned, sub-sampling PLLs have the potential to remove the power consumption of the MMD due to their dividerless operation. However, an FLL is required to maintain a robust start-up and resist frequency disturbances. Without the FLL, the sub-sampling loop will have lock-in ranges near the integer multiples of the reference clock. For example, the PLL can lock the oscillator frequency to either a frequency-controlled word (FCW) of 240.4 or 241.4. Fig. 2 shows the simulation results of the sub-sampling PLL with a loop bandwidth of around 110 kHz using a 10-MHz reference clock for various types of frequency disturbance applied to



(a)



(b)

Fig. 2. (a) Sub-sampling loop responses for various frequency disturbances applied to the oscillator. (b) Phase errors at the sub-sampling phase detector input.

the DCO. The lock-in range of a sub-sampling PLL can be estimated as about two times the loop bandwidth, as explained in [21]. In our system simulations, with the applied disturbance frequencies swept, a lock-in range of approximately ±280 kHz was observed. This PLL can correct a frequency disturbance of −100 kHz from its center frequency, as shown in Fig. 2(a) (black line). The corresponding time error at the input of the sub-sampling phase detector is small and can, thus, be mitigated quickly, as shown in Fig. 2(b) (black line). However, if a large frequency error (larger than the lock-in range) of 1 MHz is applied to the oscillator, the loop cannot produce the correct response and fails to lock back. The time error bounces back and forth due to the phase wrapping characteristics of the sub-sampling loop and has a peak-to-peak value of one DCO period, as shown in Fig. 2(b) (red line). Furthermore, the oscillator frequency will be trapped in the next lock-in range if a 10.1-MHz disturbance is applied. In this situation, the time error can be suppressed by the loop while the locked frequency is completely wrong. These frequency disturbances will have a catastrophic effect on a system that uses this PLL as a frequency or timing source. The lock-in ranges will shrink as the reference frequency is further reduced. Hence, lowering the reference frequency will lead to more locking failures in sub-sampling operation.

Fig. 3 shows the proposed fractional-N DPLL with switching feedback. It consists of a gating logic, an MMD, a D-type flip-flop (DFF), a multiplexer, and a time-domain sampler. The FB signal can be selected from either the DTC output (REFA) or the MMD output (DIV) through the multiplexer with a propagation delay of τ_{DFF}. When DIV is selected as the multiplexer input, the DPLL works in the sampling mode, which mimics the CP-PLL operation. When REFA is selected as the multiplexer input, the DPLL works in the sub-sampling mode.

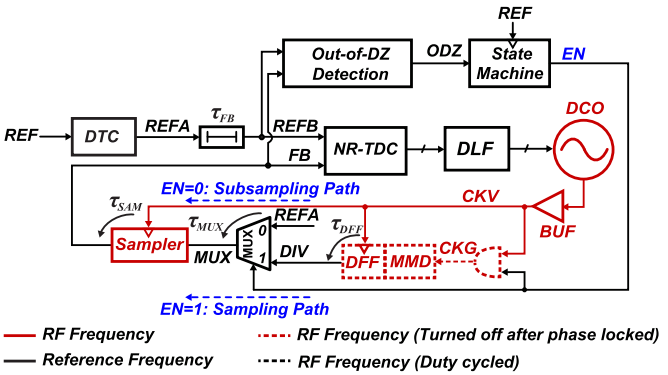
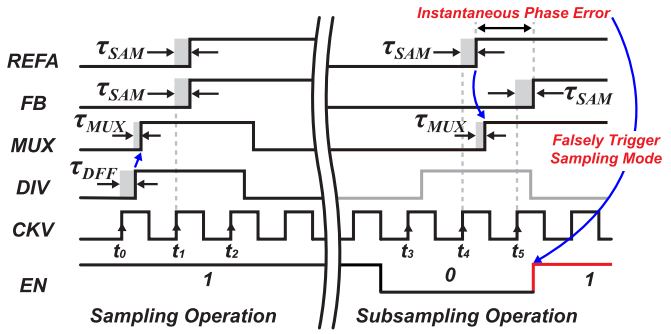


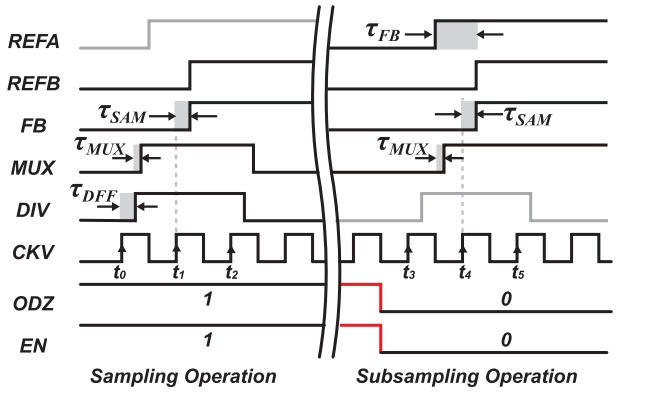
Fig. 3. Proposed switching feedback path that can seamlessly switch from the sampling mode to the sub-sampling mode.

In the sampling mode, the DFF is used to align the DIV signal to the CKV signal with a propagation delay of τ_{DFF}. The DFF operation removes jitter and non-linearity from the MMD. In this mode, the FB signal contains not only the phase information from the oscillator but also the frequency information. The MMD operation allows the oscillator to quickly recover from phase/frequency disturbances. This mode is applied during DPLL start-up, or when the DPLL is subjected to frequency disturbances and needs to recover. After the DPLL is locked, REFA is selected as the multiplexer input. The DCO phase is extracted by sampling the REFA using the CKV signal. In this mode, only the phase information from DCO is extracted at FB (frequency information is dropped). This mode is used most of the time during the DPLL operation. It removes the power consumption from the MMD and the re-timing DFF. Even though no divider is physically present in the sub-sampling mode, its open-loop transfer function still suffers from a virtual divide ratio of N, where N is the ratio of the oscillation frequency to the reference frequency. For example, a 1-ps time error at the TDC input will transfer to 0.432° phase error at 2.4 GHz, while the phase error becomes only $0.432/240 = 0.0018°$ at 10-MHz reference frequency ($N = 2.4$ GHz/10 MHz $= 240$ in this case). Thus, the transfer function of the sub-sampling mode becomes the exact same function as the sampling mode when the time difference detected by TDC is less than one DCO cycle. This guarantees the seamless switching operation of the subsampling mode and the sampling mode.

However, directly switching from the sampling mode to the sub-sampling mode in the feedback path will cause phase discontinuity due to the delays in the feedback path. An additional delay of τ_{FB} is inserted after DTC to mitigate phase discontinuity. Fig. 4(a) shows the problem that occurs when τ_{FB} is not included. In the sampling mode, the MMD output is re-timed by the DFF at t_0 with a propagation delay of τ_{DFF}. The multiplexer passes the DIV signal to the MUX with a τ_{MUX} delay. Finally, the rising edge of the CKV at t_1 samples the MUX signal and the sampler outputs the FB signal with a propagation delay of τ_{SAM}. When the frequency and the phase are locked, REFA is aligned to the FB signal. However, if the feedback is switched to the sub-sampling mode, the rising edge of the CKV at t_4 cannot sample a high

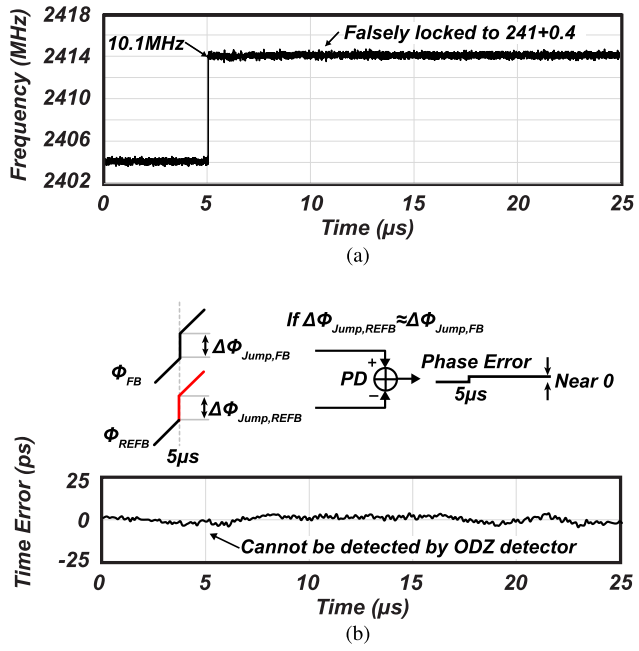


(a)



(b)

Fig. 4. (a) Proposed switching feedback without τ_{FB} delay. (b) Operation of seamless switching feedback with τ_{FB} delay.



(a) (b)

Fig. 5. (a) Frequency disturbance makes the sub-sampling loop lock to an incorrect frequency. (b) Phase error remains very small when a phase disturbance is simultaneously added to REFB.

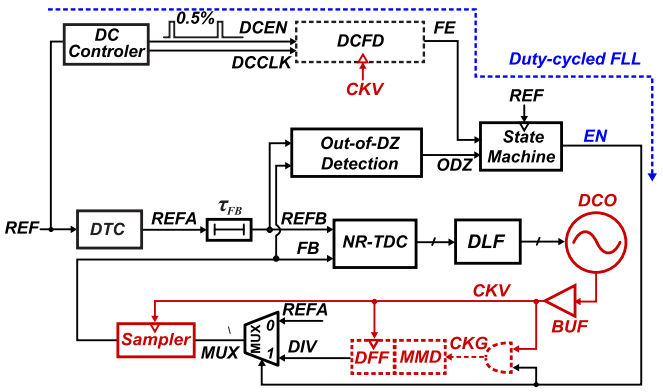


Fig. 6. Proposed DC-FLL.

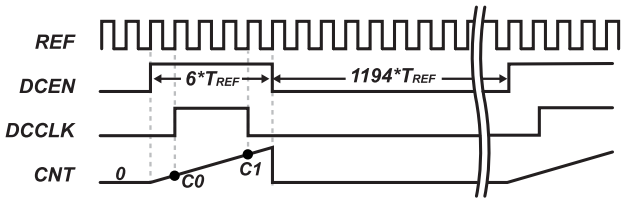


Fig. 7. Operation of DC-FLL.

voltage. Instead, the rising edge of the CKV at t_5 samples a high voltage and generates FB. The incorrect sampling at t_5 will cause an instantaneous phase error at the switching operation. As a consequence, the ODZ detector will trigger the sampling mode.

Fig. 4(b) shows the timing diagram of the proposed switching feedback operation with the additional delay of τ_{FB} between the DTC and the TDC input. In the sampling mode, DIV is synchronized with CKV by the sampler operation with a delay of τ_{SAM}. After the frequency and the phase are locked, FB aligns to REFB. REFB leads REFA because of the additional delay τ_{FB}. Now, if the loop switches from the sampling mode to the sub-sampling mode, the rising edge of CKV at t_4 can sample a high voltage. To maintain a robust switching operation, τ_{FB} should be larger than the total delay of $\tau_{SAM} + \tau_{MUX}$ and the setup time of the sampler $\tau_{Sam,Setup}$. This ensures that a high voltage can be correctly sampled at t_4. However, if τ_{FB} is too large, the rising edge of the CKV at t_4 will sample a high voltage before the edge at t_4. This incorrect sampling will cause an instantaneous phase error. Thus, τ_{FB} should be less than one minimum DCO period $T_{DCO,min}$ across the frequency tuning range of the DPLL plus τ_{MUX}. As discussed above, τ_{FB} should satisfy

$$\tau_{SAM} + \tau_{MUX} + \tau_{Sam,Setup} < \tau_{FB} < T_{DCO,min} + \tau_{MUX}. \quad (1)$$

In this design, τ_{FB} is designed to be around 120 ps in the post-layout simulation. To always satisfy (1) across process–voltage–temperature (PVT) variations, some margins are considered for τ_{FB} to cover the variations in τ_{FB}, τ_{SAM}, and τ_{MUX}. To indicate when the DPLL needs to relock, an ODZ detector is used to monitor the large phase errors introduced by frequency disturbances. When the phase error is larger than the pre-set dead zone, the ODZ signal is generated. A state machine receives this ODZ signal and immediately sets EN to 1 to activate the sampling mode for fast acquisition. After the phase is locked, the DPLL is seamlessly switched back to

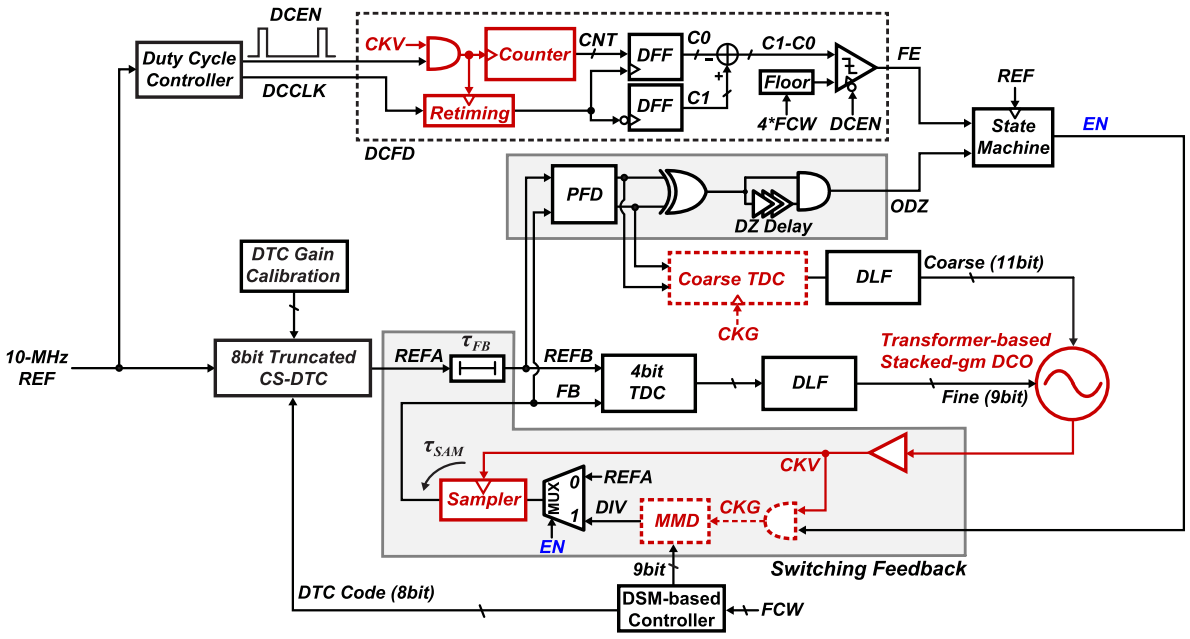


Fig. 8. Proposed ULP fractional-N DPLL with switching feedback and DC-FLL.

the sub-sampling mode to reduce power consumption. In this design, the dead zone delay is set to ± 64 ps. The dead zone time is sufficiently large so as to not be accidentally triggered by the peak jitter of the DPLL, which is $4\sigma_{\text{rms,jitter}} = 4 \times 2.5$ ps, between REFB and FB. In the proposed method, the MMD only works for a fraction of the time, and thus, its power consumption is negligible. This reduces the loop power consumption to only 158 μW using a 10-MHz reference clock, which is comparable with the DCO power consumption. This greatly improves the power-jitter tradeoff, as shown in Table I.

B. Proposed Duty-Cycled FLL

Even though the lock-in range is enhanced by the proposed switching feedback and the ODZ detector, the DPLL may still be trapped in incorrect lock-in ranges. Typically, this is not a concern, because frequency disturbances (e.g., 10.1 MHz) will result in a large timing error between the REFB and the FB, as shown in Fig. 2(b). This large phase error can be detected by the ODZ detector. However, there is an exception, as shown in Fig. 5. A 10.1-MHz frequency will make the sub-sampling PLL lock to an incorrect frequency of 2414 MHz (target frequency: 2404 MHz). This frequency jump will introduce a large phase jump ($\Delta\Phi_{\text{Jump,FB}}$) at the FB. If the phase jump $\Delta\Phi_{\text{Jump,REFB}}$ is introduced at REFB simultaneously and $\Delta\Phi_{\text{Jump,FB}} \approx \Delta\Phi_{\text{Jump,REFB}}$, as shown in Fig. 5(b), $\Delta\Phi_{\text{Jump,FB}} - \Phi_{\text{Jump,REFB}}$ will result in a near-zero phase error. This phenomenon is simulated by applying a frequency error of 10.1 MHz to a DCO running at 2404 MHz while the reference clock is shifted by about -220 ps. The timing error between FB and REFB is very small in Fig. 5(b) and, thus, cannot be detected by the ODZ detector. Hence, the frequency is locked even with the ODZ detector activated. Conventionally, an FLL is used to monitor the frequency error in the background [5] and can be used for detecting this error. However, an FLL consumes a significant amount of power due to its high operating frequency. As discussed above, the chance that the oscillator will be locked to another lock-in range without being detected by the ODZ detector is typically small. Thus, an FLL that works in the background wastes power. Furthermore, there is no need to insert a conventional FLL, which introduces an individual control loop to the DCO. Hence, a duty-cycled frequency detector (DCFD) can be used to switch the feedback from the sub-sampling mode to the sampling mode for frequency locking when the PLL is locked to incorrect frequencies, as shown in Fig. 6. A frequency resolution of at least one reference frequency (10 MHz in this design) is required for the DCFD to detect whether the frequency is locked to an incorrect lock-in range. In this article, a resolution of 2.5 MHz is designed for the DCFD.

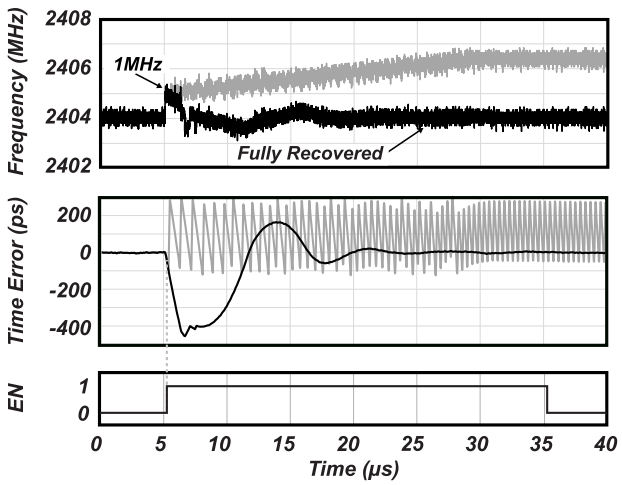
The operation of the DCFD is shown in Fig. 7 and a detailed DCFD schematic is shown in Fig. 8. The dc controller generates a DCEN signal with a pulsewidth of six t_{REF} using an internal counter clocked by the reference clock. It is used to enable the gray-code counter in the DCFD. When the DCEN enables the DCFD, the dc controller produces a DCCLK signal with four t_{REF}. As shown in Fig. 7, all the edges of the DCEN and DCCLK signals are aligned with the rising edge of the reference clock. The rising and falling edges of the DCCLK are used to read the gray-code counter outputs of C0 and C1. If the frequency is the target frequency, C1-C0 will equal the integer part of $4 \times$FCW and the comparator will output a zero. If the absolute frequency error is larger than 2.5 MHz, i.e., one-fourth of the 10-MHz reference frequency, the comparator will produce a one to enable the sampling path. With the duty-cycled operation, the FLL increases the power budget by only 3 μW. The worst case relock time will be 1200×100 ns $= 120$ μs. For some short-packet wireless applications, the long relocking time may lead to power consumption overhead for the wireless transceiver. In such applications,

the duty-cycle time can be reduced. For example, a 5% duty cycle will reduce the relock time to about 12 μs, while the power consumption of the DC-FLL will only increase to 30 μW.

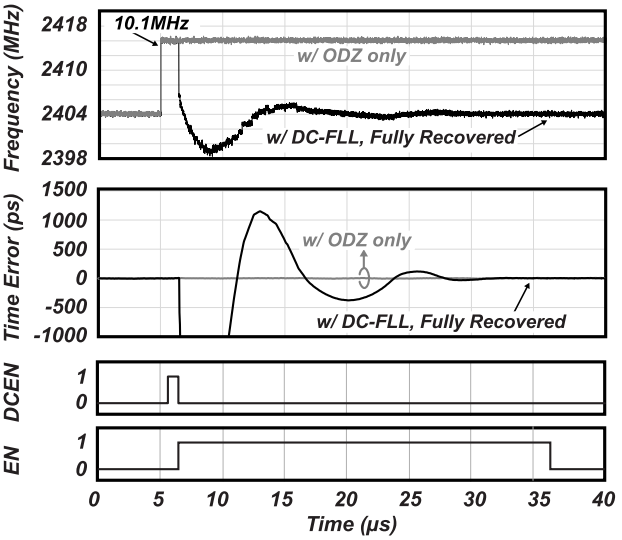
C. System Simulations

A detailed schematic of the proposed ULP fractional-*N* DPLL with switching feedback is shown in Fig. 8. The DSM-based controller is used to achieve fractional frequency synthesis. When the sampling mode is engaged for fast frequency and phase acquisition, the controller produces 9-bit integer phase information for controlling the MMD and 8-bit fractional phase information for controlling the DTC. When the sub-sampling mode is engaged, only the 8-bit fractional phase control signal is used at the DTC input (9-bit integer phase control is dropped). The loop can continue to carry out fractional frequency synthesis due to the automatic phase-warping behavior of the sub-sampling loop in the fractional-*N* mode [20]. A coarse TDC is inserted after the PFD of the ODZ detector to quantize the coarse phase error and assist with coarse phase and frequency locking through the 11-bit coarse bank of the DCO [2]. This significantly improves the phase lock time. To significantly reduce the DCO power consumption, a transformer-based stacked-g_m DCO is implemented. An 8-bit truncated CSDTC is used to improve power efficiency compared with that of the conventional architecture. The DTC gain is calibrated through the LMS algorithm.

Fig. 9 shows the loop simulations of the proposed ULP fractional-*N* DPLL when various frequency disturbances occur. In Fig. 9(a), a 1-MHz frequency disturbance is injected to the DCO. A single sub-sampling loop responds to this disturbance (gray line). For the proposed architecture, the ODZ detector detects the sudden phase jump and enables the sampling mode. After the phase is locked, EN is set to zero and the MMD is turned off while the PLL is still locked without any phase discontinuities. Fig. 9(b) shows the situation demonstrated in Fig. 5, where a 10.1-MHz frequency disturbance is applied to the sub-sampling loop. When the DCEN signal is detected, the DCFD detects the frequency error, sets EN to one, and activates the sampling loop. The frequency is successfully recovered, owing to the sampling loop and the coarse DPLL operations. As in the case shown in Fig. 9(a), the loop is set back to the sub-sampling loop to reduce power consumption without disturbing the phase-locked state. The estimated phase noise contributions of each component of the fractional-*N* DPLL are shown in Fig. 10. The DCO contributes around 50% of the jitter at a 110-kHz loop bandwidth, with the rest caused by noise such as PD noise and DTC noise. An estimated overall jitter of 2.5 ps is achieved with a figure of merit (FOM) of -238.0 dB.



(a)



(b)

Fig. 9. Proposed DPLL response to frequency errors detected by (a) ODZ detector and (b) DC-FLL.

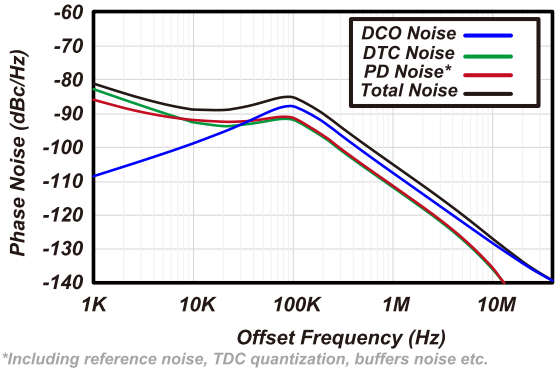


Fig. 10. Simulated phase noise of the proposed fractional-*N* ULP DPLL.

III. Building Blocks of the Proposed ULP DPLL

A. Transformer-Based Stacked-g_m DCO

To lower the power consumption of the oscillator in a PLL, a ring oscillator can be used [11]. However, a ring oscillator has poor phase noise, and thus significantly degrades the PLL phase noise. *LC* oscillators are used to improve the PLL noise performance due to the superior frequency selectivity provided by the *LC* resonator. The conventional CMOS-type *LC* DCO [2], [6], [7] is advantageous for obtaining a large

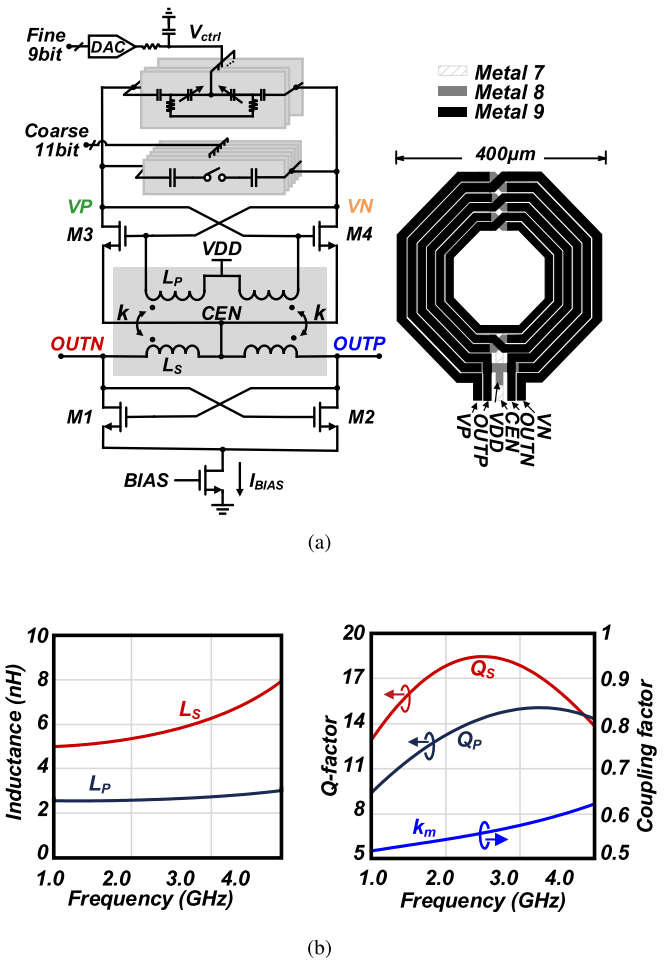


Fig. 11. (a) Proposed transformer-based stacked-g_m DCO. (b) Transformer EM simulation results.

output swing in the current-limited region, in which the output swing V_{AMP} is mainly limited by the tank impedance. Hence, for low current consumption, large cross-coupled pairs are required. However, the introduced parasitic capacitance from the large NMOS and PMOS transistors limits the load inductance and degrades the Q-factor of the tank. Thus, using a conventional CMOS-type DCO in a DPLL that targets a power consumption of lower than 300-μW is extremely difficult. Some transformer-based DCO and current-reuse structures [24]–[26] have been reported to lower power consumption. However, further DCO power reduction is difficult.

A TF-based DCO [14] is proposed to achieve sufficient output amplitude with low power consumption. A transformer-based resonator is treated as a two-port network to build the oscillator. Both the top and bottom cross-coupled pairs use NMOS transistors to provide negative resistances to attain a large g_m from each transistor, as shown in Fig. 11(a). The same dc current is shared by the stacked cross-coupled pairs. The center tap of the primary winding is connected to a voltage source, while the dc current flows into the bottom cross-coupled pair through the center tap of the secondary winding. The coupling of the transformer corresponds to positive feedback between the top and bottom oscillators. The transistor sizes in the top cross-coupled pair are 128 μm/60 nm and the gate length is 256 μm for the bottom cross-coupled NMOS pair. The use of NMOS transistors instead of PMOS transistors relaxes the current requirement, which benefits from its higher mobility. Compared with the low-power class-D voltage-controlled oscillator in [27] and [28], a smaller transistor is adopted here. Therefore, a higher oscillation frequency and a wider frequency tuning range can be achieved.

A higher Q-factor of the load inductance is desired in both windings to provide sufficient load impedance for the two cross-coupled pairs. To mitigate the Q-factor degradation, a 2:4 co-planar transformer structure is adopted. Only one cross section exists in the transformer to connect with the power supply, as shown in Fig. 11(a). In the electromagnetic (EM) simulation shown in Fig. 11(b), the inductances of the primary winding (L_P) and the secondary winding (L_S) are 2.7 and 6.0 nH at 2.4 GHz, respectively. The magnetic coupling coefficient (k_m) is 0.56. The Q-factors of the primary winding (Q_P) and the secondary winding (Q_S) are 14.4 and 18.3, respectively. A frequency tuning range of 2.1–3.1 GHz is available from the cooperation of the primary winding, which has a relatively small inductance, and an 11-bit coarse capacitor bank. The large inductance L_S ensures start-up with a small current. The positive feedback between the coupled windings provides sufficient output amplitude for the DPLL feedback.

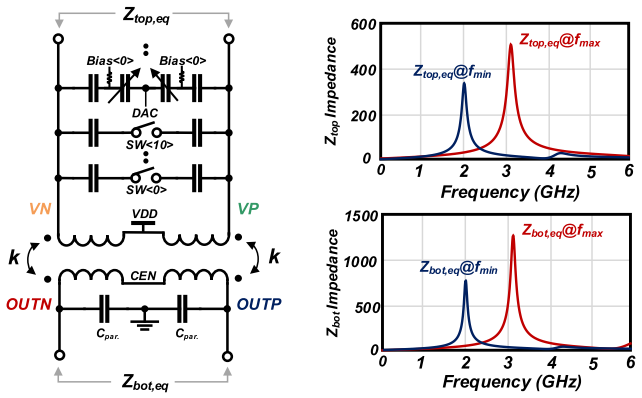
Fig. 12(a) shows the details of the tanks. A linearized varactor bank is implemented for fine-frequency tuning and a switch-controlled-capacitor bank is used for coarse-frequency tuning. As derived in [29], the main resonant frequency ω_L of the tank for $0.5 \leq k_m \leq 1$ can be estimated as

$$\omega_L^2 = \frac{1}{L_P C_P (1 + |k_m|)} \tag{2}$$

where C_P and C_S represent the top and bottom capacitances, respectively. As discussed in [30]–[32], there is another possible resonant frequency ω_H. To avoid multi-oscillation behavior during the DCO operation, the capacitor ratios of C_P and C_S are controlled to ensure that $L_S C_S / L_P C_P$ has a value of 1.1∼2.59, corresponding to a frequency range of 2.1–3.1 GHz. Thus, only a small equivalent tank resistance exists at ω_H [30]. Note that in the ULP DCO design, the transconductance gain is too small to maintain oscillation with low resistance.

The input impedance of the tank Z_{in} has been previously discussed [29]–[31], [33]. The $Z_{\mathrm{top,eq}}$ and $Z_{\mathrm{bot,eq}}$ are the differential input impedances from each side of the transformer (primary and secondary) without loading, and the simulated results of both top and bottom ports are shown in Fig. 12(b).

As shown in Fig. 13, the cross-coupled transistors must provide sufficient transconductance (g_m) to start the oscillation in the transformer. To obtain the minimum required g_m, the parallel resonance model in [29] is applied in the equivalent circuit. The load impedance of M1 and M2 transistor is equivalent to the parallel combination of $Z_{\mathrm{bot.eq}}$ and the transformed load impedance R'_{bot}. In the case of all the transistors (M1∼M4) having the same g_{m0}, the negative resistance can be obtained as $-2/g_{m0}$. According to the designed value of $L_S C_S / L_P C_P$,



(a) (b)

Fig. 12. (a) Transformer with capacitor banks. (b) Simulated input impedance from top side and bottom side.

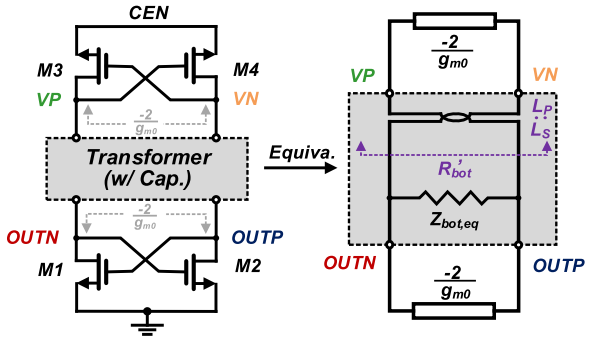


Fig. 13. Equivalent circuit of the proposed DCO.

the load impedance transfer ratio can be expressed as the turn ratio $L_P : L_S$ [29]. Meanwhile, R'_{bot} can be recast as $L_S/(-g_{m,M4}L_P)$ and $Z_{\text{bot,eq}} = \omega_L L_S Q_S(1+k)^2/(1+Q_S/Q_P) \approx \omega_L L_S Q_S$. Thus, the start-up condition is given as

$$g_{m0} > \frac{2}{(1+\frac{L_P}{L_S})\omega_L L_S Q_S}. \tag{3}$$

Note that both the top and bottom cross-coupled pairs are implemented with NMOS transistors as the active devices, which can provide higher g_{m0} than that provided by the PMOS transistors of the same size. To reduce the total power consumption of the PLL feedback path, the output amplitude of the oscillator should be sufficiently high to alleviate the power demand of the buffers. In the transformer-based DCO, the transformer-based resonator can provide a voltage gain of above $k_m N$, as demonstrated in [30]. According to the value of $L_S C_S / L_P C_P$, the input impedance of the tank $Z_{\text{top,eq}}$ can be simplified [29] as

$$Z_{\text{top,eq}} = \omega_L L_P Q_P \frac{(1+k_m)^2}{1+Q_P/Q_S}. \tag{4}$$

The differential output amplitude V_{AMP} of the OUTP and OUTN nodes can be estimated as

$$V_{\text{AMP}} \approx \frac{4}{\pi} I_{\text{BIAS}} \frac{Z_{\text{top},\omega_L}}{2} k_m N + \frac{4}{\pi} I_{\text{BIAS}} \omega_L \frac{L_S}{2} Q_S. \tag{5}$$

The impedance at the secondary port is estimated as $\omega_S(L_S/2)Q_S$ from the values of $L_P C_P / L_S C_S$ of 0.91 to 0.4 across the frequency tuning range [29]. For $k_m = 0.56$, V_{AMP} can be simplified using the above-mentioned parameters

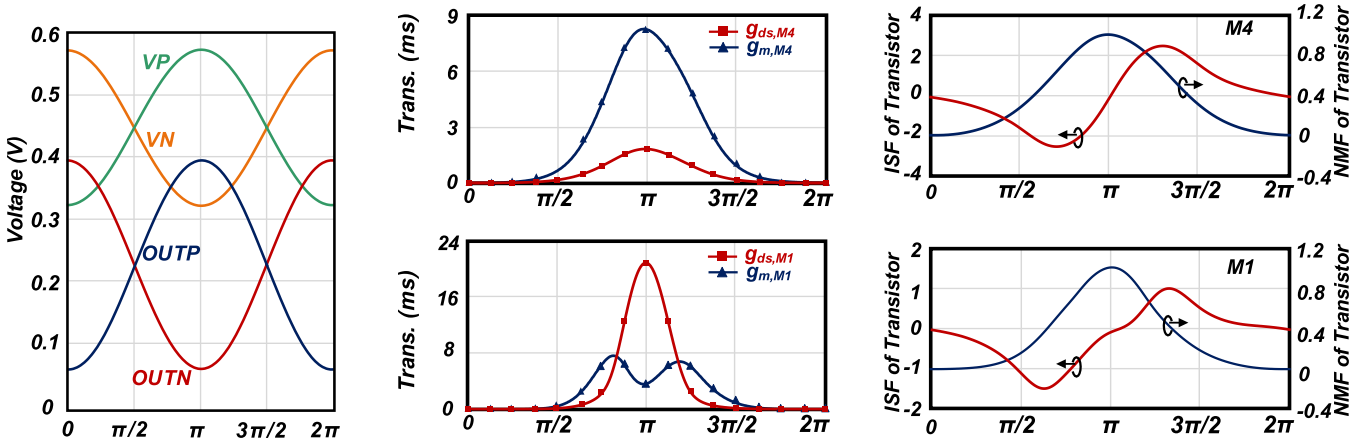
$$V_{\text{AMP}} \approx \frac{4}{\pi} I_{\text{BIAS}} \omega_L \frac{L_P}{2} Q_P \left(k_m^2 N + k_m N + \frac{L_S Q_S}{L_P Q_P} \right) \tag{6}$$

Fig. 14(a) shows the simulated transient waveform. With a 238-μA dc current, a 340-mV V_{amp} can be obtained in the post-layout simulation. The output amplitude is linearly proportional to the bias current for currents lower than 250 μA. The proposed DCO enters the voltage-limited region with a larger current. The proposed transformer-based stacked-g_m DCO guarantees oscillation under the process and temperature variations with 238-μA current consumption. Fig. 14(b) shows the simulated transconductance and channel conductance of the active devices. The simulated NMF and effective ISF of transistor M1 and the NMF of transistor M4 are shown in Fig. 14(c). Compared to the conventional class-B DCO, the effective noise power of the active devices is close to that of conventional designs. The simulated phase noise is -108 dBc/Hz at 1 MHz at a very low power consumption of 107 μW. The phase noise contribution is mainly from the tail transistor and can be reduced by replacing this transistor with a tunable resistor [34].

The proposed DCO requires a low supply voltage of 0.45 V to maintain the high-power efficiency of the DCO core. If the whole system requires a standard supply voltage, i.e., 1 V for 65-nm CMOS, the on-chip switch-capacitor (SC) dc–dc converter can be used to convert 1 V into 0.45 V for the proposed DCO supply. The efficiency of this converter can be more than 80%, as reported in [35]. If an additional linear regulator is required to improve the power supply rejection ratio, a PMOS transistor can be used as the current source (pass device) instead of the NMOS tail-current source, as shown in Fig. 11(a). A voltage of 0.55 V is sufficient for the regulator input; it adds an additional power consumption of (0.55–0.45 V) $\times$ 238 μA $\approx$ 24 μW. An SC dc–dc converter can convert 1 V into 0.55 V for the linear regulator input. Assuming 85% efficiency, the additional power consumption is (107 μW + 28 μW) $\times$ 15% = 20μW. Overall, the power consumption will increase from 155 μW to 107 μW if a 1-V supply and a linear regulator are required.

B. Highly Efficient Truncated Constant-Slope DTC

Recently, DTCs are widely explored in the fractional-N PLL designs, because they can be used into transforming any integer-N PLL to a fractional-N one [3], [7], [12], [19]–[21], [36]. This greatly reduces the design effort for a low-power fractional-N PLL and achieves promising performance. DTCs can also be used for realizing ultralow-jitter applications [19], [20], [36]. A conventional DTC is realized by placing a capacitor digital-to-analog converter (CDAC) between two inverters [3], [20], [36]. The first inverter and the CDAC are used to generate ramps with different slew rates, and the second inverter is used to detect when the ramps cross a given threshold. However, when different ramps are applied, the second inverter will produce different propagation delays. This effect greatly limits the



(a) (b) (c)

Fig. 14. (a) Simulated transient voltage waveforms of cross-coupled pair. (b) Simulated transconductance and channel conductance of M1 and M4 transistors. (c) Simulated ISF and NMF of M1 and M4 transistors in the proposed DCO.

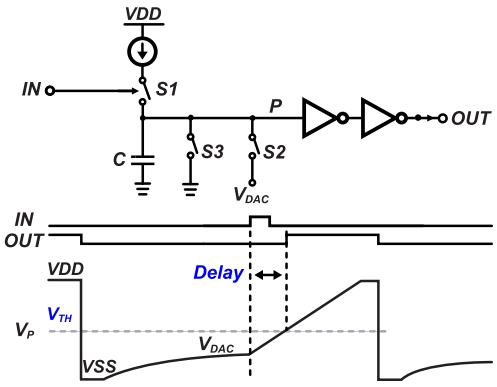
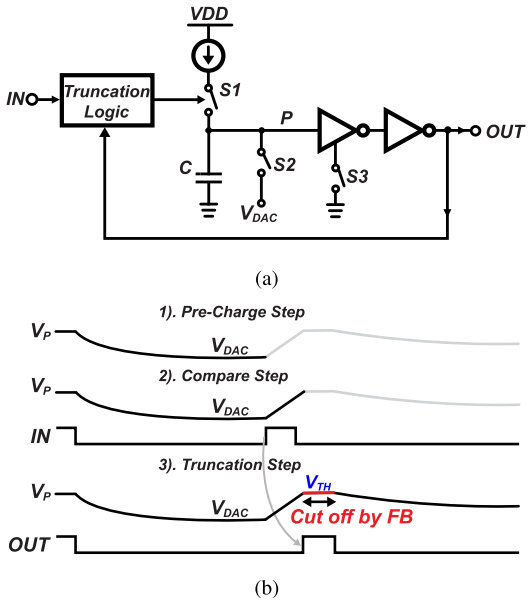


Fig. 15. Conventional CS DTC.



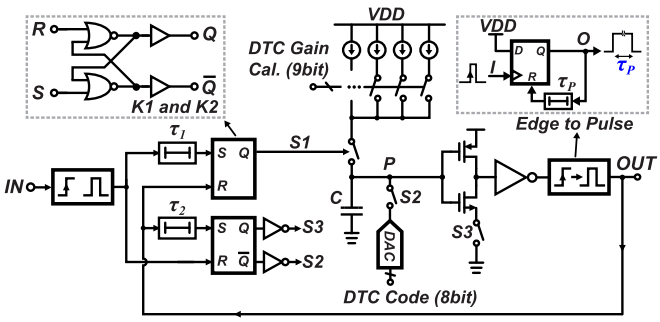
(a)

(b)

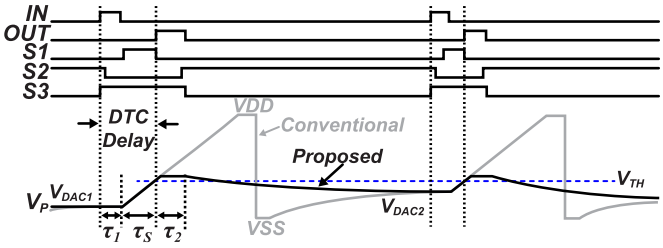
Fig. 16. Concept of (a) truncated CS DTC and (b) operation.

linearity performance of a DTC, as analyzed in [37]. The constant-slope charging method [37] is proposed to acquire a variable delay by changing the starting voltage of the ramp instead of changing the slew rate at the inverter input, as shown in Fig. 15. A DAC is used to generate the variable starting voltage by charging capacitor C (pre-charge step). Then, a ramp is generated by charging C using a current source from V_{DAC} to VDD. The delay is generated when the ramp crosses the inverter threshold V_{TH} (comparison step). Because all the ramps have the same shape in the comparator input window, this mitigates the linearity degradation from the inverter due to the code-dependent propagation delay. The CSDTC achieves good linearity with good resolution. However, the DAC needs to be fully settled to avoid linearity degradation in the starting voltage generation step. Hence, the DAC dominates the power consumption when a CSDTC is running at a high frequency. An isolated CSDTC [2] is proposed to relax the power contribution by isolating the pre-charge step and the comparison step using a dc-cut switch and an auto-zero switch. In this method, the DAC only needs to charge a small dc-cut capacitor to acquire the starting voltages. This leads to a large power reduction at a frequency of 52 MHz. However, the additional switching introduces kT/C noise, which degrades jitter performance.

In the proposed fractional-N DPLL, reference scaling is applied to the whole architecture to further reduce system power consumption. This leads to a long pre-charge time, allowing the DAC to spend more time pre-charging C. Thus, the DAC power consumption becomes less dominant. However, the current of the current source and capacitor C cannot be scaled due to the jitter requirement of the DTC [2]. Hence, the power from the current source will become dominant at a low reference clock. In this article, a CSDTC with current truncation logic is proposed to minimize the power contribution from the current source, as shown in Fig. 16(a). The concept of its operation is shown in Fig. 16(b). In the pre-charge step, the positive plate of C is discharged to DAC voltage V_{DAC}, which reuses the charge stored on C from



(a)



(b)

Fig. 17. Schematic of (a) proposed truncated CS DTC and (b) detailed operation.

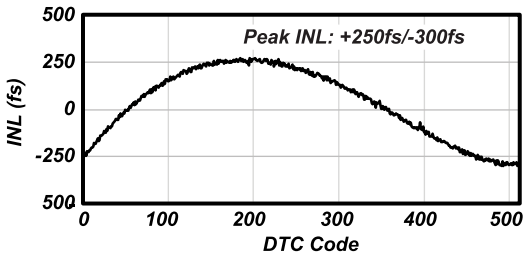


Fig. 18. INL of the proposed DTC in the post-layout simulation.

the previous cycle operation. S3 is turned off during the pre-charge step to prevent current leakage from the inverter during the discharging process. The input (IN) triggers switch S1 to charge C to acquire a ramp, and S3 is turned on to engage the inverter comparator. Once the ramp reaches the threshold voltage of the inverter, it produces an output (OUT). Then, OUT is fed back to the truncation logic to stop the current source from charging. $V_{\rm DAC}$ is held for a short time to turn off S3 and turn on S2 to start discharging C to obtain a new $V_{\rm DAC}$ for operation in the next cycle. In a conventional architecture, charging C to VDD does not contribute to delay generation; it only wastes energy. This is avoided by the proposed truncation logic, which greatly improves the power efficiency of the current source by almost 58% in simulations. Furthermore, the truncation operation well defines the ending point of the previous cycle and significantly extends the pre-charge time, which can further reduce the DAC power consumption, as shown in Fig. 17(b). Fig. 17(a) shows the full implementation of the proposed truncated CSDTC. The truncation logic is realized by two SR latches, and the timing is controlled by two delays. The delay τ_1 ensures a time margin for S3 to open before the ramp arrives, and τ_1 defines the

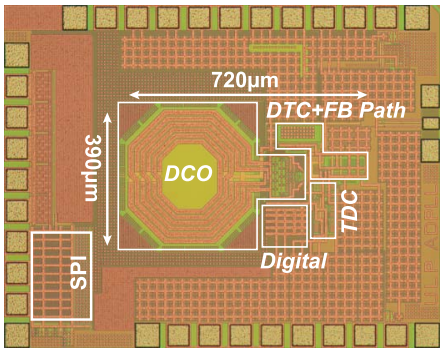


Fig. 19. Photograph of prototype chip.

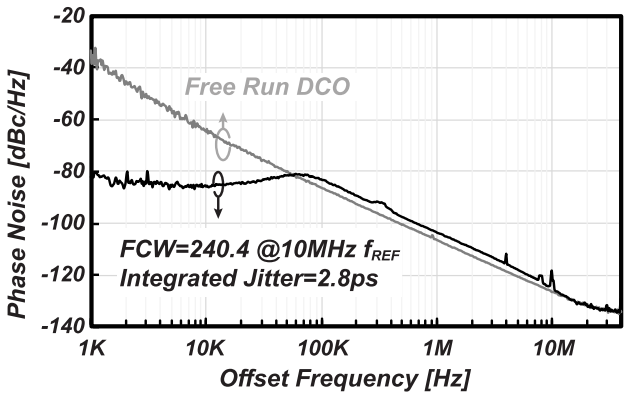


Fig. 20. Measured phase noise of a free running DCO and DPLL in the fractional-*N* mode.

pulsewidth of OUT, as shown in Fig. 17(b). A reset-type DFF is used in realizing the edge-to-pulse conversion to extend the pulsewidth for the next bock. During DPLL operation, the DTC gain is calibrated through a 9-bit current source. Fig. 17(b) compares the operation of a conventional CSDTC and the proposed CSDTC. The proposed CSDTC achieves a much smaller voltage swing at node P. The ramp during τ_S is 100% utilized for delay generation. There is almost no wasted energy during CSDTC operation. The linearity of the proposed CSDTC is mainly degraded by three sources: the DAC linearity, the charge sharing of the switching operations, and the ON/OFF resistance of the switches. These can be optimized to achieve excellent linearity, as explained in [37]. The simulated INL of the proposed CSDTC is shown in Fig. 18. The CSDTC achieves a peak INL of +250 fs/−300 fs with a resolution of 1.9 ps/LSB at a 10-MHz clock rate.

IV. Measurement

A prototype of the proposed ULP fractional-*N* DPLL was implemented in the standard TSMC 65-nm CMOS technology. A photograph of the chip is shown in Fig. 19. The DPLL occupies an area of 0.25 mm^2. Fig. 20 shows the measured phase noise of the free-running oscillator and the DPLL working in the fractional mode. The free-running oscillator was measured at a frequency of 2.46 GHz. It draws an extremely low current of 238 μA from a 0.45-V supply. The phase noise is −107 dBc/Hz at a 1-MHz offset frequency and −128 dBc/Hz

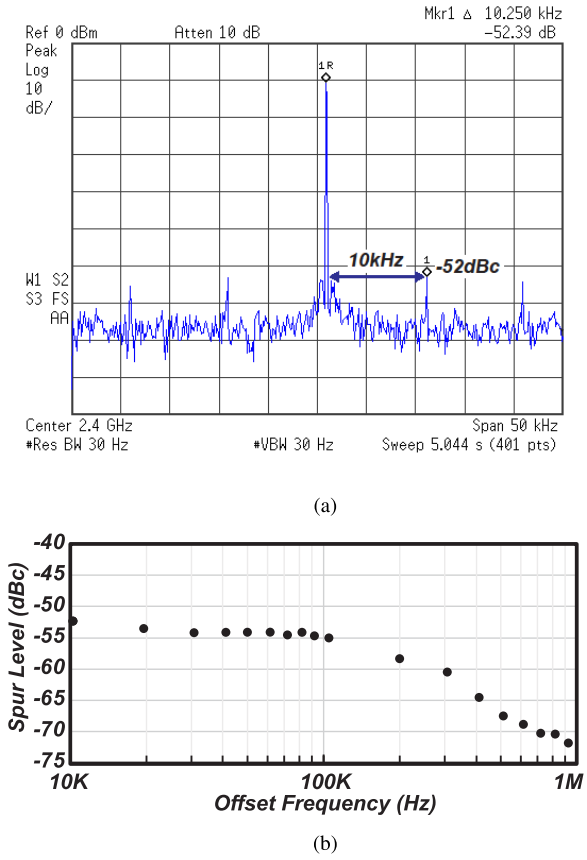


Fig. 21. (a) Measured worst case in-band fractional spur. (b) Measured fractional spur versus offset frequency.

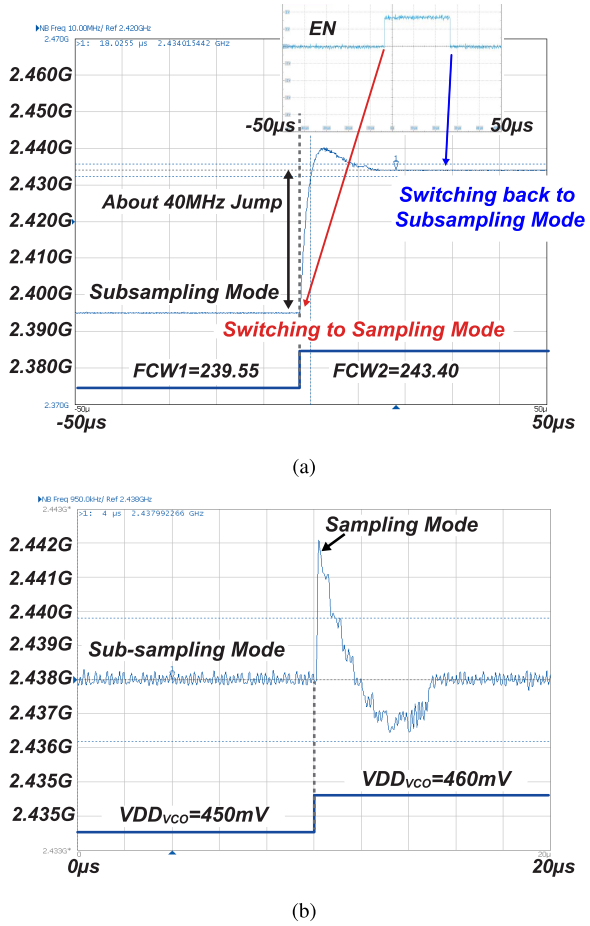


Fig. 22. (a) Measured relock time when a large frequency jump is applied. (b) Measured relock time when a small frequency jump is applied.

at 10 MHz. The measured frequency tuning range is 2.1–3.1 GHz, which corresponds to a 38% tuning range. When the loop was closed, it showed a −86 dBc/Hz in-band phase noise at a 10-kHz offset frequency. The phase noise at a 1-MHz offset after the loop was closed was −105 dBc/Hz, which is 2 dB higher than the free-running DCO phase noise at 1 MHz. This is due to the phase noise from the loop, which has less filtering from a first-order digital loop filter; this phase noise is added to the DCO phase noise. The integrated jitter from 1 kHz to 40 MHz was 2.8 ps when using an FCW of 240.4. The worst case in-band fractional spur was measured at an FCW of 240.001, as shown in Fig. 21(a). The first fractional spur occurs at around 10 kHz with an energy of −52.4 dB, which is lower than that of the main output signal. Fig. 21(b) shows the measured level of the fractional spurs across the offset frequencies.

To evaluate the operation of the switching feedback, a time-domain measurement of the DCO output frequency was conducted; the results are shown in Fig. 22(a). The measurement was done using a Keysight E5052B signal source analyzer. The DPLL was initially operating in the sub-sampling mode using FCW1 = 239.55. This corresponds to a center frequency of 2395.5 MHz at the DCO output. Then, a step signal was manually added to the FCW through an SPI controller. The new FCW was FCW2 = 243.40, which corresponds to a target settling frequency of 2434 MHz. Owing to the difference between the fractional control parts, i.e., 0.55 and 0.40, the DTC introduced instantaneous phase errors between the REFA/REFB and the FB at the inputs of the TDC. When the phase error was larger than the dead zone of the ODZ detector, EN was set to 1 and the sub-sampling mode was changed to sampling mode to recover the frequency and the phase. As shown in Fig. 22(a), the loop was initially locked to 2395.5 MHz in the sub-sampling mode. After the FCW step was applied, the loop immediately switched to sampling mode and quickly settled itself to the target frequency of 2434 MHz (within 18 μs or 180 reference cycles). After the PLL had settled, the EN signal was set to 0 to reduce power consumption. In Fig. 22(b), a step signal of 10 mV is added to the DCO supply. This voltage step introduced a small frequency disturbance at the DCO output. The small frequency error is fully recovered under 6 μs owing to the switching feedback.

The power consumption of each building block is shown in Fig. 23. Fig. 23 (left) shows the power consumption breakdown of the DPLL excluding the power from the DCO. The DCO draws current from a 0.45-V supply voltage and the rest of the DPLL blocks use 0.85 V. The power consumption breakdown of a traditional architecture is based on post-layout simulations. The proposed switching feedback path mitigates the large power consumption from the MMD, which leads to

TABLE II
COMPARISON OF THE STATE-OF-THE-ART LOW-POWER FRACTIONAL-N DPLLS

	This Work	JSSC18 [39]	ISSCC17 [7]	ISSCC14 [6]	JSSC18 [2]	JSSC18 [2]
CMOS Process	TSMC 65nm	TSMC 28nm	40nm	40nm	65nm	65nm
Osc. Architecture	LC-Osc.	LC-Osc.	LC-Osc.	LC-Osc.	LC-Osc.	LC-Osc.
Reference (MHz)	10	40	N/A	32	52	26
Frequency (GHz)	2.1-3.1	2.05 - 2.55	1.8-2.5	2.1-2.7	2.0-2.8	2.0-2.8
Power (μW)	**265**	1600	673	860	980	653
Power Eff. (μW/GHz)	**107**	696	312	358	409	272
Jitter (ps)	2.8	0.86	1.98	1.71	0.53	1.00
Worst-case Spur (dBc)	-52.4	-57.0	-56.0	-37.0	-56.0	-52.0
FOM (dB)	-236.8	-239.3	-235.8	-236.0	-245.6	-241.9
Area (mm^2)	0.25	0.33	0.18	0.20	0.23	0.23

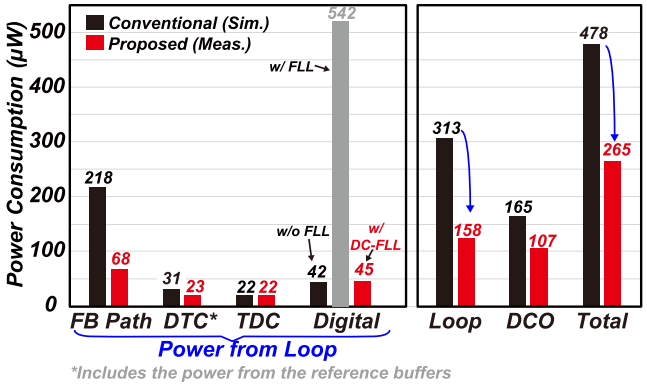


Fig. 23. Measured power consumption compared with that of conventional architecture in the post-layout simulation.

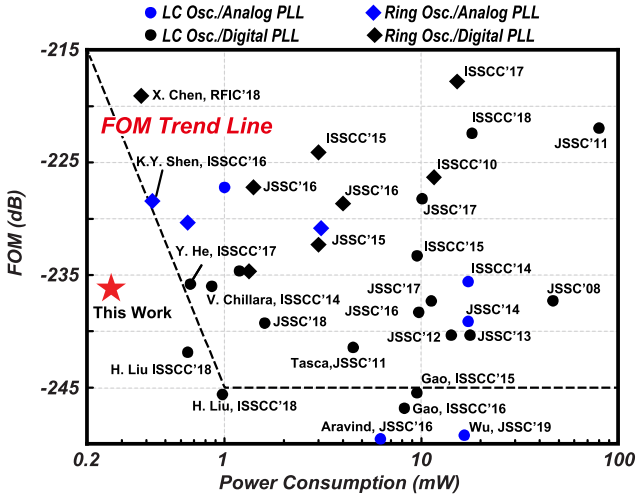


Fig. 24. FOM comparison with the state-of-the-art fractional-N PLLs.

a power consumption reduction of at least 150 μW. With the compact layout of the DCO buffer and sampler, the introduced parasitic capacitance/resistance is negligible, which reduces the power consumed by the DCO buffer. The proposed feedback path contributes only a 68-μW power consumption overhead to the whole DPLL. The proposed CSDTC reduces power consumption by 26% compared with that of a conventional CSDTC. With duty-cycled operation, the frequency detector adds only 3 μW of additional power consumption to the loop. The loop power consumption decreased from 313 μW to only 158 μW. The DCO power decreased from 165 μW using a conventional CMOS-type DCO to 107 μW using the proposed transformer-based stacked-g_m architecture. Overall, the power from the loop and the power consumed by the DCO have a good balance; they contribute almost equal jitter to the PLL output, ensuring a good power-jitter tradeoff. The DPLL achieves an FOM of -237 dB.

Table II shows a comparison with the state-of-the-art fractional-N DPLLs. The proposed DPLL achieves the lowest power consumption, which is 2.5 times lower than that for a previously published ULP fractional-N DPLL [2]. It also achieves a good jitter number, making it suitable for applications such as Bluetooth Low Energy, Zigbee, and other low-power SoCs. Fig. 24 shows a comparison with recent fractional-N PLLs (both digital and analog). As shown, ring-oscillator-based PLLs can realize very low power consumption, but their poor oscillator phase noise results in poor FOM performance. LC-oscillator-based PLLs obtain a decent FOM due to their good oscillator phase and high power. This article sets a new standard for the power consumption of LC-oscillator-based fractional-N DPLLs and simultaneously achieves a good FOM.

V. CONCLUSION

In this article, a 265-μW fractional-N DPLL with seamless sampling/sub-sampling feedback was proposed. It combines the advantages of the sampling loop and the sub-sampling

loop to achieve robust phase and frequency acquisition under frequency disturbances and low-power operation. During the switching process from the sampling to the sub-sampling loop, the phase remains locked without any discontinuities. The ODZ detector and the DCFD work in conjunction with the switching feedback, which monitors frequency disturbances and ensures that the DCO is always locked to the correct frequency. The transformer-based stacked-g_m DCO boosts R_P to help reduce the required current while maintaining robust start-up and a wide tuning range. The truncated operation helps improve the efficiency of the current source to nearly 100% for the delay generation of the CSDTC. With these techniques, the DPLL can scale its power consumption with the scaling of the reference clock. A prototype of the DPLL achieved an unprecedented low power consumption of 265 μW and a jitter of 2.8 ps, which corresponds to an FOM of -237 dB.

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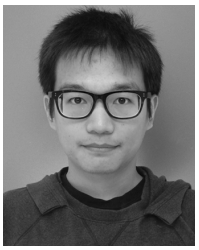

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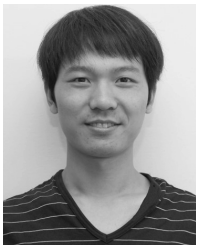

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