A 4-GHz Low-Power, Multi-User Approximate Zero-IF FM-UWB Transceiver for IoT

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***Abstract*— This paper presents a 4-GHz FM ultra-wideband (UWB) transceiver designed for the Internet of Things and body area network applications. Robustness to interferers and low power spectral density allow FM-UWB to coexist with narrowband radios, while large signal bandwidth strongly relaxes constraints on the frequency synthesis blocks enabling the full integration of the radio at low power. The transceiver, integrated with a 65-nm standard CMOS technology, consists of a transmitter and two receivers that provide two modes of operation. The transmitter consumes 575 μW while transmitting a 100-kb/s signal at 4 GHz at an output power of −11.4 dBm. A single RF IO pad is used and the fully integrated matching network is shared among the transmitter and the receivers. The low-power receiver consumes 267 μW and provides a single communication channel at 100 kb/s in the 4-GHz band, with a −57-dBm sensitivity. The second receiver provides a better performance and takes full advantage of the FM-UWB features, as it implements wireless communication with up to four parallel channels sharing the same RF band. It consumes 550 μW and provides −68-dBm sensitivity at 100 kb/s per channel. The FM-UWB architecture can tolerate a very large reference frequency offset of up to ±8000 ppm. This unique feature potentially allows for a quartz-free synthesizer, resulting in a radio with no off-chip components.**

***Index Terms*— FM ultra-wideband (UWB), FSK, fully integrated, Internet of Things (IoT), low power, multi-user (MU), transceiver, wideband, wireless.**

I. Introduction

THE increasing number of connected devices, primarily driven by the Internet of Things, results in increased wireless traffic eventually leading to congestion in commonly used bands. This calls for alternative solutions capable of coexisting with conventional radios used today. From that perspective, an interesting alternative for standard narrowband solutions, such as Bluetooth, ZigBee, IEEE 802.15.6, and others, is FM ultra-wideband (UWB). The fact that the signal power is spread over a very wide frequency band results in low power spectral density (PSD), which allows it to coexist with conventional radios without affecting their link quality. At the same time, the low PSD makes the FM-UWB signal less detectable for potential attackers, allowing for a more secure wireless connection. Finally, the FM-UWB is inherently robust against narrowband interferers and is, therefore, capable of maintaining a reliable link even in the presence of strong narrowband signals.

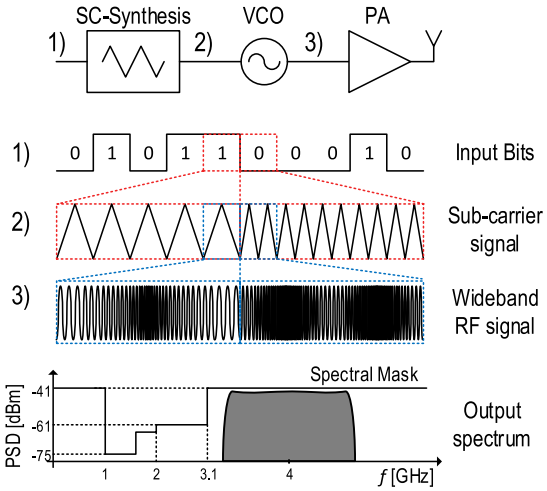

Fig. 1. FM-UWB modulation principle and signal at different points in the circuit. 1) input bits. 2) SC signal. 3) VCO output.

The transceiver proposed in this paper is targeting short-range communication systems, such as the one described in [1], where many sensor nodes are distributed on a prosthetic arm and communicate wirelessly in order to transfer the information from the sensors to the patient, allowing him to recover a sensation of touch. Such a system must be robust to interfering radios operating in its vicinity and should provide a reliable and secure link at all times, making the FM-UWB a perfect candidate. Since the targeted distance between the nodes can vary from several centimeters up to a meter, sensitivity is not a major limitation and −50 dBm is generally sufficient. The emphasis is on lowering the power consumption below 1 mW in order to minimize the burden on the battery of the prosthesis. Finally, in order to provide unobstructed use, the system must be able to operate next to commercial devices, typically transmitting around 2.4 GHz at an output power on the order of 0 dBm.

Other UWB techniques, such as impulse radio (IR) UWB, can be found in the literature. IR-UWB radios usually target higher data rates [2], but also consume power ranging from 10 to 100 mW and above. The transceiver from [3] provides a data rate of 500 Mb/s while consuming 13.3 mW, effectively achieving energy efficiency of 26 pJ/b. Low power solutions exist, targeting lower data rates, in the order of 1 Mb/s,

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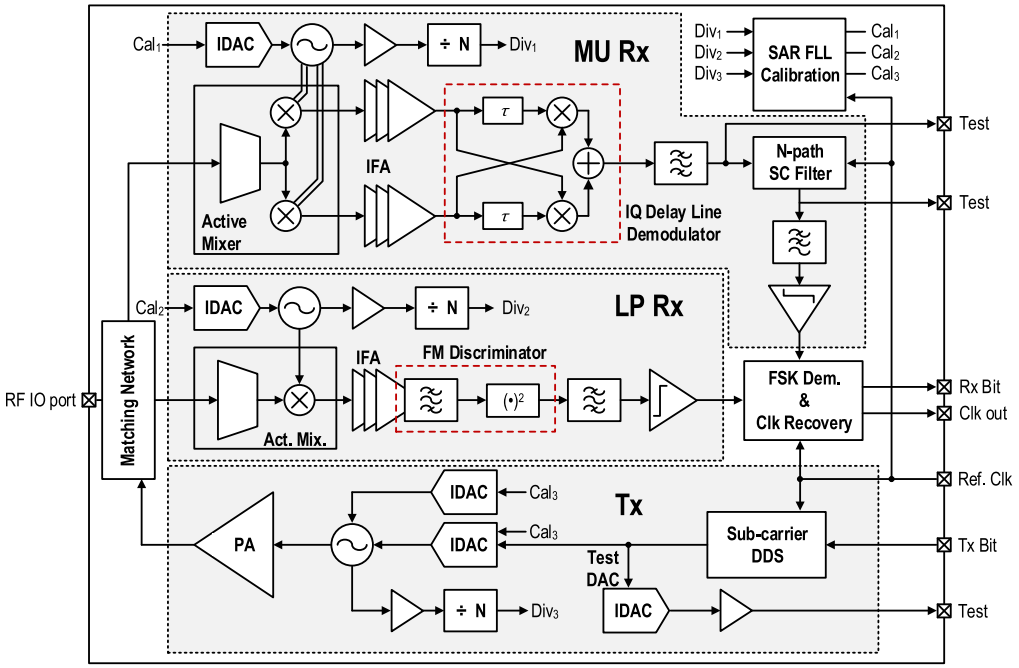

Fig. 2. FM-UWB transceiver block diagram.

and consuming power below 2 mW [4]. Although they can be used for communication, they are commonly used for ranging applications [5]. In addition, precise timing generation is required to provide proper detection of nanosecond pulses (alternatively, more complex modulation techniques can be used to loosen constraints on frequency precision [4]). Compared to IR-UWB solutions, FM-UWB can be seen as a low complexity approach that provides higher potential for miniaturization and peak power reduction. Although IR-UWB is generally a more energy-efficient solution, low peak power consumption provided by the FM-UWB is particularly useful in battery-powered applications, where a high current pulse might reduce the battery lifetime.

The principle of FM-UWB signal generation is presented in Fig. 1. It can essentially be seen as an analog implementation of a spread spectrum technique [6], where the signal is generated in two steps. Input data are first modulated onto a low modulation index, triangular FSK sub-carrier (SC). This SC signal then drives the voltage-controlled oscillator (VCO) and, in this way, creates the large modulation index RF signal. Owing to the triangular driving signal, the resulting output spectrum will be ideally broad and flat with a steep spectral roll-off. The large bandwidth provides robustness against frequency selective fading and interference [7], [8]. In addition, it also relaxes the constraints on the frequency synthesis blocks, allowing elimination of the power-hungry PLLs, and hence reduction of the transceiver power consumption. The FM-UWB also provides multi-user (MU) capability [6]. Different transmitters can share the same RF band by using different SC frequencies. Assuming that the FM demodulator on the receiver side has sufficient linearity in FM–AM conversion, different SC channels will be distinguishable. An MU approach allows an increase in network throughput, decreases latency, and generally provides more potential for protocol optimization.

This paper is organized as follows. The transceiver architecture, including the basic principles, is described in Section II. The implementation details of the transmitter and the two receivers are given in Section III. Section IV reports the measured results and provides comparison of the proposed transceiver with the state of the art. Finally, the concluding remarks are given in Section V.

II. Transceiver Architecture

The wide bandwidth of the FM-UWB signal can be exploited to reduce the power consumption of the transceiver. A power-hungry, precise frequency synthesizer is not needed and is replaced by a free-running ring oscillator that is periodically calibrated. The block diagram of the proposed transceiver is shown in Fig. 2. Similar to [9], the transmitter uses a ring oscillator for the RF signal generation, and thanks to the 500-MHz bandwidth, phase noise and frequency stability have very little impact on the link quality. The SC signal is generated digitally and used to control a digital-to-analog (DAC) converter that drives the oscillator. Calibration is done using a frequency-locked loop (FLL), using a similar principle as described in [9]. Considering that the environmental changes are slow (e.g., temperature), calibration typically needs to be done once every few hours and should only cause a negligible power overhead.

In order to eliminate the need for external components, the output matching network is fully integrated, and there is no need for external passive components. In addition, the transmitter and both receivers share a single RF IO pad. The matching network is made configurable so that it provides

good efficiency in the transmit mode and low reflection coefficient in the receive mode. This new feature was not present in the previous implementations of FM-UWB radios [9], [10], which required an external switch. In addition to reducing the size and cost of the system, there are no additional losses introduced by external components.

On the receiver side, low-power ring oscillators are used to perform down-conversion of the input FM-UWB signal. This approach was first proposed for the narrowband radios in [11] and was referred to as the "Uncertain IF" receiver because of the large variation of the LO. It was later adapted to FM-UWB in [12], where it was denoted as the "Approximate zero-IF" receiver since the direct down-conversion topology was used. The benefit of this approach is moving the gain stages and the demodulator from RF to IF, where the same gain can be achieved at an order of magnitude lower power consumption. The drawback is the impact on the noise figure of the receiver. However, since the proposed transceiver is targeting short-range communications, noise performance can be traded for lower power consumption. The LNA is omitted from the receiver and instead, an active mixer with a matching network is used as the first stage that converts the input signal directly to dc. It is then amplified by the wideband IF amplifiers before demodulation. In order to account for the frequency offset between the transmitter and the receiver, these amplifiers are designed to provide 300-MHz bandwidth, instead of 250 MHz that would be sufficient assuming an ideal LO was available (i.e., for a downconverted FM-UWB signal with an RF bandwidth of 500 MHz).

Two receivers are implemented on the same die and provide two different modes of operation. The MU receiver targets a better performance and provides multiple SC channels. This means that several FM-UWB signals can be transmitted in the same RF band simultaneously, allowing to reduce network latency and optimize communication protocols. However, to provide the good FM–AM linearity that is needed for MU communication, the MU receiver uses quadrature down-conversion and a baseband delay-line demodulator [12]. The low-power (LP) receiver exploits the properties of FM-UWB to simplify the receiver architecture. In direct down-conversion receivers, quadrature down-conversion is usually necessary to allow for correct demodulation. In the case of FM-UWB, even if only a single down-conversion branch is used, the signal can still be demodulated correctly. However, in the process of demodulation, the SC frequency doubles compared to the one that was transmitted. This effect is shown in Fig. 3, which shows the principle of operation for both MU and LP demodulators. The LP demodulator is based on a frequency discriminator that converts the input FM signal into an AM signal. The high-frequency component is then removed using an envelope detector, which finally gives the double-frequency SC signal at its output. The principle of operation of the LP receiver is further explained in the Appendix using a simplified mathematical model.

Fig. 4 shows the SC frequency plan for both receivers. The intended SC band for the MU receiver spans from 1.15 to 2.3 MHz. This provides enough bandwidth for four SC channels, each of them using a 100-kb/s, non-filtered FSK

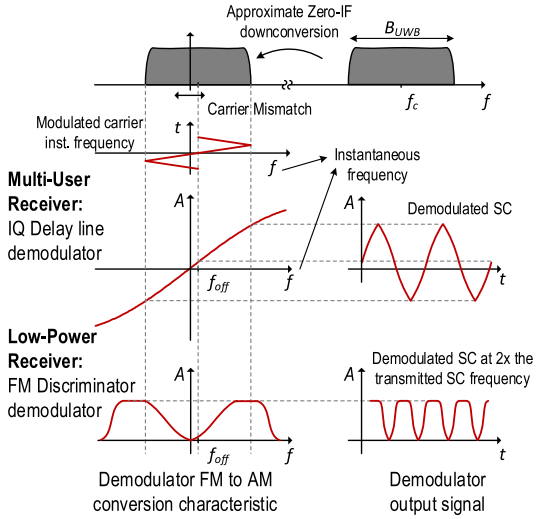

Fig. 3. FM-UWB demodulation principle.

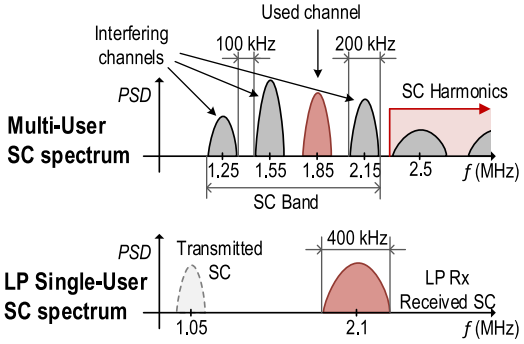

Fig. 4. FM-UWB SC frequency plan.

signal with a modulation index of 1 and requiring 200-kHz bandwidth. A 100-kHz spacing is inserted between the sub-channels in order to leave some room for channel filtering and limit the interference due to leakage of the adjacent channel [quantified by adjacent channel leakage ratio or (ACLR)]. A limiting factor on the number of channels is harmonics that always appear in the FM-UWB SC signal [6], [8] that constrains the useful band to one octave. The number of channels can be increased by either moving to higher SC frequencies or by decreasing the data rate per channel. In this case, pulse shaping was not used in order to simplify the transceiver, but it could be implemented to further lower the interference among different channels (by minimizing ACLR), which can limit the tolerable power difference between adjacent sub-channels.

Due to the high non-linearity of the FM–AM conversion of the LP receiver, only one SC signal can be demodulated at a time. If multiple FM-UWB signals are present, a capture effect will take place and the strongest channel will suppress all others [13]. In this case, the intended transmitted SC frequency is 1.05 MHz, meaning that the FSK demodulator on the receiver side should be centered at 2.1 MHz.

The wide RF bandwidth and low SC frequency place loose constraints on the precision of the frequency reference needed. As an example, consider a 2000-ppm frequency offset. At 2-MHz SC frequency, this translates into 4-kHz offset, which is relatively small compared to the 200-kHz channel

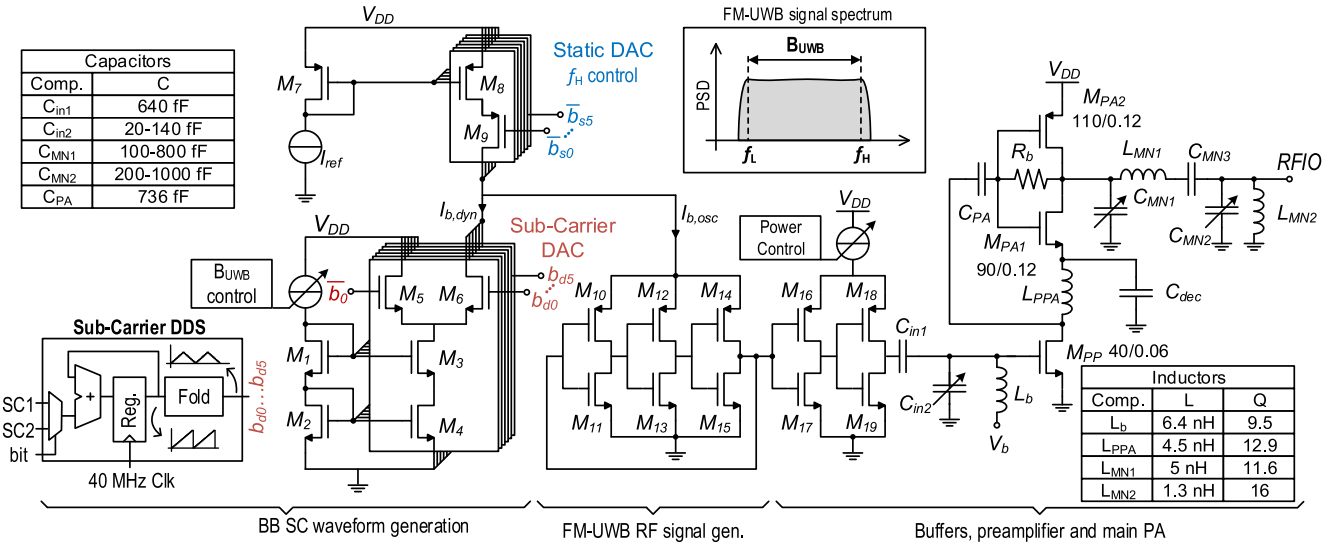

Fig. 5. Transistor-level schematic of the transmitter, and transistor sizes are given in μm.

bandwidth. At 4-GHz RF, this translates into an 8-MHz offset, which is significantly smaller than the accounted RF carrier offset of up to 50 MHz. No narrowband system can tolerate such a large frequency offset. For comparison, a 2000-ppm error in a Bluetooth receiver would result in demodulation of the wrong channel. As will see in Section IV, this receiver is highly robust against frequency offsets. Since precision on the order of 2000 ppm is achievable using on-chip *RC* oscillators, the proposed transceiver also demonstrates the feasibility to implement a radio without a quartz reference oscillator and potentially a true single die radio with zero off-chip components.

III. Transceiver Implementation

A. Transmitter

The low-power FM-UWB transmitter exploits the relaxed phase noise and frequency precision constraints of the FM-UWB modulation and uses a free-running ring oscillator to generate the RF signal. The simplified transistor-level schematic of the transmitter is shown in Fig. 5. Frequency of the ring is controlled through its bias current that is generated using two DACs. The first DAC provides a static current that determines the maximum frequency in the FM-UWB spectrum f_H. This DAC is calibrated once using the FLL and preserves the constant output current during transmission. The second DAC sinks part of the oscillator bias current and produces the modulated RF FM-UWB signal. It is controlled by the SC-DDS circuit that generates the triangular SC wave. The SC-DDS is implemented as an accumulator that runs at 40 MHz, where the SC frequency is determined by the increment M as

$$f_{\mathrm{SC}} = f_{\mathrm{clk}} \frac{M}{2^N} \tag{1}$$

where N is the number of accumulator bits. A 16-bit accumulator is used to provide the necessary frequency resolution, but only 6 bits drive the DAC. The SC-DDS always provides the full-scale 6-bit signal, and FM-UWB RF bandwidth is controlled via the DAC reference current. The reference current is calibrated by the FLL prior to transmission to provide the desired bandwidth. As opposed to the static DAC, the dynamic DAC is implemented using cascode current mirrors to provide better linearity of the output current and frequency.

The DCO is implemented as a simple three-stage ring oscillator. The three inverters are scaled progressively with increasing transistor width toward the output buffer, providing a higher driving capability at lower power consumption. Additionally, two inverters are placed for isolation between the oscillator and the power amplifier. They prevent frequency pulling and allow control of the RF carrier amplitude. Under nominal conditions, the oscillator can be tuned from 3.5 to 5 GHz. With six control bits, the static DAC provides a frequency resolution below 25 MHz, which is enough for FM-UWB. Such a large range guarantees that the output frequency f_H can be set to 4.25 GHz under all PVT conditions ($B_{\mathrm{UWB}}/2$ above the center frequency, with the dynamic DAC off). Once the DCO is calibrated, the output signal should occupy a band from $f_L = 3.75$ GHz to $f_H = 4.25$ GHz. At 4 GHz, the DCO consumes 150 μW, including the two DACs and the output buffers that provide a peak-to-peak output amplitude of 120 mV. The buffer output is also used by the frequency dividers that are part of the calibration loop.

At the targeted output power of -10 dBm, the driver and the main PA need to be considered together since the consumption of the driver becomes comparable to that of the main PA. For example, a highly efficient class-E power amplifier requires a rail-to-rail input signal which, in combination with a large output transistor needed for minimizing the output resistance, results in a prohibitively large consumption of the driver. For this reason, a linear power amplifier is a better choice. Class AB provides a good tradeoff between the driving requirements and efficiency. Both the main PA (transistors M_{PA1} and M_{PA2}) and the preamplifier (PPA, transistor M_{PP}) are biased in class AB with the difference that the PA uses a complementary structure.

In order to reduce consumption, the main PA and the PPA reuse the same current. In addition, this approach eases the

design of the output matching network. To maximize the efficiency of a class AB complementary PA, the output swing should be maximized and equal to its supply voltage V_{DDPA}. At the same time, the output voltage amplitude across the load should be $V_{\mathrm{out}} = 100$ mV to provide output power of -10 dBm. The optimal impedance seen from the PA output (assuming a lossless matching network) is then given by

$$R_{\mathrm{out,PA}} = \frac{V_{\mathrm{DDPA}}^2}{4V_{\mathrm{out}}^2} R_L. \tag{2}$$

Targeting the PA headroom between 0.6 and 0.7 V yields a transformation ratio between 9 and 12.5. Reducing the supply voltage reduces the needed transformation ratio and eases the design with limited Q-factor on-chip components. In the first iteration, the impedance transformation is done at 4 GHz using L_{MN1} and C_{MN1}. Inductance L_{MN2} is then added to equalize the impedance across the band of interest and the component values are optimized together. Capacitor C_{MN2} is added to adjust the input impedance in the receive mode. The two transistors of the PA are sized to provide the desired headroom for the nominal bias current of 480 μA. Both transistors are biased in moderate inversion. In this case, the voltage at the source of transistor M_{PA1} varies between 0.3 and 0.4 V depending on the PPA bias point, which can be tuned to control the output power. At maximum power, the PPA provides more than 250-mV output amplitude which is enough to drive the PA in saturation and provide a rail-to-rail signal at its output.

The matching network is designed to provide good efficiency and constant output power over the whole 500-MHz band. Such an approach inevitably leads to lower efficiency, which is one of the inherent drawbacks of wideband compared to narrowband systems. The simulated efficiency of the output stage (PA and PPA) is above 20% in the band of interest, with a peak of 26% close to 4 GHz. Under the same conditions, the peak output power is -9.2 dBm and varies less than 1 dB from 3.7 to 4.3 GHz, with an average current consumption of 480 μA from a 1-V supply. Since the matching network is also used in the receive mode, capacitors C_{MN1} and C_{MN2} are implemented as switched capacitor banks. Tuning the capacitance provides an input reflection coefficient below -10 dB from 3.6 to 4.35 GHz in the receive mode. All of the passive components shown in Fig. 5 are integrated and there is no need for additional external components. Moreover, since the same pad is used in both transmit and receive modes, there is no need for an extra off-chip switch.

B. Receiver

Two receivers are implemented on this chip: the MU receiver that provides the SC-FDMA and the LP receiver that aims to lower the power consumption. The most important circuit details of the two receivers are presented in this section.

As explained previously, the MU receiver needs to provide good FM–AM linearity and requires a quadrature down-conversion which results in more power consumption. In order to reduce power consumption, an active mixer is used instead of a standard LNA-first architecture. Transistor M_1 that provides voltage-to-current conversion can also be seen as the LNA. The simplified circuit schematic is shown in Fig. 6

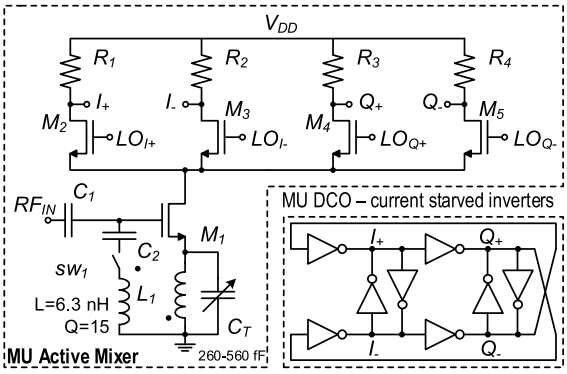

Fig. 6. RF front end and LO generation of the MU receiver.

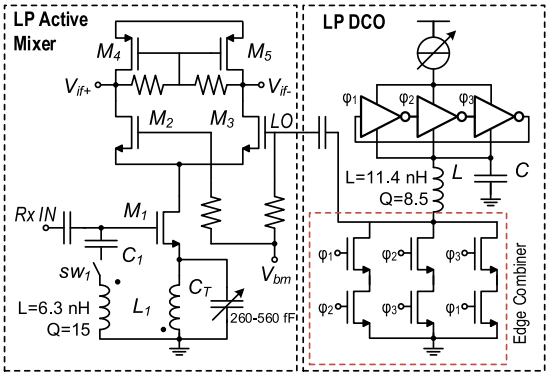

Fig. 7. RF front end and LO generation of the LP receiver.

together with the LO. In terms of noise, the circuit can be analyzed in the same way as a standard single balanced mixer [14]. Here, it was optimized for low power consumption while maintaining the noise figure below 20 dB. Since transistors M_2–M_5 are steering current of the tail transistor M_1 and do not require a rail-to-rail signal, the LO swing can be reduced compared to a passive mixer approach [15]. A transformer is used to boost the transconductance of the input stage and double the voltage gain without increasing power consumption [12], [16], [17]. A variable capacitor C_T is added to allow for tuning of the input impedance after mounting the die on the PCB and for compensation of the effects not taken into account in the simulation (e.g., the interface between the die and the PCB). The circuit achieves 13-dB differential voltage gain and noise figure around 15 dB, while consuming 100 μW. The 1-dB compression point is -16 dBm and the input-referred third-order intercept point (IIP_3) is around -3 dBm. The input transistor M_1 provides reverse isolation better than 65 dB, effectively preventing radiation of the LO signal from the antenna. To generate quadrature LO signals, a two-stage differential ring oscillator is used [18]. It is designed to cover a frequency range from 3.5 to 5 GHz in order to allow for proper calibration across all PVT corners. With six control bits, the achieved frequency resolution is below 30 MHz, which is sufficient for an uncertain IF receiver targeting a frequency offset below 50 MHz. The power consumption at 4 GHz, including the buffers, is 194 μW at 1-V supply.

The LP receiver does not require quadrature LO signals for down-conversion, which saves a significant amount of

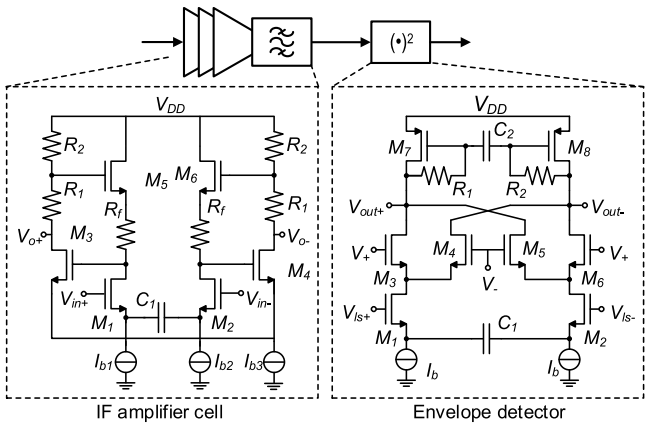

Fig. 8. IF amplifier single-stage transistor level schematic and the envelope detector (wideband FM demodulator) of the LP receiver.

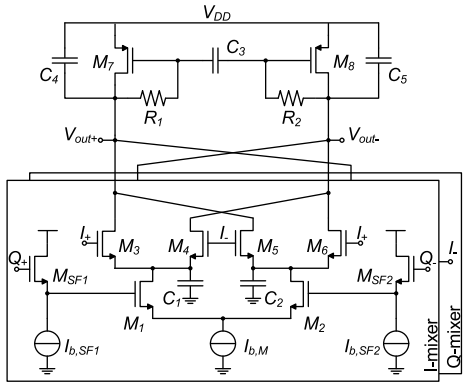

Fig. 9. Wideband FM demodulator of the MU receiver.

power in the LO implementation. The active mixer of the LP receiver is similar to that of the MU Rx except for the single LO input (Fig. 7). Since only a single-ended drive is used, the voltage gain is somewhat lower, achieving 11- and 19-dB noise figure while consuming only 70 μW. The reverse isolation is 55 dB, which is less than the MU receiver, and is a consequence of the asymmetric LO drive. The implemented ring oscillator reuses the approach from [19] in order to reduce the power consumption. The oscillator itself consists of three current starved inverters that oscillate at one-third of the desired LO frequency. The three generated phases are then combined in an edge combiner in order to triple the output frequency. The ring oscillator and the phase combiner are stacked in order to reuse the same current and are separated by an LC filter that provides a stable voltage level for the inverters and a resonant load for the combiner. Since the combiner also acts as a buffer, no additional amplifiers are needed between the LO and the mixer. The range of output frequencies lies between 3.5 and 5.2 GHz, providing again a resolution better than 30 MHz for six control bits. The power consumption of the LO at 4 GHz is 64 μW, which is approximately three times lower than the quadrature oscillator.

The IF sections of both receivers, together with the wideband FM demodulators, are shown in Figs. 8 and 9. In both the MU and the LP receiver, the mixer is followed by a three-stage IF amplifier (quadrature branches are present in the MU Rx). Each stage is implemented as a feedback Cherry-Hooper

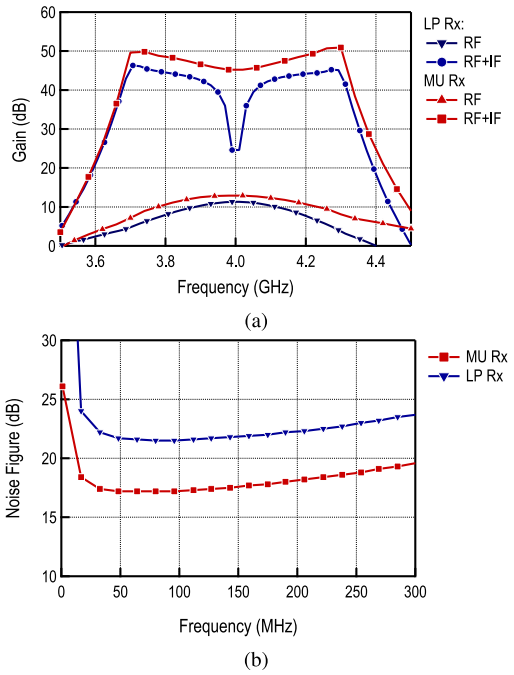

Fig. 10. (a) Simulated conversion gain of the active mixer and the full RF and IF chain of the MU and LP receivers. (b) Noise figure of the MU and LP receivers.

amplifier [20]–[22] shown in Fig. 8. It provides 300 MHz of bandwidth to account for the frequency mismatch between the transmitter and the receiver LO. The capacitor C_1 in the IF amplifier provides the high-pass part of the characteristic. In the MU receiver, it is used to prevent offset accumulation, and since the cutoff frequency is below 1 MHz (relative to the 250-MHz IF signal), it will not affect the receiver performance. In the LP receiver, a small capacitor is used in the last stage that results in a higher cutoff frequency of 100 MHz. This stage provides the necessary FM–AM conversion and is effectively a part of the wideband FM demodulator. The simulated gain characteristic and noise figure of the full front end are shown in Fig. 10 for both receivers.

The wideband FM demodulator of the LP receiver is implemented using a standard double balanced mixer shown in Fig. 8. In the LP receiver, the signal is mixed with itself and level shifters adjust the dc value of the input signal for the two inputs of the mixer. A similar circuit is used in the MU receiver, shown in Fig. 9, except that here two mixers are needed to provide the product of quadrature signals with their delayed copies and to subtract the output currents in order to perform the FM demodulation [12]. The load of the demodulator (resistors R_1 and R_2 and capacitor C_1) provides a high-pass characteristic that suppresses low-frequency components that might appear due to narrowband interferers. The consumption of both demodulators is smaller than 20 μA, which is considerably lower than other wideband FM demodulators implemented at RF that need a current of up to 3 mA. The FM demodulators are followed by low-pass filters that remove the unwanted high-frequency components. Since only one channel is supported by the LP receiver, there is no need for a sharp channel filter and a simple second-order section is sufficient. Filtered signal is fed to a comparator that provides a rail-to-rail output signal for the FSK demodulator.

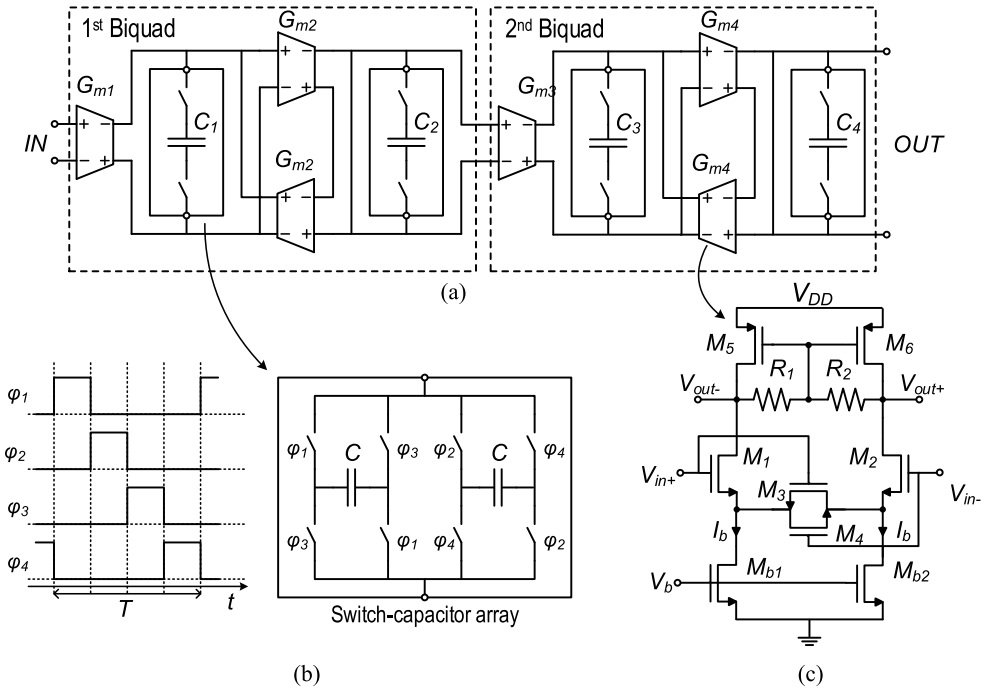

Fig. 11. (a) N-path filter circuit schematic. (b) Non-overlapping clock timing diagram and the switched-capacitor network implementation. (c) Transconductor schematic.

The MU receiver supports up to four SC channels, and before the desired channel can be demodulated, the unwanted channels must be filtered. Relatively sharp filtering is needed since the space between the adjacent channels is only 100 kHz. For a non-filtered FSK modulation and the proposed SC frequency plan, the ACLR is approximately −33 dB [12]. Accounting for roughly 13-dB SNIR needed for a BER of 10^{-3}, the maximum adjacent SC channel power difference that can be tolerated is approximately 20 dB, corresponding to 10-dB difference in power levels at RF. The channel filter is, therefore, designed to suppress a 20-dB stronger adjacent channel. The targeted attenuation is 40 dB at the adjacent SC frequency or equivalently 250 kHz away from the channel center frequency. The filter should be easily tunable to any of the channel frequencies, and it should preserve the same characteristic for all the channels.

N-path filters are an excellent candidate for the targeted specifications given their wide tuning range and high quality factor without any off-chip passive components [15], [23]–[27]. The center frequency of the filter corresponds to the sampling frequency and can easily be tuned to any channel frequency. Passbands at multiples of the desired frequency are not an issue since the SC band is limited to one octave. Solutions demonstrated at RF are adapted here for low-frequency and low-power operation.

An N-path filter can be designed starting from a standard G_m-C filter, following the approach described in [23]. It was shown that by adding switches in capacitor branches and by controlling these switches using N non-overlapping phases, a low-pass filter characteristic is translated into a passband characteristic. In order to maintain the bandwidth, the capacitor in each branch must be scaled by the number of paths, such that $C_x = C_{\mathrm{LPx}}/N$. One important issue related to RF N-path filters is the switch resistance that limits the achievable attenuation in the stopband as [28]

$$A_{\max} = \frac{2R_{\mathrm{sw}}}{R_{\mathrm{in}} + R_{\mathrm{sw}}} \tag{3}$$

where R_{in} is the input source resistance. However, the filter is driven by a high output impedance transconductor in this case, which relaxes the constraints on the switch resistance and allows for relatively small switches. Moreover, the parasitic capacitances cause a slight asymmetry around the center frequency in the transfer function. This problem can be solved by adding feed-forward capacitors [23]. Such techniques are not needed here since the small variation of around 1 dB does not influence the demodulator performance.

To satisfy the specification, a fourth-order type-1 Chebychev filter is used. The transfer function is implemented using two biquadratic sections (Fig. 11). For each biquadratic section, the transfer function is given by

$$H(s) = \frac{H_0}{\mathrm{as}^2+\mathrm{bs}+1}. \tag{4}$$

The coefficients H_0, a and b are given by

$$H_0 = \frac{G_{m1}G_{m2}}{G_{m2}^2 + G_{o1}G_{o2}}$$
$$a = \frac{C_1C_2}{G_{m2}^2 + G_{o1}G_{o2}}, \quad b = \frac{C_1G_{o2} + C_2G_{o1}}{G_{m2}^2 + G_{o1}G_{o2}} \tag{5}$$

where G_{mk} and G_{ok} are the transconductance and output conductance of OTA k, respectively. In this design, a Krummenacher differential pair is used [29], as shown in Fig. 11(c). The transistors are biased in weak inversion with the ratio $\beta_1/\beta_3 = 2$, corresponding to the minimum ripple condition.

The number of paths in an N-path filter affects filter characteristics. Generally, increasing N leads to less attenuation

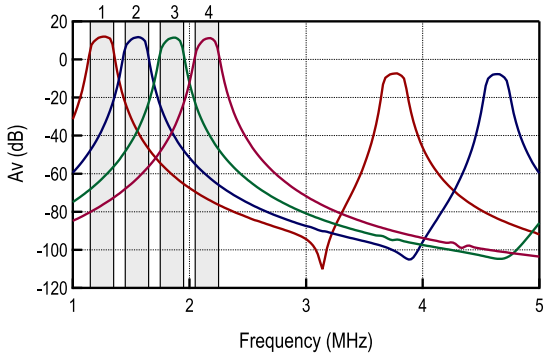

Fig. 12. Simulated transfer functions of the N-path filter.

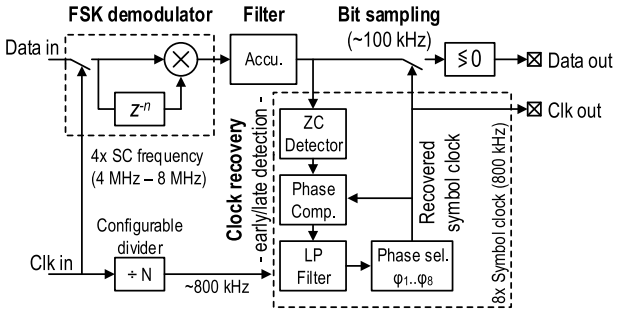

Fig. 13. Block diagram of the FSK demodulator and the clock recovery circuit.

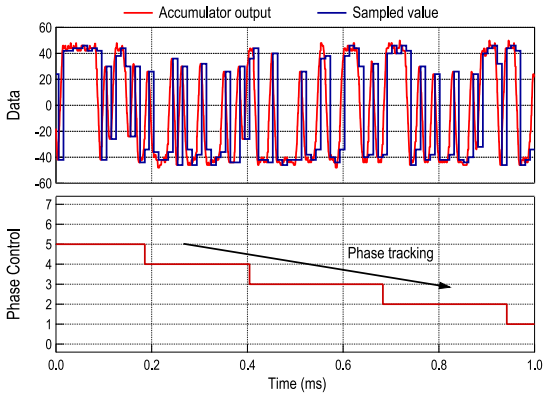

Fig. 14. Simulated waveforms of the clock recovery circuit for a receive clock 2000 ppm slower than the transmit clock.

in the passbands at the harmonics of the switching frequency, but at the same time decreases folding-back and noise [28]. Four paths are enough for this implementation, and the noise performance is not critical, as the block is located close to the end of the receiver chain. A differential structure is used to suppress harmonics at even multiples of the switching frequency. Four non-overlapping phases are derived from a single clock running at four times the sampling frequency, using flip-flop dividers.

The simulated filter frequency response is presented in Fig. 12. Four different cases are shown corresponding to four SC channels. Simulated attenuation at 250 kHz from the center frequency is 40 dB. The filter also provides 10 dB of gain, while consuming 43 μA (5 μA per transconductor and the rest for the clock distribution network). For the targeted SC channel frequency range, the input clock frequency varies from 5 to 8.6 MHz. The N-path filter is followed by a low-pass filter that suppresses higher harmonics and a comparator that precedes the FSK demodulator.

The same FSK demodulator is used by both receivers. The block diagram is shown in Fig. 13. The proposed FSK demodulator is a digital delay line demodulator. The input signal is sampled using a clock that is four times higher than the SC channel frequency (the same clock is used to derive the N-path filter clocks), and the delay is implemented as a chain of flip-flops. The original signal is "multiplied" with its delayed version using an XOR gate. The signal at the demodulator output is filtered using a windowed accumulator that acts as a matched filter for an FSK signal with no pulse shaping. The proposed FSK demodulator incurs a 1-dB loss compared to an optimal demodulator (matched filter), but is simpler and consumes a relatively small amount of power.

As explained previously, FM-UWB is inherently robust against frequency offsets. At RF, carrier offsets of up to several tens of megahertz do not cause any significant penalty in terms of BER [12]. At IF, a small frequency mismatch between the SC frequency on the transmitter and the receiver side can be tolerated. The tolerable frequency offset depends on the parameters, such as data rate and modulation index. For the parameters of this system, the acceptable frequency offset is much larger than the precision provided by a typical crystal oscillator owing to the low SC frequency. Assuming a clock recovery circuit is able to track the received signal, a crystal oscillator could be replaced by an integrated oscillator in the transceiver (e.g., an *RC* oscillator), thus enabling a full integration (zero off-chip components). The block diagram of the proposed clock recovery circuit is presented in Fig. 13. A simple early/late zero crossing detection algorithm is used to track the phase of the input signal. The clock recovery circuit uses a reference clock obtained by division of the FSK demodulator clock. The configurable divider produces an output clock at roughly 800 kHz, which is eight times higher than the symbol frequency. This clock is then divided by 8 to produce eight equidistant phases, one of which is used to sample the final result. The accumulator output is first sampled at 800 kHz to detect a zero crossing. False zero crossings due to noise are avoided by requiring a certain minimum difference between consecutive samples. Once a zero crossing is detected, a phase comparator determines whether it is early or late with respect to the current phase. The number of clock cycles between the zero crossing and the reference phase is added to or subtracted from the register of the low-pass filter (here implemented as an accumulator). Once the register reaches a required positive or negative value, the reference phase will be incremented or decremented. The proposed phase tracking circuit produces an output clock whose average frequency is equal to the transmit symbol frequency. Assuming the phase changes in every clock cycle, the proposed circuit should be able to track frequency offset of up to 1/8 of the reference frequency. At such a large offset, the limiting factor will more likely be the FSK demodulator or the preceding filter.

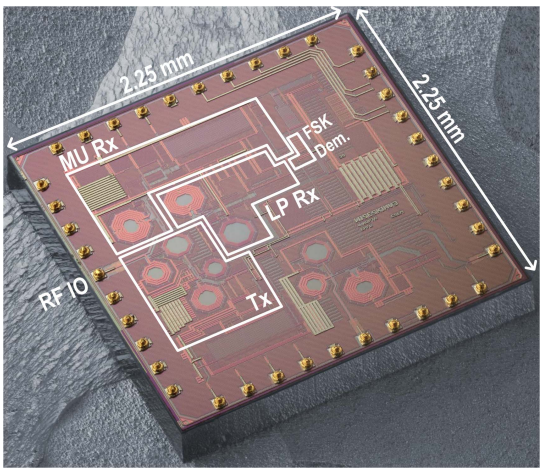

Fig. 15. Die photograph.

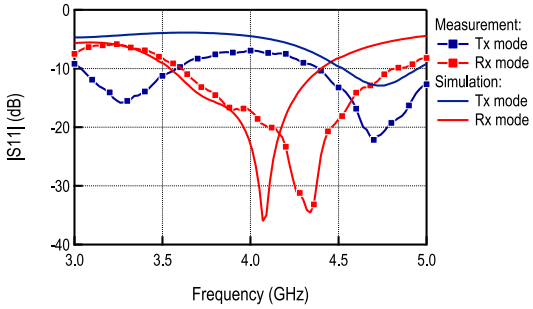

Fig. 16. Measured and simulated S_{11} parameter in the transmit and receive modes.

An example simulation result is shown in Fig. 14, where the receiver reference is 2000 ppm slower than the transmitter reference. Since the zero crossings of the received signal appear early compared to the reference, the phase control signal decrements. On every transition, the output phase advances for 1/8 of the clock period, resulting in a clock whose frequency is on average equal to the transmit clock frequency.

IV. Measurement Results

The proposed transceiver is integrated in a standard 65-nm bulk CMOS technology. The die size is 2.25 mm × 2.25 mm, and its SEM photograph is shown in Fig. 15. The transceiver occupies roughly one-third of the die area, including the matching network and the decoupling capacitors. Gold bumps, used for flip-chip bonding of the die, can be seen on top of the pads. The RF IO pad is placed between the two ground pads that were connected to a coplanar waveguide on the PCB.

The measured and simulated values of the input reflection coefficient are shown in Fig. 16. The differences are a result of the chip interface before the PCB and the transmission line that were not taken into account in the simulations. In the transmit mode, the S_{11} parameter is close to −8 dBm in the band of interest and was optimized for PA efficiency. In the receive mode, the S_{11} parameter is below −10 dBm from 3.6 to 4.8 GHz, providing good matching in the band of interest.

The performance of the transmitter output stage, comprising the PA and the PPA, is given in Fig. 17. The measurements were conducted using the on-chip ring oscillator in the

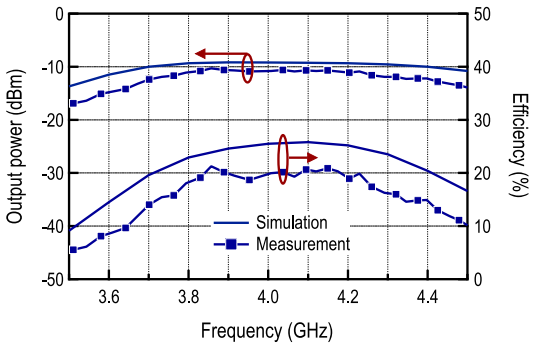

Fig. 17. Output power and efficiency of the PA together with the preamplifier.

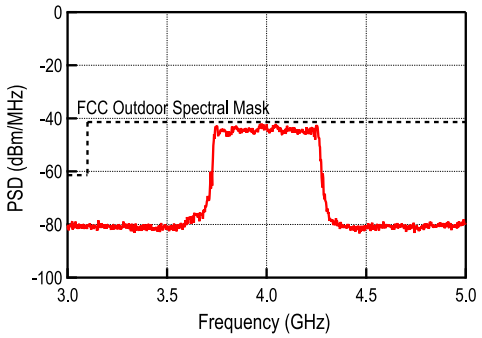

Fig. 18. Transmitted FM-UWB spectrum.

static mode. The output power is slightly lower than the simulated value with a slightly reduced bandwidth. As a result, the efficiency also drops with a peak value of 21.3%. When transmitting the 500-MHz-wide FM-UWB signal, the average efficiency is 18%, while consuming 575 μW from a 1-V supply. The spectrum of the transmitted FM-UWB signal is shown in Fig. 18. The achieved transmitter efficiency (output power divided by total power consumption) of 12.4% is better than the state of the art [9], [10], [30]; however, one should note that in this case, there will be no additional losses coming from the external TR switch needed to separate the input and output ports. The output power of the transmitter can be tuned from −11.4 to −35 dBm in steps smaller than 3 dB by controlling the DCO buffer amplitude and the PPA bias current. This can be used to reduce the power consumption of the transmitter and minimize interference with other FM-UWB users (e.g., two transmitters at different distances could adjust their output power to equalize signal levels at the receiver).

The bit-error-rate (BER) curves for the LP and MU receivers are shown in Fig. 19. In the case of the LP receiver, only one sub-channel is supported and the achieved sensitivity is around −57 dBm. For the single user case, the sensitivity of the MU receiver is −68 dBm. According to the calculation from [6], accounting for the front-end noise figure, loss due to the LO uncertainty [12], and the low-power FSK demodulator loss, the expected sensitivity is −73 dBm. The difference between the estimated and measured values is likely due to a higher noise figure compared to the simulations. The theoretical difference of 6 dB in sensitivities between the two types of receivers and approximately 5-dB higher noise figure of the LP receiver (due to single-ended LO with a lower signal amplitude) fit well with the measured sensitivity levels.

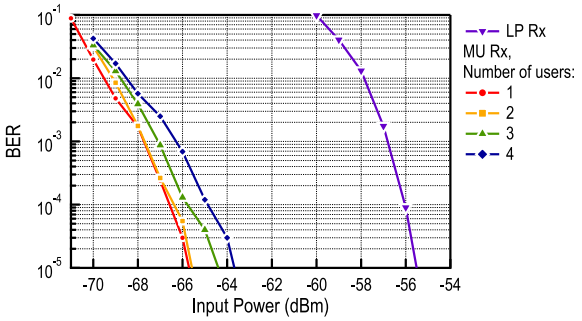

Fig. 19. BER curves for a single user (MU and LP receivers) and multiple users of the same power (MU receiver).

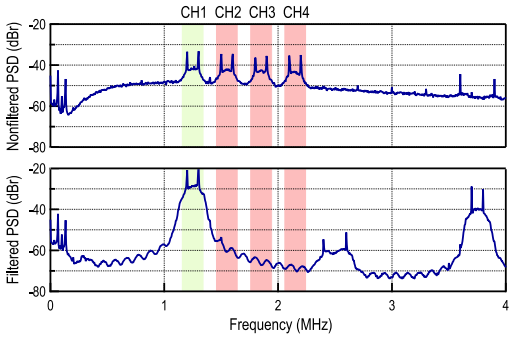

Fig. 20. Received signal before and after the N-path filter.

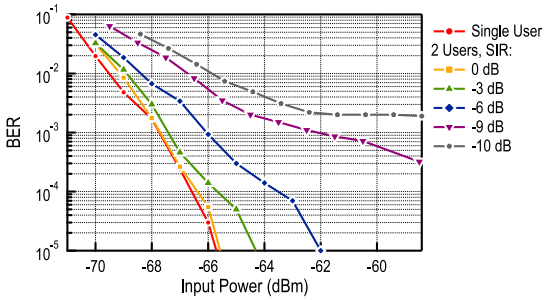

Fig. 21. BER curves for two FM-UWB users and varying SIR.

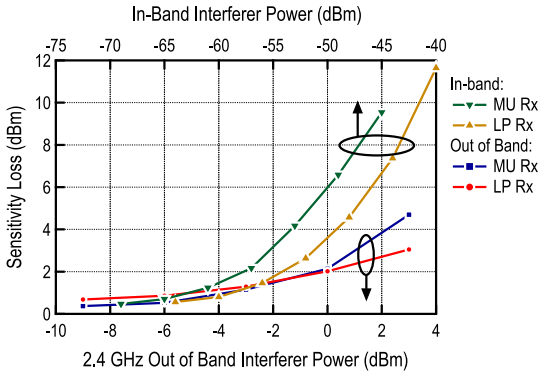

Fig. 22. Receiver sensitivity degradation as a function of interferer power.

At the same time, the LP receiver consumes 267 μW, which is the lowest power consumption reported for an FM-UWB receiver. This is roughly one-half of the 550 μW consumed by the MU receiver. Sensitivity loss is the price paid for the reduction of dc power consumption.

The MU receiver is characterized in two MU scenarios. In the first scenario, the transmit power of each user is the same, while the number of users increases. This is shown in Fig. 19. Before the intended channel can be demodulated, the adjacent interfering channels are filtered by the N-path channel filter. Fig. 20 shows the SC spectrum before and after the channel filter. Adjacent channels are suppressed by more than 40 dB. The presence of additional users raises the noise floor in the receiver (due to mixing of the noise and signal in the wideband FM demodulator [6]) and results in sensitivity loss. However, this loss remains relatively small for users of equal transmit power.

In the second scenario, a two-user case is evaluated in which the power of the interfering channel gradually increases. The BER curves for this case are shown in Fig. 21. Again, the increase of the interfering channel power results in the increase of the inter-user interference and the sensitivity decreases. With 10-dB higher interferer input power (resulting in 20-dB stronger SC), the BER saturates at 2×10^{-3}, limiting the achievable difference in power levels for this receiver. The limitation primarily comes from the leakage of the interfering adjacent channel and can be improved by pulse shaping on the transmitter side and by increasing the spacing between channels.

The receiver performance in the presence of narrowband interferers is shown in Fig. 22. Assuming that a 3-dB sensitivity degradation can be tolerated, the MU and LP receivers can support a 4.1-GHz interferer of up to -55 and -52 dBm. Another case of interest is with an out-of-band interferer at 2.4 GHz, since this is where a large number of commercial devices operate. Thanks to the sixth-order filtering in the IF amplifier, this interferer is largely suppressed and the MU and LP receivers can still operate even if the interferer power reaches 1 and 3 dBm, respectively.

The BER degradation as a function of frequency offset is shown in Fig. 23. The curves are plotted for levels that are 1 dB below the nominal sensitivity for both receivers. In the measurement, the reference clock frequency on the receiver side is adjusted in each iteration and the corresponding BER is measured. The MU receiver can tolerate up to $\pm$8000-ppm frequency offset between the transmitter and the receiver side. The limit is coming from a combination of the offset in the channel filter and the reference clock in the FSK demodulator. Since there is no need for sharp filtering in the LP receiver, the range of acceptable offset frequencies is larger and goes up to $\pm$12000 ppm. With the state-of-the-art on-chip *RC* oscillators achieving precision ranging from 2000 to 6800 ppm [31]–[33], the proposed transceiver demonstrates the feasibility of a radio that is based on an on-chip clock reference without any external components.

A comparison with the state-of-the-art FM-UWB transceivers is given in Table I. The transmitter from [9] uses a similar architecture; however, no implementations were found in the literature where the matching network is fully integrated and the receiver and transmitter use the same pin. Transceivers from [9] and [10] occupy a smaller die area, but they both require an external switch and a quartz resonator. The receiver from [34] achieves good FM–AM linearity and could support

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART TRANSCEIVERS

Parameter	[34][(1)(2)]	[10]	[9]	This Work	
				LP	**MU**
Modulation	FM-UWB	Chirp-UWB	FM-UWB	FM-UWB	
Frequency	7.5 GHz	8 GHz	4 GHz	4 GHz	
Frequency deviation	25 kHz	-	250 kHz	50 kHz	
Receiver Cons.	**9.1 mW**	**4/0.6 mW[(3)]**	**580 µW**	**267 µW**	**550 µW**
Data Rate	50 kb/s	1 Mb/s	100 kb/s	100 kb/s	
FSK Sub-channels	**No**	**No**	**No**	**No**	**4**
SIR UWB	-	-	-	-	-9 dB
Integrated MN	**No**	**No**	**No**	**Yes**	
NB Int. Power (in band)	-55 dBm	-	-52 dB[(4)]	-52 dBm	-55 dBm
NB Int. Power (@ 2.4 GHz)	-38 dBm @ 6 GHz	-	-38 dB[(4)]	3 dBm	1 dBm
Ref. Clk. Offset	-	-	-	8000 ppm	
Sensitivity	-88 dBm	-76 dBm	-80.5 dBm	-57 dBm	-68 dBm
Transmitter Consumption	-	2.8/0.42 mW[(3)]	630 µW	575 µW	
Output Power	-	-	-12.8 dBm	-11.4 dBm	
Technology	0.25 µm BiCMOS	65 nm	90 nm	65 nm	
Active area	1.79 mm^2	0.7 mm^2	0.54 mm^2	1.1 mm^2	
External components	n/a	TRX switch, quartz	TRX switch, quartz	None	

[(1)]Off-chip sub-carrier FSK demodulation [(2)]Receiver only [(3)]Without/with duty-cycling [(4)]-70 dBm input signal power

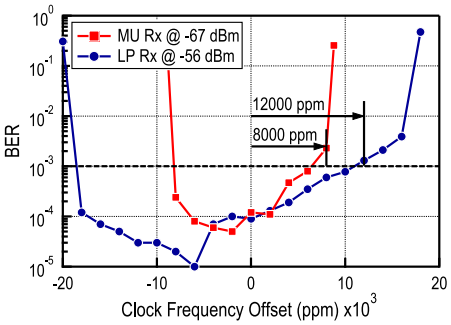

Fig. 23. BER as a function of reference clock offset.

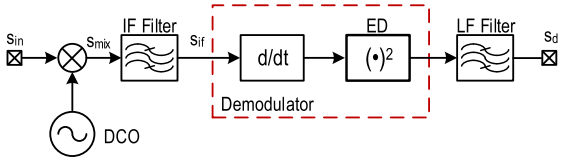

Fig. 24. Simplified model of the low-power FM-UWB receiver.

multiple users, but these features are not implemented on the chip itself. The receiver from [9] achieves low power and good sensitivity, but cannot support multiple SC channels. The proposed MU receiver combines the two approaches to provide low power operation and MU communication, with the entire receiver chain integrated on a single die. In addition, it provides a low-power mode in which the receiver consumes only 267 μW. The transceiver described in [10] uses a similar architecture to other FM-UWB transceivers, but exploits the chirp-UWB (C-UWB) modulation to move to higher data rates and employs symbol-level duty cycling to reduce power consumption and arrive at a number comparable to the proposed receiver. The use of C-UWB and duty cycling could enable further power reduction in the future implementations of the proposed approximate zero-IF receiver.

V. CONCLUSION

A fully integrated FM-UWB transceiver targeting short-range communications in the potential IoT and WBAN applications is proposed. Two receivers are integrated providing a low-power mode, in which the receiver consumes 267 μW, and an MU mode in which the receiver consumes 550 μW. The MU mode allows up to four devices to share the same RF band through the use of SC FDMA, thus providing means to decrease latency in networks with a large number of users. Both receivers can tolerate in-band narrowband interferers, as well as relatively strong out-of-band interferers located around 2.4 GHz. Finally, the receivers are robust against reference clock offset and can demonstrate operation without the need for a precise external quartz resonator. The transmitter consumes 575 μW while transmitting a 100-kb/s FM-UWB signal centered at 4 GHz at -11.4 dBm. The transmitter shares the same RF IO pad with the two receivers with a fully integrated matching network unlike the previous implementations that needed an external switch for antenna connection.

APPENDIX
LOW POWER FM-UWB RECEIVER PRINCIPLE

The operation of the LP demodulator can be explained using a simplified receiver model presented in Fig. 24. The FM-UWB signal at the receiver input can be represented as

$$s(t) = A\cos(\omega_c t + \phi(t)) \tag{6}$$

where ω_c is the center frequency and $\phi(t)$ is the integral of the SC wave $m(t)$ given by

$$\phi(t) = \Delta\omega \int_{-\infty}^{t} m(t)\mathrm{d}t. \tag{7}$$

The SC wave $m(t)$ is normalized to the interval $[-1,1]$, and $\Delta\omega$ is the frequency deviation corresponding to half of the

FM-UWB signal bandwidth $\Delta\omega = 2\pi\,\Delta f = \pi\,B_{\mathrm{UWB}}$. After down-conversion, the signal at the mixer output is given by

$$s_{\mathrm{mix}}(t) = \mathrm{kA}\cos(\omega_c t + \phi(t) + \phi_0)\cos(\omega_{\mathrm{osc}} t) \tag{8}$$

where k is the mixer constant, assumed to be equal to 1 in the following derivation for simplicity. The IF low-pass filter removes all the high-frequency components, resulting in the signal at the filter output given by

$$s_{\mathrm{if}}(t) = \frac{A}{2}\cos(\omega_o t + \phi(t)) \tag{9}$$

where ω_o is the offset frequency that is equal to the difference of the LO frequency and the signal center frequency. The following stage, a differentiator, converts the FM signal into an AM signal given by

$$\frac{ds_{\mathrm{if}}(t)}{dt} = \frac{A}{2}\sin(\omega_o t + \phi(t))\left(\omega_o\tau_0 + \tau_0\frac{d\phi(t)}{dt}\right) \tag{10}$$

where τ_0 is the time constant of the differentiator. The resulting signal is then demodulated using the envelope detector. Here, an ideal square law envelope detector is assumed (corresponding to the self-mixing approach used in the implementation), resulting in the output signal given by

$$\begin{aligned} s_{\mathrm{d}}(t) &= \frac{A^2}{4}\sin(\omega_o t + \phi(t))^2\left(\omega_o\tau_0 + \tau_0\frac{d\phi(t)}{dt}\right)^2 \\ &= \frac{A^2}{8}(1 - \cos(2\omega_o t + 2\phi(t)))\left(\omega_o\tau_0 + \tau_0\frac{d\phi(t)}{dt}\right)^2. \end{aligned} \tag{11}$$

The low-pass filter following the envelope detector will practically remove the fast changing component $\cos(2\omega_o t + 2\phi(t))$, resulting in the signal at the filter output given by

$$s_{\mathrm{d}}(t) = \frac{A^2}{8}\left(\omega_o\tau_0 + \tau_0\frac{d\phi(t)}{\mathrm{dt}}\right)^2. \tag{12}$$

For simplicity, let us assume that the SC signal is a sine wave $m(t) = \sin(\omega_{sc} t)$. Inserting (7) into (12) then gives

$$\begin{aligned} s_{\mathrm{d}}(t) &= \frac{A^2}{8}(\omega_o\tau_0 + \Delta\omega\tau_0\sin(\omega_{\mathrm{sc}} t))^2 \\ &= \frac{A^2}{8}\tau_0^2(\omega_o^2 + 2\omega_o\Delta\omega\sin(\omega_{\mathrm{sc}} t) + \Delta\omega^2\sin^2(\omega_{sc} t)). \end{aligned} \tag{13}$$

In the ideal case, the offset frequency is zero, $\omega_o = 0$, and the remaining useful term is found at twice the SC frequency

$$s_{\mathrm{d},2}(t) = \tfrac{A^2}{16}\Delta\omega^2\tau_0^2\cos(2\omega_{\mathrm{sc}} t). \tag{14}$$

The final FSK demodulation can now be performed using this signal. Interestingly, if an ideal differentiator is used and if infinite IF bandwidth is assumed, the amplitude of the second harmonic will be independent of the frequency offset. However, in practical systems, the maximum tolerable frequency offset is limited by the IF amplifier bandwidth. Compared to an equivalent delay-line demodulator, where the output signal amplitude is proportional to $A^2/4$ [12], the proposed LP demodulator provides the output signal amplitude that is four times smaller. Using the approach described in [6], the SNR at the demodulator output is then given by

$$\mathrm{SNR}_{\mathrm{out}} = \frac{B_{\mathrm{UWB}}}{B_{\mathrm{SC}}}\frac{(\mathrm{SNR}_{\mathrm{in}})^2}{1 + \mathrm{SNR}_{\mathrm{in}}} \tag{15}$$

where B_{SC} is the SC bandwidth and $\mathrm{SNR}_{\mathrm{in}}$ is the SNR at the receiver input. Using the standard formula for the FSK modulation, the BER can be calculated as [6]

$$\mathrm{BER} = \frac{1}{2}\mathrm{erfc}\left(\sqrt{\frac{\mathrm{SNR}_{\mathrm{out}}}{2}}\right). \tag{16}$$

Due to the reduced SNR at the LP demodulator output, its sensitivity is 6 dB lower compared to an equivalent delay-line demodulator, revealing a tradeoff between performance and power consumption for the proposed receiver architecture.

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