A 28-GHz CMOS Phased-Array Transceiver Based on LO Phase-Shifting Architecture With Gain Invariant Phase Tuning for 5G New Radio

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***Abstract*— This paper presents a 28-GHz CMOS four-element phased-array transceiver chip for the fifth-generation mobile network (5G) new radio (NR). The proposed transceiver is based on the local-oscillator (LO) phase-shifting architecture, and it achieves quasi-continuous phase tuning with less than 0.2-dB radio frequency (RF) gain variation and 0.3° phase error. Accurate beam control with suppressed sidelobe level during beam steering could be supported by this work. At 28 GHz, a single-element transmitter-mode output P_{1dB} of 15.7 dBm and a receiver-mode noise figure (NF) of 4.1 dB are achieved. The eight-element transceiver modules developed in this work are capable of scanning the beam from −50° to +50° with less than −9-dB sidelobe level. A saturated equivalent isotropic radiated power (EIRP) of 39.8 dBm is achieved at 0° scan. In a 5-m over-the-air measurement, the proposed module demonstrates the first 512 quadrature amplitude modulation (QAM) constellation in the 28-GHz band. A data stream of 6.4 Gb/s in 256-QAM could be supported within a beam angle of ±50°. The achieved maximum data rate is 15 Gb/s in 64-QAM. The proposed transceiver chip consumes 1.2 W/chip in transmitter mode and 0.59 W/chip in receiver mode.**

***Index Terms*— 28 GHz, 256 quadrature amplitude modulation (QAM), 512-QAM, beamforming, CMOS, error vector magnitude (EVM), fifth-generation mobile network (5G) new radio (NR), local-oscillator (LO) phase shifter, phased array, transceiver.**

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I. Introduction

THE incoming fifth-generation mobile network (5G) utilizes the millimeter-wave spectrum to provide a high-throughput and low-latency experience. Within the frequency range 2 (FR2) defined in the 5G new radio (NR) standard, the 28-GHz band is available in various countries around the world. Fig. 1 shows the spectrum allocation for the 28-GHz band. Within the wide-frequency spectrum, the 5G NR band n257, which is from 26.5 to 29.5 GHz, features a maximum channel bandwidth BW_c of 400 MHz.

Different from the transceivers designed for the under 6-GHz band, the silicon-based millimeter-wave phased-array transceivers demand a larger array size. Highly directional transmission links will be established to cover the communication distance. In this context, accurate beam control is required for providing stabilized data communication and avoiding interference [1], [2]. During the past few years, radio frequency (RF), local-oscillator (LO), and baseband phase-shifting architectures are utilized in millimeter-wave phased-array transceivers. RF phase-shifting architecture, which shares the mixer and LO distribution, can reduce area and power consumptions [2]–[9]. However, RF phase shifters suffer from gain variation during the phase tuning, which is usually more than 0.5 dB [10]–[13]. Baseband phase-shifting architecture can realize very predictable and high-resolution phase tuning with the baseband analog circuits [14]. However, due to the large fractional bandwidth for the baseband phase shifters, gain and phase mismatches will arise along the frequency between the transceiver elements. In addition, the quadrature LO distribution not only consumes power and area but also degrades the I/Q imbalance of the transceiver.

By saturating the mixer with enough LO voltage swing, LO phase-shifting architecture can realize fine phase tuning with greatly improved gain and phase errors [15]–[17]. Although the LO distribution consumes additional area and power, the induced area and power consumptions could be suppressed

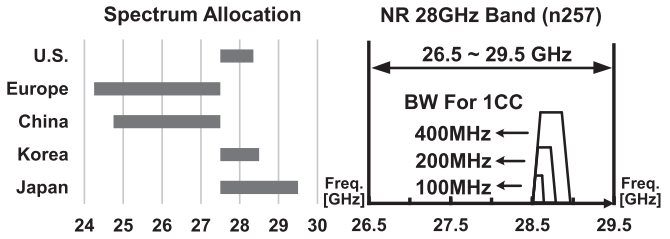


Fig. 1. (a) 28-GHz spectrum allocation for 5G usage in various countries. (b) 5G NR band n257.

by the power-efficient design and the LO sharing between the transmitter and receiver. In this work, a 28-GHz phased-array transceiver chip based on the LO phase-shifting architecture is introduced. The proposed transceiver chip is fabricated in a 65-nm CMOS process featuring low manufacturing cost. The proposed LO phase shifter achieves a measured RF gain variation of less than 0.2 dB and an rms phase error of 0.3°. The eight-element transceiver modules in this work are capable of scanning the beam from −50° to +50°. The accurate beam control with suppressed sidelobe level is realized during the beam scan. At a distance of 5 m, the proposed module demonstrates the first 512 quadrature amplitude modulation (QAM) constellation in the 28-GHz band. A data link of 6.4 Gb/s in 256-QAM is maintained within a scan angle of −50°–+50°.

This work is an extension of [15] and is organized as follows. The design considerations for the proposed transceiver are presented in Section II. Section III introduces the specific circuit schematics for the LO, transmitter, and receiver. The measured characteristics for the proposed transceiver along with the eight-element modules are demonstrated in Section IV. Finally, conclusions are drawn in Section V.

II. Architecture Considerations

An optimized error vector magnitude (EVM) performance over a long communication distance is supposed to be maintained by the future 5G millimeter-wave phased-array transceivers. High-speed, low-latency, and stabilized data links with suppressed sidelobe and spurious levels are required over all beam scan angles. As a result, careful considerations on the noise figure (NF), linearity and beam control will be necessary for designing a 5G millimeter-wave phased-array transceiver. The remaining part of this section will explain the detailed requirements from 5G along with the design considerations.

A. Communication Distance

To obtain sufficient 5G communication distance, a large array size is required for 5G base station (BS) using a CMOS millimeter-wave phased-array transceiver. The 5G NR standard allows a maximum equivalent isotropic radiated power (EIRP) of 75 dBm/100 MHz to the BS and 43 dBm to user equipment (UE) [18]. Usually, within a reasonable power consumption, a single-element transmitter output power of around 12 dBm (antenna gain included) can be realized for modulation schemes such as 64-QAM or 256-QAM in CMOS process [19], [20]. Thus, an array size of over 256 will

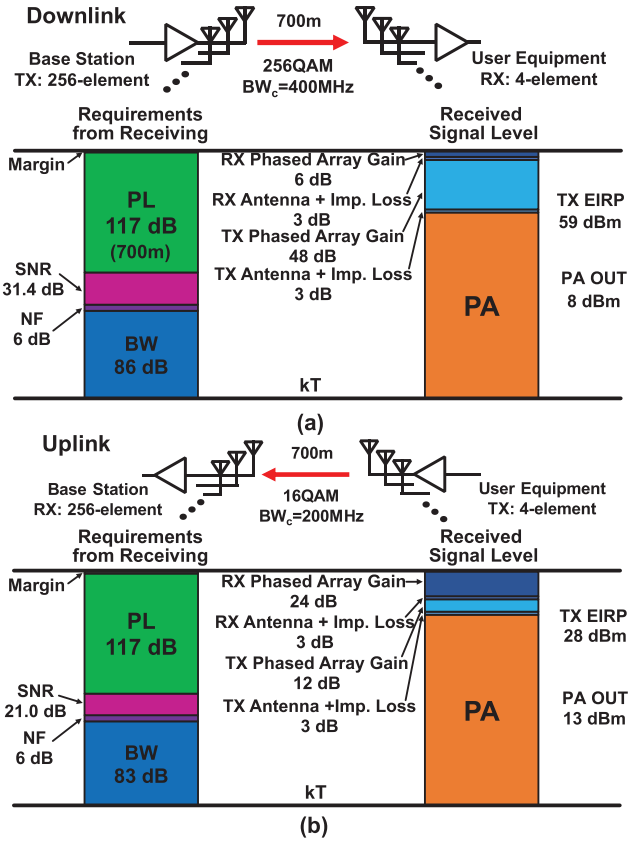


Fig. 2. Link budget examples for (a) 5G downlink and (b) 5G uplink.

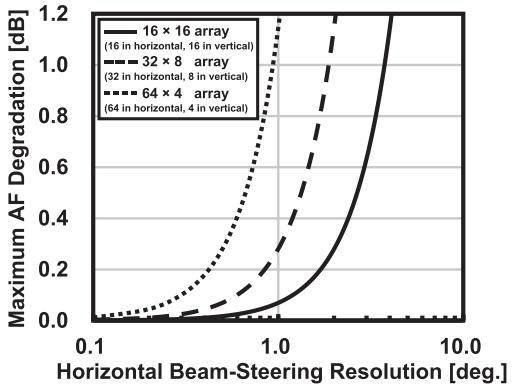


Fig. 3. Calculated the maximum AF degradation due to the insufficient beam-steering resolution.

be required to realize a 60-dBm EIRP. Fig. 2 shows link budget examples for a 400-MHz downlink in 256-QAM and a 200-MHz uplink in 16-QAM. The array sizes are 256 for the BS and 4 for the UE. The communication distance is 700 m, which corresponds to a line-of-sight (LOS) free-space path loss (FSPL) of 117 dB at 28 GHz. After receiving, the downlink and the uplink still maintain signal-to-noise ratios (SNRs) over 31.4 and 21 dB for the downconversion and demodulation, respectively.

B. Beam-Steering Resolution

Large-sized millimeter-wave phased-array transceivers with narrow beamwidth are required in 5G. Insufficient beam-steering resolution in such a large-sized array will cause SNR degradation [3]. Fig. 3 shows the calculated

maximum array factor (AF) degradation against the horizontal beam-steering resolution for a 256-element array. Considering complex modulation schemes, such as 64-QAM and 256-QAM, the degradation from AF should be kept under 0.1 dB. From Fig. 3, a horizontal beam-steering resolution of 1.2° is necessary for a 16×16 array. However, for array sizes of 64×4 and 32×8, a less than 1° resolution, corresponding to a phase tuning resolution larger than 6 bits, will be required. The beam-steering resolution improvement can be achieved by using the averaging effect of a large-sized array, which relieves the requirement on the phase-shifting resolution. However, the potentially degraded sidelobe suppression will result in unwanted interference over the whole space [2].

To improve the phase tuning resolution, design considerations are required for the phase-shifting architecture, magnitude and phase errors, power consumption, and area. Adding an additional least significant bit (LSB) to the passive RF phase shifters [12], [21] could improve the resolution, but the circuit for the LSB will induce extra insertion loss and area cost. The gain error performance will also be degraded during the phase shifting. RF active vector summing phase shifters [13], [22] can solve these problems to some degree. However, the limited linearity caused by the variable-gain amplifier (VGA) still requires compensation in the RF path. Phase error due to the I/Q generation mismatch will also arise within the operational bandwidth. As a result, to support accurate beam control with suppressed sidelobe level, the RF gain-invariant LO phase-shifting architecture is adopted in this work. The sidelobe regrowth caused by the gain variation during the phase tuning can be significantly suppressed. When compared with the RF phase shifters, the LO phase shifters only need to cover a limited frequency range. A much-improved phase tuning step with sufficiently small phase error could be achieved by LO phase-shifting architecture.

At the same time, because the LO phase shifters are located in the LO path, the gain variation of the LO phase shifters during the phase tuning will not influence the RF path signal-to-noise-and-distortion ratio (SNDR). As a result, an optimized transceiver SNDR along with stabilized data communication can be realized during the beam steering.

C. Spurious Emissions Limitation

The enlarged array size for a CMOS phased-array transceiver also demands a much more stringent level for spurious radiation [23], [24]. The BS transmitter spurious emission limit defined in 5G NR for FR2 is less than $P_{\text{spur\_TRP}} = -13$ dBm/MHz [25]. Regarding the BS type 2-O requirement, the maximum radiated LO leakage power per element can be found through dividing $P_{\text{spur\_TRP}}$ by N, where N is the array size. When consider a 256-element array, the corresponding $P_{\text{LO\_leak}}$ should be kept under −37.1 dBm. Concerning the image rejection ratio (IRR), a similar equation can be derived

$$IRR > \frac{P_{\text{out}}}{P_{\text{spur\_TRP}} \cdot BW_{\text{t}}} \cdot N \tag{1}$$

where P_{out} denotes the radiated power of the transmitter and BW_{t} is the maximum transmission bandwidth in megahertz for a corresponding BW_c. Fig. 4 shows the LO leakage limitation and the required IRR for a single-element transmitter against the array size. For BW_c of 100 MHz together with P_{out} of 15 dBm, the IRR should be larger than 32.3 dBc for a 256-element array.

Even when the total radiated LO leakage and image power meet the spurious emission limits, careful design is still required for the image and LO leakage radiation patterns. For phased-array transceivers based on the LO phase shifting, all RF frequency components are shifted with the same phase. Thus, beam squinting will occur in the image and LO leakage beams. Fig. 5 shows the analysis model for the image and LO leakage patterns. When the linear array with N isotropic radiators in the figure scans the beam to θ_0, the beam patterns $F_{\text{IM}}(\theta)$ and $F_{\text{LO}}(\theta)$ for the image signal, and the LO leakage, respectively, can be calculated by summing over the transmitter elements. For simplicity, the ωt terms are omitted in the

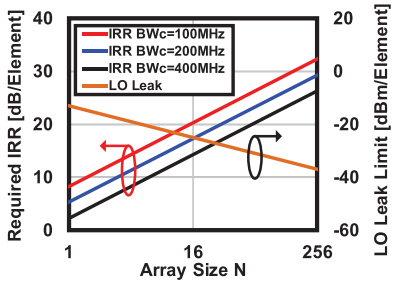


Fig. 4. Calculated LO leakage limitation and the required IRR against the array size N.

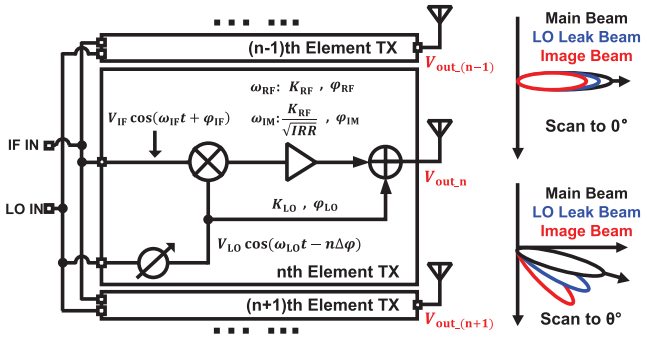


Fig. 5. Analysis model for LO leakage and image signal.

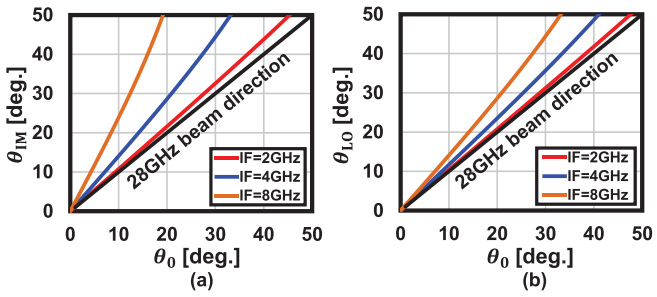


Fig. 6. Calculated (a) image beam direction θ_{IM} and (b) LO leakage beam direction θ_{LO} against RF beam direction θ_0 with different IFs.

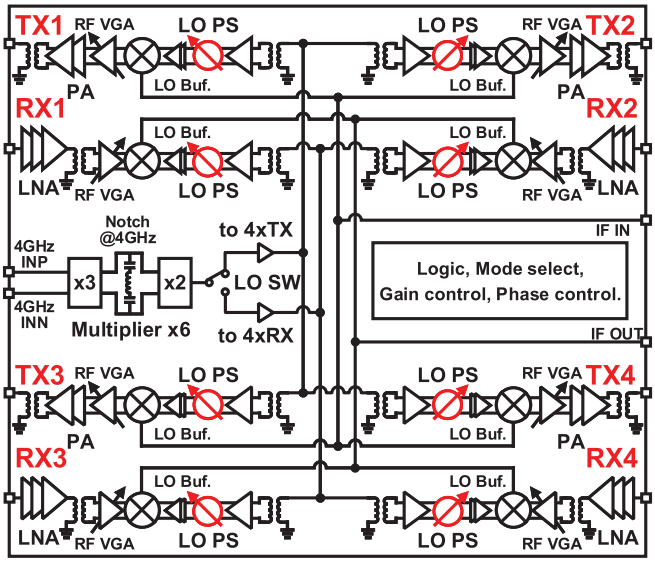


Fig. 7. System block diagram of the proposed phased-array transceiver.

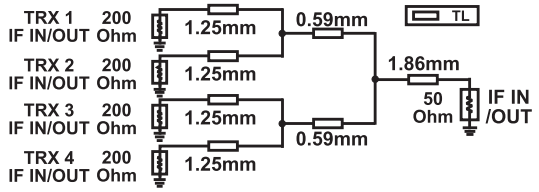


Fig. 8. TL branching network for IF combining and splitting.

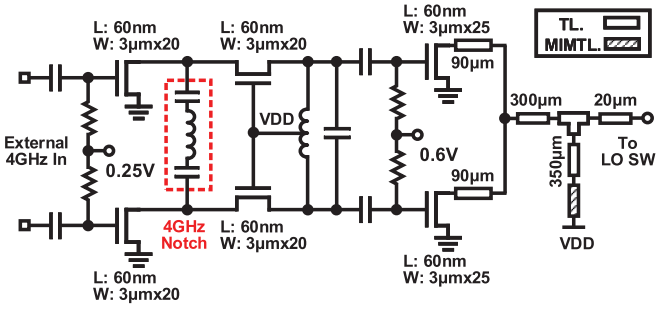


Fig. 9. Circuit schematic of multiplier.

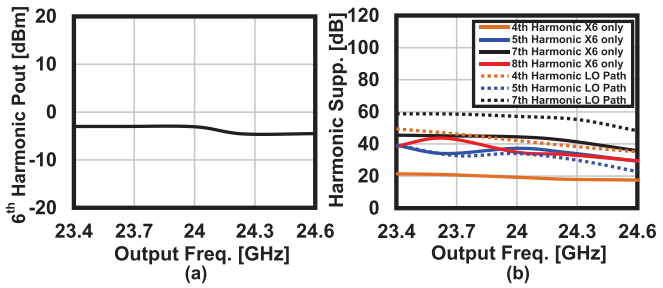


Fig. 10. Measured (a) sixth-order harmonic output power and (b) harmonic suppression for multiplier.

following equations [26]:

$$F_{\mathrm{IM}}(\theta) = \frac{K_{\mathrm{RF}} V_{\mathrm{IF}} V_{\mathrm{LO}}}{2\sqrt{IRR}} \frac{\sin\left[0.5Nd(k_{\mathrm{IM}}\sin\theta - k_{\mathrm{RF}}\sin\theta_0)\right]}{N\sin 0.5d(k_{\mathrm{IM}}\sin\theta - k_{\mathrm{RF}}\sin\theta_0)} \tag{2}$$

$$F_{\mathrm{LO}}(\theta) = K_{\mathrm{LO}} V_{\mathrm{LO}} \frac{\sin[0.5Nd(k_{\mathrm{LO}}\sin\theta - k_{\mathrm{RF}}\sin\theta_0)]}{N\sin 0.5d(k_{\mathrm{LO}}\sin\theta - k_{\mathrm{RF}}\sin\theta_0)} \tag{3}$$

where k_{RF}, k_{IM}, and k_{LO} denote the propagation constants for the RF signal, the image signal, and the LO leakage, respectively, while d represents the spacing between elements. Different from the RF beam direction θ_0, the image and LO leakage beam directions θ_{IM} and θ_{LO} are given as follows:

$$\sin\theta_{\mathrm{IM}} = \frac{\omega_{\mathrm{RF}}}{\omega_{\mathrm{IM}}}\sin\theta_0 \quad \sin\theta_{\mathrm{LO}} = \frac{\omega_{\mathrm{RF}}}{\omega_{\mathrm{LO}}}\sin\theta_0. \tag{4}$$

The analysis above shows that the image and LO leakage also benefit from the AF. When the RF beam is steered to θ_0 ($\theta_0 \neq 0°$), the image and LO leakage beams can point in completely different directions due to beam squinting. In consideration of a 256-element array, the radiated image and LO leakage will cause potential interference. As a result, an intermediate frequency (IF) range of 2.5–5.5 GHz and an LO range of 23.4–24.6 GHz are selected in this work not only due to the frequency generation plan but also because of the directions of LO leakage and image beams. The image and LO leakage in the transmitter are also well-suppressed without any lossy notch filters, which contributes to a power- and area-efficient designs.

III. Circuit Implementation

Fig. 7 shows the block diagram of the proposed four-element phased-array transceiver. A superheterodyne architecture is adopted in this work to remove the in-band LO leakage and image. The element transmitter in this work consists of a two-stage power amplifier (PA), a one-stage RF VGA, and an upconversion mixer, while the element receiver includes a three-stage low-noise amplifier (LNA), a one-stage RF VGA, and a downconversion mixer. Fig. 8 shows the branching network for combining/splitting the 4-GHz IF signal. The branching network is designed using the 50-Ω transmission lines (TLs). The simulated splitting loss is 7.5 dB at 4 GHz, including the splitting ratio and distribution loss. The required 24-GHz LO is generated by multiplying the external 4-GHz signal by six. An amplifier-based LO switch is utilized to redirect the 24-GHz LO to the transmitter array or to the receiver array. The LO distribution in this work is realized in a single-ended formation. The single-ended LO is transformed into a differential before the transceiver elements. The coupling between the LO and the IF distributions can induce gain and phase mismatch among the transceiver elements, so the crossing component for the distribution is carefully designed. The measured coupling ratios are less than −45 dB at 24 GHz and less than −60 dB at 4 GHz. An LO phase shifter designed for the optimized gain and phase errors is utilized to maintain the required phase shifting. A logic block for digital control is also integrated into the chip for controlling the bias and switches. The transceiver chip can be changed between transmitter and receiver modes by the

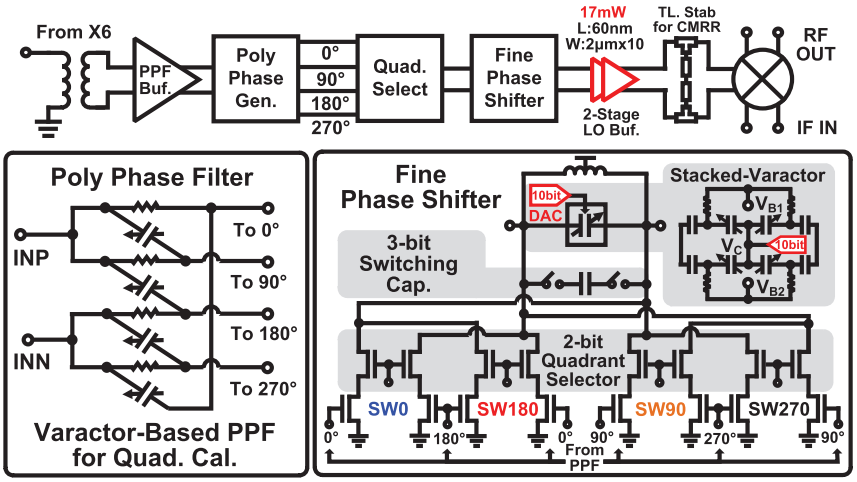


Fig. 11. Block diagram of the LO for each element transceiver and circuit schematic of the proposed LO phase shifter.

logic controller. In addition, functions such as gain control, poly-phase filter (PPF) quad-phase calibration, and fine phase tuning are realized with an external microprocessor through the digital control block.

A. LO

Fig. 9 shows the circuit schematic of the multiplier. This work utilizes a frequency tripler and doubler to realize the required sixfold multiplication. Because the seventh harmonic of the multiplier falls inside the operational bandwidth, harmonic suppression of the multiplier is optimized into consideration of improving the EVM and decreasing the spurious emissions. The proposed tripler has a differential topology [27]. Thus, the even-order harmonics, which fall close to the desired third-order output, are suppressed. To further prohibit the strong external 4-GHz signal from entering the doubler, an *LC* notch filter designed at the fundamental frequency is inserted. The doubler in this work also adopts differential topology. The differential outputs are combined together for suppressing the odd-order components. The output matching networks are designed based on the 50-Ω TLs. The TLs with shunt metal–insulator–metal (MIM) capacitors to ground (MIM-TL) are utilized for the power supply. The gate bias of the doubler is optimized for a higher second-order harmonic [28]. Fig. 10(a) demonstrates the measured saturated power of the desired sixth-order output for a stand-alone multiplier. Within the frequency range of 23.4–24.6 GHz, the saturated output power is around −3 dBm. The measured harmonic suppressions are shown in Fig. 10(b). The fifth-, seventh-, and eighth-harmonic suppressions for the multiplier are larger than 30 dB, while the fourth-harmonic suppression is around 20 dB. The measured harmonic suppressions for the complete LO path, including the multiplier, the LO switch, and the phase shifter, are also shown in the same figure. The fourth-, fifth-, and seventh-order harmonic suppressions at 24-GHz LO frequency are larger than 30 dB.

The proposed LO phase shifter designed for each transceiver element is shown in Fig. 11. To realize a fine phase-shifting step, the 24-GHz LO is first sent for the quad-phase generation. Afterward, the generated quad-phase LOs are selected by a quadrant selector and, finally, shifted by a fine phase-shifting stage. As a result, the fine phase shifter in this work only needs to cover 90°. Thus, a linear and high-resolution phase tuning can be achieved. For the quad-phase generation, a constant-magnitude PPF is adopted in this work [29]. Varactors controlled by the 10-bit digital-to-analog converters (DACs) are utilized in the PPF. The quadrature phase mismatch after fabrication can be compensated by tuning the varactor. A tuning range larger than 20° is maintained at the LO frequency of 24 GHz. With the default bias setting, a PPF phase mismatch of 5.1° is measured at 24 GHz. After tuning the varactor, the phase mismatch is reduced to less than 0.1°. The imbalance of the quad-phase outputs can also be influenced by the input common-mode signal and the load impedance variation. Thus, a differential buffer with enhanced common-mode rejection is inserted before the PPF to suppress the common-mode generated by the on-chip balun. Concerning the load impedance variation during the fine phase tuning, the quadrant selector in this work adopts a cascode switching array topology to provide the required isolation between the PPF and the fine tuning stage. The load impedance variation is suppressed during the phase shifting.

The circuit schematic of the fine phase shifter is also shown in Fig. 11. To cover a 90° tuning range, an *LC* tank is utilized in this work. Considering an LO frequency of ω_{LO} and tank quality factor of Q, the magnitude and phase responses can be expressed using the following equations:

$$A = \sqrt{1 + Q^2\left(\frac{\omega_{\mathrm{LO}}}{\omega_0} - \frac{\omega_0}{\omega_{\mathrm{LO}}}\right)^2}$$
$$\varphi = \arctan\left(Q\left(\frac{\omega_0}{\omega_{\mathrm{LO}}} - \frac{\omega_{\mathrm{LO}}}{\omega_0}\right)\right) \tag{5}$$

where ω_0 denotes the resonant frequency for the *LC* tank. To maintain a phase shift from −45° to +45°, the capacitance tuning range of C_1 to C_2 is required to be covered, where

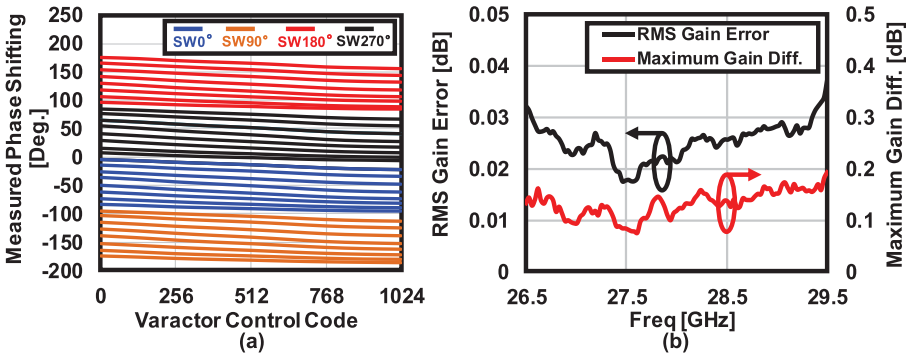


Fig. 12. Measured (a) phase shift at 28 GHz and (b) RF path gain variation and corresponding rms gain error for the LO phase shifter.

C_1 and C_2 are defined by

$$C_1 = \frac{2Q^2}{L\omega_{\mathrm{LO}}^2(2Q^2 + \sqrt{1+4Q^2}+1)} \tag{6}$$

$$C_2 = \frac{2Q^2}{L\omega_{\mathrm{LO}}^2(2Q^2 - \sqrt{1+4Q^2}+1)}. \tag{7}$$

Q for the tank is reduced to extend the capacitance tuning range. The high-resolution phase tuning is realized with a 3-bit capacitor bank together with a 10-bit DAC-controlled varactor. The stacked varactor in this work is designed to achieve a wider phase coverage along with the linear phase tuning. The measured raw gain variation of the phase shifter is 2.7 dB at 24 GHz.

After the LO phase shifter, a two-stage differential LO buffer is inserted. A small transistor size of 0.06 μm/2 μm $\times$ 10 is selected for saturating the LO driving power with reduced power consumption. The two-stage LO buffer only consumes 17 mW when measured. Furthermore, to suppress the LO leakage due to the imbalanced differential LO, a shunt-shorted TL stub for common-mode rejection is inserted before the mixer.

Fig. 12(a) shows the measured phase shift for the proposed LO phase shifter. A 360° tuning range and a tuning step of less than 0.04° are achieved by the proposed circuit. Thanks to isolation from the quadrant selector, the phase control code for the fine stage could be shared within the four quadrants. The measured rms phase error is only 0.3° due to the code sharing. The measured RF gain variation is shown in Fig. 12(b). With the help of the power-efficient LO buffers, the measured RF gain variation is less than 0.2 dB within a frequency range of 26.5–29.5 GHz. The calculated rms gain error is less than 0.04 dB. Thus, an RF gain-invariant, quasi-continuous phase tuning is realized with a sufficiently small phase error, allowing the proposed LO phase shifter to accurately control beam.

The required calibration also benefits from the proposed LO phase shifter. Because of the gain-invariant phase tuning, the accurate calibration could be maintained with a simple procedure. In addition, by choosing the part of the control codes, the phase shifter can be easily configured into a coarse phase-shifting mode if the accurate calibration is not required. The calibration time could be further shortened depending on the required calibration accuracy.

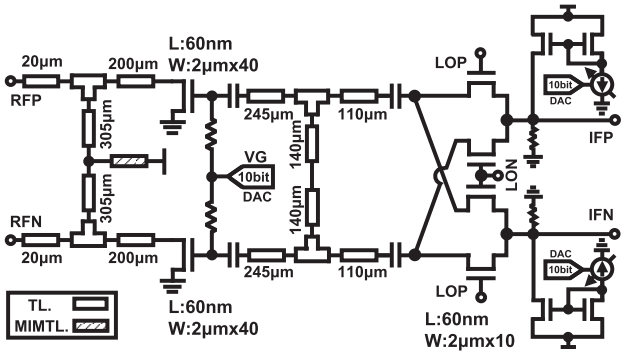


Fig. 13. Circuit schematic of upconversion mixer and RF VGA.

B. Transmitter

The transmitter proposed in this work adopts a differential topology. Fig. 13 shows the upconversion mixer along with the RF VGA. A double-balanced passive mixer is used to suppress the LO leakage through both the IF and RF sides. To save power, the transistor size in the mixer is optimized for a large LO swing. Two current sources are attached to the IF input for adjusting the dc offset [30], [31]. A designed tuning resolution of 0.1 mV is realized by the 10-bit DACs. To calibrate the magnitude mismatch between different elements, a DAC-controlled TL-based RF VGA is used to realize a less-than-0.1-dB gain tuning resolution along with a 10-dB tuning range. The phase variation of the VGA can be easily compensated by gain-invariant phase tuning.

Regarding the 5G CMOS PA design, larger output power with higher power-added efficiency (PAE) is always desirable. To achieve larger power delivery, the PA in this work also adopts differential topology. Fig. 14 shows the circuit schematic of the proposed two-stage PA. The input of the driver stage is designed based on the reliable and compact TL matching. Both the driver and final stages are designed based on the common-source (CS) topology. At the output, a balun optimized with low insertion loss is utilized to combine the differential signals to single-ended. The 3-D model for the

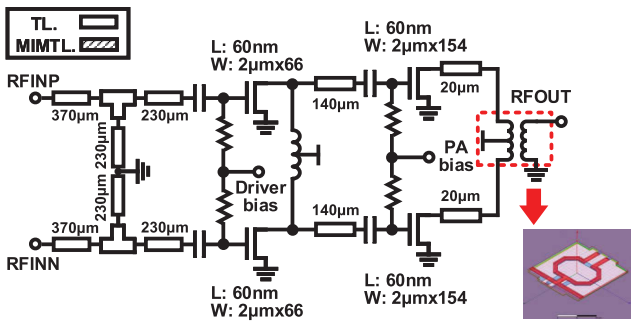


Fig. 14. Circuit schematic of differential PAs.

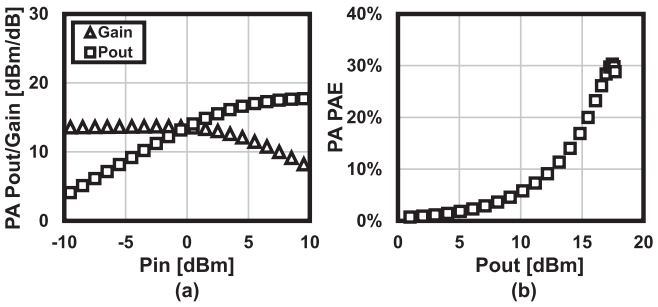


Fig. 15. Measured (a) output power and gain and (b) PAE of PA.

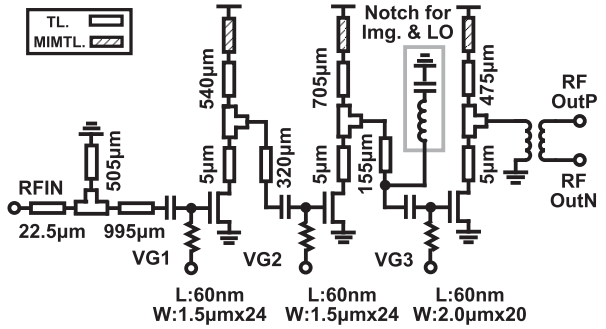


Fig. 16. Circuit schematic of LNA.

balun together with the dc supply line is also shown in the figure. The simulated insertion loss of the balun is 0.6 dB at 28 GHz. Fig. 15 shows the on-wafer measurement result for the stand-alone PA. The measured gain at 28 GHz is 13.5 dB. The achieved saturated output power is 17.7 dBm with an output $P_{1\,\mathrm{dB}}$ of 16.1 dBm. Fig. 15(b) demonstrates the corresponding PAE against the output power. The peak PAE realized by this work is 30.6% at a 17.5-dBm output. The measured PAE at $P_{1\,\mathrm{dB}}$ is 23.2%.

C. Receiver

A 28-GHz receiver demands optimizations with respect to NF and linearity. As a result, a three-stage CS LNA with an optimized NF is utilized in this work. Fig. 16 shows the circuit schematic of the LNA. The single-ended LNA is designed based on TL matching. At the RF input, a shunt stub shorted to ground is applied for electrostatic discharge protection.

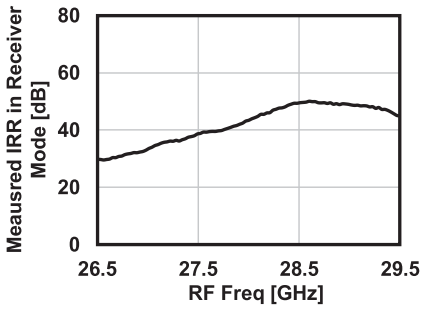


Fig. 17. Measured receiver-mode IRR against input RF frequency.

Regarding the potentially received out-of-band interferences, such as the LO leakage and image mentioned in Section II, an *LC* notch designed at the image and LO frequency is inserted at the third stage. Fig. 17 shows the measured IRR for the receiver against the input RF frequency. The measurement is carried out with a fixed LO frequency of 24 GHz. Within the 5G NR band n257, the measured IRR is always higher than 30 dB. The rejection at the 24-GHz LO frequency is higher than 22 dB. In addition, the single-ended output of the LNA is further transformed into differential output by a 28-GHz balun. A differential RF VGA is inserted to suppress the balun mismatch and provide the variable gain.

The downconversion mixer in LO phase-shifting phased-array transceivers is exposed to spatial blockers. Careful design considerations will be required both in system and building block levels. In this work, a passive double-balanced mixer with an optimized IIP3 is utilized for downconversion. A simulated IIP3 of 15 dBm is achieved for the mixer, which will not limit the blocker-tolerance of system. Facing a strong spatial blocker, the receiving performance can be improved by decreasing the gain of the LNA and RF VGA.

IV. Measurement Results

The proposed 28-GHz four-element phased-array transceiver is fabricated in a standard 65-nm CMOS process. Fig. 18(a) shows a die micrograph of the chip. The chip size is 3 mm × 4 mm. Table I denotes the core area breakdown of the key building blocks. A single-element transceiver occupies an on-chip area of 1.85 mm^2. To evaluate the characteristics of the proposed transceiver array, RF printed circuit boards (PCBs) are designed for the transmitter and receiver arrays separately. Fig. 18(b) shows the PCB for the transmitter array. Two chips are wire-bonded to the PCB. The transmitter outputs from the chips are connected to 50-Ω TLs and further distributed symmetrically to subminiature push-on micro (SMPM) connectors. This work assumes a 0.5-nH bond wire inductance. Matching networks for compensating the inductance are inserted on both the chip and the PCB. The insertion loss of the PCB is measured by comparing the saturated transmitter-mode output power of the on-wafer measurement and the PCB measurement. A PCB loss of 6.04 dB is observed at 28 GHz including the bond wire and the SMPM connectors. The measured magnitude and phase mismatches between channels are less than 2.9 dB and 9.2°, respectively. During the

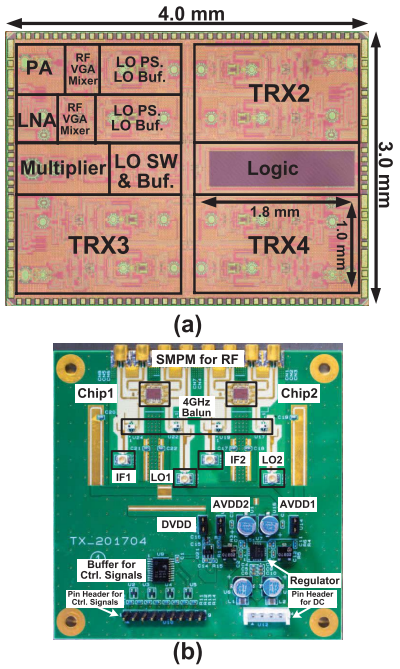


Fig. 18. (a) Die micrograph of four-element phased-array transceiver chip. (b) Photograph of transmitter-mode RF PCB.

TABLE I
CORE AREA OF BLOCKS

Blocks	Core Area $[\mathrm{mm}^2]$
PA	0.18
RF Buf. & Mixer	0.16
LO Phase Shifter & Buf.	0.25
LNA	0.24
Multiplier	0.3
LO SW &Buf.	0.27
Logic	0.64

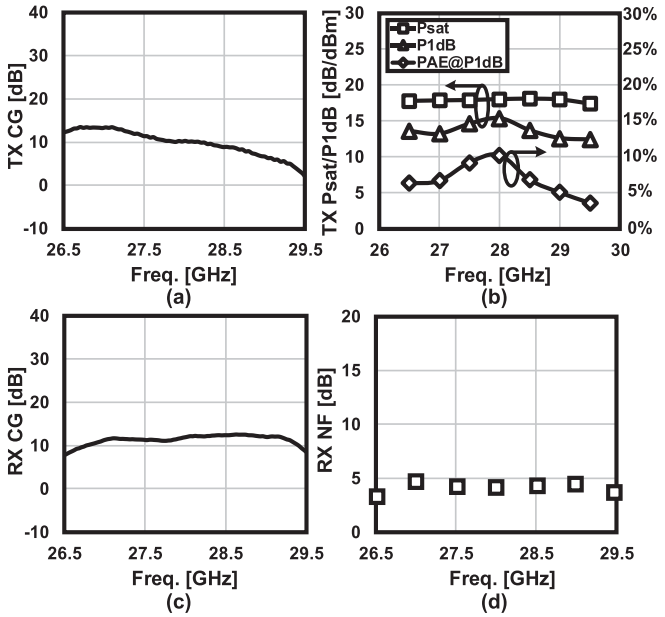


Fig. 19. Measured transceiver characteristics. (a) Transmitter-mode conversion gain. (b) Transmitter-mode linearity and PAE. (c) Receiver-mode conversion gain. (d) Receiver-mode NF.

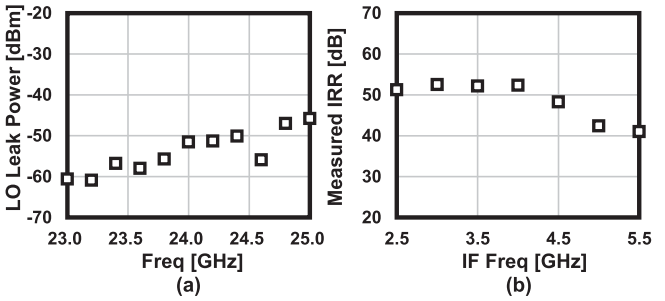


Fig. 20. Measured transmitter-mode (a) LO leakage and (b) IRR.

over-the-air (OTA) measurement, the mismatches are compensated by tuning the RF VGA and LO phase shifter. For evaluating the receiver array, a similar PCB is also implemented.

Fig. 19 shows the measured characteristics of a single-element transmitter and receiver. Within the frequency range of 26.5–29.5 GHz, the measured transmitter-mode conversion gain is around 10 dB. Fig. 19(b) shows the measured on-wafer output power and the PAE at $P_{1\,\mathrm{dB}}$ of the transmitter. The proposed transmitter achieves a saturated output power of 18.0 dBm along with an output $P_{1\,\mathrm{dB}}$ of 15.7 dBm at 28 GHz. The measured 28-GHz PAE is 10.3% at $P_{1\,\mathrm{dB}}$. Fig. 19(c) shows the measured conversion gain against the frequency for the receiver. The flat frequency response of the receiver optimizes the EVM performance. The measured NF for the receiver in this work is less than 5 dB from 26.5 to 29.5 GHz. At 28 GHz, the achieved NF is 4.1 dB. Fig. 20(a) demonstrates the measured LO leakage power against the frequency for the transmitter. A less than −50 dBm leakage power can be observed at 24 GHz. Regarding the image rejection, the measured IRR is larger than 40 dBc from 2.5- to 5.5-GHz IF. Spurious emissions are suppressed by this work.

Fig. 21(a) shows the measured single-carrier (SC) mode EVM in 64-QAM for the transmitter. The peak EVM in 64-QAM is −41.1 dB for a 100-MHz bandwidth and −36.7 dB for a 800-MHz bandwidth. Concerning the required −26-dB transmitter EVM in 64-QAM for a less than 10^{-3} TX-to-RX bit error rate [32], the proposed transmitter achieves a 11.7-dBm output power. Fig. 21(b) demonstrates the measured EVM in 256-QAM. The peak EVMs in 256-QAM are −37.1 and −40.8 dB for the 100- and 800-MHz bandwidths, respectively. An output power of 6.1 dBm in 256-QAM is achieved at the −32.9-dB EVM. Still, a larger than 1-dB margin is left at the output power mentioned above for the required −31.5-dB transmitter EVM in 256-QAM. For the single-element receiver, the output power, IM_3, and the output noise floor are measured at 28 GHz and shown in Fig.21(c). The calculated SNDR of the receiver with a different bandwidth is shown in Fig. 21(d). The maximum SNDRs are 40.8, 39.3, and 38.1 dB for bandwidths of 100, 400, and 800 MHz, respectively.

The transmitter and receiver PCBs are further implemented into eight-element transmitter and receiver modules. Fig. 22 shows a photograph of the transmitter module. A total of eight

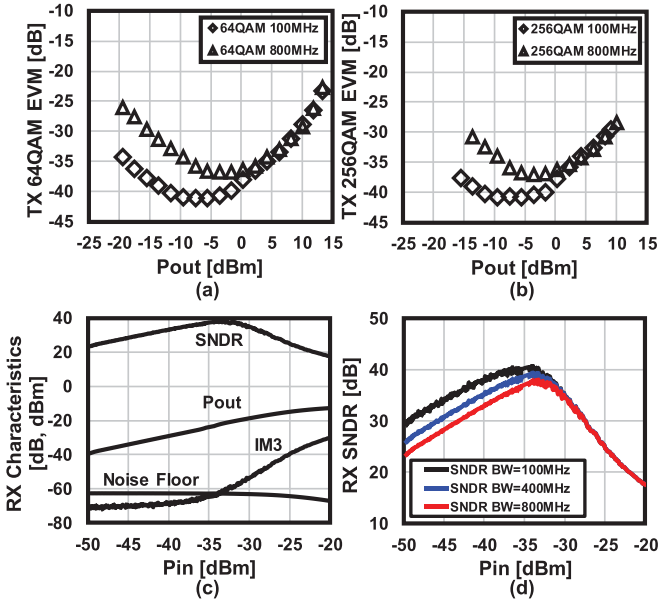


Fig. 21. Measured (a) TX EVM in 64-QAM, (b) TX EVM in 256-QAM, (c) RX output power, IM3, noise floor, and SNDR at 28 GHz, and (d) RX SNDRs with different input signal bandwidths.

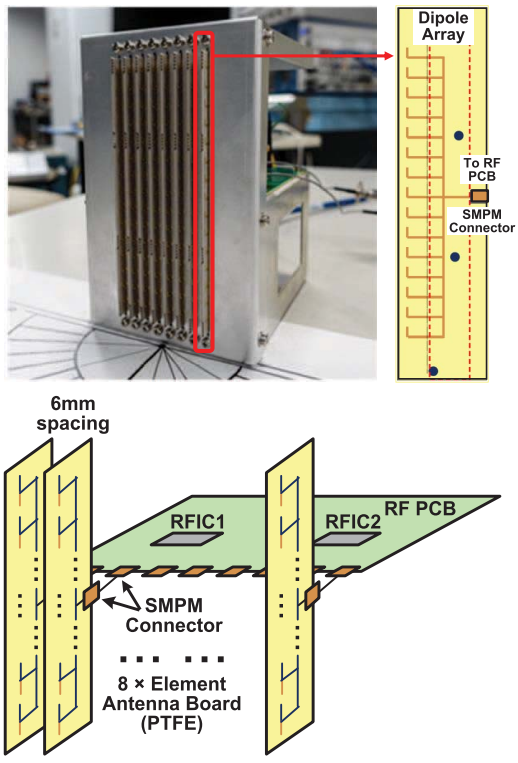


Fig. 22. Photograph and schematics of eight-element transceiver module and dipole-array antenna.

antenna elements are connected to the PCB through the SMPM connectors with a 6-mm spacing. The 15-element dipole-array antennas are utilized for the element antenna in this work [33], [34]. A cosecant-squared shaping beam in elevation is achieved by the dipole array. The measured element-antenna gain at 0° in elevation is 11.9 dBi.

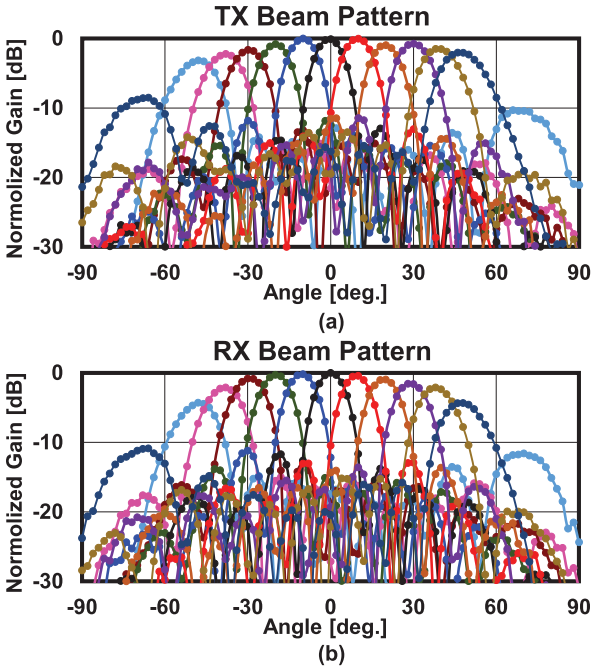


Fig. 23. Measured beam patterns for eight-element transceiver module. (a) TX mode. (b) RX mode.

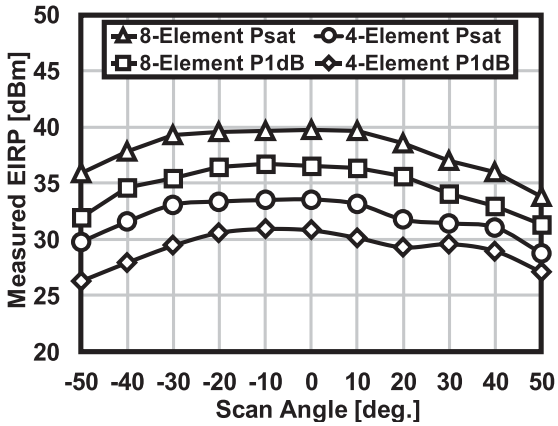


Fig. 24. Measured EIRPs for (a) four-element and (b) eight-element phased-array transceiver modules.

The beam patterns of the eight-element transceiver modules are evaluated with an additional standard gain horn antenna. The normalized beam patterns in the azimuth plane are demonstrated in Fig. 23 with beam scan angles from −50° to +50°. Thanks to the sufficiently small amplitude and phase errors, the measured sidelobe levels are always lower than −9 dBc for the TX mode and −11 dBc for the RX mode. The achieved peak-to-null ratios at 0° scan are higher than 29 and 23 dB for the TX and RX modes, respectively. The measured EIRPs against the beam scan angle for the transmitter module are shown in Fig. 24. The achieved saturated EIRP is 39.8 dBm for eight-element transmitter and 33.6 dBm for the four-element transmitter at 0° scan. The observed 6-dB difference in EIRP matches with the theory. The measured EIRPs at $P_{1\,\mathrm{dB}}$ are 36.5 and 30.8 dBm for the eight-element and four-element transmitters, respectively.

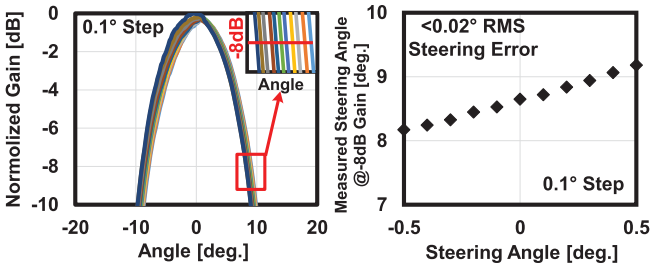


Fig. 25. Measured beam-steering performance of the proposed eight-element phased-array transceiver.

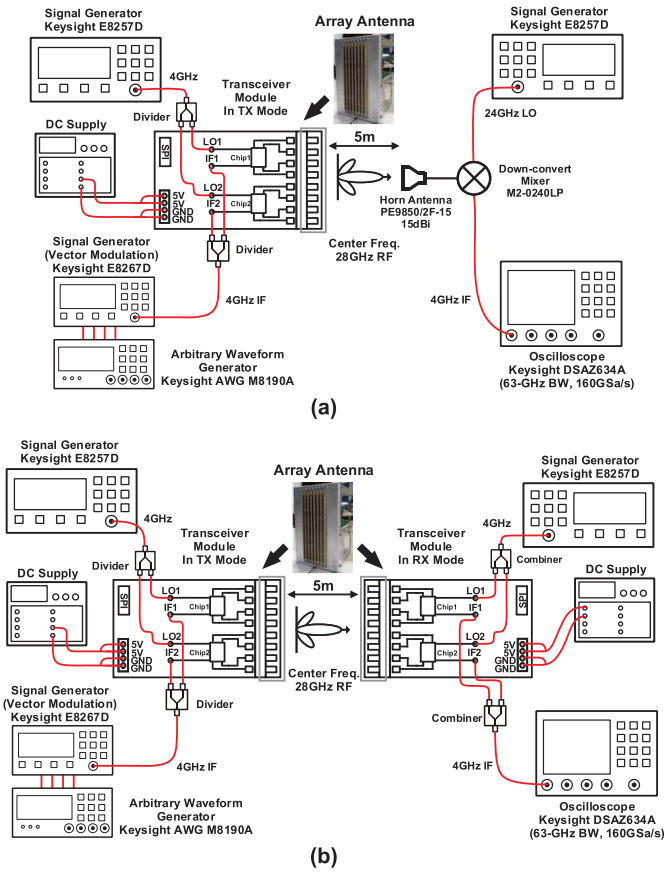
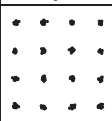
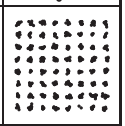
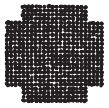


Fig. 26. Equipment setup for the 5-m OTA measurement. (a) TX EVM measurement. (b) TX-to-RX EVM measurement.

The beam-steering performance is also measured. Fine varactor tuning of the phase shifter, which covers 30°, is utilized in this measurement. The proposed transmitter module is capable of steering the beam with a 0.1° resolution from −50° to +50° in azimuth plane with the help of the very-fine phase-shifting resolution. The normalized beam patterns for the beam-steering are shown in Fig. 25. The rms steering error is calculated from the angles at a normalized gain of −8 dB. With the help of the gain-invariant and quasi-continuous phase tuning, the proposed transceiver module demonstrates an rms steering error of less than 0.02° from −0.5° to +0.5°.

During the OTA measurement, the performance of the eight-element phased-array transceiver is also evaluated with

5m OTA Measurement	Modulation	QPSK	16QAM	64QAM
	Symbol rate	2.5GS/s	2.5GS/s	2.5GS/s
	Bandwidth*	3.1GHz*	3.1GHz*	3.1GHz*
	Data rate	5Gb/s	10Gb/s	15Gb/s
	Beam direction	0°	0°	0°
	Constellation**			
	TX EVM (RMS)**	-28.8dB (3.6%)	-28.7dB (3.7%)	-27.9dB (4.0%)
	TX-to-RX EVM (RMS)***	-25.5dB (5.3%)	-25.1dB (5.6%)	-25.2dB (5.5%)

5m OTA Measurement	Modulation	256QAM	512QAM
	Symbol rate	1.6GS/s	0.8GS/s
	Bandwidth*	2.0GHz*	1.0GHz*
	Data rate	12.8Gb/s	7.2Gb/s
	Beam direction	0°	0°
	Constellation**		
	TX EVM (RMS)**	-30.9dB (2.9%)	-35.0dB (1.8%)
	TX-to-RX EVM (RMS)***	-29.3dB (3.4%)	-32.7dB (2.3%)

*The roll-off factor is 0.25.
**Constellation, and TX EVM are measured with an external downconverter.
***TX-to-RX EVM(RMS) is measured through TX and RX, which is equivalent to –SNR(MER).

Fig. 27. Summarized constellation, TX EVM, and TX-to-RX EVM for eight-element phased-array transceiver module in 5-m OTA measurement.

TABLE II
POWER CONSUMPTION OF BLOCKS

	Sub Blocks	Power Consumption [mW]
TX	PA	179.8
	RF Buf.	31.6
	Mixer	0.6
RX	LNA	30.6
	RF Buf.	19.5
	Mixer	0.7
LO	Multiplier	37.1
	LO Switch & Buf.	28.0
	PPF Buf.	44.4
	LO Phase Shifter	10.3
	2-Stage LO Buf.	16.6

the SC-mode modulated signal. Fig. 26 demonstrates the equipment setups for the TX and TX-to-RX constellation measurements. One transmitter module is used for the TX measurement. The modulated signals in QPSK, 16-QAM, 64-QAM, and 256-QAM with a 4-GHz frequency offset are generated by an arbitrary waveform generator (AWG). The radiated signal within a beam angle of −50°–+50° is received by a standard gain horn antenna at a 5-m distance. An external downconverter is utilized to downconvert the received signal to low frequency. The EVM and constellation are evaluated with an oscilloscope. For the TX-to-RX measurement, one transmitter module and one receiver module are utilized. The TX-to-RX EVMs are also tested at a 5-m distance. The beam directions for both modules are set to 0°, 20°, and 50°. The summarized TX constellation, TX EVM, and TX-to-RX EVM at 0° are shown in Fig. 27. Within a 5-m distance, the proposed eight-element module achieves the maximum data rates of 5 Gb/s in QPSK, 10 Gb/s in 16-QAM, 15 Gb/s in

TABLE III
PERFORMANCE COMPARISON OF 28-GHz PHASED-ARRAY TRANSCEIVERS

	This work		Qualcomm [5]	LG [3]	IBM [2]	UCSD [8]	
Process	65nm CMOS		28nm CMOS	28nm CMOS	0.13μm SiGe	0.18μm SiGe	
P1dB/path	15.7dBm		12.0dBm***	9.5dBm***	14.0dBm***	10.5dBm***	
Psat/path	18.0dBm		14.0dBm***	10.5dBm***	16.4dBm***	12.5dBm***	
RX NF	4.1dB		4.4-4.7dB***	6.7dB***	3.7dB***	4.6dB***	
TX Gain/path @28GHz	10dB		15dB*	N/A	32dB	17dB*	
RX Gain/path @28GHz	12dB		15dB*	N/A	34dB	17dB*	
Integration/chip	4xTRX		24xTRX	8xTRX	32xTRX	4xBeam Former	
PDC/path	TX: 299mW @11.0dBm/path RX:148mW		TX: 119mW @11.0dBm/path RX: 42mW	TX: 85mW @3.0dBm/path RX: 50mW	TX: 319mW/pol. @16.4dBm/path RX: 206mW	TX: 200mW @10.5dBm/path RX: 130mW	
Chip Area	12mm^2		29mm^2	7mm^2	166mm^2	12mm^2	
PS Architecture	LO PS		RF PS	RF PS	RF PS	RF PS	
RMS Gain Error	< 0.04dB		N/A	Gain var. < 1dB	Gain var. < 1.5dB	< 0.8dB	
RMS Phase Error	0.3°		N/A	7°	<0.8°	<6°	
Phase Res./Step	2+3+10 bit/0.3° ****		3 bit/45°	3 bit/45°	41 Seg./4.9°	6 bit/6° ****	
Module Array Size	8×1		4×1	4×2	8×8	8×4	
Antenna Integration	Antenna on PCB		Antenna on PCB	Antenna in Package	Antenna in Package	Antenna on PCB	
EIRP@Psat	39.8dBm		35.0dBm/pol.	31.5dBm	54.0dBm/pol.	45.0dBm	
Polarization	Single-Pol.		Dual-Pol.	Dual-Pol.	Dual-Pol.	Single-Pol.	
Dimensions of Beam Scanning	Azimuth only		Azimuth +Elevation	Azimuth +Elevation	Azimuth +Elevation	Azimuth +Elevation	
Beam Steering Res.	0.1°		N/A	N/A	1.4°	1°	
Distance	5.0m		N/A	2.5m	N/A	5.0m	
Constellation	64QAM	512QAM	64QAM	64QAM	256QAM*	16QAM	256QAM
Max Symbol Rate	2.5GS/s	0.8GS/s	0.4GS/s (TX only)*	20MS/s	N/A	1.5GS/s	0.25GS/s
Max Data Rate	15Gb/s	7.2Gb/s	N/A	120Mb/s	3.5Gb/s*	6Gb/s	2Gb/s
TX-to-RX EVM (800MS/s)	1.7%**	2.3%**	TX EVM=0.9% (100MS/s)	3.5% (20MS/s)	N/A	6.1%*	2.1% (250MS/s)

* Estimated from the material. ** Referred to the RMS magnitude of the constellation. *** TRX switch included. **** Step limited by phase error.

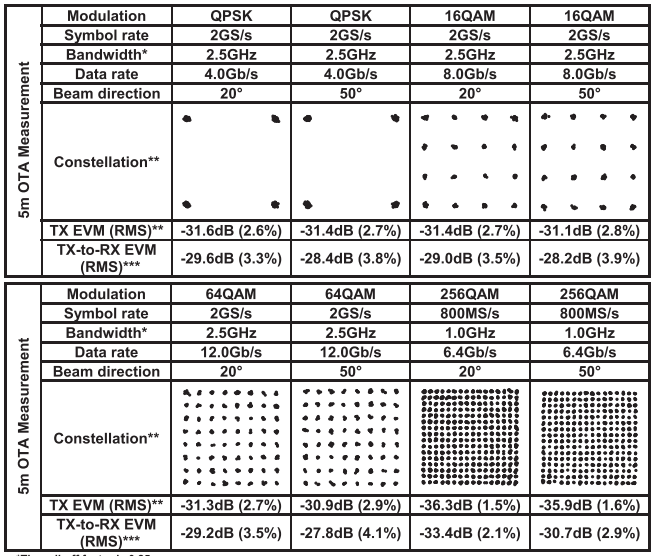


Fig. 28. Measured beam-scan performance of eight-element phased-array transceiver module in 5-m OTA measurement.

64-QAM, 12.8 Gb/s in 256-QAM, and 7.2 Gb/s in 512-QAM. The corresponding TX EVM and TX-to-RX EVMs are, respectively, −28.8 and −25.5 dB for QPSK, −28.7 and −25.1 dB for 16-QAM, −27.9 and −25.2 dB for 64-QAM, −30.9 and −29.3 dB for 256-QAM, and −35.0 and −32.7 dB for 512-QAM. All of the measured EVMs meet the requirements for a bit error rate of 10^{-3}. The beam scan performance summary of the eight-element module is demonstrated in Fig. 28. At a 5-m distance, the data streams of 2 GSymbol/s in QPSK, 16-QAM, and 64-QAM and 800 MSymbol/s in 256-QAM are supported by the proposed module within ±50°. Data rates of 4 Gb/s in QPSK, 8 Gb/s in 16-QAM, 12 Gb/s in 64-QAM, and 6.4 Gb/s in 256-QAM are realized.

Table II shows the power consumption breakdown for the proposed phased-array transceiver. The measured power consumption in transmitter mode for the whole chip is 1.2 W at an output power of 11 dBm per path. In receiver mode, the power consumption is 0.59 W. Table III shows the comparison of this work with some state-of-the-art 28-GHz phased-array transceivers. The proposed LO phase-shifting transceiver chip achieves measured rms gain and phase errors of less than 0.04 dB and 0.3°, respectively. Excellent transmitter linearity and receiver NF characteristics are also maintained with moderate power consumption. Regarding the 5-m OTA measurement, the proposed eight-element module reports the constellations up to 512-QAM. The achieved data rates in 256-QAM and 512-QAM are 12.8 and 7.2 Gb/s, respectively. A maximum data rate of 15 Gb/s in 64-QAM is realized by the module.

V. Conclusion

In this work, a CMOS 28-GHz four-element phased-array transceiver designed for 5G NR is implemented. The proposed transceiver based on the LO phase-shifting architecture achieves an RF gain-invariant and continuous phase tuning. The measured rms gain and phase errors are less than 0.04 dB and 0.3°, respectively. The accurate beam control can be supported by this work. For a single-element transceiver, a transmitter mode $P_{1\,\mathrm{dB}}$ of 15.7 dBm and a receiver mode NF of 4.1 dB are maintained with moderate power consumption. The eight-element transceiver modules developed in this work are capable of scanning the beam from $-50°$ to $+50°$ with a suppressed sidelobe level. During the 5-m OTA measurement, the proposed eight-element modules report the first 512-QAM constellation in the 28-GHz band. A data rate of 15 Gb/s in 64-QAM is realized by the modules. In addition, within a beam scan angle of $\pm 50°$, the developed modules support 6.4-Gb/s data rate in 256-QAM.

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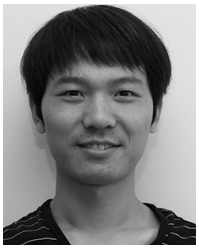

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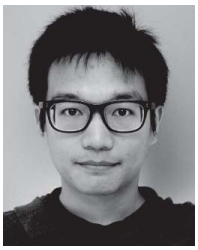

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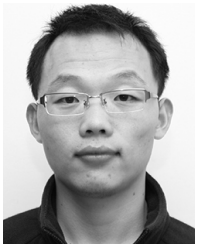

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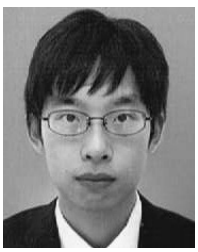

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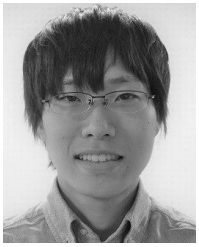

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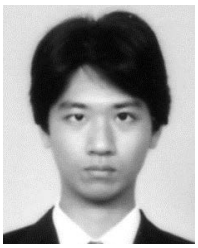

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