A Nonuniform Sparse 2-D Large-FOV Optical Phased Array With a Low-Power PWM Drive

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***Abstract*— Integrated optical phased arrays (OPAs) capable of adaptive beamforming and beam steering enable a wide range of applications. For many of these applications, a large scale 2-D OPA with full phase control for each radiating element is essential to achieve a functional low-cost solution. However, the scalability of such OPAs has been hampered by the optical feed distribution difficulties in a planar photonics process, as well as the high power consumption associated with having a large number of phase control units. In this paper, we present a two-chip solution low-power scalable OPA with a nonuniform sparse aperture, providing radiation pattern adjustment and feed distribution feasibility in a CMOS compatible silicon photonics process. The demonstrated OPA with a 128-element aperture achieves the highest reported grating-lobe-free field-of-view (FOV)-to-beamwidth ratio of 16°/0.8°, which is equivalent to a 484-element uniform array. This translates to at least 400 resolvable spots, 30 times more than the state-of-the-art 2-D OPAs. Moreover, by utilizing compact phase shifters in a row–column power delivery grid, we reduce the number of required drivers from 144 to 37. A high-swing pulsewidth modulation (PWM) driving circuit featuring breakdown voltage multipliers and soft turn-on activation significantly reduces the power consumption of the system. The electronic driver chip and the integrated photonic chip are fabricated on a 65-nm CMOS process and a thick silicon-on-insulator (SOI) silicon photonics process, occupying 1.7 mm^2 and 2.08 mm^2 of active area, respectively.**

***Index Terms*— Free-space optical communication, integrated optics, light detection and ranging (LiDAR), nonuniform sparse aperture, optical phased array (OPA), optical switching devices, optoelectronics, phased array imaging systems, silicon photonics.**

I. Introduction

FORMING and steering an optical beam has a wide range of applications, such as target detection and tracking [e.g., light detection and ranging (LiDAR)], volumetric mapping and surface metrology, optical wireless communication, and image projection [1], [2]. Optical beamforming and beam steering have been demonstrated utilizing mechanical and electrical approaches, such as using a deflecting mirror [3], micro-electro-mechanical (MEMs) device arrays [4], [5], gradient refractive-index-based systems [6], and liquid crystal cell arrays [7]. However, these approaches are generally bulky, slow, expensive, and prone to failure. Moreover, many of these approaches are limited to simple steering of an existing beam and are generally incapable of arbitrary waveform generation.

Coherent arrays, such as phased arrays, are capable of waveform manipulation (e.g., forming and steering beams) purely by controlling the relative phase and amplitude of the waveform at each element. They do not require any mechanical movement, and have been used extensively in RF, microwave, and mm-wave systems [8]. Effective realization of an *optical* phased array can open up many new opportunities. Due to the smaller wavelengths of interest and the benefits of a large number of elements, on-chip integration of optical phased arrays (OPAs) presents a natural path for implementation with the typical benefits of cost and form factor reduction.

Reliable integration of a reasonably large number of optical components in silicon-based process technologies has become possible using various flavors of silicon-on-insulator (SOI) processes, which can be made in a compatible fashion with commercial CMOS. This new possibility enables a broad range of new architectures and system applications [9], [10], reminiscent of the state of integrated electronics in the 60′s and 70′s. There have been several different attempts at implementing functional OPA transmitters and receivers on silicon photonic platforms [11]–[27].

Silicon photonics platforms are often based on an SOI process (Fig. 1), where the top silicon layer is etched and doped to realize passive and active elements, such as dielectric waveguides, power splitters/combiners, phase shifters, grating couplers, and optical modulators. These components operate at wavelengths above $\lambda = 1.1\ \mu$m to avoid photon absorption due to the silicon bandgap. The performance of a photodetector is often enhanced by the inclusion of a germanium layer, which has a lower bandgap and enables efficient photon absorption for wavelengths up to $\lambda = 1.8\ \mu$m. There are also metal layers for routing and electrical access to the devices. Most of today′s silicon photonics processes provide a single layer of silicon with multiple etch depths. This presents optical routing challenges in the implementation of certain complex systems using a large number of components.

In a regularly spaced phased array, the number and spacing of elements play a central role in its beamforming and beam-steering capabilities by affecting the beamwidth, angular resolution, grating lobe spacing, and power. Increasing the number of elements reduces the beamwidth, while increasing the spacing of the elements (above $\lambda/2$, where λ is the

Manuscript received September 10, 2018; revised December 24, 2018 and January 24, 2019; accepted January 26, 2019. Date of publication February 22, 2019; date of current version April 23, 2019. This work was supported by Caltech Innovation Initiative. This paper was approved by Guest Editor Mona Hella. *(Corresponding author: Reza Fatemi.)*

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Digital Object Identifier 10.1109/JSSC.2019.2896767

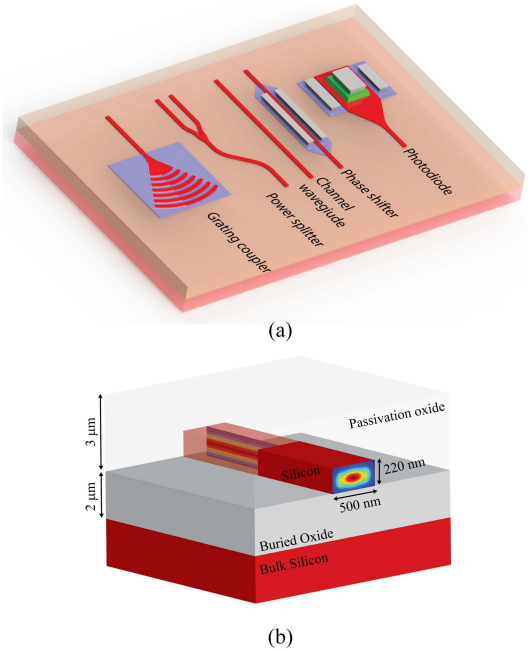


Fig. 1. (a) Simplified schematic of a typical silicon photonics platform consisting a bulk silicon substrate and a buried oxide layer (BOX). Optical components are fabricated using the silicon layer on the BOX. (b) Single-mode dielectric channel waveguide, mostly used to route a guided optical wave on silicon photonics chips.

wavelength) results in (often undesirable) grating lobes in the radiation pattern. Achieving a small element spacing does not present as great a challenge in 1-D OPAs [17]–[23], where long and narrow elements can be tightly packed. However, a 1-D OPA cannot be steered in both directions without a more complex and expensive precise tunable laser source, which also compromises its spectral purity and multibeam projection capabilities. Integrated 2-D OPAs, capable of single wavelength 2-D beam steering using purely electronic element-level full phase control, have been demonstrated for a small number of elements with a limited grating lobe-free field-of-view (FOV) [24]–[26], [28]. However, scaling such 2-D arrays to a large number of elements presents a major challenge due to the area required for optical feed distribution, relatively large size of the optical antennas compared to the wavelength, and electromagnetic (EM) interaction between elements. These issues enforce a large minimum inter-element spacing which leads to multiple closely spaced grating lobes, limiting the OPA′s useful FOV. Moreover, attempts to implement a pseudo-random array of radiating sources that are locked together results in limited FOV due to the large size of the light emitting laser cells [28].

Another major issue in scaling integrated OPAs is the power consumption of both the phase shifters and their driver circuitry, which scales with the size of the array. A useful OPA needs to provide independent phase control for individual elements in order to achieve full 2-D steering and enable phase calibration to mitigate fabrication mismatch, crosstalk between phase shifters, and thermal and electrical drifts. However, this results in high power consumption and necessitates a large number of interconnects between the optical and electrical components, increasing the complexity and the chip area occupied by the system.

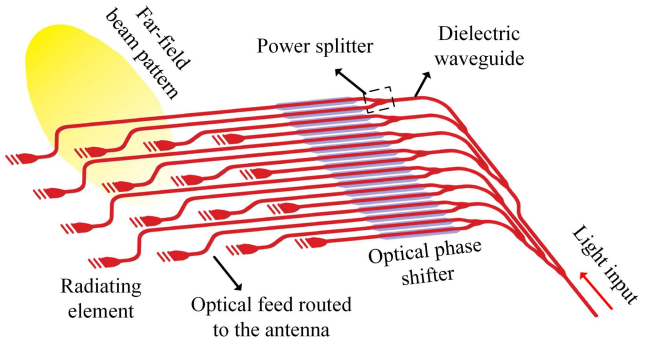


Fig. 2. Simplified diagram of an integrated silicon photonics OPA transmitter including an input optical signal which is routed on-chip using dielectric waveguides, a power splitter tree, phase shifter network, and an array of radiating elements.

In this paper, a scalable 2-D OPA architecture is presented utilizing a sparse aperture and a low-power pulsewidth modulation (PWM)-driven phase shifter network with a row–column electrical access. A phased array synthesis algorithm is developed for designing 2-D nonuniform sparse apertures that provide enough room for planar optical feed distribution in a silicon photonics process while adjusting the far-field radiation pattern for minimum sidelobe and beamwidth. A proof-of-concept sparse aperture OPA on a 27×27 uniform grid is implemented that achieves a grating-lobe-free FOV and beamwidth equivalent to that of a 484-element uniform array—a specification which is not feasible to achieve using conventional architectures due to planar routing difficulties [29]. To reduce the power consumption of the OPA, a switching PWM-driven phase shifter network with compact phase shifters and a row–column power delivery grid is designed that significantly reduces the number of required electrical drivers and increases their efficiency [30].

II. Silicon Photonics OPA With a Sparse Aperture

To implement a 2-D phased array capable of beam steering, an array of radiators (e.g., implemented as silicon grating couplers) must be fabricated on the chip. In a single layer silicon photonic process, the optical signals need to be phase shifted and routed to these radiators using dielectric waveguides in the same silicon layer [25], as shown in the simplified model of an integrated OPA in Fig. 2. Directive transmission and beam steering are performed by controlling the relative phase of the optical wave fed to each radiating element by means of electronically tunable phase shifters, similar to conventional microwave arrays [8]. While this may be manageable for small arrays, the spacing of the elements will need to increase to accommodate the routing waveguides as the number of elements increases. In addition, a minimum spacing is required between adjacent waveguides and/or radiators to keep the coupling at a minimum satisfactory level. This increase in spacing, in turn, results in a larger number of closely spaced grating lobes in the radiation patterns of the 2-D OPAs, as shown in Fig. 3.

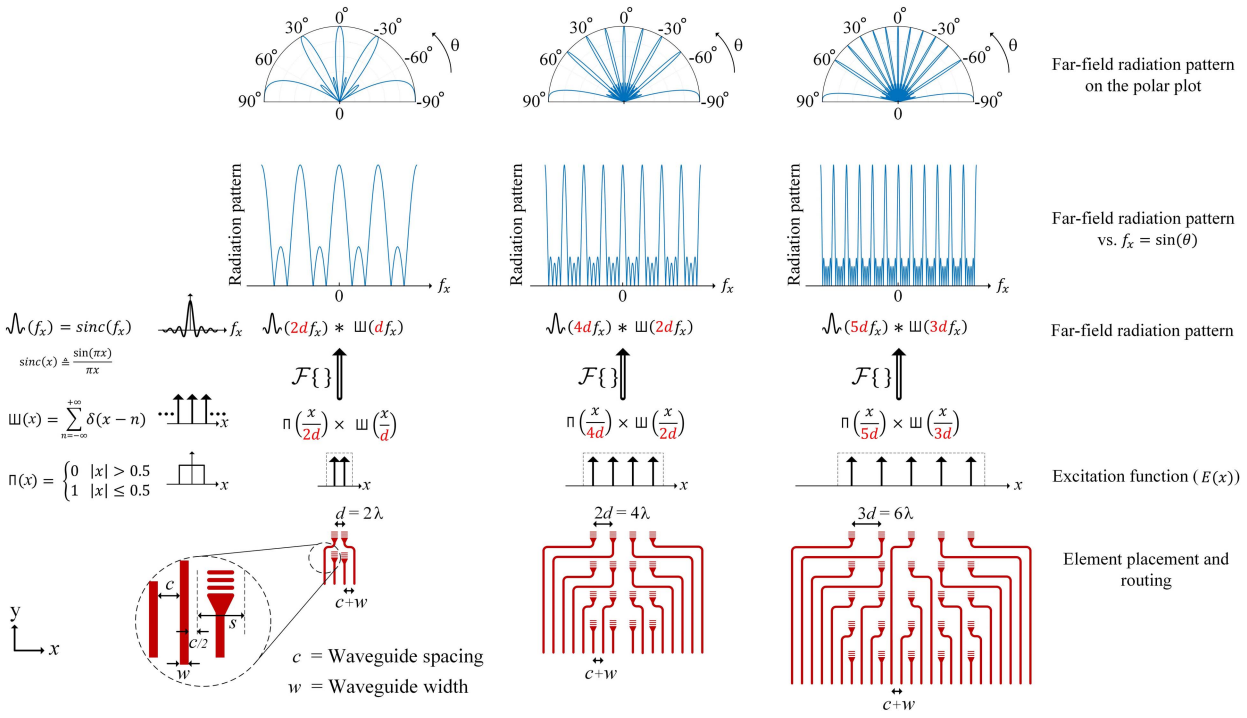


Fig. 3. Illustration of the large inter-element spacing imposed by the optical feed distribution as the array size scales. The excitation of the three different 2-D arrays is modeled as windowed impulse trains. Fourier transform of the excitation yields the far-field pattern of the array. As the element spacing of the array increases and impulses are spaced further apart, grating lobes get more compact as the *scaling* theorem predicts for Fourier transform.

We can gain a better understanding of the impact of element placement and spacing on the far field by noting that the far-field pattern, $P(\theta, \phi)$, for an electromagnetically active surface with a complex field profile of $E(x, y) = a(x, y)e^{i\psi(x,y)}$ on the xy plane is given by a modified Fourier transform, that is,

$$P(\theta,\phi) = \mathcal{F}\{E(x,y)\} = \iint_{-\infty}^{\infty} E(x,y)e^{-i2\pi(xf_x+yf_y)}dxdy$$
$$= \iint_{-\infty}^{\infty} a(x,y)e^{i\psi(x,y)}e^{-i2\pi(xf_x+yf_y)}dxdy \quad (1)$$

where

$$f_x = \frac{1}{\lambda}\sin\theta\cos\phi, \quad f_y = \frac{1}{\lambda}\sin\theta\sin\phi \quad (2)$$

in which θ and ϕ are the elevation and azimuth angles, respectively, and λ is the free-space wavelength. This relationship can be derived by breaking the electromagnetically active surface into infinitesimal segments $dxdy$, and calculating the far-field radiation pattern by coherent sum of the field generated by each segment. For the segment at coordinates (x, y), there is a path length difference l_{xy} for the radiated wave reaching a point in the far field at θ and ϕ compared to the segment at the origin. This path length difference corresponds to a phase shift of $2\pi l_{xy}/\lambda = 2\pi(xf_x + yf_y)$. The overall far-field radiation pattern is the continuous sum (integral) of the field generated by each segment while accounting for their different path lengths, l_{xy}, as in (1).

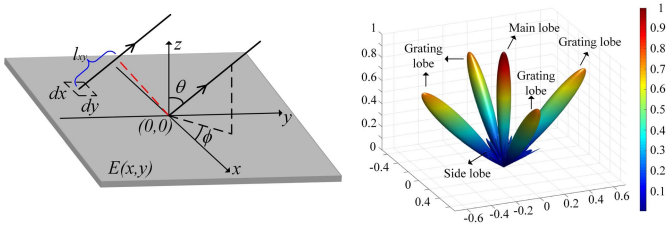
In many practical implementations, the excitation function, $E(x, y)$, can be estimated by an array of discrete radiating point sources. These discrete sources can be viewed as impulses (Dirac deltas), and hence, the field profile of a finite uniform array with element at coordinates $(x_m, y_n) = (\text{md}, \text{nd})$ (d is the element spacing) can be expressed as

$$E(x,y) = a(x,y)e^{i\psi(x,y)} = \sum_{m,n} a_{\text{mn}}e^{i\psi_{\text{mn}}}\delta(x-\text{md}, y-\text{nd}) \quad (3)$$

which through (1) immediately translates to the better known expression

$$P(\theta,\phi) = \mathcal{F}\{E(x,y)\} = \sum_{(m,n)} a_{\text{mn}}e^{-i\frac{2\pi}{\lambda}l_{\text{mn}}+i\psi_{\text{mn}}}$$
$$l_{\text{mn}} = \text{md}\sin\theta\cos\phi + nd\sin\theta\sin\phi \quad (4)$$

where a_{mn} and ψ_{nm} are the amplitude and phase of the wave generated by the element at (md, nd). Fig. 4(b) shows the far-field pattern of a 4×4 array with $d = 1.5\lambda$ element spacing and $\psi_{\text{nm}} = 0$ for all the elements, illustrating the main beam, grating lobes, and side lobes.



(a) (b)

Fig. 4. (a) Active EM surface with a continuous excitation $E(x, y)$. The far-field radiation pattern can be calculated by breaking the surface into infinitesimal segments and count for the contribution of each segment considering its path length difference l_{xy} for angles θ and ϕ. (b) Far-field radiation pattern for a 4×4 uniform array with $d = 1.5\lambda$ element spacing.

The effect of routing and the effect of area occupied by the optical feed distribution on the far-field radiation pattern are visualized in Fig. 3. In this figure, three uniform 2-D arrays with different element counts and their associated feed distributions are illustrated. The field profile $E(x, y)$ and the far-field pattern are shown in 1-D to simplify the visualization and are equally applicable to the 2-D case. In the 1-D case ($\phi = 0$), l_{xy} reduces to l_x and the Fourier transform will be in terms of the variable $f_x = (1/\lambda)\sin(\theta)$, as shown in Fig. 3. The three different arrays are each modeled by a finite number of uniformly spaced impulses; these arrays require increased element spacing due to routing constraints as the number of elements grows. This can be mathematically shown as the product of an infinite impulse train with impulse spacing of kd, i.e., $\sqcup\!\sqcup(x/\mathrm{kd})$ and a truncating pulse of $\sqcap(x/\mathrm{Nd})$. The far-field pattern is the Fourier transform of this product, which is the convolution of an impulse train and a *sinc* function, defined as $\sin(\pi x)/(\pi x)$ [the Fourier transforms of the two functions $\sqcup\!\sqcup(x/d)$ and $\sqcap(x/(Nd))$, respectively] and plotted versus f_x and versus θ on the polar plots shown in Fig. 3. Based on the *scaling theorem*, stretching $E(x, y)$ by a factor of α squeezes its Fourier transform by the same factor. Therefore, scaling the optical 2-D array results in closely compacted grating lobes and a limited useful FOV.

As explained earlier, the relatively large size of the optical waveguides and optical antennas—and consequently, the large area required for the optical feed distribution—is the main challenge in scaling the 2-D photonic array. Generally, the size of the silicon photonics components and waveguides is limited by the wavelength of interest ($\lambda = 1550$ nm in this design) and the refractive index (for silicon, $n = 3.47$). Despite silicon's relatively large n, the necessary mode confinement at $\lambda = 1550$ nm still results in large footprint compared to the wavelength. While a multi-layer photonics process could alleviate the routing limitation to some extent, the complexity, cost, and area overhead of such approaches present alternative challenges to the realization of large scale OPAs.

In general, for a uniform $N \times N$ array with element spacing d and antenna size s, the useful waveguide routing space at the circumference of the array is $4(N-1)(d-s)$. Therefore, the maximum number of waveguides that can be routed to feed the $N \times (N-1)$ elements with waveguide feed routed into the array is $4(N-1)(d-s)/(c+w)$, in which w is the waveguide width and c is the minimum waveguide spacing to avoid coupling (Fig. 3). As a result, the total number of optical feed for the N^2 elements imposes a limit of

$$N_{\max} \leq \frac{4(d-s)}{c+w} \tag{5}$$

on the maximum number of elements that can be embedded in the aperture. This indicates that scaling the array requires an increased element spacing as well. Moreover, it is assumed in (5) that all the four sides of the aperture are used for routing. However, in a practical design, the minimum waveguide bend radius reduces the feasible room for routing and further restricts the number of elements embedded in the array.

The inter-element spacing of the discrete radiating elements, which are used to estimate $E(x, y)$, can also be nonuniform

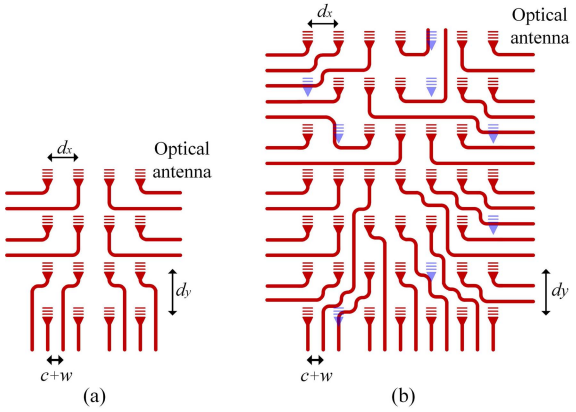


Fig. 5. (a) 4×4 uniform array with element spacings d_x and d_y. The size of the array with this spacing is limited to the optical feed distribution feasibility. (b) 41-element nonuniform sparse array on a 7×7 grid with the same grid spacing of d_x and d_y that results in the same grating lobe-free steering range. Blue antennas show the non-occupied spaces on the grid. The sparse array achieves a larger scale and a better performance due to the larger number of elements.

creating a sparse array. Although uniform arrays are more commonly used and are mathematically more tractable, a sparse array can potentially be designed to have the free space for the optical feed distribution necessary to implement a large scale OPA. Fig. 5 illustrates the scaling feasibility of the sparse array as opposed to a uniform array with two exemplary arrays. The sparse array can accommodate more elements (41 elements compared to 16 elements shown in Fig. 5) and potentially achieve a narrower beamwidth and lower sidelobe level. In addition to the scaling feasibility, sparse element placement provides additional degrees of freedom for adjusting the array factor to trade sidelobe and beamwidth properties. Since the aperture is larger than a uniform 41-element array, narrower beamwidth is also achievable. Since all the inter-element spacings are divisible by a common unit, which means that the elements are on a not-fully populated uniform grid, the radiation pattern is a periodic function with the same period of a uniform array on the same grid, and thus, the same grating lobes spacing.

Conventionally, sparse arrays have been used in electronic systems for applications with a narrow beamwidth requirement [31]. A large aperture array has a narrow beamwidth but the complexity, handling difficulties, and cost of the large number of elements in a large uniform array is undesirably immense. Some applications require a narrow beamwidth, but do not necessarily require the largest possible antenna gain; in these cases, some of the elements can be removed which results in a sparse array at the cost of increased sidelobe levels (within the tolerance of the system). Although the selection of the elements to be retained in the array has a great impact on the radiation pattern, there is no closed form solution for deriving the optimum set of elements for a specific array requirement. Therefore, various optimization algorithms [32]–[35] as well as random element placement techniques [36], [37] were investigated, which are mainly focused on keeping the peak or the average sidelobe level below the required limit while reducing the number of elements.

Sidelobe level of a sparse array reduces as the number of elements increases [31]. However, the rate of reduction is slower than a fully populated grid. This results in a smaller directivity for sparse arrays compared to uniform arrays. However, for OPA design, a sparse array is desirable due to the significantly lower complexity, acceptable array performance, and smaller number of elements. In designing a sparse OPA, in addition to element locations, amplitude of the optical wave fed to each radiating element can be adjusted to achieve a better performance as has been done for electrical phased arrays [33], [38].

As explained earlier, a sparse array structure can be used to scale the aperture of an OPA. Therefore, the purpose of using a sparse array in an integrated OPA as proposed here is to place a larger number of elements in the aperture, which stands in marked contrast to conventional sparse arrays in the RF and microwave domains, where thinning the array minimizes the number of elements. Moreover, there are stronger criteria beyond a well-shaped radiation pattern for designing a sparse aperture OPA, which is the feasibility of implementing the feed distribution network. Therefore, conventional sparse array design methods and the limitations they face are not pertinent here and a different design approach should be devised for a sparse aperture OPA.

III. Aperture Design

The aperture of an OPA transmitter is an array of nano-photonic antennas fed with phase-adjusted optical signals. The antennas are transducers, coupling the guided light to the free space mode. As mentioned in section II, in a silicon photonics OPA, both the antenna and the array designs face serious challenges due to the large sizes of the optical components. Therefore, on one hand, designing a small footprint antenna with a high radiation efficiency is necessary to avoid large element spacings and a limited steering range. On the other hand, a sparse array aperture with well-designed inter-element spacings is required to implement a large scale OPA. In this section, the design of the nano-photonic antenna and the array is explained.

A. Nano-Photonic Antenna

An optical antenna is often made of a dielectric material to avoid high optical loss in the antenna structure. Moreover, it should provide sufficient beamwidth in both θ and ϕ directions for beam steering. Conventionally, grating couplers have been used for radiating light off the chip [25]. However, a standard grating coupler has a large footprint, which is not desirable for the array. Here, a custom nano-photonic antenna [shown in Fig. 6(a)] is designed which has compact dimensions of 2 μm $\times$ 5 μm. This antenna is comprised of a tapered slab for broadening the optical mode delivered by the feed waveguide, and multiple dielectric sections perpendicular to the direction of propagation for diffracting the light and radiating it into free space. Moreover, a slab layer is placed inline with the propagation of light to help in confining the light in the antenna region. The two pieces on the sides both diffract part of the wave propagating to the sides as well as being part of the routing network. These pieces are holistically designed with the antenna to improve its performance. Fig. 6(b) shows the radiation pattern of the antenna that achieves 51% radiation efficiency at a wavelength of 1550 nm with a small footprint.

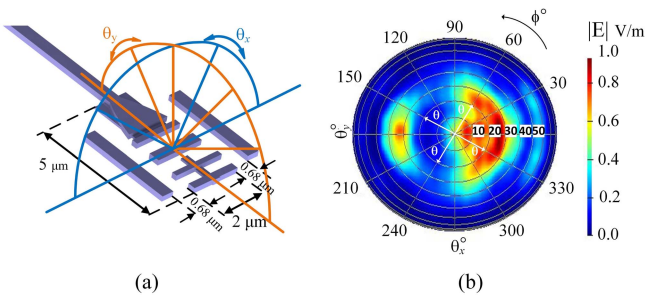


Fig. 6. (a) Schematic of the nano-photonic antenna. (b) Far-field radiation pattern of the antenna.

B. Sparse Array Design

For designing the sparse array aperture, we developed a genetic optimization algorithm [39] that searches for an array with the desired specifications. A set of constraints are defined in the algorithm that consider the feasibility of the feed distribution, average sidelobe level, peak sidelobe level, and the beamwidth. The maximum sidelobe peak relative to the main beam is allowed to be as large as -16 dB near the main beam and -10 dB at the edge of the FOV. The sidelobe level far from the main beam is more relaxed due to the extra suppression provided by the antenna pattern. While achieving a smaller sidelobe level is possible, the extra freedom can be put into a narrower beamwidth. A narrower beamwidth also translates into lower power consumption since less phase shifters are used compared to a larger uniform array with the same beamwidth.

A genetic algorithm starts with a set of possible solutions and through an evolutionary process moves toward the best answer [35]. Every element in the search space is encoded into a DNA (in analogy to its biological definition) which is a sequence of binary values uniquely representing a possible solution. Initially, the algorithm generates a set of solutions as the first generation of the *society*. Through a sequence of crossover and mutations, the next generation of the society is produced using a pair of *parent* solutions for each new member. Next, according to the optimization criteria, the fittest are kept and others are removed from the society (*natural selection*). As this process iterates, the society evolves and gets closer to the global optimum solution. The genetic algorithm is a suitable choice for sparse array design on a grid since the presence or absence of each element can be represented by a single bit, resulting in a DNA with a small length and a fast thorough search. This is not the case for problems with continuous variables, for which only a finite number of bits can be used to represent each variable in the DNA, leading to a tradeoff between achieving an optimal solution and the runtime. Moreover, in a genetic algorithm, the mutation operation implicitly tries to avoid numerous non-global optimum points in the sparse array search space. While this

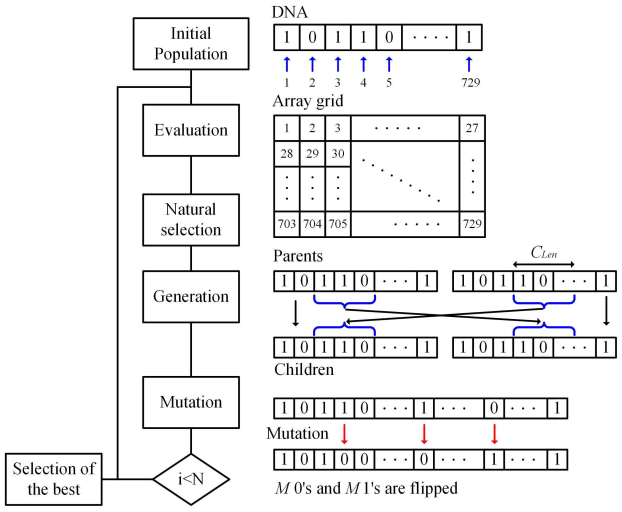


Fig. 7. Flowchart of the genetic algorithm used for sparse array design.

optimization is performed for a 128-element array, it fully lends itself to a larger scale aperture with more elements and different design criteria. The number of required generation (iterations) depends on the size of the array that is being designed. For the presented work, with 128 elements on 729-spot grid, the maximum number of generations is set to a 1000 iteration. The optimum result is achieved after about 500 iterations and the extra 500 is the margin to determine if the convergence is achieved. The grid size with 729 spots has enough sparsity to provide the room required for routing.

The flowchart diagram of the design algorithm is shown in Fig. 7. The search algorithm operates on a 27 × 27 grid array, and each solution is represented by a string of 729 (27 × 27) bits, with 128 of them being "1." Based on this vector, the location of the 128 elements is defined, the feed distribution network is designed, and the array factor, sidelobe level, and beamwidth are calculated. The first generation is generated randomly (the members having good features of each optimization criteria) so that there is a large diversity of genes for the subsequent generations to *inherit*.

In the iteration loop, members are paired together to create the next generation after being shuffled randomly. In the DNA of each pair, a random location is chosen and a piece of DNA with a length of C_{Len} bits is selected from the parents. Two children are produced that have one piece of each parent. In the DNA of the children, the mutation operation is implemented by randomly flipping M bits with the value of "0" and M bits with the value of "1." These children are then added to the society, doubling the population. Eventually, after assigning a measure of fitness to each member by evaluating the array factor parameters and the feed distribution feasibility, *natural selection* is applied by removing the lower half of the society based on the fitness factor.

The measure of fitness is calculated by scoring the sparsity (local crowdedness), the maximum and average sidelobe levels, and the beamwidth of each solution. These scores are then summed up with weights that are changed manually after multiple iterations, eventually achieving a solution with the desired features. Fig. 8 shows the final 128-element aperture

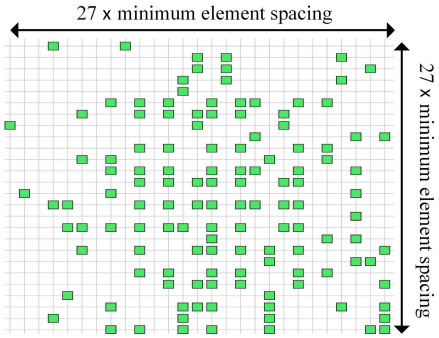


Fig. 8. Designed 128-element sparse aperture on a 729-spot grid.

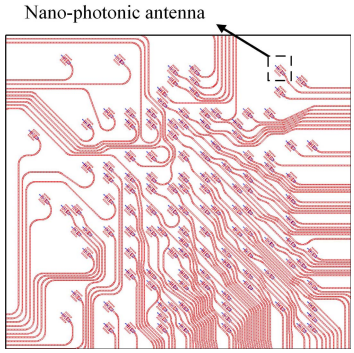


Fig. 9. Sparse aperture with optical feed distribution and nano-photonic antennas.

used in our implementation, with a grid spacing of 5.6 μm= 3.6λ. For this spacing, which is the minimum spacing limited by the antenna size, the grating lobes are 16° apart. The peak sidelobe level is kept below −16 dB near the main beam and less than −10 dB far from the main beam. Moreover, the average sidelobe level is −21 dB relative to the main beam power. Since the overall pattern of the OPA is the product of the array pattern and the antenna pattern, as the beam is steered to larger angles, side lobes are amplified by the center part of the antenna pattern while the main beam is partially suppressed, degrading the sidelobe rejection. Moreover, grating lobes are suppressed by the antenna pattern to minimize the leakage to the grating lobes which is about 7 dB. The fully routed feed distribution network is shown in Fig. 9. The antennas are placed in a 45° angle relative to the aperture coordinates, enabling optical routing through two sides of the aperture without sharp bends (sharp bends cannot confine the light within the waveguide properly and suffer from high optical loss). There is less feed routing from the other two sides to have the room for the bends. The array pattern is shown in Fig. 10 for $\phi = 0$. This array achieves a beamwidth of 0.64° with a grating-lobe-free steering range of 16°, which is equivalent to a uniform array with 484 elements on the same grid.

To demonstrate the scalability of this approach, a 512-element sparse array on a 108 × 108 grid (11664-spot grid) is designed. This array has 4 times as many elements and is 16 times larger in area (4 times more sparse) compared to the 128-element array. This array achieves better than 19-dB peak sidelobe rejection and 0.14° beamwidth on a grid with 5.6 μm

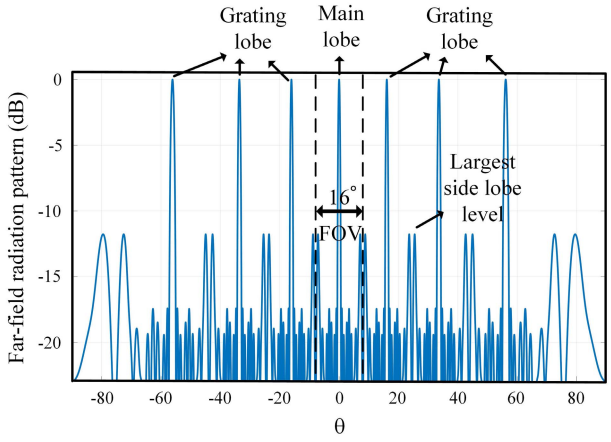


Fig. 10. Far-field radiation pattern of the sparse array for $\phi = 0$.

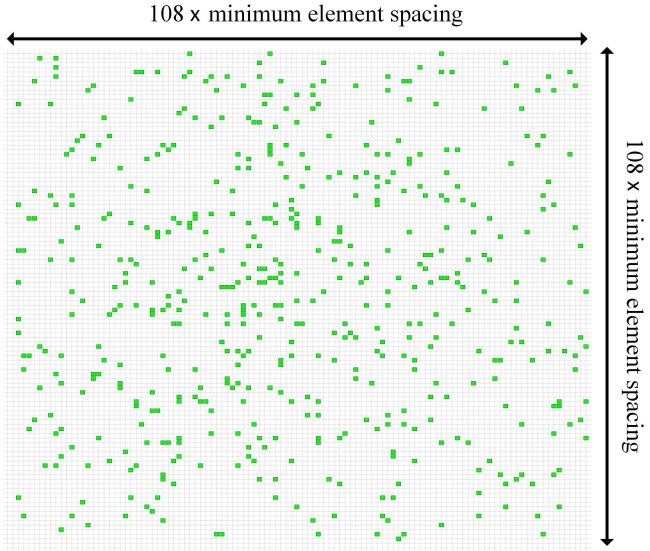


Fig. 11. Designed 512-element sparse aperture on a 11 664-spot grid.

grid spacing. The element locations and far-field patterns of the 512-element array are illustrated in Figs. 11 and 12, respectively. Further performance improvement can be achieved by including the amplitude control capability to the optical signals fed to the array elements.

IV. Phase Shifter Network

A dedicated phase shifter for each radiating element is required for electronic beam steering in both azimuth and elevation angles. Moreover, it is critical to have phase shifters that are individually controlled and can provide the full 2π phase shift to compensate for the phase offsets in the optical paths. These offsets are caused by fabrication mismatches and non-idealities, producing small variations in the refractive index of the integrated dielectric waveguides [40]. These variations cause phase errors that accumulate as the length of the waveguides increase, resulting in fixed offsets. In addition, drift and crosstalk between the phase shifters introduce extra error in the phase accuracy of the optical signals feeding the radiating elements, necessitating full phase shifter control. However, the power consumption of these phase shifters and

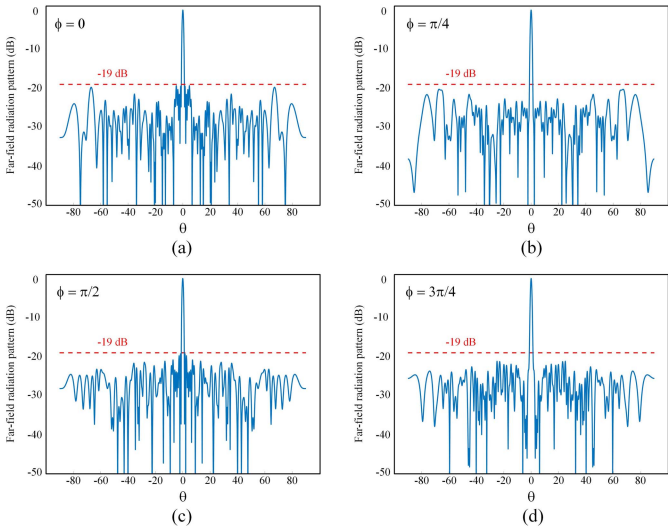


Fig. 12. Far-field radiation pattern of the 512-element sparse array with $\lambda/2$ grid spacing for (a) $\phi = 0$, (b) $\phi = \pi/4$, (c) $\phi = \pi/2$, and (d) $\phi = 3\pi/4$. This pattern is plotted for grid spacing $\lambda/2$ and has only a single lobe in the visible range; increasing the grid spacing broadens the visible range and includes periodic repetition of the same pattern and grating lobes. $\lambda/2$ spacing pattern that contains all the information about the pattern, is plotted for better visibility of the pattern.

their driver circuitry present a challenge in the realization of a large scale OPA. Here, we utilized a PWM-driven row–column power delivery network for the tunable optical phase shifters that reduce the number of required phase shifter drivers and significantly lowers their internal power consumption. Next, we will discuss the design of the individual phase shifters and the phase shifter network.

A. Phase Shifter

An ideal high-performance optical phase shifter features low optical insertion loss, low power consumption, and small crosstalk between phase shifters. A thermal optical phase shifter is used in this design. This phase shifter′s operation is based on the silicon refractive index′s dependence on temperature. Silicon has a refractive index temperature dependence of $\beta = dn/dT = 1.86 \times 10^{-4} K^{-1}$ [41] at a wavelength of 1550 nm. Therefore, changing the temperature of a silicon waveguide with a length l by ΔT results in an index change of $2\pi\beta l \Delta T/\lambda$. By providing enough temperature change a 2π phase shift can be achieved. A thermal phase shifter is advantageous in optical systems due to its lower optical loss and lower power consumption compared to other types of integrated phase shifters and modulators [42]. Accordingly, thermal phase shifters and nano-heater modulators have been used in many recent OPA demonstrations [16], [18]–[20], [22]–[24], [26].

The primarily coupling mechanism between the phase shifters is thermal crosstalk. Since power consumption of a phase shifter varies with the phase shift it provides, local heat generated at each phase shifter leaking to the other phase shifters affects their performance and phase shift.[1] Scaling the

[1]This is not specific to the thermal phase shifters. A broad range of nano-photonic phase shifters suffer from thermal crosstalk due to the varying power consumption versus phase shift.

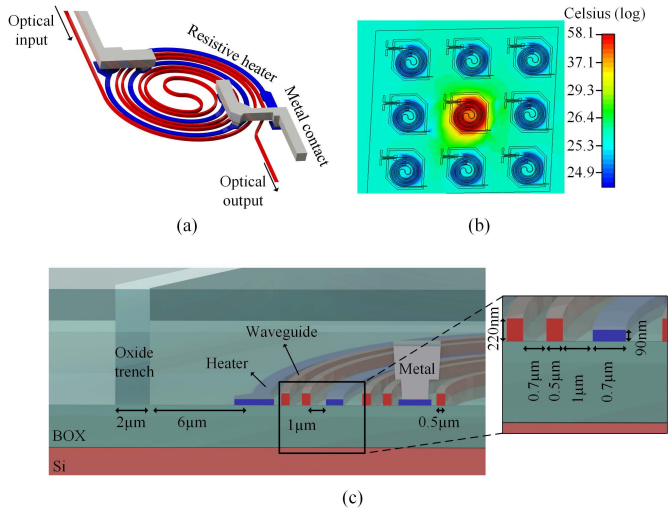


Fig. 13. (a) Compact spiral phase shifter. (b) Thermal simulation of the phase shifter. (c) Cross section of the phase shifter (not to scale).

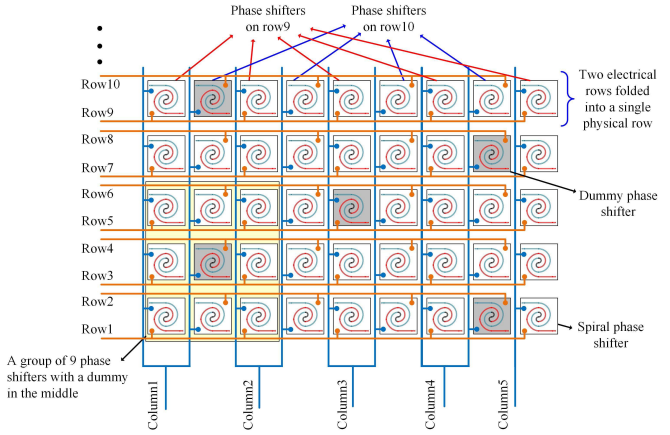


Fig. 14. Design of the phase shifter with a folded row–column electrical access grid.

OPA and embedding more phase shifters increases the total crosstalk that further disturbs the phase tuning and beamforming procedures. Therefore, a compact thermally isolated phase shifter is essential for a large scale OPA.

Here, an efficient spiral thermo-optical phase shifter is designed with a compact form factor and negligible crosstalk. Fig. 13 shows the schematic and thermal simulation of the designed tunable phase shifter. 300 μm of dielectric waveguide is wrapped in the form of a spiral along with a doped layer of silicon which forms a resistor. The doped layer has more than 1 μm clearance with the optical waveguides resulting in a negligible optical insertion loss due to the interaction of the optical wave with the doped region. Passing a current through the 1-KΩ resistor increases the local temperature and results in a longer optical path length, which corresponds to a phase shift. The phase shifter provides a 2π phase shift for 18 mW of power consumed by the distributed resistor. The compactness of the phase shifter results in high lateral thermal isolation. To further increase the isolation between the phase shifters, an oxide etch offered by the process is placed around the phase shifter to reduce the lateral thermal conductance. There is a thermal path to the substrate through the 2-μm thick BOX layer, which results in heat depletion and defines the thermal time constant of the phase shifter. Since silicon has a high thermal conductance, temperature across the bulk can be assumed to be uniform to the first order. Therefore, placing phase shifters more than 20 μm apart yields low thermal crosstalk.

B. Row–Column Power Delivery Network

Power delivery and activation of the phase shifters is realized through a row–column access grid which provides a scalable and compact electrical interface. The 128 phase shifters, one for each radiating element, along with 16 dummy phase shifters, are placed in a 16×9 row–column grid (Fig. 14). These phase shifters are electrically connected as a 32×4 matrix (columns 1–4) plus a column of 16 rows (column 5). This forms a folded row–column network in which four pairs of physical columns are jointly driven with their associated phase shifters being connected to separate rows. This folded architecture reduces the optical path length on the chip, which corresponds to lower loss and higher coherence between the element feeds. Moreover, the electrical length of the columns is reduced by half, which results in lower resistance, or equivalently, a smaller metal width for routing. This, in turn, decreases the optical loss and the chip area occupied by the metal routing.

The dummy phase shifters are uniformly distributed in the network. Although silicon has a high thermal conductivity, these dummy phase shifters are placed to further reduce the temperature gradient in the bulk silicon and, thus, crosstalk between phase shifters. The dummy phase shifters are identical to the other phase shifters and are electrically connected to the row–column grid, but are not optically active (no optical input–output). Each group of nine phase shifters has a dummy phase shifter at the center of the group (Fig. 14). By actively adjusting the power flowing through the dummy phase shifter, the local temperature of the bottom bulk silicon is controlled.

The folded row–column architecture significantly reduces the number of required phase shifter drivers from 144 (for an individual access network) to 37, reducing the complexity of the electronic circuitry. However, a time-sharing mechanism should be implemented to deliver power to the phase shifters at each column sequentially, which necessitates a dedicated circuit.

V. Phase Shifter Network Driver

To increase the efficiency of the driver circuitry, the rows of the phase shifter network are driven with a PWM signal [as opposed to a digital to analog converter (DAC), as used in earlier works [20]]. The PWM driver is a switching mode circuit which has superior power consumption compared to a DAC, as either the voltage or the current across the switches will be small at any point in time. The phase shifter network is driven periodically by the driver circuitry—each column is switched to a constant positive voltage for one-fifth of the cycle while the rows are individually connected to ground for a digitally controlled period of time. By adjusting the relative

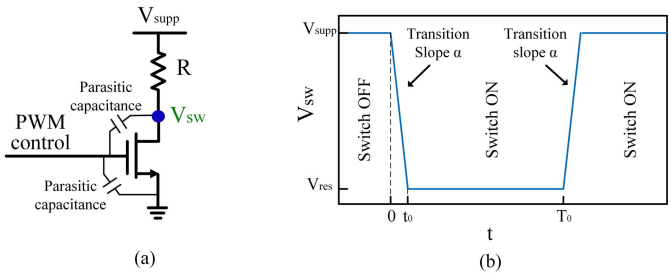


Fig. 15. (a) Schematic of a simplified PWM driver. (b) Simplified voltage drop on the switch.

timing, the power delivered to each phase shifter and, thus, its effective phase shift is determined.

To illustrate the lower power consumption of the PWM driver, the simplified model shown in Fig. 15(a) is considered. There are two main sources of loss for this system; the dynamic power wasted due to charging and discharging the capacitors, and the power consumed by the switch due to its finite voltage drop. The dynamic power consumption is negligible compared to the power delivered to the phase shifters because of the small capacitors and relatively low switching frequency of the driver for the presented OPA. To quantify this factor, power dissipation by a 1-pF capacitor, which is much larger than the capacitances in the circuit, charged and discharged to 2.5 V (the maximum tolerable voltage by the transistors) with 4 MHz switching frequency (used for this system) is considered. The power consumption is

$$P = \mathrm{fCV}^2 = 4\ \mathrm{MHz} \times 1\ \mathrm{pF} \times (2.5\mathrm{V})^2 = 25\ \mu\mathrm{W} \quad (6)$$

which is much smaller than the average power delivered to a phase shifter (≈10 mW).

The finite voltage drop on the switch during the transitions and ON-state also results in power consumption by the switch and reduces the efficiency. The power consumption by the switch can be studied by considering the simplified output voltage for the system [Fig. 15(b)]. Here, the switching transition is approximated with a straight line with slope of $\alpha = V_{\mathrm{supp}}/t_0$. By integrating the power in a cycle and averaging over a cycle, we achieve

$$P_{\mathrm{sw}} = \frac{1}{T}\int_0^T \frac{V_{\mathrm{sw}}(V_{\mathrm{supp}} - V_{\mathrm{sw}})}{R}dt \approx \frac{V_{\mathrm{supp}}^2 t_0}{6RT} + \frac{V_{\mathrm{supp}}V_{\mathrm{res}}}{R}$$
$$P_{\mathrm{total}} \approx \frac{V_{\mathrm{supp}}^2}{R}$$
$$\eta = \frac{P_{\mathrm{total}} - P_{\mathrm{sw}}}{P_{\mathrm{supp}}} = 1 - \frac{t_0}{6T} - \frac{V_{\mathrm{res}}}{V_{\mathrm{supp}}} \quad (7)$$

in which P_{sw} is the power consumed by the switch, P_{total} is the total power delivered by the supply, and η is the power efficiency. Other parameters in (7) are defined in Fig. 15. Therefore, power consumption of a PWM driver with a small residual voltage drop on the switch and fast transition times is significantly lower than a DAC. A DAC is always connected between the supply voltage source and the load it is driving. The difference between V_{supp} and the load voltage will drop on the DAC resulting in a large power dissipation compared to a PWM driver.

Although using the PWM power delivery network increases the efficiency of the system and reduces the power consumption, for the time sharing between N columns (here $N = 5$), the required peak driving voltage increases by a factor of $\sqrt{N}$. In addition to the high voltage swing, N phase shifters are being driven by a single driver, which requires higher current handling capability. Due to the additional constraints on the area imposed by electrical routing and electromigration limits, yet even a higher drive voltage is desirable. Given the power required for a 2π phase shift, the resistance of the phase shifter is adjusted in accordance with the maximum available voltage to minimize the current. Another desired characteristic for the driver is fast switching to enable precise phase control and avoid the non-linear dependence of power on duty cycle, due to the slow rise and fall times. These requirements, along with the breakdown and reliability issues in a CMOS technology, present an interesting design challenge for the driver.

In the presented work, optical phase shifters are designed for a peak drive voltage of 10 V with 8-bit pulsewidth resolution. Since 10 V is beyond the voltage breakdown of standard transistors in high-speed CMOS processes, a breakdown voltage multiplier [43] switching stack is designed to provide the PWM switching, guaranteeing reliability for the transistors. Moreover, to further protect the transistors from overvoltage and reduce the switching time, a soft turn-on circuit is implemented as an interface between the digital PWM generator and the switching stack, which initiates the switching in a controlled fashion.

A. Switching Stack

Fig. 16 shows the design of the high voltage swing switch to perform a fast PWM switching with a 10-V peak voltage. The switch uses a breakdown-voltage multiplier architecture including a stack of five thick-gate-oxide 2.5-V transistors (M_1–M_5). The total voltage on the stack is distributed among these transistors to prevent overvoltage on the devices and guarantee reliability. This architecture also features a positive feedback self-charging/discharging mechanism, consisting of transistors M_6–M_8 and a resistive divider for performing fast switching with a small rise/fall time.

The performance and design procedure of the switch can be better understood by considering the operation of the transistors as they go through the switching cycle. During the steady OFF-state, the gate of M_1 is shorted to ground by the digital PWM generator circuitry, which results in zero current passing through the stack. The gate voltage of M_2 is connected to a constant 2.5-V voltage source, which leads to the drain node of M_1 being charged to this voltage as well. This is the maximum possible voltage on the drain, which eliminates the possibility of voltage breakdown for M_1. When the circuit is actively operating, there is not enough time for the M_1 drain node voltage to get fully charged to 2.5 V that guarantees breakdown safety for the transistor. For transistors M_2–M_5, the resistive bias network provides a voltage distribution along the stack, with extra breakdown safety margin for each transistor to prevent them experiencing overvoltage during the OFF-state.

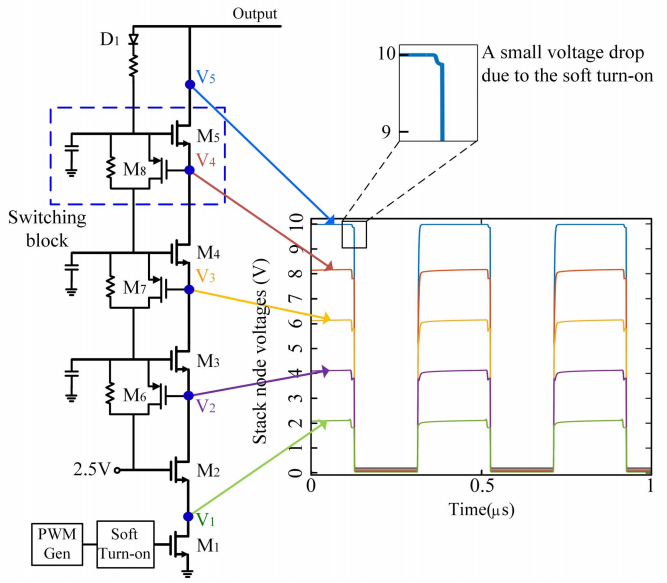


Fig. 16. Stack of five transistors to form a high swing switch. $(W/L)_{1-5} = 64\ \mu m/0.28\ \mu m$, $(W/L)_{6-8} = 4\ \mu m/0.28\ \mu m$, $C_1 = 364\ fF$, $C_2 = 164\ fF$, $C_3 = 110\ fF$.

The transition to the ON-state is initiated by increasing the gate voltage of M_1, which sinks current through the stack. Exceeding the breakdown voltage during the transition states is more likely due to the time varying voltages over the transistors. In transition to the ON-state, the PMOS transistors M_6–M_8 form positive feedback loops to discharge the gate voltages of M_3–M_5 as the output voltage drops. All the gate voltages are eventually brought to 2.5 V, which keeps the stack in the ON-state.

The transition time and the details of the switching mechanism can be better explained considering a single block of the stack shown in Fig. 17, in which M_n is the switching transistor and M_p forms the positive feedback. During the OFF-state, the current through the stack is zero, and thus, the source and gate voltages of M_n and M_p are equal, turning them off. As I_1 increases, it discharges C_b and reduces the source voltage of M_n (C_b and C_g include the total parasitic capacitance between the nodes they are connected to). In the absence of the capacitor C, the time constant of the gate node is very small. Therefore, the gate voltage of M_n will also drop while its drain voltage is still at its previous value, resulting in drain–source and drain–gate overvoltage. To avoid this scenario, capacitor C is added to provide the charge for C_g as the source voltage of M_1 drops [Fig. 17(a)]. This results in a gate–source voltage increase for M_n that eventually activates the transistor. The time that it takes for I_1 to lower the source voltage by V_{th} (the threshold voltage) and activate the NMOS transistor of the i' th block in the stack can be calculated by taking the average of I_1, namely, I_{ave}, which yields

$$\tau_i = (C_n + C_p)\frac{V_{\text{th}}}{I_{\text{ave}}} = C_u L^2 V_{th}(1+\alpha)\frac{1}{I_0} \tag{8}$$

where

$$C_n + C_p = C_u WL(1+\alpha), \quad I_{\text{ave}} = \frac{W}{L} I_0. \tag{9}$$

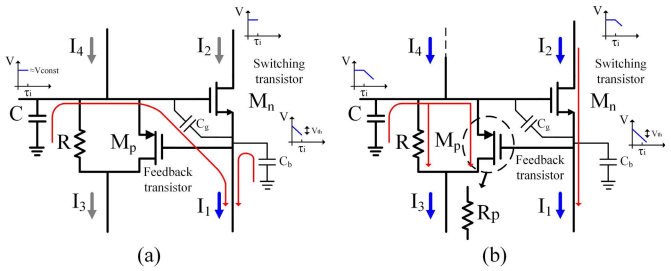


Fig. 17. Single block of the stack. (a) Before activation. (b) After activation.

where C_n and C_p are the total parasitic capacitances due to M_n and M_p, respectively, and are connected to the source node of M_n. $\alpha = C_p/C_n$ is related to the size ratio of M_p and M_n, $C_u = C_n/(WL)$ is the normalized capacitance which is a technology-dependent constant, W and L are the width and length of M_n, respectively, and $I_0 = I_{\text{ave}}/(W/L)$ is the normalized average current with respect to the transistor sizing.

Once V_{gs} exceeds V_{th}, both M_n and M_p turn on[2] and M_n starts lowering its drain voltage, starting the activation process for the upper block of the stack. Therefore, the total switching fall time is

$$\tau_{\text{tot}} = \sum_{i=1}^{N=5} \tau_i. \tag{10}$$

where τ_1 and τ_2 are the time delays caused by M_1 and M_2, respectively, and can be calculated easily considering their parasitic capacitances.

To investigate the possibility of overvoltage, we need to further analyze the stack block shown in Fig. 17 after V_{gs} exceeds V_{th}. Once M_n and M_p are active, M_n starts sinking current and activating the upper block. At this point, M_p can be modeled by an average resistance R_p which is in parallel with R [Fig. 17(b)]. Therefore, the gate voltage of M_n drops with a time constant τ_p. This time constant for the gate voltage of M_3 is $\tau_p = (R||R_p)C$, which results in[3]

$$V_{g,M3} = (V_{g0} - 2.5V)e^{-t/\tau_p} + 2.5V. \tag{11}$$

Based on (8), the smaller size of M_p reduces α and subsequently the delay time τ. However, there are two extreme cases that lead to overvoltage and, thus, define the sizing of M_p and the value of C. On the one hand, the capacitor C should be large enough to initially hold the gate voltage that turns M_n into a strong ON-state. Otherwise, due to the current passing through C_g, the gate and source voltages of M_n will drop while the drain voltage is still high, which results in drain–source overvoltage. On the other hand, a very large C and, consequently, large τ_p, delays the gate voltage drop while the source node of M_n is discharging and leads to gate–source overvoltage. To avoid this situation, the size of M_p

[2]It is assumed that they have the same threshold voltage to simplify the analysis while extending it for different threshold voltages is straightforward.

[3]Once the upper blocks are activated, extra current is sourced to the gate node through I_4 (Fig. 17), which can be modeled by an increase of the time constant τ_p. Moreover, the gate voltage time constant includes other factors that are in the current path to the 2.5V voltage source. However, the circuit analysis to derive the more exact time constant is straightforward.

can be increased to reduce τ_p at the expense of a larger α. Therefore, C should be chosen to be the smallest value that strongly turns on M_n and results in the largest I_0 for the upper stage. The size of M_p should be as small as possible considering the value of C. M_4 and M_5 have more complicated expressions for their gate voltages since the drain voltages of M_7 and M_8 vary over time. Using all these equations results in all the sizings for maximizing I_0 for each stage and minimizing τ_{tot}.

Once the stack is fully switched, it connects the output node to ground with a voltage drop across the switch. The ON-voltage of the stack switch depends on the current passing through the switch and on the size of the transistors. Since the operation of the switch depends on I_0 to the first order, which is normalized to the size of the transistors, for a larger total current or lower ON-voltage drop, the size of the structure can be adjusted.[4] Here, the ON-voltage is adjusted to be less than 203 mV for 10.3 mA of current, which results in a high driver efficiency due to the low power consumption in the switch. During the ON-state, since the drain voltage of M_5 is lower than its gate voltage, diode D_1 (Fig. 16) is used to prevent the reverse current from flowing through the resistors.

Finally, the last phase in the switching cycle is switching back to the OFF-state. Once M_1 is turned off by the control circuitry, its drain starts to charge up by the current M_2 provides. Increased voltage on the drain node reduces the strength of M_2 and the ability to transfer the current M_3 delivers, which results in a voltage rise on the drain of M_2. The same mechanism happens sequentially for all the transistors in the stack, and eventually, the midpoint voltages return to their OFF-state values. During this procedure, the gate voltages of $M_3 - M_5$ should also increase to their OFF-state values in the same ratio as the increase in drain voltages, which prevents overvoltage on the drain gates. While the relative values of the biasing resistors define the voltage distribution on the gates, their absolute values are calculated based on the time constant required during the rise time.

B. Soft Turn On

It is shown in (8) that the delay of the stack transistors sequentially turning on is mainly due to the threshold voltage, $V_{\text{th}} = 0.475$ V, of the transistors. Moreover, the lag between the ON-time of these transistors increases the drain–source voltage and necessitates extra voltage margin. Here, the soft turn-on block is designed to achieve faster switching and further protect the stack from experiencing voltages exceeding the transistor breakdown voltage rating. The soft turn-on block first partially turns the switch on such that a small current of 160 μA passes through the stack and puts all transistors at the edge of turn on. Then, full switching occurs which results in all the voltages dropping to their minimum value.

The soft turn-on block includes a delay cell (Fig. 18) that delays the digital switching signal while sending it through another path, which increases the gate voltage of M_1 to V_{GS9}

[4]Second-order effects related to the sizing can be adjusted through investigation of the node voltages.

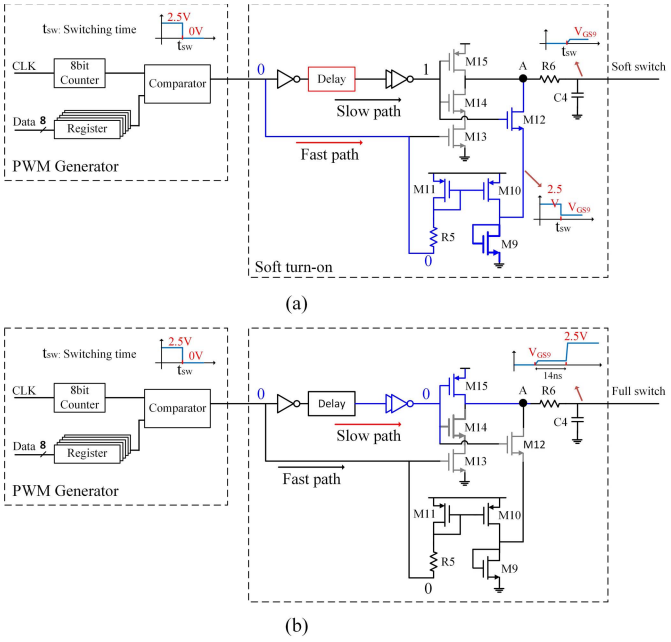


Fig. 18. (a) Initial activation through the fast path raises the output trigger voltage by V_{th}. (b) Full switching through the main path after 14 ns of delay.

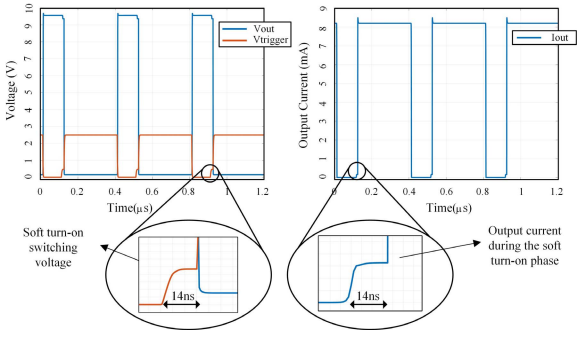


Fig. 19. Simulation result for the generated PWM signals with soft turn-on switching. The soft turn-on circuit delays the strong switching signal for 14 ns and pre-activates the stack.

(M_9 is a relatively large transistor). When a switching signal is generated by the PWM generator, M_{13} disconnects the path from node "A" to ground through M_{14}, and V_{GS9} is transferred to this node via M_{12}. R_6 and C_4 form a low-pass filter to damp the switching spikes. As a result, M_1 and, subsequently, all the transistors in the stack, are put on the verge of turn on. When the switching signal passes through the delay block after 14 ns, M_{15} connects node "A" to VDD for full switching, and M_{12} disconnects the soft turn-on circuit (Fig. 19). The 14 ns is enough time for the stack soft turn on including a 6-ns safety margin.

VI. System Design

Fig. 20 shows the block diagram of the two-chip sparse OPA system comprising the silicon photonic and the CMOS electronic chips. The optical input port is a focusing grating coupler that couples the laser light at 1550 nm provided by an optical fiber into an on-chip dielectric waveguide. The focusing grating coupler has 6 dB of insertion loss. To split the optical power into 128 equal-power branches, two power

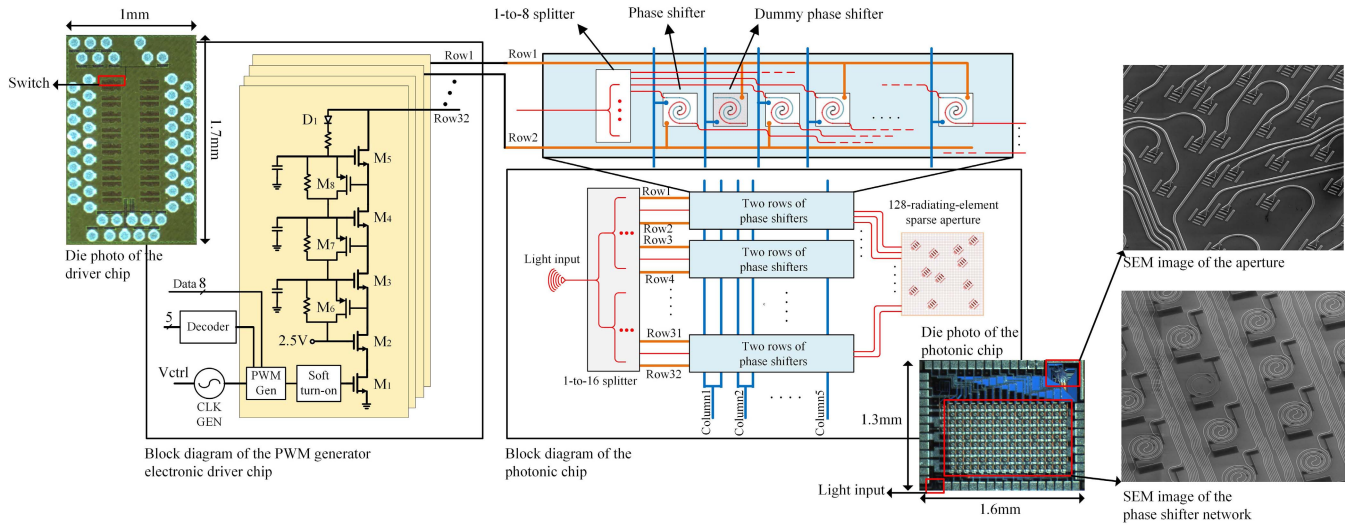


Fig. 20. Schematic of the OPA chip set and the die photos of the fabricated chips.

splitter structures are used in series. The first power splitter is a 1-to-16 four layer binary tree power divider and provides an input optical signal to each of the folded rows. Each folded row has a 1-to-8 embedded power splitter (three-layer binary tree) that further divides the optical power and feeds the eight optically active phase shifters in the row [Fig. 21(d)]. Each individual splitter is a symmetric Y-Splitter [44] providing an even amplitude distribution between output branches [Fig. 21(a)]. These splitters with input reflection of −28 dB have a small compact footprint that makes them robust to fabrication mismatches and temperature variation. The phase shifter network is powered by the electronic chip and can be adjusted to tune the optical phases for an arbitrary wavefront that is eventually radiated via the nano-photonic antennas. The processed light by the phase shifter network is routed to the aperture such that the optical path difference between the 128 branches is minimized.

Silicon substrate of the chip is a good thermal conductor and results in a relatively uniform heat distribution in the bulk. Thus, in case of a temperature variation, since the temperature of all the optical waveguides on the chip changes together, ideally, temperature variation has no effect on the far-field pattern if all the path lengths to the radiating elements are matched. However, fabrication mismatches that induce path length mismatches result in different phase shift variations for different paths. Moreover, in case of a temperature gradient, different waveguides are exposed to different temperature values. The location of the beam does not change with temperature and it gets buried in the side lobes eventually for very large temperature gradient or temperature change. To compensate for any potential large thermal gradient over the chip, three resistive heaters are placed at the corners of the photonic chip. Also, dummy phase shifters uniformly placed in the phase shifter network are used to cancel the local thermal gradient. To measure the substrate temperature, three points to absolute temperature (PTAT) sensors, which are each a set of 5-to-1 ratio junction diodes, are placed on the photonic chip outside of the phase shifter network. The current sources

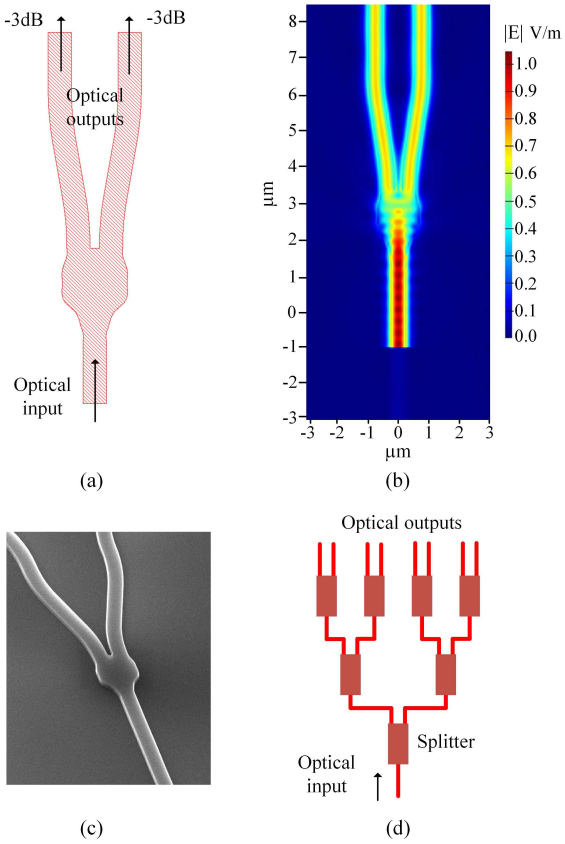


Fig. 21. (a) Single 3-dB splitter with a small footprint of the splitting region. (b) EM simulation of the 3-dB splitter showing a uniform power distribution and negligible input port mismatch. (c) SEM image of the fabricated splitter. (d) 1-to-8 binary tree splitter network.

driving these diodes and the voltage readout circuitry are external to the photonic chip.

The electrical connections to the rows and columns of the phase shifter network are routed to bonding pads fed by the electronic chip. The electronic chip includes 32 individually controlled PWM drivers that are connected to the phase shifter rows. Each PWM driver has a stack switch, a soft turn-on

block, and a digital PWM generator as explained in Section V. The pulsewidth for each driver is digitally programmable via the on-chip digital controller, which makes a convenient interface for the system. The PWM drivers operate with a cycling rate of 4 MHz, which is high enough to avoid phase shift ripples due to the pulse driving signals. The electrical columns of the phase shifter network are switched between 0 and 10 V by a multiplexer that selects which column should be powered.

Fig. 20 shows the die photograph of the two fabricated chips. The photonic chip is fabricated in a silicon photonics process with a 2 μm BOX thickness and a 220-nm silicon device layer for the realization of optical components. There are also two etch levels of 90 and 150 nm for the silicon layer, multiple n-type, and p-type doping layers, and two metal layers available for designing various electro-optical systems. The electronic chip is fabricated in a standard 65-nm CMOS process that offers thick oxide transistors with a 2.5-V breakdown voltage rating.

VII. Measurement Setup and Results

The measured optical loss of the on-chip waveguides is 2.5 dB/cm which is a small value for a chip with milliliter scales and does not have a considerable effect in the performance of the system. Each individual power splitters have 0.4 dB of insertion loss resulting in a 2.8 dB overall insertion loss of the splitter network. The output power of the splitter three networks is uniformly distributed within less than 1-dB variation. This is due to the geometrical symmetry of the splitters and their compact size that makes them robust to fabrication mismatches and thermal variation. As the number of elements increases, a splitter tree with more layers is required to split the power between branches. The insertion loss of the splitter is inevitably added to the overall loss of the system. However, adding every layer to the splitter tree doubles the number of output branches. This logarithmic growth of the optical loss versus the number of elements has a small effect on the performance of the system as it scales.

The spiral phase shifters are characterized by forming a Mach-Zehnder modulator test structure. Fig. 22(a) shows the modulator, in which the input light is split into two branches with a phase shifter on one of the arms and then recombined. The phase shifter is driven by different power levels, which correspond to different phase shifts, and causes varying amplitudes in the output waveguide, which is a function of the phase shift. The amplitude response of the modulator versus the applied voltage and the calculated phase shift of the phase shifter are illustrated in Fig. 22(b). Since the two arms are not length matched in this case, the constructive interference associated with the zero phase shift between the arms happened at an offset voltage. This compact spiral phase shifter provides a π phase shift for a drive power of 10.6 mW. The frequency response of the phase shifter is also measured in the Mach-Zehnder architecture [Fig. 22(c)], providing a 3-dB bandwidth of 19 KHz. This response is fast enough to follow any mechanical movements and calibration in applications such as wireless optical communication.

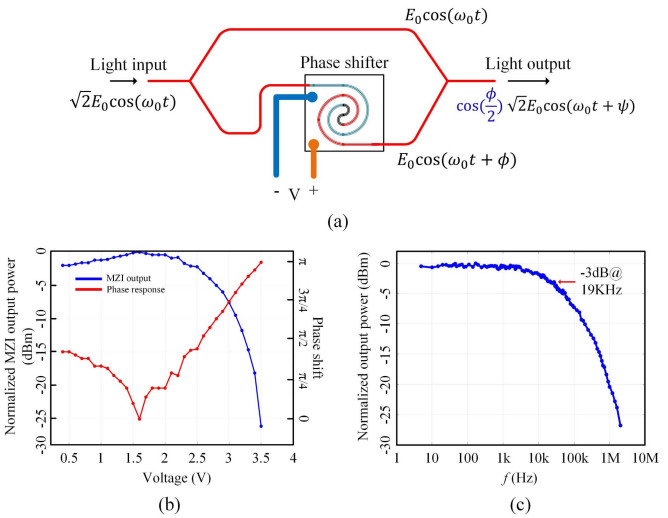


Fig. 22. (a) Mach-Zehnder modulator for characterizing the phase shifter. (b) Output power of the Mach-Zehnder modulator versus the applied voltage to the phase shifter and its corresponding phase shift. (c) Frequency response of the phase shifter.

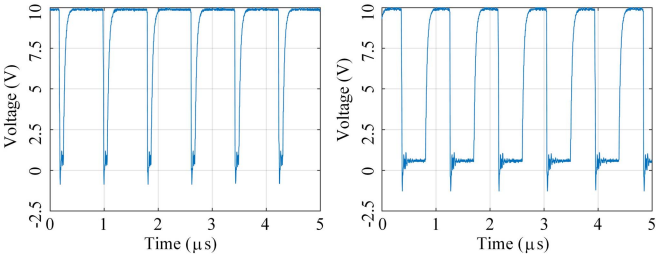


Fig. 23. Exemplary PWM signals generated for driving two of the rows with two different duty cycles.

The PWM driver is designed to operate with an adjustable cycling rate of 0.7–14 MHz, which is high enough for the phase shift ripples to get suppressed due to the frequency response of the phase shifter. Fig. 23 shows the two exemplary PWM signals generated for driving two of the rows with two different duty cycles. The fall time, which is the result of the switch action is 12 ns and the rise time is 71 ns dominated by the parasitics of the interface at the output node. Each PWM driver has an ON-voltage of 480 mV for the whole switch stack, leading to a significantly lower power consumption by the driver compared to conventional DAC-driven OPAs. The power consumption of the PWM driver that drives a row of phase shifters is 1.3 mW for π phase shift. The soft turn-on block consumes less than 10 μW which is not a considerable value.

To characterize the OPA system, the two chips are mounted on a printed circuit board (PCB) and connected electrically, as shown in Fig. 24(a). The PCB also includes a microcontroller to provide a digital interface between the drivers and a computer, as well as the required components for powering the chips and a readout for the PTAT sensors. A laser source of wavelength 1550 nm with 2-dBm output power is coupled to the photonic chip through the focusing grating coupler. To capture the far-field pattern of the radiation via the aperture,

TABLE I
COMPARISON TABLE

	This work	Caltech (2015) [25]	USC (2015) [26]	USC (2018) [20]	MIT (2017) [21]	Intel (2016) [22]	MIT (2016) [23]
Aperture	2D	2D	2D	1D	1D	1D	1D
Number of radiating elements	128	16	64	1024	1024	128	50
Minimum element spacing	5.6 μm	50 μm	33 μm	2 μm	4 μm	5.4 μm	2 μm
Maximum steering angle	16°	1.8°	1.6°	45°	23°	80°	46°× 36°
Beamwidth	0.8°	0.5°	0.45°	0.03°	0.021°	0.14°	0.85°× 0.1°
Side-lobe suppression (dB)	12*	6	11	9	10	8.9	8
Power consumption mW**	10.6 mW	N.R.	19.2 mW	54 mW	N.R.	80 mW [20]	17.4 mW
Integrated electronics/photonics	Yes/Yes	No/Yes	Yes/Yes	Yes/Yes	No/Yes	No/Yes	No/Yes

* Side lobe level is reported for the broad-side beam
** Per element at π phase shift

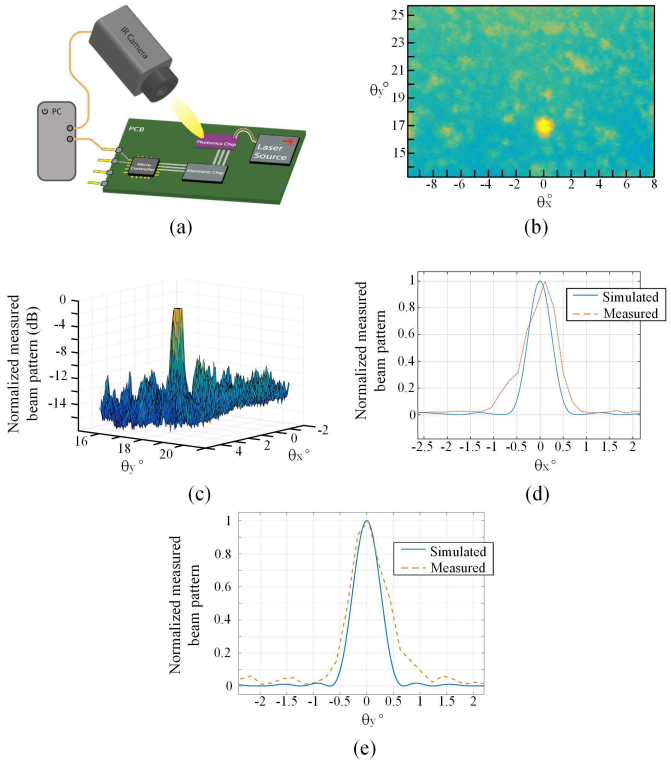


Fig. 24. (a) Measurement setup. (b) Radiation pattern of the formed beam (yellow spot) captured by the IR camera. (c) Captured pattern by the IR camera. (d) Simulated and measured results of the beam pattern for $\phi = 0$. (e) Simulated and measured results of the beam pattern for $\phi = \pi/2$.

an IR camera is placed 30 cm away from the aperture without a lens. The far-field region approximately starts at 3 cm, and thus, the camera is well in the far-field region. Light emitted by the OPA aperture impinges on the photodetectors and the camera records the pattern. A desktop computer is used to collect the output of the camera and PTAT temperature sensor. It also sends commands to the micro-controller for programming the electronic chip, controlling the pulsewidths and, eventually, the corresponding phase shifts. Therefore, a closed feedback loop is formed whereby the computer can process the data and adjust the phase shifters. The IR camera outputs its captured image in gray-scale values. The OPA is calibrated using an optimization procedure to form a beam. The optimization algorithm changes the phase shift of the elements by changing the power delivered to its phase shifter, and the result of the change in the far field is fed back to the optimizer through the IR camera. A gradient decent algorithm maximizes the power directed to a certain pixel region on the camera aperture forming an optical beam.

By adjusting the phase shifters, an optical beam is formed that is captured by the IR camera. Fig. 24(b) shows the image formed on the aperture of the IR camera with its lens removed, which corresponds to the projected far-field pattern. The yellow spot shows the high-intensity region which corresponds to the formed optical beam. The camera output is reconstructed in 3-D [Fig. 24(c)], showing the minimum sidelobe suppression of at least 12 dB for the broadside beam (θ_x and θ_y are the elevation angles for azimuth angles of $\phi = 0$ and $\phi = \pi/2$, respectively). The radiation pattern of the OPA is also measured using a single photodetector that is moved along the θ_x axis. Fig. 24(d) and (e) show the simulation versus the pattern measurement, which achieves a beamwidth of 0.8° and a steering range of 16° in both steering angles. This is the largest steering range over beamwidth ratio among all reported 2-D OPAs.

The beam steering capability of the sparse OPA is demonstrated in Fig. 25. Fig. 25(a) shows the beam steered to several angles over the 2-D FOV by purely controlling the phase of the radiating elements. By sequentially adjusting the phase shifters to steer the beam to different angles, an image can be projected without utilizing a lens. This lens-free projection capability is illustrated by projecting the letter "A" through sequential beam steering [Fig. 25(b)].

Table I summarizes the performance of this sparse OPA transmitter chip set with a PWM drive, and compares it against state-of-the-art OPAs in the literature. Previously reported OPAs with 2-D apertures suffer a small steering range

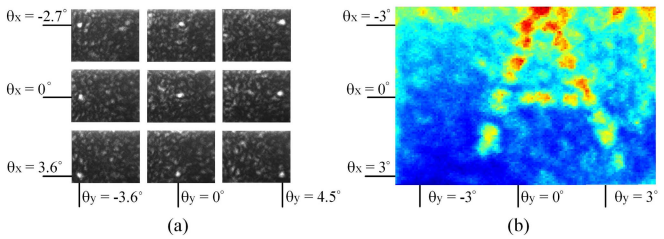


Fig. 25. (a) Illustration of the beam steering capability by forming a beam at multiple angles. (b) Letter "A" projected by beam steering.

(as listed in Table I) due to the large size of their nano-photonic antennas and the area required for optical feed distribution. While large element spacing results in a narrow beamwidth, the steering range over beamwidth, which defines the total number of resolved spots, is limited in these works. The OPAs with a 1-D aperture achieve a higher resolution but are able to steer the beam in only one dimension using the adjustable phase shifters.

The power consumption of our OPA is also listed in Table I, which shows a mean power of 10.6 mW per radiating element for a given beamforming configuration.[5] Two factors are not included in the power consumption comparison: the PWM drive and the power consumption of an equivalent uniform array. The power efficiency of the PWM driver further distinguishes the low-power design of the presented OPA system. Moreover, the beamwidth of this design is equivalent to a uniform OPA with 484 elements, which means there would be a higher overall power consumption if a 484-element array was used.

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