A 0.006 mm^2 1.2 μW Analog-to-Time Converter for Asynchronous Bio-Sensors

Lieuwe B. Leene, *Member, IEEE*, and Timothy G. Constandinou, *Senior Member, IEEE*

***Abstract*— This paper presents a low-power analog-to-time converter (ATC) for integrated bio-sensors. The proposed circuit facilitates the direct conversion of electrode bio-potential recordings into time-encoded digital pulses with high efficiency without prior signal amplification. This approach reduces the circuit complexity for multi-channel instrumentation systems and allows asynchronous digital control to maximize the potential power savings during sensor inactivity. A prototype fabricated using a 65-nm CMOS technology is demonstrated with measured characteristics. Experimental results show an input-referred noise figure of 3.8 μV_{rms} for a 11-kHz signal bandwidth while dissipating 1.2 μW from a 0.5-V supply and occupying 60 × 80 μm^{2}silicon area. This compact configuration is enabled by the proposed asynchronous readout that shapes the mismatch components arising from the multi-bit quantizer and the use of capacitive feedback.**

***Index Terms*—Analog-to-time conversion, asynchronous, bio-sensor, delta-sigma, instrumentation, low noise, low voltage.**

I. Introduction

THE current trend in sensor systems is to integrate many analog sensors together with larger digital systems to provide smart data collection for miniaturized wearables or low-cost system-in-package (SiP) electronics [1], [2]. The digital-oriented design flow of these systems compels designers to look for sensor interfaces that accommodate the trends in CMOS technology scaling and smaller supply voltages for digital power reduction. For this reason, many data converters and sensing circuits have utilized voltage controlled oscillators (VCOs) to convert analog signals into a periodic digital waveform where information is encoded by its frequency. This type of conversion is highly applicable at every technology node and the time encoded output is considerably more robust than the voltage output of conventional amplifiers when considering supply noise and the process, voltage, and temperature (PVT) variations. The time-domain concept has seen extensive use in recent publications because the voltage-to-frequency conversion provides high gain and exceptional dynamic range [3]–[5] that can also accommodate conventional chopper techniques [6], [7].

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The authors are with the Department of Electrical and Electronic Engineering, Imperial College London, London SW7 2AZ, U.K. (e-mail: l.leene@imperial.ac.uk; t.constandinou@imperial.ac.uk).

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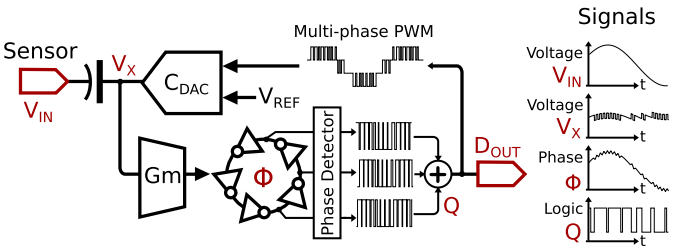

Fig. 1. Proposed ATC that provides closed loop conversion of an analog input voltage into an asynchronous multi-bit digital data stream.

The conversion from analog to frequency is not the only means by which analog circuits can encode signals in the time domain. It is well known that both synchronous [8] and asynchronous [9] oversampling modulators will generate a pulsewidth-modulated (PWM) output bit stream. However, these realizations conventionally do not perform integration in the time domain and instead use charge pumps that suffer from typical drawbacks in advanced CMOS technologies such as gain degradation and limited voltage swing [10]. In contrast, the modulating characteristic of oscillators can negate component mismatch in any proceeding digital-to-analog conversion since the digital output inherently provides data-weighted averaging [5].

In order to retain high performance and minimize the requirement of ideal analog components, time-based systems should be designed in a fashion where only small error signals are processed in the analog domain with constrained linearity. Signals with large dynamics should be time-encoded and manipulated with robust digital logic. The proposed analog-to-time converter (ATC) realization that follows this concept is shown in Fig. 1. This topology presents an asynchronous delta–sigma modulator (ADSM) that accumulates a phase difference between two oscillators to realize time-based integration and utilizes capacitive feedback to linearize the conversion.

Here, the sensor's voltage fluctuations on V_{IN} modulate the pulsewidth of the PWM signal generated by the phase detector by combining multiple phases from each stage in the oscillator. In this fashion, the output bitstream D_{OUT} can effectively resolve finer quantization levels. In contrast to prior oscillator-based systems that are clocked, the asynchronous operation proposed here enables the high-speed signal processing with oscillator-based filters [11] or a continuous-time digital core [12]. Both avoid the need for a high-speed clock when processing a large number of recording channels and can therefore enable substantial power saving.

This paper is a first step toward realizing a sensor system that fundamentally only processes using the time-encoded signals and can potentially operate using a supply voltage of only several hundred millivolts since the circuit can accurately convert millivolt level signals without prior analog signal amplification [13], [14]. This is because oscillator-based integrators can operate with a voltage headroom close to transistor threshold voltage without diminishing loop gain or dynamic range. This advantage is not diminished by practical issues and large common-mode interference or electrode offset can be rejected because the sensor input is capacitively coupled to the main feedback loop. There are a number of established techniques such as using a dc servo loop or performing ripple rejection, which prevent these issues from degrading circuit performance [15]. This means that the voltage appearing at V_X well controlled through feedback and that the amplifier can maximize power efficiency factor (PEF) [16] without requiring additional voltage overhead to accommodate voltage fluctuation at its input.

This paper presents the implementation and modeling aspects of the oscillator-based ATC using the following organization. Section II details the instrumentation topology and Section III describes the corresponding transistor level implementation, Section IV discusses the impact of technology and mismatch parameters of this circuit, Section V presents the measured results of a fabricated prototype, and Section VI concludes this paper.

II. Concept and ATC Architecture

This section introduces the operating principle and circuit dynamics of the proposed instrumentation system that is used to sense intra-cortical neural activity using a conventional electrode instrumentation setup. Such a scenario would record activity *in vivo* or *ex-vivo* from 1 Hz to 10-kHz frequency band where the signals are no larger than a few millivolts in amplitude [17]. The circuit sensitivity must match the noise characteristics of the electrode or biological tissue and target a noise floor of around 50 nV/$\sqrt{\text{Hz}}$ [18]. These sensitivity conditions require the circuit to dissipate several microamps and easily leads to a circuit bandwidth much larger than 10 kHz. For this reason, this ATC will provide gain for a bandwidth exceeding 10 kHz since it is more resource effective to rely on proceeding processing stages to perform filtering when necessary.

A block diagram of the proposed architecture is shown in Fig. 2(a). For clarity, this shows the single-ended equivalent of the fully differential circuit that was implemented. The difference in potential between the two electrode inputs V_R and V_{IN} is chopped at the chopper frequency f_{chp} to generate an up-modulated voltage waveform that couples the input onto V_X through C_I. The essential mechanism here is that signals appearing on V_X induce a current that feeds into two oscillators with different polarities after being demodulated. This current forces the oscillators to accumulate a relative phase difference because the phase is dependent on the integral of injected current [19]. This phase difference is then evaluated for each oscillator tap using XOR logic to

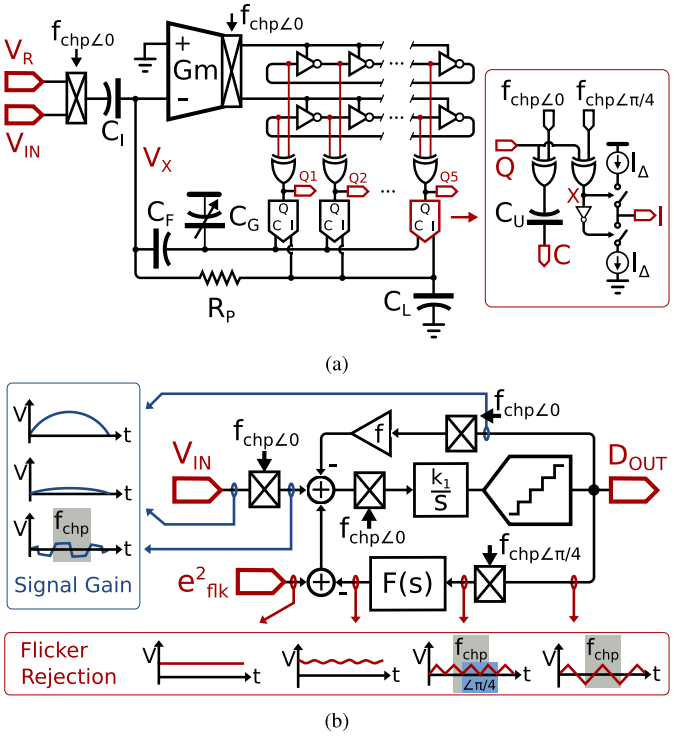

Fig. 2. Detailed system topology and equivalent analytical model of the proposed chopper stabilized ATC. (a) Block diagram showing the main transconductor that controls the phase difference of the pseudo-differential oscillator. Each output phase is processed in parallel by a DAC to provide capacitive feedback for signal amplification and flicker rejection using a charge-pump. (b) Equivalent small-signal model showing the signal path (blue) and the flicker rejection path (red).

yield multiple time-encoded PWM signals that can also be chopped using digital logic. The resulting digital signal is capacitively coupled onto V_X in parallel to close the loop. This is the main signal amplifying path that realizes a first-order asynchronous $\Delta\Sigma$ modulator and this sense using N phase detectors in parallel represents asynchronous quantization of the phase difference with a resolution of $\log_2(1+N)$ bits. Using this interpretation, we can construct the corresponding analytical model that is shown in Fig. 2(b) and will assist in deducing the design's parameter dependencies

$$H(s) = \frac{1}{s/k_1 + Nf} \approx \frac{1}{s \cdot \frac{NC_{\text{gate}}V_{\text{RG}}}{\text{Gm}} + \frac{C_F}{C_I}\frac{C_U}{C_U + C_G/N}} \quad (1)$$

$$f = \frac{C_F}{C_I + C_F} \cdot \frac{NC_U}{C_F + NC_U + C_G}. \quad (2)$$

First, the expression in (1) can be derived to characterize the signal amplifying loop. The feedback factor f evaluated in (2) corresponds to the capacitive coupling of a particular PWM phase Q on to V_X with respect to the capacitors C_I, C_F, C_G, and C_U. In this case, C_G can be digitally tuned to provide varying gain settings (41–53 dB). The oscillator's integration factor k_1 is derived by evaluating the impulse sensitivity function (ISF). The ISF captures how the oscillator phase is affected as a function of charge being injected into the virtual supply of the oscillator V_R [19]. Following the derivation for (2) in [11], this factor can be assumed constant

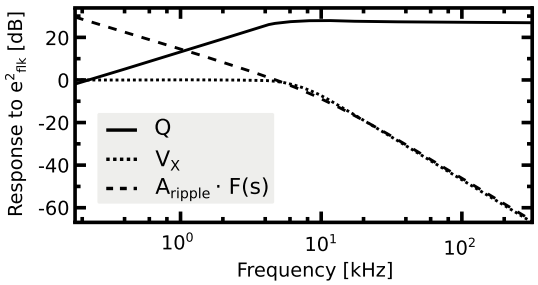

Fig. 3. Closed loop response of the flicker rejection loop due to input-referred noise e^2_{flk} evaluated with respect to the ripple magnitude seen at Q (solid), the feedback seen at V_X (dotted), and the open loop response $F(s) \cdot A_{\text{ripple}}$ (dashed).

and is simply dependent on the transconductance Gm, loading capacitance of each delay stage C_{gate}, and the voltage across the oscillator V_{RG} such that $k_1 = \text{Gm}/(\text{NC}_{\text{gate}} V_{\text{RG}})$.

The second control loop is used to reject near-dc aggressors that will appear at the input of the main transconductor. Chopping will prevent the input-referred noise profile from being corrupted by flicker noise but in turn several large tones will appear at harmonics of f_{chp} because off-set is being up-modulated. Moreover, because this structure is not providing narrowband amplification, the feedback must actively suppress these tones to avoid the output from being saturated and distorted. These components are $V_{\text{RG}}\ A_{\text{ripple}} = k_1/f_{\text{chp}}$, which induces a 90° phase shift. The phase shift can be corrected for by using the chopper clock that is delayed by 1/4th of the period when demodulating Q to recover the off-set. The flicker rejection further depends on the transfer function $F(s)$ which represents how the recovered signal is smoothed and fed back onto V_X. Using a charge pump in addition to the pseudo-resistor R_P will yield an expression for $F(s)$ according to (3), where C_L and I_Δ represent the main integration capacitor and charge pump bias current, respectively. This is also shown in Fig. 2

$$F(s) = \frac{N I_\Delta}{s(C_L C_I R_P s + C_L + C_I)}. \tag{3}$$

Combining $F(s)$ and A_{ripple} will then predict how the noise aggressors at V_x are removed. The frequency-dependent response in Fig. 3 evaluates this control mechanism at different points in the loop using the following implemented circuit parameters: $N = 5$, $f_{\text{chp}} = 75$ kHz, $C_I = 288$ fF, $C_G = 69$ fF, $C_F = C_U = 14$ fF, $R_P = 100$ Mω, $C_L = 1.6$ pF, and $I_\Delta = 5$ nA. This shows the influence of noise at the input (e^2_{flk}) with respect to the ripple at the ATC output and the fluctuations on V_X as a function of frequency. First, note that the increased chopper frequency enables this circuit to increase its bandwidth and reject more of the low-frequency band including common-mode signals that asymmetrically couple onto V_X. In addition, the second-order low-pass characteristic provides increased rejection of the chopper and oscillator tones such that the two control loops operate in isolation. A known drawback of increasing f_{chp} is the reduction in input impedance but as shown in Section IV-A, this reduction can be mitigated with technology scaling and using a smaller value for C_I.

Given these dynamics, there is still an important distinction to be made with regards to the rate of information seen at the output and the 3-dB bandwidth for signal amplification that in this case is the product of $f\ k_1 \approx 250$ kHz. The digital output will encode an effective number of bits (ENOB) that relates to the ATC's precision [i.e., signal-to-noise and distortion ratio (SNDR)] and presents pulsewidth information of every cycle that in this case is oversampled by N parallel phases. However, for one phase, the entropy rate can be estimated in terms of f_{osc} (SNDR-1.76)/6.02. This highlights an important motivation for time-domain processing since this information rate may easily be 10× larger than a clocked digital bitstream that maximally yields 1 bit per clock cycle. Optimistically, this implies that time-domain techniques achieve a proportional boost in power efficiency since the digital power dissipation is a function of f_{osc} even though a higher rate of information is being processed. For the latter to hold, we must require the analog and oscillator sub-blocks to operate with the negligible power budget.

III. Circuit Implementation

The transistor schematic for the proposed ATC is shown in Fig. 4, and the size of each device is listed in Table I. This circuit can be segmented into four parts corresponding to the transconductor, oscillator, delay stage, and flicker rejection circuit. Each sub-block, including the capacitor array, will be described in the following. This configuration uses two bias voltages V_{BN} and V_{BP} to source the annotated drain currents. Both of these voltages are derived on-chip using a simple current mirror structure and a 1-μA off-chip reference. Furthermore, an external reference voltage V_C is used to control the common mode voltage of V_R that is placed at $V_{\text{DD}}/2$. Note that the 65-nm technology used here provides transistors that can be configured with 150-mV (lvt), 250-mV (vt), and 350-mV (hvt) threshold voltages (V_{TH}). The lvt option is used exclusively to reduce the supply voltage to 0.5 V with the exception of M_{23-24} which use a 250-mV threshold.

A. Low-Noise Transconductor

The complementary style transconductor [Fig. 4(a)] is adopted from [20] to exploit two aspects of oscillator-based integration. The first is that the operating conditions and transistor characteristics do not influence the loop gain of the time-based integrator but rather affect the noise characteristics which are already improved due to current recycling. Second, the voltage fluctuation across V_X and V_S is negligible particularly if all transistors in the Gm cell and oscillator are in sub-threshold operation. This implies that the circuit can operate reliably with a narrow V_{DS} margin for each transistor since the gate voltage V_X is carefully controlled in closed loop and there is little concern for instability. The self-biasing cascodes $M_{3,6}$ biases each input pair with V_{DS} that is highly correlated with the threshold voltage and provides abundant dummy devices to improve matching. The cascodes also reduce the parasitic gate capacitance of the transconductor by reducing the Miller effect that may otherwise lead to increased noise.

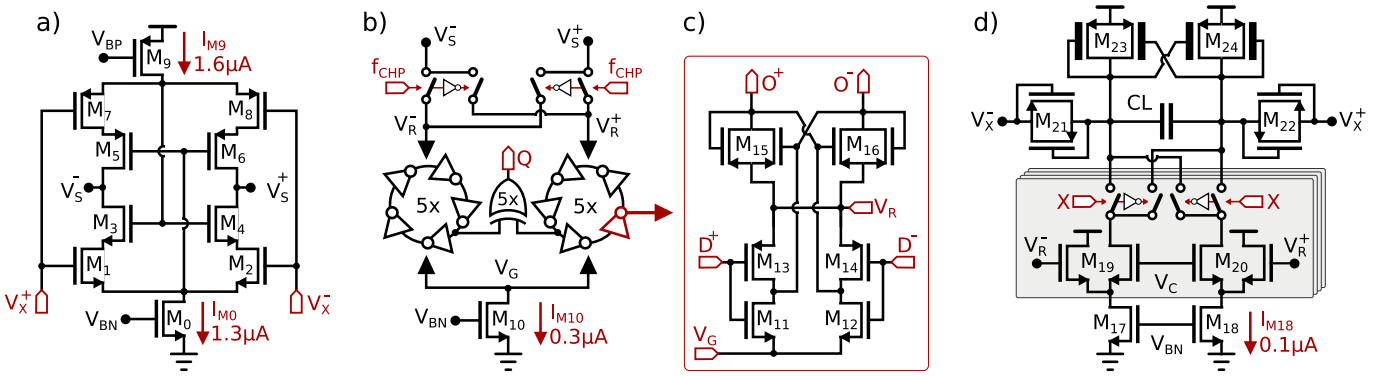

Fig. 4. Transistor level implementation of the ATC circuit in Fig. 2(a). Here, the complementary structure represents (a) main transconductor. (b) Pseudo-differential oscillator where each delay cell is shown in (c). (d) Flicker rejection stage where only the gray section is replicated for each phase. Note that all devices have their body connected to the corresponding supplies with the exception of M_{5-8} which have the body connected to the drain of M_9. Furthermore, M_{13-16} and M_{21-22} their body connected to V_R and either terminal of C_L, respectively.

TABLE I
DEVICE SIZING IN MICROMETERS WITH THE LABELS FROM FIG. 4

Device	Size (W/L)	Device	Size (W/L)
M_0	26/5	M_{15-16}	0.2/2.5
M_{1-2}	16/0.25	M_{17-18}	2/5
M_{3-4}	2/1	M_{19-20}	10/0.2
M_{5-6}	4/0.5	M_{21-22}	1.6/0.4
M_{7-8}	0.8/1.4	M_{23-24}	0.96/4
M_9	32/0.1	Logic	0.3/0.1
M_{10}	6/5	Switch_{CHP}	1/0.1 (P_{type})
M_{11-12}	1.5/2.4	Switch_X	1/0.2 (N_{type})
M_{13-14}	2.3/2.5	C_L	21/21

Achieving good noise performance for this configuration relies on minimizing the drain–current noise from each transistor in the oscillator when referred to the input [7]. As the ratio I_{M10}/I_{M0} is reduced, the noise efficiency factor (NEF) of this circuit will asymptotically decrease to the optimal value for this topology (i.e., $\eta\sqrt{2}$) [21]. On the other hand, I_{M10} controls the oscillation frequency which must be sufficiently large such that the oscillator harmonics lie out of band similar to the chopper harmonics.

The lack of filtering requirements allows the asynchronous implementation to choose a large f_{osc} by reducing C_{gate} such that any intermodulation products with f_{chp} do not fall in-band [22], and the circuit size is minimized. When using this configuration as a clocked $\Delta\Sigma$ modulator [23], this freedom is lost because k_1 must be directly related to the oversampling ratio. If the system can afford, a fast oversampling clock f_{osc} can still be large but it would be more effective to choose f_{osc} close to the Nyquist frequency such that the harmonics of f_{osc} can be removed reliably during decimation as they have already been shaped by the loop filter. This circuit also constrains the minimum value for N due to the limited linearity of the transconductor for a given input range. This is because the ratio $2V_{\text{DD}}\ f/(N+1)$ determines the maximum peak-to-peak amplitude of the error signal seen at V_X. Fortunately, for high-gain applications, f is small resulting in sub-millivolt signal at V_X, and therefore high linearity can be achieved while using just a few phases in parallel.

B. Pseudo-Differential Oscillator

The main feature of the oscillators [Fig. 4(b)] used by this ATC is that it uses differential logic and the delay stage [Fig. 4(c)] is biased around the middle of the supply making the digital buffers for phase detection more power efficient. The corresponding advantages are best contrasted with a simple inverter delay cell that uses a capacitive load to ground. First, the inverter-based implementation would experience voltage spikes on V_R due to discontinuous conduction of current but would also contaminate the ground with the ac current pulses. The configuration adopted from [24] exhibits continuous charging and discharging currents that can be confined within the virtual supply nodes V_G/V_R. Moreover, using switching transistors that are several square micrometers in size to load for the preceding gate reduces the sensitivity to process variation with smaller area requirements since the transistor gate capacitance achieves a higher density than poly-poly or metal-oxide-metal (MOM) capacitors.

C. Flicker Rejection Stage

The flicker removal circuit [Fig. 4(d)] biases the input of the transconductor by feeding back common-mode and differential-mode signals using a cross-coupled load to enable low voltage operation without an additional common-mode feedback circuit [20]. The differential feedback provides flicker cancellation by demodulating the digital output using a switched current digital to analog converter (DAC) that integrates on C_L which is a large vertical metal-insulator-metal (MIM) capacitor placed over the analog circuitry. The diode connected devices M_{21-22} represent pseudo-resistors of 100 Mω that provide a resistive path to V_X and further smooth high-frequency tones from f_{chp} and f_{osc}. A significant variation in resistive value is inherently expected but it is important to note that it does not influence the signal amplifying path and the non-dominant poles are far away from the 8-kHz bandwidth of $F(s)$ in (3) by virtue of not using a second analog integrator that may compromise stability. The common mode feedback regulates V_R with respect to V_C by biasing the common mode of V_X. For this loop, the gain arises from transconductance ratio $\text{gm}_{M19-M20}/\text{gm}_{M23-M24}$ together

with the drain resistance ratio $\text{rds}_{M10}/(\text{rds}_{M0} + \text{rds}_{M9})$. This readily provides over 30 dB of gain with the dominant pole provided by the pseudo-resistors that will also attenuate the input common-mode signals.

D. Capacitive Feedback Network

Both electrode inputs feed into separate capacitor arrays that off-set the scaled PWM signal generated at the output to calculate the differential error signal on V_X. Each array is 20×23 μm^2 in size and uses 28 elements in a 4×7 configuration with 2.7×2.7-μm^2 horizontal MOM capacitors with six fingers on metal layers 2–7. The following allocation is used: $C_I = 17\times$, $C_F = 1\times$, $C_U = 5\times$, $C_G = [0\text{–}5]\times$. The particular configuration in Fig. 2 can readily accommodate changes in dynamic range or adjustments in N. This is because f is dominated by the ratio C_F/C_I such that the design can freely change the number of phases being fed back without significantly changing the amplification dynamics. In addition, increasing C_F will extend the dynamic range of the circuit since the noise floor will remain unchanged while providing less signal gain and having excessive circuit bandwidth.

IV. Impact of Technology Parameters

This section further highlights two features of the proposed topology that can be taken advantage of in advanced CMOS technologies where mismatch and process variation are the leading concern for designers. First, we will summarize the scaling properties that arise while chopping in the input signal, and then, we will show that also for the asynchronous case, the time-domain integration fundamentally helps with mitigating mismatch in digital-to-analog conversion using a behavioral model as an example.

A. CMOS Scaling of Chopper Impedance

First, consider the input impedance R_{IN} of the simple chopper structure used here [25]. For sensor applications, it is essential to maintain a large input impedance that avoids signal attenuation because many integrated sensors exhibit a source resistance of several megaohms

$$C_I = 10C_{\text{GM}} = \frac{20}{3} W L C_{\text{ox}} \tag{4}$$

$$f_{\text{chp}} = 2f_{\text{cor}} = \frac{2K_F}{WLC_{\text{ox}}^2 e_{\text{gd}}^2}. \tag{5}$$

The expression in (4) is first used to select C_I as $10\times$ the parasitic capacitance C_{GM} seen on V_X due to the transconductance. This configuration avoids degrading the noise performance during amplification [17]. C_I is further equated in terms of the width W and length L of the input transistors. The chopper frequency is placed at exactly twice the corner frequency f_{cor} which is the frequency at which the flicker noise is equal to the thermal noise floor $e^2{}_{\text{gd}}$ of the target input-referred noise profile. Rearrangement of the terms will yield (5), which uses the trap density K_F to estimate for flicker noise for a specific fabrication process [26]

$$R_{\text{IN}} = \frac{1}{2C_I f_{\text{chp}}} = \frac{3C_{\text{ox}} e_{\text{gd}}^2}{80K_F} \tag{6}$$

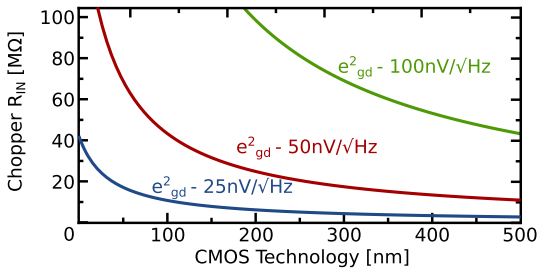

Fig. 5. Chopper-based input impedance as a function of CMOS technology using typical process parameters $K_F = 3.2e-38$ and $C_{\text{ox}} = 1.6e-12$ [F/μm^2]/L where L is the technology feature size in nanometre with the oxide thickness being estimated as 1/50 times the feature size.

Equation (6) calculates the expected input resistance and provides a first-order estimation of amplifier impedance with respect to process parameters. The fact that R_{IN} depends linearly on C_{ox} implies that input resistance can be improved by using more advanced technologies. The expected values for R_{IN} are plotted in Fig. 5 as a function of CMOS technology with varying noise requirements. Eventually, the gate leakage will inhibit this trend as the associated shot noise limits the sensitivity for technologies beyond 65 nm. This result primarily constrains the selection of transistor size [25] that in turn determines f_{chp} and f_{osc}.

B. Modulated Mismatch in Oscillators

Mismatch due to process variation is the primary cause of distortion during multi-bit signal conversion. Minimizing this source of nonlinearity is essential for both synchronous and asynchronous $\Delta\Sigma$ modulators because mismatch in the feedback DAC is not shaped by the loop filter [27]. Fortunately, the modulating property of the oscillator can remove this distortion if the phase readout is performed in a parallel fashion [5]. Here, we will concisely demonstrate that property arises because the mismatch induced components are simply being averaged and induce a dc-offset together with tones at the harmonic components of f_{osc}. This uses a mapping that relates the phase difference x to the generated PWM waveform as a function of time τ defined in (7). The following expression in (8) then evaluates the analog feedback voltage that appears on V_X in the ideal case for a given a phase difference of $\Delta\phi$ between the two oscillators

$$A(\tau, x) \triangleq \begin{cases} 1 & \tau\,(\text{mod}1) < x \\ 0 & \text{otherwise} \end{cases} \tag{7}$$

$$V_X(t) = f \cdot \sum_{k=0}^{N-1} \underbrace{A\left(t \cdot f_{\text{osc}} + \frac{k}{N},\ \Delta\phi\right)}_{Q_k(t)} \tag{8}$$

$$Q_k(t) = \left(1 + \frac{\sigma_{C,k}}{C_U}\right) A\left(t \cdot f_{\text{osc}} + \frac{k}{N},\ \sigma_{\tau-\mu,k} + \Delta\phi\right). \tag{9}$$

There are two-independent sources of mismatch for each phase: the deviation in capacitor weights of C_U $\sigma_{C,k}$ and the differential delay variation in oscillator stages as a fraction of the oscillation period $\sigma_{\tau,k}$ that includes the digital gates

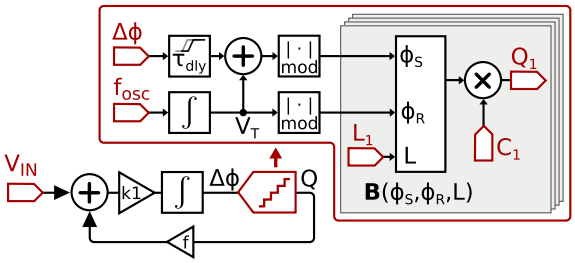

Fig. 6. Continuous-time multi-phase VCO model for evaluating parameter sensitivity with transient simulations using the logical operator **B** in (10).

generating Q (i.e., inverters and XOR-gate). These are used to formulate (9) that considers a particular phase of $Q(t)$ and the random mismatch variables that have process dependent normal distributions. The variation in delay will locally increase/decrease the pulsewidth of Q for a specific phase k. This is a time-invariant component of the gate delay while $\Delta\phi$ and T_{osc} are signal dependent. Precisely formulating the cumulative variation of σ_τ will relate the transistor sizing, gate capacitance, and threshold voltage of each delay during operation.

Notice that A is a linear function of $\Delta\phi$ with a gain of 1 for the dc component of the PWM output which can be further expanded to extract the high-frequency behavior. However, by design, these components are intentionally avoided which should reveal that the capacitor weights are always uniformly averaged irrespective of $\Delta\phi$. Closed-loop operation feeds back each $\sigma_{\tau,k}$ such that the sum all components has zero mean, that is $\sigma_{\tau-\mu,k} = \sigma_{\tau,k}$-$(\sum_{k=0}^{N-1} \sigma_{\tau,k}/\text{N})$. The residual variation in delay for each phase inevitably induces spurs at harmonics of f_{osc}.

Verifying this behavior is best done by modifying the behavioral model commonly used for oscillators [28] to accommodate multi-phase readout using the above-mentioned expressions. Such a model is shown in Fig. 6. This configuration uses an internal time variable at V_T that accumulates according to f_{osc}. Given a set of quantization levels L_k or equivalently the number of phases, a logical function **B** will compute the corresponding PWM waveform of Q, which are weighted by the associated capacitor C_k. In this case, the digital gate delay arising from computing the phase difference and applying feedback to the capacitive DAC can also be modeled by adjusting τ_{dly}

$$\mathbf{B}(\phi_S, \phi_R, L) \triangleq (\phi_S > L > \phi_R) \vee (\phi_S < \phi_R < L) \vee (L < \phi_S < \phi_R). \quad (10)$$

The logical expression in (10) simply compares the two phases with respect to L and evaluates the digital condition for which the output should be high. This representation implies that the delays correspond to the interval between each level which can be distributed uniformly as $L_k = (0.5 + k)/L$ for integers k from 0 to $N - 1$. By distributing the quantization levels from 0 to 1, the corresponding delays are inherently normalized to the periodicity of $\phi_{S/R}$ without explicitly having to compute values with respect to f_{osc} even when it is dynamically changing. In addition, a difference in oscillator frequency between X_{1-2} can also be accommodated

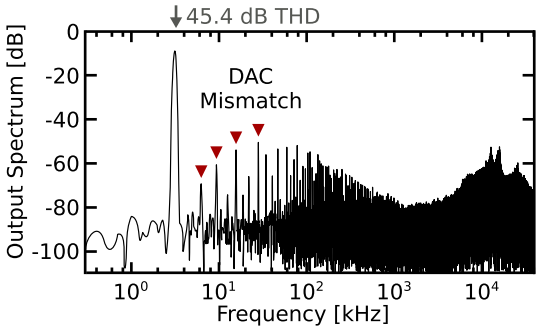

Fig. 7. Simulated output spectrum with a 2.5-kHz input at −6 dB of the full input range for an equivalent asynchronous flash quantizer with 2.6 bits of resolution and 5% mismatch in $\sigma_{\tau,k}$ and $\sigma_{C,k}$.

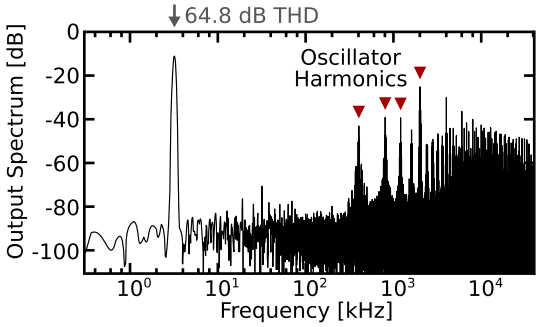

Fig. 8. Simulated output spectrum with a 2.5-kHz input at −6 dB of the full input range for an asynchronous VCO quantizer with 2.6 bits of resolution, 300 kHz f_{osc} and 5% mismatch in $\sigma_{\tau,k}$ and $\sigma_{C,k}$.

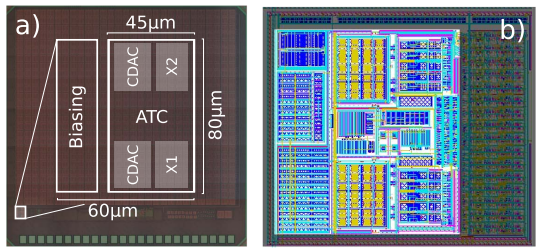

Fig. 9. (a) Micro-photograph of the fabricated prototype showing an annotated floor plan. (b) Poly layer together with the first three metal layers of the circuit layout.

by adding a second integrated frequency component to the summation node.

Now the impact of mismatch can be simulated by adding parameter variation in the quantizer levels and the feedback weights (f). The analogous case where the mismatch is not modulated (i.e., f_{osc} is 0) loosely corresponds to a flash-based ADC since the phase is simply being compared with N thresholds. The corresponding spectra of the flash quantizer is shown in Fig. 7 and the oscillating quantizer is shown in Fig. 8 where we observe the distortion components in different bands of the spectrum.

V. Measured Results

The commercially available Taiwan Semiconductor Manufacturing Company (TSMC) 65-nm CMOS low power mixed signal (MS) RF technology (1P9M 6X1Z1U RDL) was used to prototype the proposed circuit and demonstrate measured noise and linearity characteristics. The chip micro-photograph of this prototype is shown in Fig. 9. The setup used to take

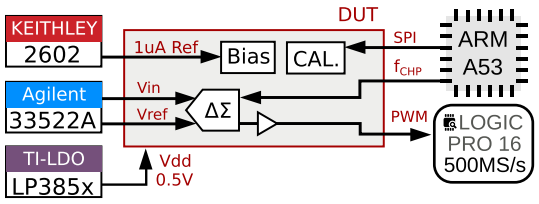

Fig. 10. Experimental setup used for characterizing the ATC for low-noise signal conversion showing the respective instruments that were used.

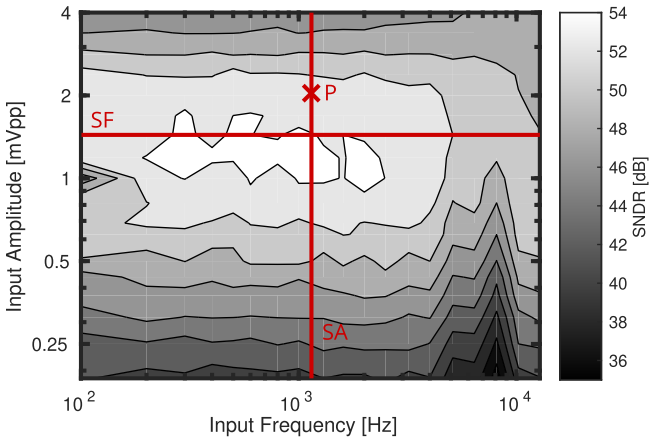

Fig. 11. Characterization sweep evaluating the SNDR performance using differential sinusoid at the input with varying amplitudes and frequencies.

these measurements is shown in Fig. 10 and uses a custom printed circuit board to regulate V_{DD} on-board with additional decoupling.

The external biasing allows this setup to first tune the circuit sensitivity by adjusting the 1-μA reference current which scales all bias currents proportionally and then using V_C, the oscillation frequency can be fine-tuned as V_R is controlled which modulates I_{M10}. The supply voltage can be tuned but reducing the supply below 0.5-V limits the biasing current and reduces the circuit sensitivity. Similarly, increasing the supply is mainly constrained by the buffers that digitize the oscillator waveform and can induce a large leakage current beyond a voltage of 0.65 V.

The tone generated by the Agilent signal generator is attenuated resistively by a factor of 10 to achieve a low-noise differential test signal at the input of the instrumentation circuit. Two phases from the asynchronous output Q are captured at 500 MS/s using high-speed digital scope which can then be post-processed off-line to investigate the features of separate PWM signals during different operating conditions. Both the chopper tones and PWM carrier can be observed outside the signal bandwidth at harmonics of 78 and 350 kHz, respectively.

The characterization procedure evaluates the SNDR for varying input amplitudes and frequencies. For a particular device, this characteristic is shown in Fig. 11. In extension, Figs. 12 and 13 show the distortion components as a function of amplitude along single amplitude (SA) and the frequency along single frequency (SF), respectively. Fig. 14 shows what the input-referred power spectral density of Q looks like for a particular operating point at P. Here, the lowest gain setting of 41 dB was used to demonstrate operation with the maximum dynamic range. Although the circuit bandwidth

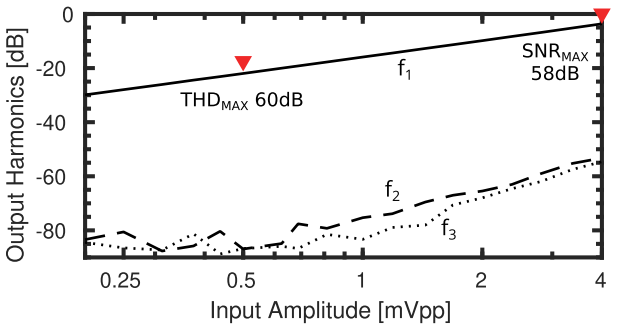

Fig. 12. Measured output harmonics due to a differential mode 1-kHz input signal at different amplitudes corresponding to the SNDR measurement along SA in Fig. 11.

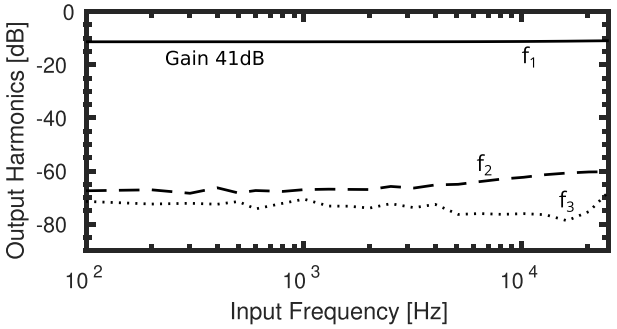

Fig. 13. Measured output harmonics due to a differential mode 1.5-mVpp input signal at different frequencies corresponding to the SNDR measurement along SF in Fig. 11.

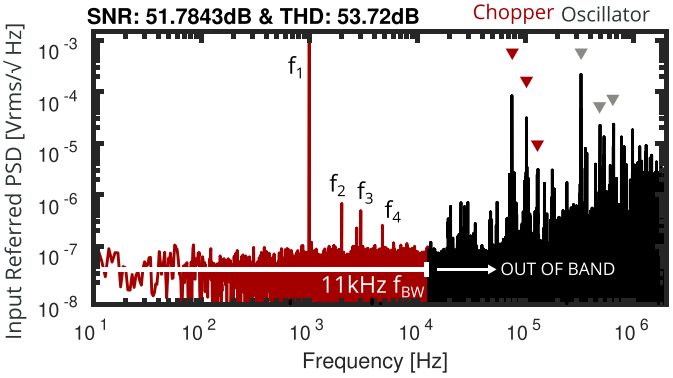

Fig. 14. Measured output spectrum due to a differential 2-mVpp input signal at 1 kHz corresponding to the SNDR measurement at point P in Fig. 11.

theoretically exceeds the range of frequencies resolved here, the interfering tones shown in Fig. 14 prevent inaccurate measurements to confirm this result. Using a similar procedure, the common-mode rejection ratio (CMRR) is characterized and shown in Fig. 15. Again, Figs. 16 and 17 show the distortion components due to a common-mode input as a function of amplitude along SA and frequency along SF, respectively. Due to the limited voltage overhead from the current sources in the transcondutor, the high-frequency common-mode interference can result in degenerated operation as they are not attenuated by the pseudo-resistor. This mode of failure where the oscillators are saturated is out-lined by the dashed region.

Note that flicker noise from each oscillator is not removed by the chopper configuration in Fig. 4. However, there is no apparent 1/f noise profile in the 10–100-Hz band even though

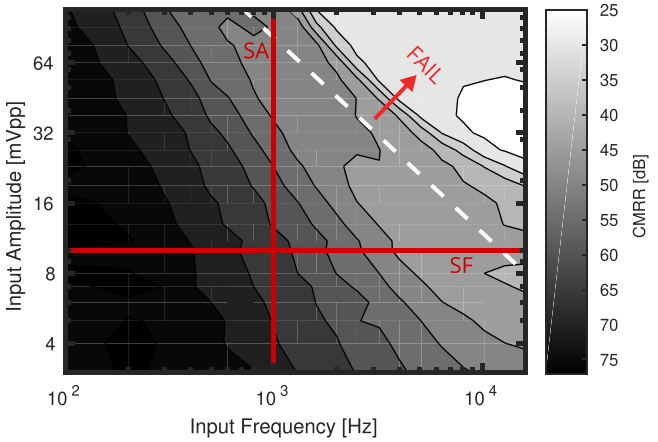

Fig. 15. Characterization sweep evaluating the CMRR performance using large common-mode sinusoid at the input with varying amplitudes and frequencies.

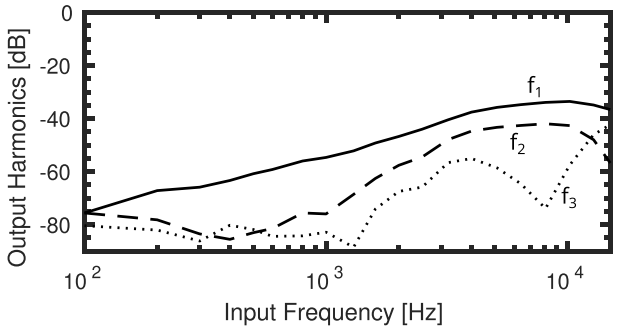

Fig. 16. Measured output harmonics due to a common mode 10-mVpp input signal at different frequencies corresponding to the CMRR measurement along SF in Fig. 15.

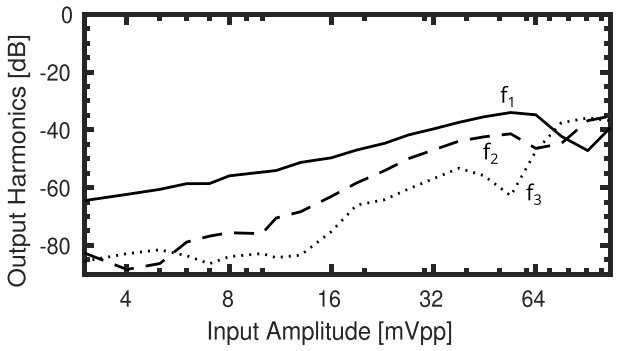

Fig. 17. Measured output harmonics due to a common mode 1-kHz input signal at different amplitudes corresponding to the CMRR measurement along SA in Fig. 15.

the oscillators are small in size. This is because the rms gate-voltage fluctuation due to flicker noise at each device is scaled by the open-loop gain of the ATC when referred to the input.

The maximum achieved total harmonic distortion was 60 dB for a 1-kHz sinusoidal input. The main source of performance degeneration in this circuit for larger input signals is due to the use of poorly regulated bias currents in the differential pair and relying on pseudo-differential phase read-out that allows some common-mode fluctuation at V_S to couple to the output Q. Either introducing cascodes or using a folded cascode topology may improve linearity at the cost of increasing the required voltage headroom or reducing the noise efficiency. However,

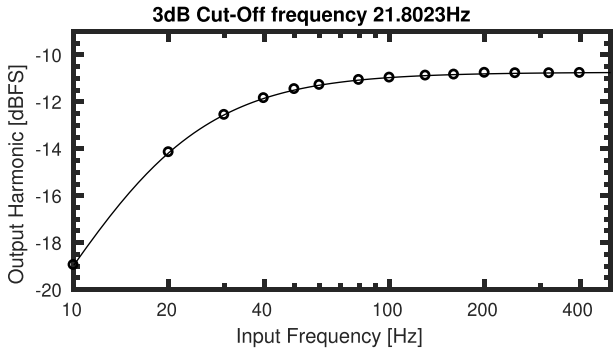

Fig. 18. Measured frequency response due to differential 2-mVpp input signal that is capacitively coupled to the ATC input using 0.47-nF capacitors.

the dynamic range exceeding 50 dB should be sufficient for the physiological range of amplitudes for neural activity given that there are no external aggressors present during recording. We can further confirm the effectiveness of the mismatch rejection technique as the Monte Carlo simulation results indicate that each phase should exhibit 1.1% standard deviation in coupling factor for a $3-\sigma$ confidence interval. This should lead to a similar distortion characteristic shown in Fig. 7 with a large number of dominant harmonics being generated due to mismatch errors. Instead, distortion is dominated by the second and third harmonic typical of more conventional analog nonlinearity.

The input impedance of this circuit was estimated by removing the resistive attenuation network and instead capacitively coupling the signal generator to the input. This assumes that the input will exhibit a *RC* time constant that is dominated by the coupling capacitor and the resistive/leakage component from the chopper in combination with the electrostatic discharge protection that can be measured directly. The frequency-dependent response is shown in Fig. 18. The 3-dB cutoff frequency was estimated at 21.8 Hz. In this case, two 0.47-nF capacitors were used to couple both inputs which implies the input resistance is around 31 Mω. Parasitics at the input or capacitor variation can inflate this value and it is likely the impedance is closer to the analytical estimate of 22 Mω according to (6).

The detailed system characteristics are summarized in Table II. The system power dissipation was specified at 1.3 μW from these measurements. The relative power and area utilization of each sub-circuit is compared in Fig. 19. As expected, a large fraction of both power and area is used by the main analog circuits that consist of the low-noise transconductor and the flicker rejection stage. This distribution maximizes the NEF and shows that the asynchronous digital logic can provide additional functionality without a significant resource overhead. In relation to the work in [7], this ATC topology exhibits a significant reduction in power budget although input-referred noise figure is slightly increased. This improvement is not as pronounced in comparison with [8] but instead the figure of merit is superior. Other works show that both time-based and voltage-based instrumentation can achieve near ideal noise efficiency but only select topologies enable more advanced CMOS process to yield a smaller silicon

TABLE II
SYSTEM CHARACTERISTICS AND COMPARISON WITH STATE OF THE ART

Parameter	[unit]	**This Work**	[8]	[29]	[7]	[6]	[30]	[31]	[32]	[33]	[34]
Year		**2017**	2017	2017	2017	2017	2016	2016	2015	2013	2012
Application		**EAP**	ECG	LFP	-	LFP	ECG	EAP	EAP	EAP	EAP
Technology	[nm]	**65**	40	130	40	40	65	65	90	180	65
Modality		**Time**	Time	Volt.	Time	Volt.	Volt.	Volt.	Volt.	Volt.	Mix
Supply-V	[V]	**0.5**	0.6	1.2	1.2	1.2	0.6	1	1	0.45	0.5
Supply-I	[A]	**2.55 µ**	5.5 µ	5.3 µ	14 µ	2.5 µ	3 n	3.3 µ	2.8 µ	2.1 µ	10 µ
Bandwidth	[Hz]	**11 k**	150	500	5 k	200	370	8.2 k	10.5 k	10 k	10 k
Input Range	[mVpp]	**4**	40	-	8	100	25	220	1	1	1
CMRR	[dB]	**>60⋆**	60	90	97	-	60	>80	>45	73	75
SFDR	[dB]	**60**	56	72	70	79	75	>40	>37	>46	>34
Noise Floor	[V/$\sqrt{\text{Hz}}$]	**36 n**	0.6 µ	46n	32 n	-	1.4 µ	27.5n	35n	29n	100n
RMS Noise	[μV_{rms}]	**3.8**	7.8	1.1	2.3	5.2	26	4.1	3.04	3.2 µ	4.9 µ
Area	[mm^2]	**0.006**	0.015	0.013	0.015	0.135	0.15	0.042	0.137	0.25	0.013
NEF / PEF		**2.2 / 2.4**	8.1 / 39	2.9 / 10	4.7 / 27	22 / 581	2.1 / 2.6	3.2 / 10	1.9 / 3.6	1.57 / 1.1	5.99 / 18

⋆ For common-mode frequencies <200 Hz

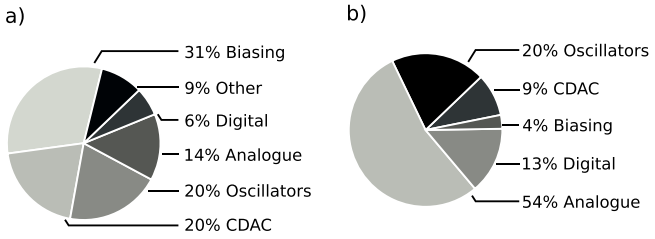

Fig. 19. Power and area contributions from each sub-circuit. (a) System area: 85 × 70 μm^2. (b) System power: 1.28 μW.

footprint. The pioneering work in [34] already demonstrated that resource efficient signal acquisition is best realized by combing signal quantization and amplification into a single loop. The main drawback was that this mixed signal topology was still relatively complex for hundreds of channels and linearizing the feedback for closed loop quantization came with a considerable reduction in noise efficiency. However, the $\Sigma\Delta$ operation of the clocked VCO and the $\Sigma\Delta$ modulated DAC in the feedback enable a powerful technique that trades off excessive bandwidth for reduced circuit size or DAC complexity. The same technique is applied here to enable a compact multichannel configuration. Our future work will extend on the current prototype by additionally providing electrode off-set cancellation for *in vivo* experiments with multi-channel recording capabilities.

VI. CONCLUSION

This paper proposes a chopper stabilized ATC to enable high-impedance electrode instrumentation for integrated sensing systems that require ultralow-voltage operation for power saving. The time-domain techniques enabled by this ATC topology alleviate the difficulty of performing precise instrumentation in advanced CMOS technologies while also providing improved power efficiency together with a substantial reduction in size. The presented configuration achieves a power budget of 1.2 μW for a 36-nV/$\sqrt{\text{Hz}}$ noise floor requirement and a compact silicon footprint of 0.006 mm^2. In extension to presenting the implementation details, this paper also provides essential modeling and analytical tools for further optimization. This will enable other mixed-signal systems that require high-noise efficiency, high speed, or asynchronous signal conversion to effectively adopt time-based techniques and utilize the presented circuit implementation.

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Lieuwe B. Leene (S'13–M'16) received the B.Eng. degree in electronic engineering from the Hong Kong University of Science and Technology, Hong Kong, in 2011, and the M.Sc. and Ph.D. degrees in electronic engineering from the Imperial College London, London, U.K., in 2012 and 2016, respectively. He is currently a Research Associate with the Centre for Bio-inspired Technology, Department of Electrical and Electronic Engineering, Imperial College London. His current research interests include low noise instrumentation systems, brain-machine interfaces, data converters, and mixed signal processing techniques for bio-medical applications.

Timothy G. Constandinou (AM'98–M'01–SM'10) received the B.Eng. and Ph.D. degrees in electronic engineering from Imperial College London, London, U.K., in 2001 and 2005, respectively.

He is currently a Reader of neural microsystems within the Circuits and Systems Group, Department of Electrical and Electronic Engineering, Imperial College London, and also the Deputy Director of the Centre for Bio-Inspired Technology. His current research interests include neural microsystems, neural prosthetics, brain-machine interfaces, implantable devices, and low-power microelectronics.

Dr. Constandinou is a Fellow of the IET, a Chartered Engineer, and a member of the IoP. He is a member of the IEEE BioCAS Technical Committee and the IEEE Brain Initiative Steering Committee. Within the IEEE, he serves for several committees/panels, regularly contributing to conference organization, technical activities, and governance. He was the Technical Program Co-Chair of the 2010, 2011, and 2018 IEEE BioCAS conferences, the General Chair of the BrainCAS 2016 and NeuroCAS 2018 workshops, the Special Session Co-Chair of the 2017 IEEE ISCAS Conference, and the Demonstrations Co-Chair of the 2017 BioCAS Conference. He is the Chair of the IEEE Sensory Systems Technical Committee. From 2017 to 2019, he serves on the IEEE Circuits and Systems Society Board of Governors. He is currently an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS.