A Low-Flicker-Noise 30-GHz Class-F_{23} Oscillator in 28-nm CMOS Using Implicit Resonance and Explicit Common-Mode Return Path

Yizhe Hu, *Student Member, IEEE,* Teerachot Siriburanon, *Member, IEEE,* and Robert Bogdan Staszewski, *Fellow, IEEE*

***Abstract*— This paper presents a millimeter-wave (mmW) frequency generation stage aimed at minimizing phase noise (PN) via waveform shaping and harmonic extraction while suppressing flicker noise upconversion via proper harmonic terminations. A 2nd-harmonic resonance is assisted by a proposed embedded decoupling capacitor inside a transformer for explicit common-mode current return path. Class-F operation with 3rd-harmonic boosting and extraction techniques allow maintaining high quality factor of a 10-GHz tank at the 30-GHz frequency generation. We further propose a comprehensive quantitative analysis method of flicker noise upconversion mechanism exploiting latest insights into the flicker noise mechanisms in nanoscale short-channel transistors, and it is numerically verified against foundry models. The proposed 27.3- to 31.2-GHz oscillator is implemented in TSMC 28-nm CMOS. It achieves PN of −106 dBc/Hz at 1-MHz offset and figure-of-merit (FoM) of −184 dBc/Hz at 27.3 GHz. Its flicker phase-noise ($1/f^3$) corner of 120 kHz is an order-of-magnitude better than currently achievable at mmW.**

***Index Terms*— 30 GHz, explicit common-mode (CM) return path, fifth generation (5G) communication, flicker noise reduction, implicit resonance, impulse sensitivity function (ISF), low phase noise (PN), millimeter-wave (mmW), oscillator, periodic transfer function (PXF).**

I. Introduction

TRADITIONAL cellular bands, i.e., <6 GHz, suffer from a severe bandwidth (BW) congestion and can barely cope with the increasing demands for data. Consequently, the fifth generation (5G) of cellular communications starts to utilize lower range of millimeter-wave (mmW) frequency bands, e.g., 28 GHz. To support higher data rates, more complex modulation schemes are being introduced, thus placing challenging requirements on phase noise (PN) of local oscillators. It is well known that for mmW oscillators, the quality (Q) factor degradation of a tuning varactor or a switched-capacitor (sw-cap) tuning network leads to worse PN in the thermal ($1/f^2$) noise region. To mitigate such degradation, the following solutions have been devised: the oscillator's resonant frequency gets lowered but then increases via a frequency multiplier, such as a doubler/quadrupler in [1] and [2], sub-harmonic injection locking [3], [4], and transformer-based class-F oscillator with a tuned power amplifier (PA) to extract its 3rd harmonic [5].

Yet, despite those PN improvements in the $1/f^2$ region, the flicker PN ($1/f^3$) corner of >10-GHz oscillators appears to always exceed ∼1 MHz, as surveyed in Fig. 1. Moreover, the underlying cause, i.e., the flicker ($1/f$) noise of MOS transistors, tends to worsen as CMOS scales, which will further degrade the integrated PN, thus limiting the achievable data rates in mmW transceivers. Considering an example of a mmW type-II all-digital PLL (ADPLL) shown in Fig. 2, the loop BW needs to be limited to <400 kHz to suppress the typical 10-ps quantization noise of its time-to-digital converter (TDC), according to the system simulations in

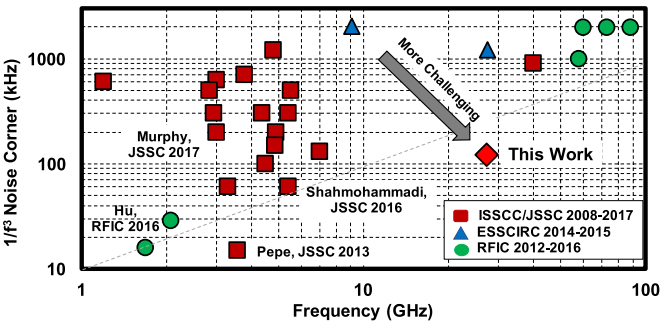


Fig. 1. Survey of $1/f^3$ corner of state-of-the-art RF and mmW oscillators.

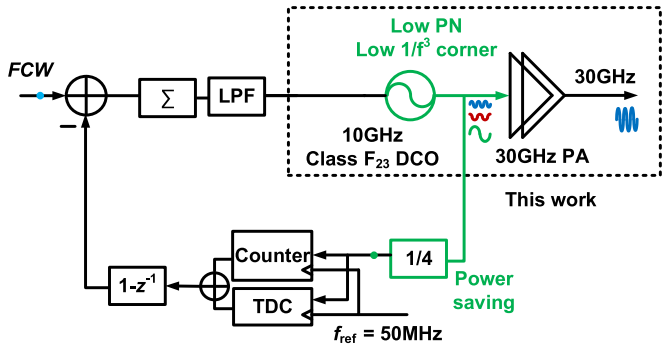


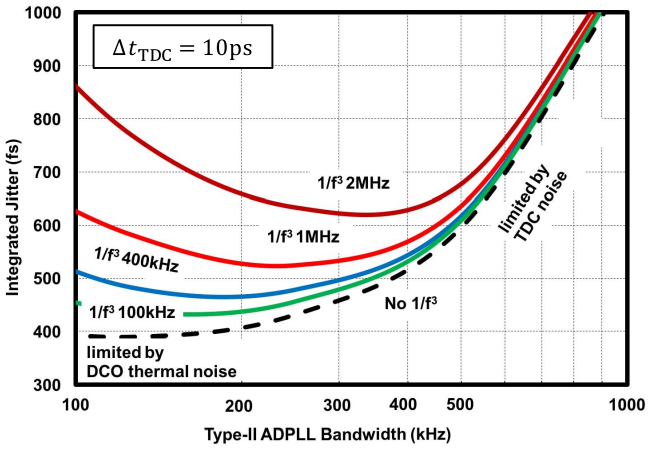
Fig. 2. Intended architecture of a 30-GHz ADPLL focused on its low-power and high-performance aspects.

Manuscript received December 1, 2017; revised February 22, 2018 and March 17, 2018; accepted March 18, 2018. Date of publication April 24, 2018; date of current version June 25, 2018. This paper was approved by Guest Editor Andrea Bevilacqua. This work was supported by the Science Foundation Ireland under Grant 14/RP/I2921. *(Corresponding author: Yizhe Hu.)*

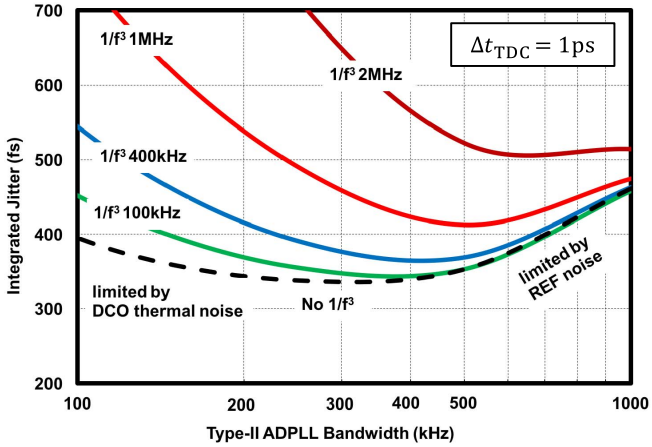
The authors are with the UCD School of Electrical and Electronic Engineering, University College Dublin, Dublin 4, Ireland (e-mail: yizhe.hu@ucd.ie).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2018.2818681



(a)



(b)

Fig. 3. Simulated integrated PN (translated to jitter) across loop BW of a type-II 30-GHz ADPLL for various $1/f^3$ noise corners of the oscillator. Conditions: PN_{DCO} at 10 MHz = -120 dBc/Hz, $f_{ref} = 50$ MHz, $\sigma_{ref} = 1$ ps. TDC resolution: (a) 10 ps and (b) 1 ps.

Fig. 3(a). Even with the TDC resolution as fine as 1 ps [see Fig. 3(b)], the loop BW must still be maintained quite narrow in order to prevent the reference noise from dominating the ADPLL's PN. This is due to the high multiplication ratio N of mmW PLLs (e.g., $N = 600$ for a 30-GHz oscillator locked to a typical $f_{ref} = 50$-MHz reference). Even the best realistic attempts at reducing the remaining ADPLL PN contributors will unfortunately leave the oscillator's $1/f^3$ PN as the limiting factor preventing from breaking through the 520 and 410 fs integrated jitter limits for the TDC resolution of 10 ps (typical state-of-the-art) and 1 ps (yet to be achieved), respectively. Consequently, techniques to lower the $1/f^3$ PN are highly desired for mmW generation.

Recent studies [6]–[8] deal with the flicker noise reduction in voltage-biased RF oscillators, i.e., in which the conventional mechanism of $1/f$-noise upconversion via the tail current source does not appear anymore [18]. In [6] and [9], it is suggested that the non-zero dc value of the effective impulse sensitivity function (ISF) is mainly caused by a 3rd harmonic current entering a capacitive path, resulting in the $1/f^3$ PN degradation. However, the effect of 2nd harmonic current is entirely neglected. Shahmohammadi *et al.* [7] explain that

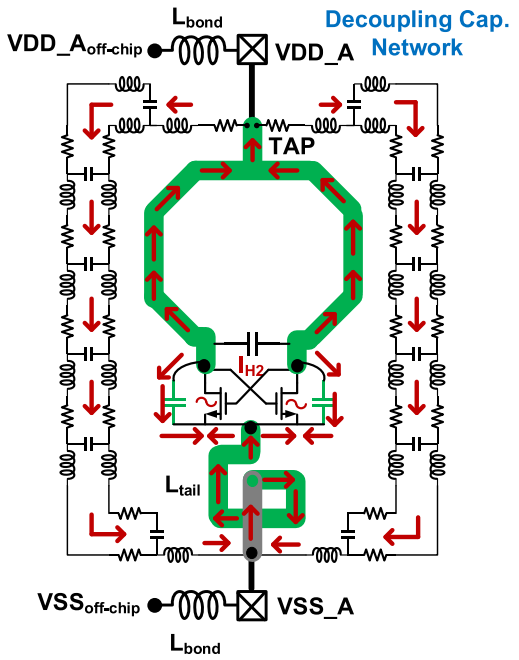


Fig. 4. Diagram of a conventional voltage-biased mmW oscillator with a tail inductor further showing its parasitic CM return path.

the $1/f$ noise upconversion is due to an asymmetry between rising and falling edges of the tank's voltage waveform, which is a consequence of a 2nd harmonic current (I_{H2}) entering the capacitive path. The effects of the 3rd harmonic current are shown as benign. That was further experimentally supported in [8], but the rigorous quantitative analysis of flicker noise upconversion is still missing in [7] and [8]. It appears that the lack of a complete numerical verification and the over-simplification of employed flicker noise model cause some contradictions and ambiguities in the currently available theory of flicker noise upconversion and reduction mechanism. Moreover, a direct translation of the above techniques [6]–[8] into mmW does not appear so straightforward. For example, employing a high-frequency oscillator with a one-turn inductor [10] or a conventional 1:2 transformer [7], [11] could suffer from high $1/f^3$ PN corner due to the uncontrolled 2nd harmonic current return path of the decoupling capacitor, as shown in Fig. 4, thus shifting the expected common-mode (CM) resonant frequency.

This paper proposes a 30-GHz frequency generation scheme shown in Fig. 5 using a 3rd harmonic extraction from a class-F_{23} oscillator operating at 10-GHz fundamental. It features a special 1:2 transformer including a proposed embedded decoupling capacitor for the precise control of the CM current return path [12]. Its PN in the $1/f^2$ thermal region is kept low via the 3rd harmonic resonance, and its $1/f^3$ PN corner is greatly improved (by an order-of-magnitude versus state-of-the-art) via a precise implementation of the 2nd harmonic resonance and the proposed explicit CM return path.

In Section II, the $1/f$-noise reduction mechanism based on the 2nd harmonic resonance in mmW voltage-biased oscillators is numerically verified in the 28-nm technology. Details of the proposed 30-GHz frequency generation scheme, focusing on an accurate implementation of the 2nd harmonic resonance,

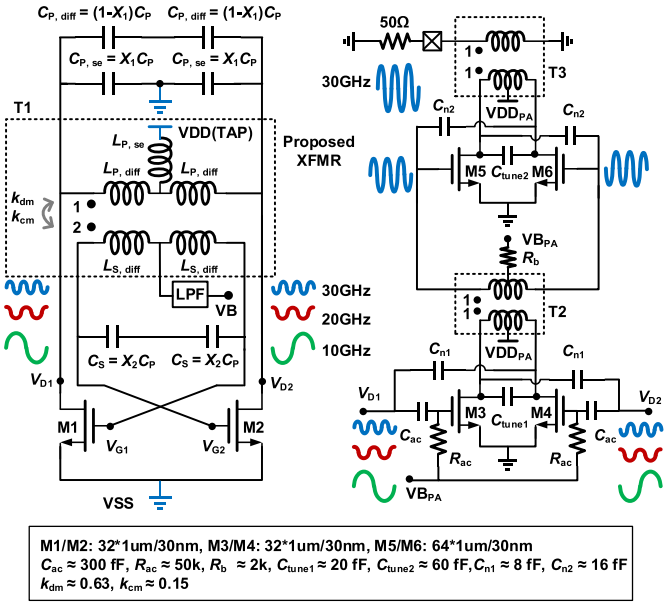


Fig. 5. Schematic of the proposed 30-GHz class-F_{23} oscillator using 2nd-harmonic resonance and 3rd-harmonic extraction.

are revealed in Section III. In Section IV, the proof-of-concept 30-GHz oscillator demonstrates the lowest $1/f^3$ PN corner of 120 kHz among mmW oscillators.

II. Flicker Noise Upconversion and CM Return Path in mmW Oscillators

A. Current Return Path in mmW Oscillators

The conventional voltage-biased mmW oscillator with one-turn inductor [see Fig. 4] can be modeled as shown in Fig. 6(a). The circuit includes a cross-coupled pair (M1, M2, with their parasitic capacitances C_{se1}), sw-cap bank with its elements shown in Fig. 6(b) (C_{diff} and the switch parasitics C_{se2}), main inductor (L_{diff}, L_{se}), decoupling capacitor network for the supply/ground (C_{decap} and its parasitic inductance L_{decap}), and tail inductor (L_{tail}). Two supplies are used, i.e., "analog" supply (VDD_A/VSS_A) for the oscillator core and "digital" supply (VDD_D/VSS_D) for the sw-cap bank. In addition, L_{bond} is used to model wirebonding inductors from the external supply ($VDD\_A_{off\text{-}chip}$, $VDD\_D_{off\text{-}chip}$, $VSS_{off\text{-}chip}$) to the IC wirebonding pad (PAD), while L_{wire} models the interconnecting wire inductances from PAD to the local supplies and grounds. C_{decap_bank} is used to model a local decoupling capacitor for the sw-cap bank, while $C_{decap,\,off\text{-}chip}$ and $L_{decap,\,off\text{-}chip}$ model the off-chip decoupling capacitor and its parasitic inductance, respectively.

In RF, and especially mmW circuits, defining local supply points, i.e., VDD_A or VSS_A, as ac grounds is not so straightforward. To start with, "current return path" should be considered. The differential-mode (DM) return path is for the DM current (e.g., I_{H1}, I_{H3}) from the drain of M1 to the drain of M2, and then from the source of M2 back to the source of M1, and vice versa. Thus, the (half-circuit) tank inductance in DM (L_{dm}) is simply L_{diff}, while the DM capacitance (C_{dm}) is dominated by C_{diff} when sw-cap is ON and by the parasitic C_{se2} when sw-cap is OFF. It was only very recently that the CM return path got introduced into the RF oscillator design for the purpose of $1/f^2$ and $1/f^3$ PN reductions [7], [8], and [11]. The path carries the CM current (e.g., I_{H2}) from the drain of M1/M2 to the source of M1/M2, and then back around. Hence, it is more appropriate to take the source node of cross-coupled pair (VSOURCE) as a reference rather than VSS_A for the CM return path analysis. One part of the CM return path includes the implicit CM tank, decoupling capacitor network, and tail filter, while the other part goes directly through the transistor's intrinsic capacitance C_{se1} ($=C_{ds1} + C_{gs2}$ for CM signal), shown in Fig. 6(c). Note that the parasitic single-ended capacitance of the sw-cap bank (C_{se2}) cannot be readily seen by the CM current, irrespective of whether the switch is ON or OFF, since it is connected to different supplies (i.e., "digital") through a large wirebonding inductance. Therefore, for most properly constructed oscillators, their implicit CM tank would comprise only the CM inductance of the main inductor. The on-chip decoupling capacitor network (L_{decap}, C_{decap}) needs to be properly constructed to provide a tight local return path for the CM current. However, its parasitic inductance L_{decap} is typically neglected by RF oscillator designers, often leading to detrimental effects on the flicker noise upconversion [11].

This consequence of neglecting the L_{decap} effects is becoming more critical now for mmW oscillator designs. As shown in Fig. 7(a), L_{decap} is modeled for different considerations of supply injection points ($VDD_{inj1,2,3}$). According to electromagnetic simulations in Fig. 7(c), the parasitic inductance could be neglected only when the injection point (VDD_{inj3}) is physically close to VSS. Fig. 7(b) offers an intuitive explanation. At very high frequencies, all the C_{unit} capacitors are seen as a short and so the LC network becomes inductive, resulting in VDD_{inj3} having the shortest return path. However, in the conventional mmW oscillator with a one-turn inductor, the supply injection point [VDD_A as shown in Fig. 6(a)] is physically far from VSS_A, thus introducing a significant inductance (several hundred pH). Finally, a parallel resonant LC tank can be seen by the CM current, [see Fig. 6(c)], in which the total CM inductance L_{cm} can be described as $L_{diff}+2L_{se}+2L_{decap}+2L_{tail}$, while the total CM capacitance C_{cm} is only C_{se1}. Obviously, both the parasitic L_{decap} and the deliberate L_{tail} have large influence on the CM resonant frequency (i.e., $1/(2\pi\sqrt{L_{cm}C_{cm}})$) in the mmW oscillator.

B. Flicker Noise Modulation and Upconversion

According to the theory of ISF [14], the flicker noise upconversion from M1/2 in Fig. 6 to PN involves two steps: 1) low-frequency voltage noise at the gate, $v_{1/f}$ at $\Delta\omega$ (e.g., $2\pi \times 10$ kHz), is modulated to cyclostationary current noise $i_{1/f,cyclo}$ around different harmonics $k\omega_0 \pm \Delta\omega$ through a noise modulation function (NMF) and 2) the current noise $i_{1/f,cyclo}$ turns into PN through its corresponding ISF.

It is well known that the flicker NMF is modeled by a time-varying transconductance [7]. However, this model only considers the $1/f$ noise mechanism due to the carrier number fluctuation (CNF), which means the carriers will be randomly trapped and released by impurities on the Si/SiO_2 interface.

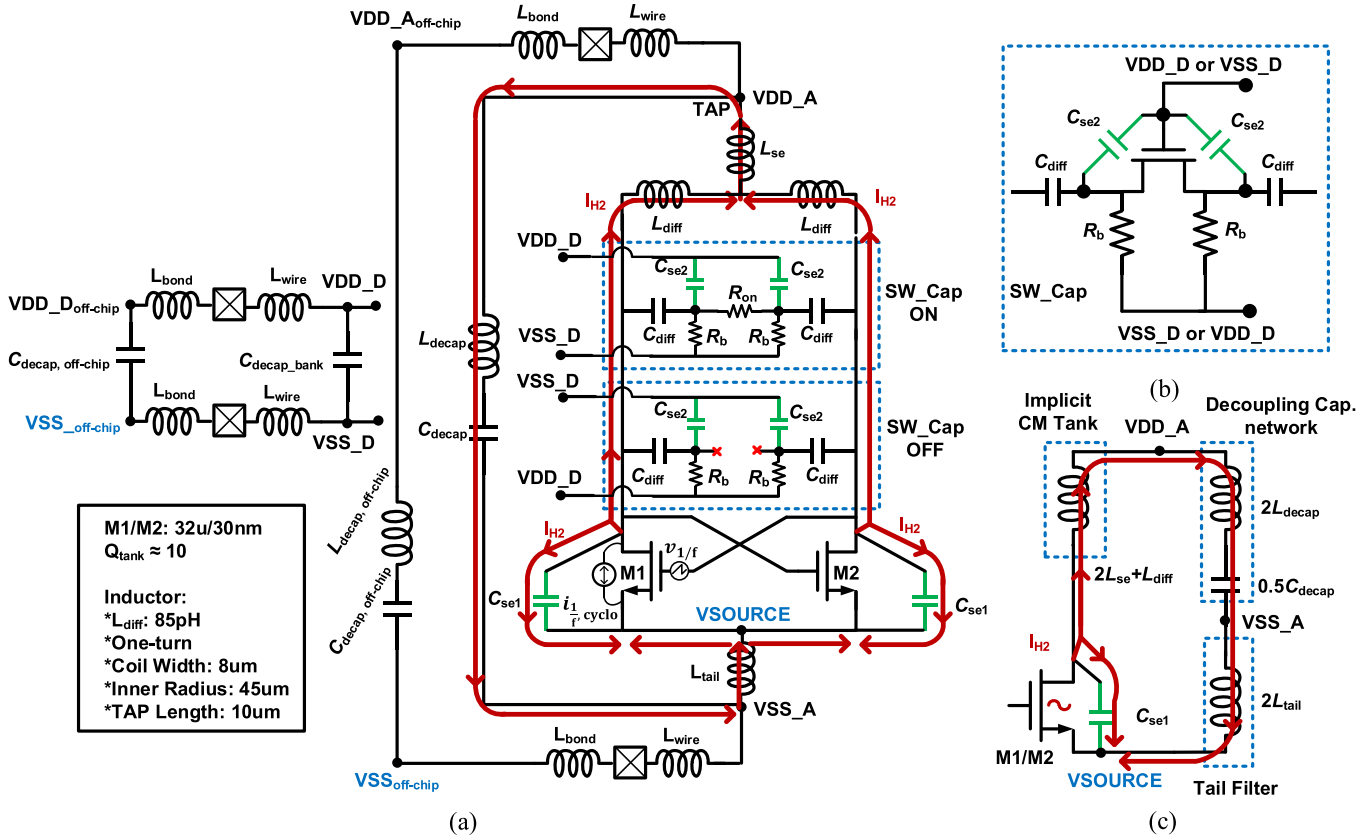


Fig. 6. (a) Model of a conventional 30-GHz oscillator with tail filtering and its CM return path. (b) Conventional sw-cap tuning element. (c) Half-circuit of the CM return path.

As CMOS technology scales, another $1/f$ noise mechanism, called correlated mobility fluctuation (CMF), is becoming increasingly important since the trapped electrons in a short channel will have a larger influence on Coulomb scattering of neighboring free electrons, thus changing the average electron mobility (see Fig. 8). A more accurate $1/f$ noise model for the nanoscale CMOS considering both CNF and CMF was verified in [13], which is described as

$$\overline{I_{1/f}^2} = \overline{V_{1/f}^2} \times (g_m + \Omega I_{\rm D})^2 \tag{1}$$

where $\overline{V_{1/f}^2}(= K/(WL\Delta\omega))$ is the power spectral density (PSD) of flat-band voltage, K and Ω (unit: V^{-1}) are process parameters. The first and second terms in parenthesis represent CNF and CMF, respectively. Thus, the flicker NMF $m(t)$ in nanoscale CMOS could be modified as periodically modulated transconductance and harmonic current

$$m(t) = G_m(t) + \Omega I_{\rm D}(t) \tag{2}$$

where $G_m(t)$ and $I_{\rm D}(t)$ can be obtained by applying the discrete steady-state waveform point of $V_{\rm GS}$, $V_{\rm DS}$ to dc simulations.

Assume the flicker gate-voltage noise $v_{1/f}$ at $\Delta\omega$ (e.g., $2\pi \times 10$ kHz) in M1/2 is expressed as

$$v_{1/f}(t) = \sqrt{2} V_{1/f,\rm rms} \cos(\Delta\omega t + \gamma) \tag{3}$$

where $V_{1/f,\rm rms}$ is rms value of $\overline{V_{1/f}^2}$, and γ is an initial random phase. Thus, the cyclostationary flicker noise current is as follows:

$$\begin{aligned} i_{1/f,\rm cyclo}(t) &= v_{1/f}(t) \times m(t) \\ &= \sqrt{2} I_{1/f,\rm rms}(t) \cos(\Delta\omega t + \gamma) \end{aligned} \tag{4}$$

where $I_{1/f,\rm rms}(t)$ ($\approx V_{1/f,\rm rms} \times m(t)$) is the periodically modulated rms value of flicker current noise. It can be directly simulated by dc/NOISE simulations using the discrete waveform point of $V_{\rm GS}$ and $V_{\rm DS}$ from periodic steady-state (PSS) simulations, while the introduced model $V_{1/f,\rm rms} \times m(t)$ is mainly used to intuitively and physically explain the complex behavior of $I_{1/f,\rm rms}(t)$ in the large-signal operation and advanced CMOS technology.

Further, assume the non-normalized ISF $h_{\rm DS}$ associated with $V_{\rm DS}$ of M1/2 is

$$h_{\rm DS}(t) = \frac{1}{2} h_0 \cos\theta_{\rm h0} + \sum_1^N h_k \cos(k\omega_0 t + \theta_{{\rm h},k}) \tag{5}$$

where $h_{\rm k}$ and $\theta_{{\rm h},k}$ are the magnitude and phase of $k_{\rm th}$ harmonic term, respectively. Note that $\theta_{\rm h0}$ is either 0 or π depending on the sign of dc term $h_{\rm DS}$. Thus, the phase noise is

$$\begin{aligned} \phi(t) &= \int_{-\infty}^{t} h_{\rm DS}(\tau) \cdot i_{1/f,\rm cyclo}(\tau) d\tau \\ &\approx \frac{\sqrt{2} h_{\rm eff,dc}}{\Delta\omega} \sin(\Delta\omega t + \gamma) \end{aligned} \tag{6}$$

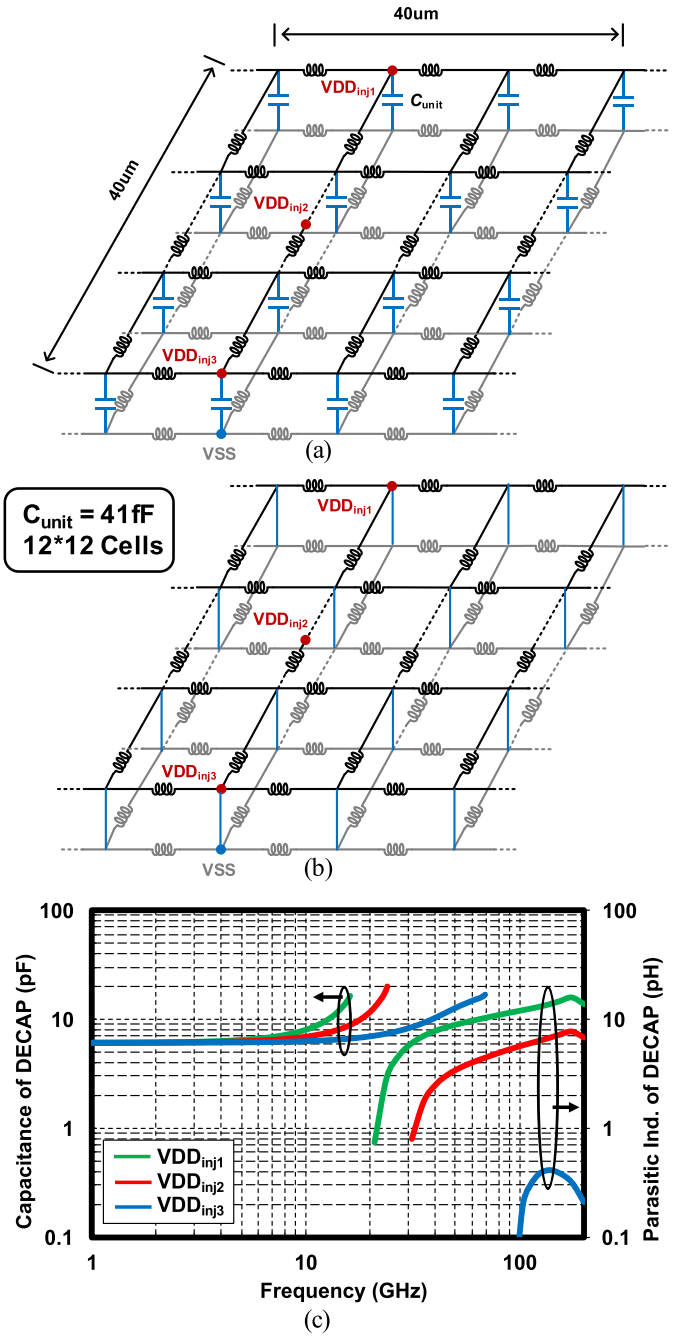


Fig. 7. (a) Decoupling capacitor network for the proposed mmW oscillator. (b) High-frequency model of the decoupling capacitor network. (c) Effective parasitic inductance at different supply injection points.

where $\phi(t)$ is mainly dominated by the slow frequency term, and $h_{\text{eff,dc}}$ is the dc value of non-normalized effective ISF $h_{\text{eff}}(t)$ $(=h_{\text{DS}}(t) \times I_{1/f,\text{rms}}(t))$, which is defined as

$$h_{\text{eff,dc}} = \frac{1}{T}\int_0^T h_{\text{DS}}(t) \cdot I_{1/f,\text{rms}}(t)dt \tag{7}$$

where T $(=(2\pi/\omega_0))$ is the oscillation period.

The phase noise $\phi(t)$ appears at V_{DS} of M1/2, showing two correlated terms at $\omega_0 \pm \Delta\omega$

$$V_{\text{DS}} \approx V_{\text{H1}}\cos(\omega_0 t + \theta + \phi(t)) \approx V_{\text{H1}}\cos(\omega_0 t + \theta)$$

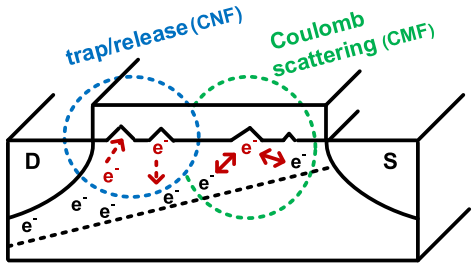


Fig. 8. Newly discovered flicker noise mechanism in nanoscale CMOS [13].

$$+\frac{V_{\text{H1}}\sqrt{2}h_{\text{eff,dc}}}{2\Delta\omega}\cos((\omega_0+\Delta\omega)t+\theta+\gamma)$$
$$-\frac{V_{\text{H1}}\sqrt{2}h_{\text{eff,dc}}}{2\Delta\omega}\cos((\omega_0-\Delta\omega)t+\theta-\gamma) \tag{8}$$

where V_{H1} and θ are the 1st harmonic amplitude and phase of V_{DS}, respectively. Hence, the single-sideband to carrier ratio (SSCR) can be written as

$$\mathcal{L}(\Delta\omega) = \frac{1}{2}\left(\frac{V_{\text{H1}}\sqrt{2}h_{\text{eff,dc}}}{2\Delta\omega}\right)^2 / \frac{1}{2}V_{\text{H1}}^2 = \left(\frac{\sqrt{2}h_{\text{eff,dc}}}{2\Delta\omega}\right)^2 \tag{9}$$

which is the flicker PN at $\omega_0 \pm \Delta\omega$ caused by a single transistor M1 or M2. The final SSCR caused by cross-coupled pair is $2 \times \mathcal{L}$. It is important to address an apparent non-physicality of (9): $h_{\text{eff,dc}}^2$ itself is proportional to $1/\Delta\omega$, since $I_{1/f,\text{rms}}^2(t)$ is proportional to $1/\Delta\omega$. Thus, the $\mathcal{L}(\Delta\omega)$ is ultimately proportional to $1/\Delta\omega^3$.

C. Numerical Verification

To verify the proposed equations (7) and (9), it is necessary to get the periodically modulated rms value of flicker current noise $I_{1/f,\text{rms}}(t)$ and non-normalized ISF $h_{\text{DS}}(t)$. The former is based on the dc/NOISE simulations using the steady-state waveform point of V_{GS} and V_{DS} from PSS simulation. For the latter, it can be acquired by periodic transfer function (PXF) simulations [19], which is more accurate and much faster than the conventional transient simulation method [14].

Following the similar method in [19], we could also derive periodic transimpedance from a small-signal current source across drain–source of M1/2 at $(\omega_0+\Delta\omega)+(k-1)\omega_0$ to the small output voltage of V_{DS} at $(\omega_0+\Delta\omega)$ as

$$|H(k-1)| = \frac{V_{\text{H1}}h_k}{4\Delta\omega} \tag{10}$$
$$\angle H(k-1) = \theta - \theta_{\text{h},k} \tag{11}$$

where $k-1$ is the index of sideband of PXF, $|H(k-1)|$ and $\angle H(k-1)$ are the magnitude and phase of periodic transimpedance, which can be simulated directly by PXF. The magnitude V_{H1} and initial phase θ of 1st harmonic V_{DS} can be simulated by PSS with harmonic balance (HB) engine, which solves for the steady-state of cosines rather than sines. Thus, it is easy to extract non-normalized ISF based on (5), (10), and (11).

Both qualitative and quantitative analysis of the flicker noise upconversion and reduction mechanism of mmW oscillator are demonstrated in Fig. 9. The periodically modulated flicker current noise $I_{1/f,\text{rms}}(t)$ at 10-kHz models the process of

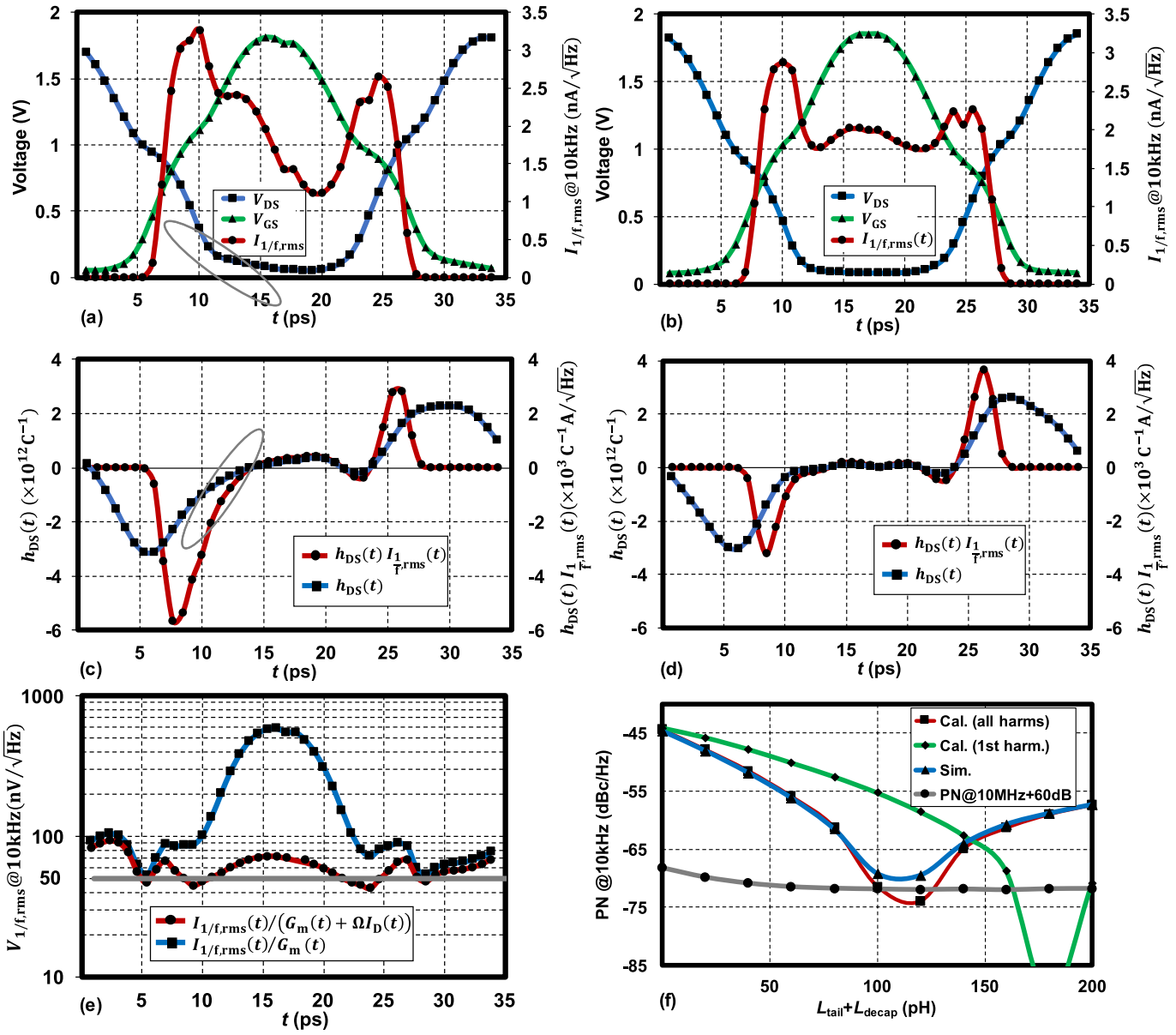


Fig. 9. Discrete waveform point of V_{GS}, V_{DS} in one period based on PSS simulations, and corresponding rms value of flicker current noise $I_{1/f,\mathrm{rms}}$ at 10 kHz based on dc/NOISE simulations: (a) $L_{\mathrm{tail}}+L_{\mathrm{decap}}=0$ pH, (b) $L_{\mathrm{tail}}+L_{\mathrm{decap}}=120$ pH (for 2nd harmonic resonance). Non-normalized ISF function $h_{\mathrm{DS}}(t)$ based on PXF simulations and $h_{\mathrm{DS}}(t)\times I_{1/f,\mathrm{rms}}(t)$: (c) $L_{\mathrm{tail}}+L_{\mathrm{decap}}=0$ pH and (d) $L_{\mathrm{tail}}+L_{\mathrm{decap}}=120$ pH. (e) Flicker noise model verification. (f) Numerical verification of PN at 10 kHz.

flicker noise modulation, as shown in Fig. 9(a) ($L_{\mathrm{tail}}+L_{\mathrm{decap}}=0$ pH) and Fig. 9(b) ($L_{\mathrm{tail}}+L_{\mathrm{decap}}=120$ pH, achieving the 2nd harmonic resonance). The flicker noise peaks in the regions where M1/2 operates in saturation, (i.e., $t\approx$10 and 25 ps), while it also keeps relatively high levels in the triode region (i.e., $t\approx 12$ to 22 ps). Although a complex Berkeley short-channel IGFET model (BSIM) flicker noise model is employed in the process development kit (PDK) of TSMC 28-nm technology, the CNF/CMF model could still be fairly accurate and provide a physical understanding about flicker noise behavior in a large-signal operation.

As a means of verifying the efficacy of the adopted CNF/CMF model in (1), let us contrast it with the currently used CNF-only model by examining the flatness of $V_{1/f,\mathrm{rms}}(t)$ at $\Delta\omega/2\pi=10$ kHz in both cases. A quick inspection of Fig. 9(e) reveals that $I_{1/f,\mathrm{rms}}(t)/(G_m(t)+\Omega I_{\mathrm{D}}(t))$ is fairly constant. Conversely, $I_{1/f,\mathrm{rms}}(t)/G_m(t)$ is far from being constant, which means that the presently used CNF model cannot accurately describe the physical flicker noise modulation process of oscillators in the nanoscale CMOS technology.

The non-normalized ISF $h_{\mathrm{DS}}(t)$ based on PXF ($N=7$) and effective non-normalized ISF $h_{\mathrm{eff}}(t)$ ($=h_{\mathrm{DS}}(t)I_{1/f,\mathrm{rms}}(t)$) are shown in Fig. 9(c) for $L_{\mathrm{tail}}+L_{\mathrm{decap}}=0$ pH, and in Fig. 9(d) for $L_{\mathrm{tail}}+L_{\mathrm{decap}}=120$ pH. From the $h_{\mathrm{eff}}(t)$ waveform, it is obvious that the flicker noise mainly affects the PN during two saturation regions, having an opposing influence on phase change of V_{DS} in each region. When the 2nd harmonic current enters the non-resistive path, it causes asymmetries between

the rising and falling parts of V_{DS}, as shown in Fig. 9(a) (gray cycle), leading to asymmetries of $h_{DS}(t)$ [see Fig. 9(c)]. Note that $h_{DS}(t)$ is approximately proportional to the derivative of $V_{DS}(t)$. Further, as shown in Fig. 9(c), phase change in the falling part of V_{DS} [i.e., negative area of $h_{eff}(t)$, gray circle] is much larger than phase change in the rising part [i.e., positive area of $h_{eff}(t)$], which means $h_{eff,dc} \neq 0$, i.e., a flicker noise upconversion. However, forcing the 2nd harmonic current to enter the resistive path would make the rising and falling parts of V_{DS} more symmetric [shown in Fig. 9(b)], causing the phase change in the two regions to cancel each other within one period [i.e., $h_{eff,dc} = 0$, as shown in Fig. 9(d)]. It is worthwhile to point out that the other flicker noise reduction mechanism, i.e., the introduction of phase shift between V_{DS} and V_{GS} [6], can be also explained by $h_{eff}(t)$, since its positive and negative areas can be adjusted to be equal by the phase shift between $h_{DS}(t)$ (mainly depending on V_{DS}) and $I_{1/f,rms}(t)$ (mainly relying on V_{GS}). An alternative approach would use a transformer to introduce the phase shift between its primary (i.e., V_{DS}) and secondary (i.e., V_{GS}) windings.

The resulting PN at 10-kHz offset shown in Fig. 9(f) shows almost a perfect agreement between the calculations ($N = 7$, red line) based on (7) and (9) with simulations ($N = 10$, blue line), thus demonstrating the effectiveness of proposed theory. Note that merely considering the PN contribution from the 1st harmonic ISF (green line) cannot provide the required match to the simulations, except for the single point where $L_{tail} + L_{decap} = 0$ pH (i.e., Van der Pol oscillator [9]). The thermal PN at 10 kHz (represented by "PN at 10 MHz + 60 dB") can be suppressed as long as the $L_{tail} + L_{decap}$ is large enough, suppressing the "loaded-Q" effect no matter whether the 2nd harmonic resonance happens (gray line) (see [2]).

It is worthwhile to calculate the PN at 10 kHz by replacing the precise simulated value of $I_{1/f,rms}(t)$ with the best-fit CNF/CMF model: 50 nV/$\sqrt{\text{Hz}}$ $\times$ $[G_m(t) + \Omega I_D(t)]$ with $\Omega = 3$ V^{-1}, as calculated during the non-cut-off region (i.e., from 6 to 28 ps) and indicated as the gray line in Fig. 9(e). When $L_{tail} + L_{decap} = 0$ pH, the PN at 10 kHz based on CNF/CMF model is -43.73 dBc/Hz, while the accurate PDK result is -44.35 dBc/Hz [i.e., using $I_{1/f,rms}(t)$]. As mentioned, the CNF/CMF model shows a good accuracy for quantitative analysis and also helps designers to intuitively understand the complex behavior of modulated flicker noise. Of course, the most accurate quantitative analysis is still with the simulated $I_{1/f,rms}(t)$, but the demonstrated accuracy of the flicker PN prediction in (1) is within 1 dB.

In conventional mmW oscillators, the optimum $L_{tail} + L_{decap}$ for the 2nd harmonic resonance is only $\sim$100 pH, since the inductance in the implicit CM tank $L_{diff} + 2L_{se}$ is already dominant. Unfortunately, due to the physical distance between VDD_A and VSS_A in conventional mmW oscillators, the $L_{tail} + L_{decap}$ could hardly be made less than 200 pH, which means mmW designers would have difficulties in forcing the 2nd harmonic current to enter the resistive path to suppress the flicker noise. Therefore, for mmW oscillators, the CM return path should be properly constructed for the accurate harmonic termination.

III. Circuit Description

In [5], a class-F oscillator (first introduced in [16]) with a 3rd harmonic extraction has demonstrated low $1/f^2$ PN at mmW frequencies. However, the $1/f^3$ PN corner still exceeds 1 MHz. In [7], a class-F_{23} oscillator has achieved both low $1/f^2$ PN and low $1/f^3$ PN corner at carrier frequencies below 7 GHz. Unfortunately, direct application of those techniques at mmW frequencies may not deliver the same level of $1/f^3$ performance. In this section, we demonstrate the proposed class-F_{23} oscillator with the 3rd harmonic extraction, which achieves both the best-in-class $1/f^2$ PN and record-low $1/f^3$ PN corner at mmW frequencies. As discussed in Section II, the uncontrolled return path of the 1:2 transformer could shift the desired CM resonance which will lead to the degradation of the $1/f^3$ corner. To solve the above issue, the proposed class-F_{23} oscillator employs a transformer with an explicit CM return path using an embedded decoupling capacitor [12]. The detailed circuit operation of the oscillator as well as details of the transformer with embedded decoupling capacitor and the capacitor bank design will be discussed in the following.

A. Operational Principle of Class-F_{23} Oscillator

Fig. 5 shows the circuit schematic of the proposed class-F_{23} oscillator, while the proposed layout is presented in Fig. 10. The oscillator exploits the 3rd harmonic resonance in the DM tank (class-F_3 operation), and the 2nd harmonic resonance in the CM tank (class-F_2 operation). The former deals with the DM tank, including the primary DM inductance $L_{P,dm}$ ($=L_{P,diff}$), secondary DM inductance $L_{S,dm}$ ($= L_{S,diff}$), DM magnetic coupling factor k_{dm}, primary DM capacitance $C_{P,dm}$ ($= C_P$), and secondary DM capacitance $C_{S,dm}$ ($=C_S$). According to [16], the fundamental frequency ω_0 can be approximately derived as: $\omega_0 = 1/\sqrt{(L_{P,diff}C_P + L_{S,diff}C_S)}$, while the ratio betwen two DM resonance frequencies ω_3/ω_0 is determined by

$$\frac{\omega_3}{\omega_0} = \sqrt{\frac{1 + X + \sqrt{1 + X^2 + X\left(4k_{dm}^2 - 2\right)}}{1 + X - \sqrt{1 + X^2 + X\left(4k_{dm}^2 - 2\right)}}} \tag{12}$$

where $X = (L_{S,diff}C_S)/(L_{P,diff}C_P)$. Thus, for the assumed 1:2 turns-ratio transformer (given $L_{S,diff}/L_{P,diff}$), through tuning of the secondary-to-primary capacitor ratio X_2 ($= C_S/C_P$), the $\omega_3/\omega_0 = 3$ condition can be achieved for the class-F_3 operation. Note that k_{dm} is generally chosen around 0.61 to get a strong 3rd harmonic [5]. Due to the low CM coupling factor k_{cm}, only the primary CM tank is considered [7], which includes the primary CM inductance $L_{P,cm}$ ($= L_{P,diff}+2L_{P,se}$) and the primary CM capacitance $C_{P,cm}$ ($= C_{P,se}$). Thus, the CM resonance frequency ω_2 is $1/\sqrt{((L_{P,diff} + 2L_{P,se})C_{P,se})}$. The ratio between ω_2 and ω_0 is derived as follows:

$$\frac{\omega_2}{\omega_0} = \sqrt{\frac{L_{P,diff}C_P + L_{S,diff}C_S}{(L_{P,diff} + 2L_{P,se})C_{P,se}}} = \sqrt{\frac{L_{P,diff} + L_{S,diff}X_2}{(L_{P,diff} + 2L_{P,se})X_1}} \tag{13}$$

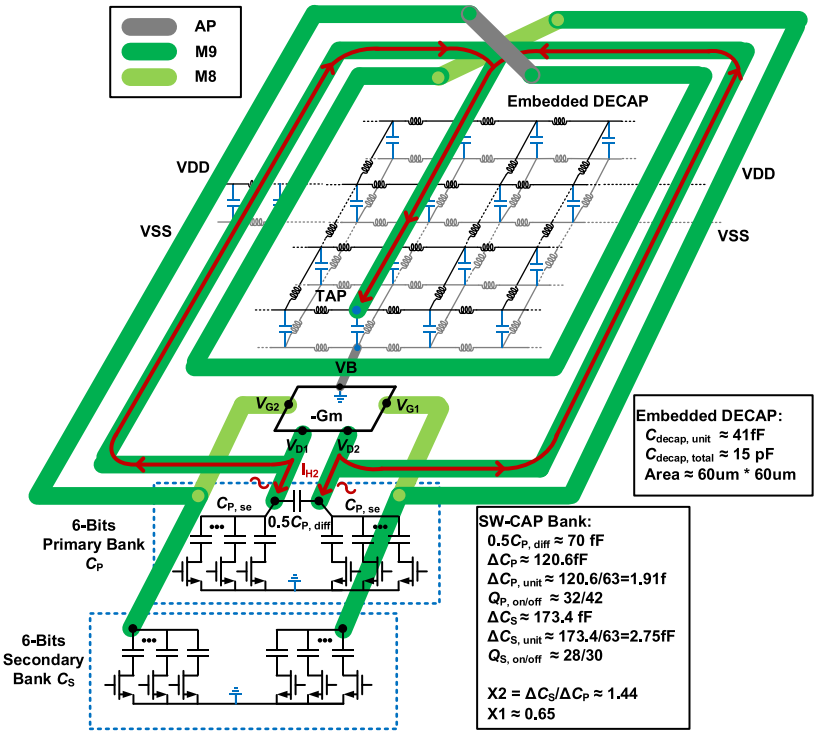


Fig. 10. Proposed layout of class-F_{23} oscillator with embedded decoupling capacitor and the design of sw-cap banks.

where X_1 ($= C_{P,se}/C_P$) is the ratio of CM capacitance in the primary tank. Through tuning of X_1 to the $\omega_2/\omega_0 = 2$ condition, the class-F_2 operation can be achieved. Thus, the secondary-to-primary capacitor ratio (X_2) helps in achieving the class-F_3 operation, forcing the 3rd harmonic current to enter the resistive path, thus boosting the 3rd harmonic voltage. On the other hand, the primary CM capacitance ratio (X_1) enables the class-F_2 operation, forcing the 2nd harmonic current to enter the resisitive path, thus maintaining the symmetry between the rising and falling parts of output waveform, ultimately helping to reduce the flicker noise upconversion.

B. Proposed Transformer With Embedded Decoupling Capacitor for Explicit CM Return Path

To explicitly define the CM return path, the proposed 1:2 transformer with the embedded decoupling capacitor is shown in Fig. 10. By bringing as close as practically possible the tap of primary coil to the source node of MOS transistors, the shortest return path for the CM current can be secured. According to the study shown in Fig. 7, the parasitic inductance of the embedded decoupling capacitor network can be safely neglected, thus allowing for the CM inductance L_{cm} to be modeled accurately. Size of the 1:2 transformer is optimized for the intended operating frequency to achieve high Q-factor but without too much coupling to the substrate. In this paper, the self-resonant frequency (where DM coupling factor k_{dm} reaches 0) is about 5× of the operating frequency. Thus, the outer diameter of transformer is chosen to 220 μm (see Fig. 11), with the self-resonance at ∼50 GHz. The coil width is set at 10 μm with consideration of skin effect, while the coil space is 7 μm to make k_{dm} about 0.63. It is well recognized

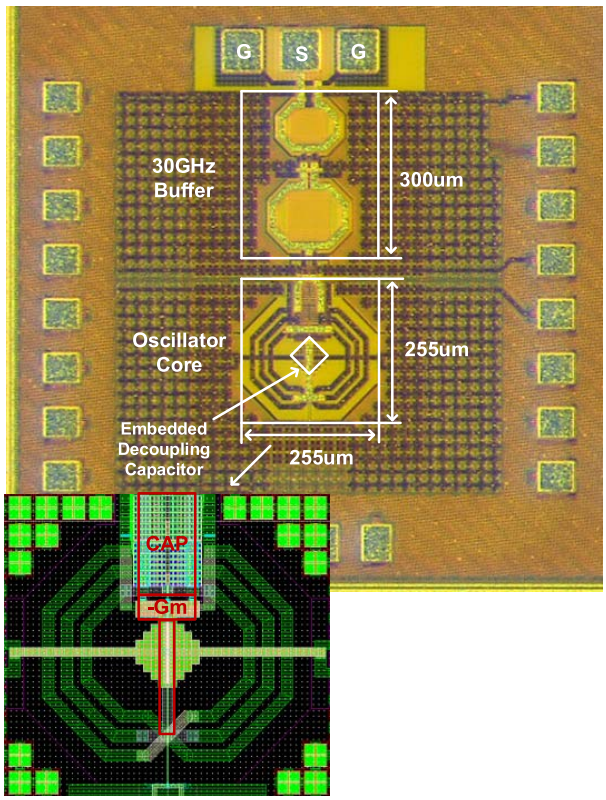


Fig. 11. Chip micrograph and zoomed-in view layout area of the embedded decoupling capacitor network.

that placing the embedded decoupling capacitor inside the coil may degrade the Q-factor. From the electromagnetic (EM) simulation, if the decoupling capacitor area is less than 25% of the coil's internal area, the degradation would be about 1 and

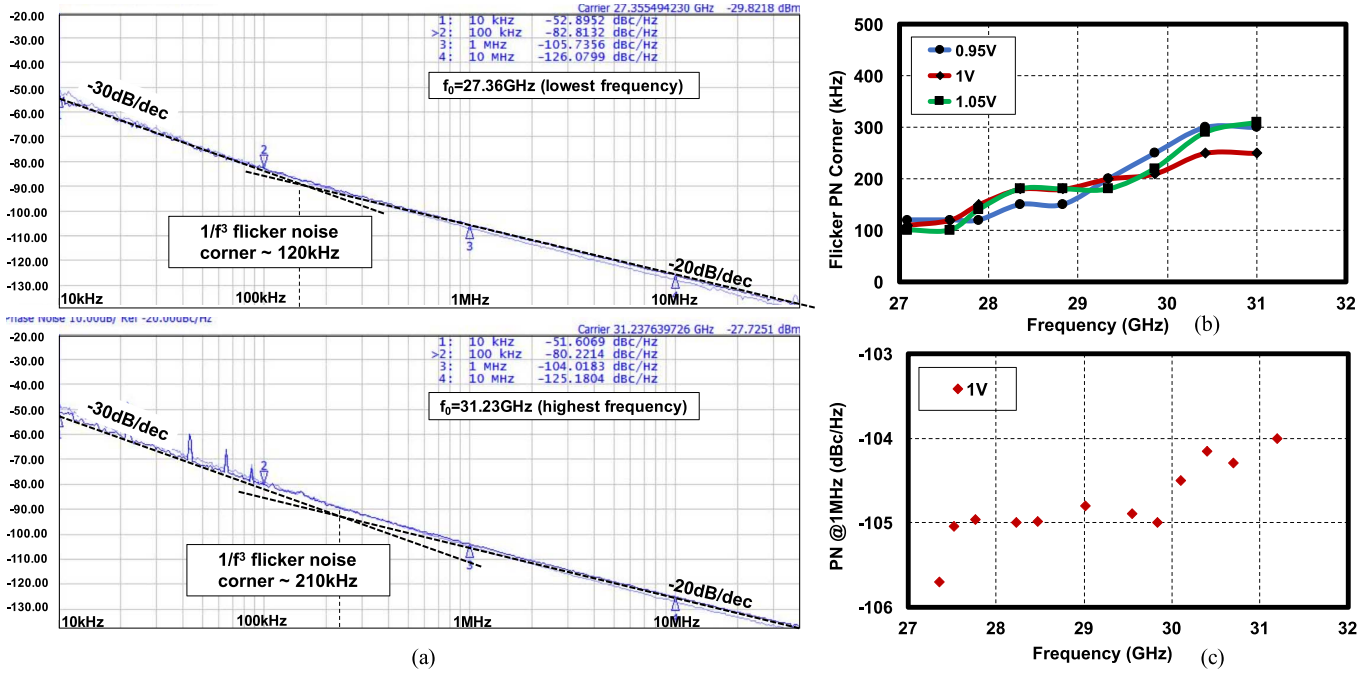


Fig. 12. (a) Measured PN plots at 27.36 and 31.23 GHz. (b) Measured flicker PN corner over tuning range (c) Measured PN @1-MHz over tuning range

without affecting the inductance and coupling factor. On the other hand, the embedded decoupling capacitor should still be large enough to provide the short path for the CM current, which is 15 pF in this case. According to simulations using the circuit model in Fig. 5, X_2 is about 1.44 to get the 3rd harmonic resonance. It means

$$\frac{C_{\mathrm{S,min}}}{C_{\mathrm{P,min}}} = \frac{C_{\mathrm{S,max}}}{C_{\mathrm{P,max}}} = \frac{\Delta C_{\mathrm{S}}}{\Delta C_{\mathrm{P}}} = X_2. \tag{14}$$

Two 6-bit single-ended capacitor banks $C_{\mathrm{P,se}}$ and $C_{\mathrm{S,se}}$ are designed for the primary and secondary banks (shown in Fig. 10), in which $\Delta C_{\mathrm{P}} = 120.6$ fF and $\Delta C_{\mathrm{S}} = 173.4$ fF. The quality factor of the capacitor banks is about 30 at 10 GHz, thus facilitating the overall high Q-factor of the tank. A fixed differential capacitor of $0.5C_{\mathrm{P,diff}}$ (=70 fF) is put in the primary tank, to enable the 2nd harmonic resonance when the sw-cap control word is in the middle (=32 for the 6-bit code), which makes X_1 about 0.65. For a more accurate control of the CM resonance, the fixed differential capacitor can be replaced with several bits of the differential capacitor bank [8].

C. Third-Harmonic Extraction—Two-Stage 30-GHz PA

As shown in Fig. 5, a two-stage 30-GHz PA is used to boost the 3rd harmonic signal and to suppress the fundamental and 2nd harmonics [5], [20]. The passive ac-coupling circuit (R_{ac} and C_{ac}) is inserted between the oscillator and PA. C_{ac} is chosen $\sim$10$\times$ of the input capacitance of 1st stage PA, and R_{ac} (=50 kΩ) is chosen large enough to make the corner frequency much lower than the oscillator output frequency to ensure low coupling losses. Two 1:1 transformers (T2 and T3) vertically stack two one-turn inductors (M9 for the primary coil, and AP for the secondary coil). They are used for coupling between the 1st and 2nd stages, and also to the ground–signal–ground (GSG) PAD (see Fig. 11). To decrease the insertion loss in each transformer for the given frequency (i.e., 30 GHz), the diameter of the transformer's coils is optimized for high Q-factor. With the help from EM simulations, the diameters of T2 and T3 are chosen around 120 μm. Two tuning capacitors ($C_{\mathrm{tune1}} = 20$ fF and $C_{\mathrm{tune2}} = 60$ fF) are used to make the resonant frequency of the 1st and 2nd tank stages equal and around 30 GHz in order to boost the 3rd harmonic oscillator output and to suppress its fundamental. On the other hand, R_{b} is used to further suppress the 2nd harmonic within the PA. The C_{n1} (=8 fF) and C_{n2} (=16 fF) are the neutralization capacitors to cancel the Miller effect at the input stage, improving the PA's stability.

IV. Experimental Results

The prototype of the proposed 30-GHz frequency generation stage comprising the 10-GHz class-F_{23} oscillator and the two-stage 30-GHz PA is fabricated in TSMC 28-nm low power CMOS. The chip micrograph is shown in Fig. 11 and it occupies a core area of 0.15 mm^2. While the power supply line is fed into the embedded decoupling on the left- and right-hand sides, the CM inductance is fed directly right near the source of cross-coupled pair as shown in the zoomed-in layout of the proposed transformer. Thus, the CM return path is well defined.

To verify the proposed technique, PN is evaluated using an Agilent E5052B signal source analyzer (SSA) and a 11970A harmonic mixer. The measured tuning range (TR) is from 27.3 to 31.2 GHz (14%) and Fig. 12(a) shows the measured PN at 27.3 and 31.2 GHz. At the 27.3-GHz carrier, drawing 12 mW from 1-V supply of the main oscillator, it achieves -82.8 and -126 dBc/Hz at 100 kHz and 10 MHz offsets, respectively. The supply pushing is only 37 MHz/V which is in line with recently published best-in-class reports. Fig. 12(b)

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART RF AND mmW OSCILLATORS

		JSSC'17 [8]	JSSC'13 [6]	JSSC'16 [7]	JSSC'13 [16]	ESSCIRC'15 [17]	ESSCIRC'15 [15]	JSSC'16 [5]	A-SSCC'15 [10]	**This Work**	
Feature		Implicit Resonan.	Drain Resistances	Implicit Resonan.	Class-F	Class-B	Tail Resonance	Class-F	Tail Resonance	Implicit Resonance in Class F_{23} and Explicit Common-Mode Return Path	
Technology (nm)		28	65	40	65	28	65	65	28	**28**	
V_{DD} (V)		0.9	1.2	1.0	1.25	0.9	1.0	0.7/1.0	0.9	**1.0**	
Tuning Range (%)		27	18	25	25	32	10	25	17	14	
Core Area (mm^2)		0.19	0.08	0.13	0.13	0.13	0.2	0.13	N/A	0.15	
Freq. (GHz)		3.3	3.3	7	7.4	12.7	27.5	57.8	23.5	27.3	31.2
Power (mW)		6.8	0.72	10	15	8.3	23*	24*	7.2	12/22*	13/23*
Phase Noise (dBc/Hz)	100k	-106	-94	-102	-98	-80	-72	-72	-74	-83	-80
	1M	-130	-114	-124	-125	-107	-100	-100	-102	-106	-104
	10M	-150	-134	-144	-147	-132	-126	-122	-127	-126	-125
FoM** (dBc/Hz)	100k	-188	-186	-189	-184	-172	-167*	-173*	-172	**-181/-178***	**-179/-177***
	1M	-192	-186	-191	-191	-179	-177*	-181.5*	-180	-184/-181*	-183/-180*
	10M	-192	-186	-191	-193	-184	-181*	-183.7*	-186	-184/-181*	-184/-181*
$1/f^3$ Corner (kHz)		200	20	130	700	4000	1200	1000	3000	**120**	**210**
Freq. Pushing (MHz/V)		N/A	15@1.2V	23@1V	50@1.25V	N/A	N/A	N/A	N/A	37@1V	

*Including power consumption from frequency multiplier/first-stage buffer, **FoM = PN -20log(f_{osc}/f_{offset})+10log(P_{DC}/1mW)

shows measured flicker noise corner across the TR and at three supply levels: 0.95, 1, and 1.05 V. It increases almost monotonically from 100 to 300 kHz across the TR and is quite stable over voltage changes. The measured PN at 1-MHz offset is shown in Fig. 12(c). Table I compares this paper with other flicker-noise-aware designs (albeit at single gigahertz) as well as mmW CMOS oscillators. The techniques using tail filtering improve PN performance in the far-out $1/f^2$ region [10], [15], but fail to maintain the same PN FoM at 1-MHz offset which can deteriorate the system data rate. The 3rd harmonic peak-to-peak output swing of the 1st stage buffer in the proposed circuit is ∼2 V, consuming ∼10 mW. Additional stage of buffers can help further suppress the fundamental harmonic, and deliver enough power to the load [5]. The proposed oscillator achieves 120 and 220 kHz flicker noise corners at 27.3- and 31.2-GHz carriers, respectively, which confirms validity of the proposed approach. This is the lowest $1/f^3$ corner reached among the >10-GHz oscillators, which usually report >1 MHz, and comparable to those oscillators with flicker-noise-aware designs but at much lower frequencies [7], [8]. To the best of authors' knowledge, the proposed oscillator achieves the best PN FoM at 100-kHz offset while maintaining competitive FoM at 1 MHz across its TR when compared with >10-GHz oscillators.

V. CONCLUSION

A 30-GHz frequency generation stage using a 3rd harmonic extraction and a 2nd/3rd harmonic tuning is proposed. A new 2nd harmonic resonance technique with careful consideration and control of parasitics in the CM current return path results in state-of-the-art performance with an order-of-magnitude reduction in flicker noise among >10-GHz oscillators. The proposed simulation method of periodically modulated rms value of flicker current noise $I_{1/f,\mathrm{rms}}(t)$ and effective non-normalized ISF for flicker noise $h_{\mathrm{eff}}(t)$ [$= h_{\mathrm{DS}}(t) \times I_{1/f,\mathrm{rms}}(t)$] are instrumental in the first-ever numerical verification of flicker noise reduction mechanism using 2nd harmonic resonance. This further provides a powerful tool to quantitatively study other low-flicker noise oscillator topologies.

ACKNOWLEDGMENT

The authors would like to thank Microelectronic Circuits Centre Ireland for technical support, Integrand Software for EMX license and TSMC for chip fabrication. They also would like to thank Prof. Andrea Bonfanti, Dr. Federico Pepe, Dr. Hsieh-Hung Hsieh and Zhirui Zong for their fruitful discussions, and Paulo Vieira for his lab assistance.

REFERENCES

[1] B. Sadhu, M. Ferriss, and A. Valdes-Garcia, "A 52 GHz frequency synthesizer featuring a 2nd harmonic extraction technique that preserves VCO performance," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1214–1223, May 2015.

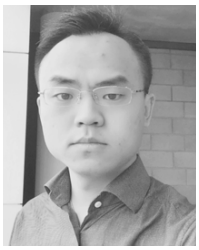
[2] L. Iotti, A. Mazzanti, and F. Svelto, "Insights into phase-noise scaling in switch-coupled multi-core LC VCOs for E-band adaptive modulation links," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1703–1718, Jul. 2017.

[3] T. Siriburanon *et al.*, "A low-power low-noise mm-Wave subsampling PLL using dual-step-mixing ILFD and tail-coupling quadrature injection-locked oscillator for IEEE 802.11ad," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1246–1260, May 2016.

[4] C.-H. Tsai, G. Mangraviti, Q. Shi, K. Khalaf, A. Bourdoux, and P. Wambacq, "A 54–64.8 GHz subharmonically injection-locked frequency synthesizer with transmitter EVM between −26.5 dB and −28.8 dB in 28 nm CMOS," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2017, pp. 243–246.

[5] Z. Zong, M. Babaie, and R. B. Staszewski, "A 60 GHz frequency generator based on a 20 GHz oscillator and an implicit multiplier," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1261–1273, May 2016.

[6] F. Pepe, A. Bondanti, S. Levantino, C. Samori, and A. L. Lacaita, "Suppression of flicker noise up-conversion in a 65-nm CMOS VCO in the 3.0-to-3.6 GHz band," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2375–2389, Oct. 2013.
[7] M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "A 1/f noise upconversion reduction technique for voltage-biased RF CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2610–2624, Nov. 2016.
[8] D. Murphy, H. Darabi, and H. Wu, "Implicit common-mode resonance in LC oscillators," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 812–821, Mar. 2017.
[9] A. Bonfanti, F. Pepe, C. Samori, and A. L. Lacaita, "Flicker noise upconversion due to harmonic distortion in Van der Pol CMOS oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 7, pp. 1418–1430, Jul. 2012.
[10] Q. Shi, D. Guermandi, J. Craninckx, and P. Wambacq, "Flicker noise upconversion mechanisms in K-band CMOS VCOs," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2015, pp. 1–4.
[11] M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "Tuning range extension of a transformer-based oscillator through common-mode Colpitts resonance," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 4, pp. 836–846, Apr. 2017.
[12] Y. Hu, T. Siriburanon, and R. B. Staszewski, "A 30-GHz class-F_{23} oscillator in 28 nm CMOS using harmonic extraction and achieving 120 kHz $1/f^3$ corner," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2017, pp. 87–90.
[13] E. Ioannidis, C. Theodorou, T. Karatsori, S. Haendler, C. Dimitriadis, and G. Ghibaudo, "Drain-current flicker noise modeling in nMOSFETs from a 14-nm FDSOI technology," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1574–1579, May 2015.
[14] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1999.
[15] T. Siriburanon *et al.*, "A 28-GHz fractional-N frequency synthesizer with reference and frequency doublers for 5G cellular," in *Proc. IEEE 41st Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 76–79.
[16] M. Babaie and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.
[17] B. Hershberg, K. Raczkowski, K. Vaesen, and J. Craninckx, "A 9.1–12.7 GHz VCO in 28 nm CMOS with a bottom-pinning bias technique for digital varactor stress reduction," in *Proc. IEEE 40th Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 83–86.
[18] A. Bevilacqua and P. Andreani, "An analysis of 1/f noise to phase noise conversion in CMOS harmonic oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 5, pp. 938–945, May 2012.
[19] F. Pepe, A. Bonfanti, S. Levantino, P. Maffezzoni, C. Samori, and A. L. Lacaita, "An efficient linear-time variant simulation technique of oscillator phase sensitivity function," in *Proc. SMACD*, Sep. 2012, pp. 17–20.
[20] W.-L. Chan and J. R. Long, "A 58–65 GHz neutralized CMOS power amplifier with PAE above 10% at 1-V supply," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 554–564, Mar. 2010.



Yizhe Hu (S'17) was born in Chenzhou, Hunan, China. He received the B.Sc. degree (*summa cum laude*) in electronic engineering from the Harbin Institute of Technology, Harbin, China, in 2013. He is currently pursuing the Ph.D. degree in microelectronics from University College Dublin, Dublin, Ireland.

From 2013 to 2014, he was with Fudan University, Shanghai, China, where he was involved in the RFIC design. Since 2016, he has been consulting for the PLL Group of HiSilicon, Huawei Technologies, Co., Ltd., Shenzhen, China, where he was involved in designing 16 nm DCOs and ADPLLs. His current research interests include RF/millimeter-wave-integrated circuits and systems for wireless communications.

Mr. Hu serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I/II, and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION.

Teerachot Siriburanon (S'10–M'16) was born in Paknam, Samut Prakan, Thailand. He received the B.E. degree in telecommunications engineering from the Sirindhorn International Institute of Technology, Thammasat University, Pathumthani, Thailand, in 2010, and the M.E. and Ph.D. degrees in physical electronics from the Tokyo Institute of Technology, Tokyo, Japan, in 2012 and 2016, respectively.

In 2016, he joined University College Dublin, Dublin, Ireland, as a Post-Doctoral Researcher, where he is currently under Marie Skłodowska-Curie Individual Fellowship Program. His current research interests include CMOS wireless transceiver systems and clock/frequency generations for wireless and wireline communications.

Dr. Siriburanon was a recipient of the Japanese Government (MEXT) Scholarship from 2010 to 2015, the Young Researcher Best Presentation Award at Thailand–Japan Microwave in 2013, the ASP-DAC Best Design Award in 2014 and 2015, the IEEE SSCS Student Travel Grant Award in 2014, the IEEE SSCS Predoctoral Achievement Award in 2016, and the Tejima Research Award in 2016. He serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and on the Editorial Review Board of the IEEE SOLID-STATE CIRCUITS LETTERS.

Robert Bogdan Staszewski (M'97–SM'05–F'09) was born in Bialystok, Poland. He received the B.Sc. (*summa cum laude*), M.Sc., and Ph.D. degrees in electrical engineering from the University of Texas at Dallas, Richardson, TX, USA, in 1991, 1992, and 2002, respectively.

From 1991 to 1995, he was with Alcatel Network Systems, Richardson, TX, USA, where he was involved in SONET cross-connect systems for fiber optics communications. In 1995, he joined Texas Instruments Incorporated, Dallas, TX, USA, where he was elected as a Distinguished Member of Technical Staff (limited to 2% of technical staff). From 1995 to 1999, he was involved in advanced CMOS read channel development for hard disk drives. In 1999, he co-started the Digital RF Processor (DRP) Group within Texas Instruments Incorporated with a mission to invent new digitally intensive approaches to traditional RF functions for integrated radios in deeply scaled CMOS technology. From 2007 to 2009, he was a Chief Technology Officer with the DRP Group. In 2009, he joined the Delft University of Technology, Delft, The Netherlands, where he currently holds a guest appointment of a Full Professor (*Antoni van Leeuwenhoek Hoogleraar*). Since 2014, he has been a Full Professor with the University College Dublin, Dublin, Ireland. He has authored or co-authored four books, five book chapters, 220 journal, and conference publications, and holds 170 issued U.S. patents. His current research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters, and receivers.

Dr. Staszewski was a recipient of the 2012 IEEE Circuits and Systems Industrial Pioneer Award. He was the Chair of the Technical Program Committee (TPC) of the IEEE Dallas Circuits and Systems Workshop from 2005 to 2008. He was a TPC Member of the IEEE International Solid-State Circuits Conference from 2008 to 2012, the IEEE Radio frequency Integrated Circuits Symposium from 2010 to 2014, and the IEEE International Symposium on Radio Frequency Integration Technology from 2009 to 2014. He has been a TPC Member of the IEEE International Symposium on Circuits and Systems since 2010 and the IEEE European Solid-State Circuits Conference (ESSCIRC) since 2013. He is an upcoming TPC Chair of 2019 ESSCIRC in Krakow, Poland.