

An FDD Wireless Diversity Receiver With Transmitter Leakage Cancellation in Transmit and Receive Bands

Daniele Montanari¹, *Student Member, IEEE*, Gerardo Castellano, Ehsan Kargaran, Giacomo Pini², *Student Member, IEEE*, Saheed Tijani, Davide De Caro, *Senior Member, IEEE*, Antonio Giuseppe Maria Strollo, *Senior Member, IEEE*, Danilo Manstretta³, *Member, IEEE*, and Rinaldo Castello, *Fellow, IEEE*

Abstract—Antenna-coupling group delay limits the cancellation bandwidth of conventional self-interference cancellers (SICs), making it difficult to ensure isolation in both transmit (TX) and receive (RX) bands. Isolation over both bands is achieved in the dual-path receiver architecture proposed in this paper. The main path consists of a highly linear current-mode RX with a passive RF SIC. The auxiliary path implements a notch in the TX band followed by an adaptive digital equalizer whose output is used to suppress the TX noise leakage in the RX band. The main and auxiliary receiver prototypes, implemented in 28-nm CMOS technology, operate between 1 and 2 GHz, occupy an area of 0.51 and 0.12 mm², and have a power dissipation of 32–40 and 26–64 mW, respectively. The stand-alone RX has a noise figure (NF) of 4–5 dB and an out-of-band IIP3 of 18 dBm. Turning on the passive canceller results in an effective IIP3 of 25–29 dBm and a degradation of the NF of less than 0.8 dB. Thanks to its high dynamic range, the auxiliary path suppresses the TX noise by >29 dB while degrading the RX NF by only 1 dB at 23-dBm TX output power.

Index Terms—Frequency-division duplexing (FDD), full duplex (FD), receiver (RX), self-interference (SI), SI cancellation (SIC), surface acoustic wave (SAW)-less, transmitter (TX) leakage, wideband.

I. INTRODUCTION

IN RECENT years, self-interference cancellation (SIC) techniques have emerged as the primary means to deal with the challenges of wideband transceivers, where little or no RF filtering is available. This applies especially to systems involving simultaneous transmission and reception, such as frequency-division duplexing (FDD) and full duplex (FD) [1]–[3]. In commercial FDD systems, to connect transmitter (TX) and receiver (RX) to the main antenna

with low loss, while ensuring high isolation between them, passive external surface acoustic wave (SAW)-based duplexers are almost always used. Most mobile terminals are also equipped with a diversity antenna and use SAW filters in front of the diversity antenna receiver to attenuate blockers and TX leakage. In fact, given the limited antenna isolation (in the order 20–30 dB [14]), diversity receiver linearity and reciprocal mixing with the receiver local oscillator phase noise are major issues [15]–[21]. TX leakage cancellation techniques, where a vector modulator connected to the transmitter or an auxiliary transmitter [22]–[26] injects a replica TX signal at the receiver input, have been proposed to relax the receiver requirements. The frequency separation between TX and RX can be exploited to improve the linearity of the receiver through filtering, e.g., embedding N-path filters in the receiver front-end [27]–[35], [57]. However, a major source of sensitivity degradation is the noise generated by the TX in the receive band that leaks to the RX. This is even more true if external duplexers are replaced with passive on-chip solutions such as the hybrid transformer [10]–[13], which isolate the receiver from the transmitter through electrical balancing and therefore provide little TX out-of-band (OOB) emission filtering. Since the frequency separation between transmit and receive bands can be as high as 400 MHz, ensuring high isolation between TX and diversity RX (ISO_{TX-RX}) in both bands using SIC is a major challenge [13], [36]–[38]. Techniques such as quantization noise shaping in digital transmitters [39]–[41] and analog filtering using sharp N-path filters [48] can be introduced to lower the TX receive-band noise. Nonetheless, as will be shown in the remainder of this paper, several design issues have to be addressed in order to approach the performance of an SAW-based diversity receiver for demanding standards such as LTE [42]. In this paper, a highly linear diversity receiver for dual-antennas FDD systems with transmitter leakage cancellation in both TX and RX bands is proposed.

This paper is divided as follows. Section II reports the LTE system specifications. The diversity and the auxiliary path designs are described in Sections III and IV, respectively. Section V describes the digital noise reduction (DNR). The measurement results of the complete system are reported in Section VI.

Manuscript received December 9, 2017; revised February 15, 2018; accepted March 19, 2018. Date of publication April 19, 2018; date of current version June 25, 2018. This paper was approved by Guest Editor Andrea Bevilacqua. This work was supported by the Italian PRIN Project “Advanced Nanometer IC Technologies for Next Generation Transceivers” under Grant 2015ABZ44K. (Corresponding author: Daniele Montanari.)

D. Montanari, E. Kargaran, G. Pini, S. Tijani, D. Manstretta, and R. Castello are with the Department of Electrical, Computer, and Biomedical Engineering, University of Pavia, 27100 Pavia, Italy (e-mail: daniele.montanari01@universitadipavia.it).

G. Castellano, D. De Caro, and A. G. M. Strollo are with the Department of Electrical Engineering and Information Technology, University of Naples “Federico II,” 80125 Naples, Italy.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2018.2821139

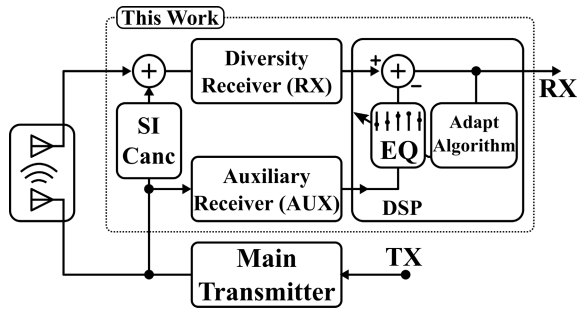


Fig. 1. Proposed system architecture.

II. SYSTEM SPECIFICATIONS

A. System Architecture

Fig. 1 shows the complete system block diagram of the proposed FDD RX. The diversity RX is connected directly to the diversity antenna and receives a strong TX leakage. The RF SIC block taps the TX output signal and injects it at the LNA input to reduce the TX leakage signal power, and hence non-linear and reciprocal mixing effects of the RX. Antenna-antenna coupling has a typical delay of 2–3 ns [14], which limits SIC bandwidth. Since SIC is optimized for the TX band, it is not effective in cancelling the receive-band TX noise. The auxiliary (AUX) receiver senses the receive-band TX noise and feeds the DNR block, which suppresses it in the digital domain. The diversity RX with RF SIC has been presented in [46], while the AUX has been presented in [47]. Here, we present additional circuit design details and experimental results of the two receivers, together with the design of the digital equalization block and the overall system performance.

B. System and Building Blocks Requirements

For a 20-MHz LTE channel, the required sensitivity is -94 to -90.5 dBm, which corresponds to a maximum noise figure (NF) of 8–11.5 dB. In practice, state-of-the-art LTE transceivers have lower NF but gain compression, reciprocal mixing, and receive-band TX noise leakage can degrade the NF. Receiver phase noise requirements are dictated by reciprocal mixing with the largest OOB blocker of -15 dBm. To avoid performance degradation, SIC must lower the TX leakage below -15 dBm. Considering a maximum TX power of 23 dBm and 25 dB of ISO_{TX-RX} , a minimum RF cancellation of 13 dB is required. The requirements of the AUX will be derived in Section II-C. For inter-modulation tests, the minimum desired signal level is 9 dB above sensitivity. The most stringent IIP3 requirements are set by the inter-modulation between OOB blocker and the TX leakage and depend on the relative frequencies of the blocker with respect to the TX and RX ones. Fig. 2 reports the required IIP3 as a function of TX–RX isolation for two cases: 1) when the blocker appears at a frequency offset from the desired signal equal to $|1/2f_{TX}-f_{RX}|$ (IIP3_{HFS}) and 2) when the blocker is at $|2f_{TX}-f_{RX}|$ frequency offset (IIP3_{FFS}). Notice that, when SIC is used, the values reported in Fig. 2 correspond to the effective IIP3, i.e., the IIP3 of a receiver without SIC that gives the same third-order distortion (IM3). The required RX IIP3 is more relaxed and can be inferred from the same plot

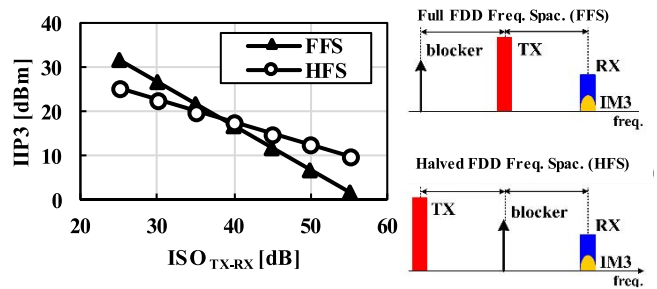


Fig. 2. IIP3 requirements versus TX–RX isolation for different frequency spacing: HFS and FFS.

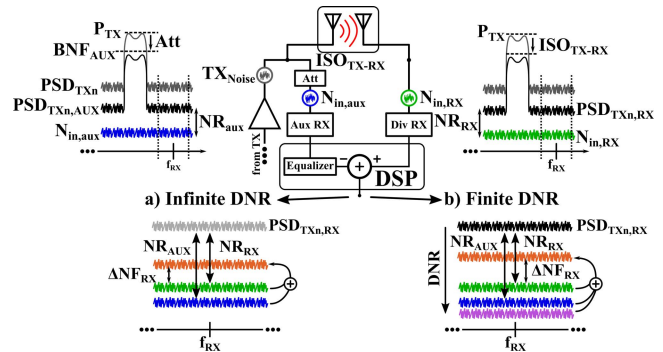


Fig. 3. Simplified block diagram showing the noise levels in different points of the system considering (a) infinite DNR and (b) finite DNR.

when the cancellation in dB is added to the ISO_{TX-RX} on the x -axis.

C. TX Noise in the RX Band

Fig. 3 shows a simplified block diagram of the receiver with TX noise reduction where the noise levels in different points of the system are indicated. The TX output is composed of a modulated signal with power P_{TX} [dBm] and a white noise with power spectral density (PSD) normalized to the TX power PSD_{TXn} [dBc/Hz]. Due to the limited ISO_{TX-RX} , part of the TX output is coupled to the diversity RX, degrading its sensitivity. We define the ratio between the TX noise leakage and the RX own input referred noise as the RX noise ratio (NR_{RX}). The RX NF (NF_{RX}) increases by $10 \log(1 + NR_{RX})$ due to TX noise leakage. Fig. 4 reports NF_{RX} degradation (ΔNF_{RX} [dB]) as a function of P_{TX} assuming $ISO_{TX-RX} = 25$ dB, $PSD_{TXn} = -154$ dBc/Hz and a NF_{RX} of 5.5 dB when no TX is present. ΔNF_{RX} is not negligible when P_{TX} exceeds 5 dBm and it reaches 12 dB with the TX at full power ($P_{TX} = 23$ dBm).

Sensitivity degradation can be strongly reduced by sensing the TX noise through the AUX and subtracting it out from the RX signal. Digital equalization is necessary in order to maximize the correlation between the AUX and RX signals, therefore minimizing the difference (error) signal. While the noise sources of AUX and RX are uncorrelated, the TX noise in the RX band appears at the output of the two paths as a correlated component and it is strongly suppressed. We define the amount of suppression as DNR. Finite correlation between the TX noise at the AUX and RX outputs limits the final

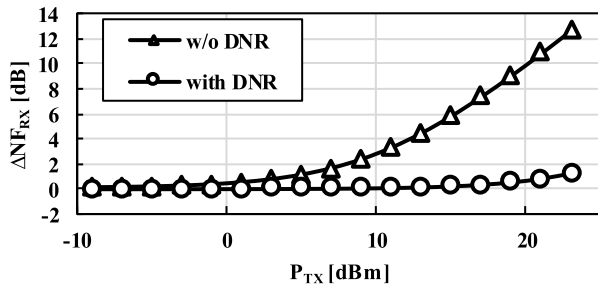


Fig. 4. ΔNF_{RX} versus TX power level for $PSD_{TXn} = -154$ dBc/Hz without DNR and with 28 dB of DNR.

DNR value, as will be explained in Section V. For this reason, the residual TX noise after the digital equalization process contributes to the final ΔNF_{RX} too [Fig. 3(b)]. Even assuming an infinite DNR, the NF_{RX} is still degraded due to the noise added by the AUX. To quantify this additional noise contribution, we can observe that the equalizer has to match the TX noise level at the output of AUX with the one at the output of RX to minimize ΔNF_{RX} . Hence, after equalization, the TX noise levels at the output of the two paths are both equal to PSD_{TXn} when referred to the RX input [$PSD_{TXn,RX}$ in Fig. 3(a)]. If we define the ratio between the TX noise at the AUX input and the AUX own input-referred noise as the AUX noise ratio [NR_{AUX} in Fig. 3(b)], ΔNF_{RX} depends only on the ratio between NR_{RX} and NR_{AUX} . For example, if NR_{AUX} and NR_{RX} were equal, ΔNF_{RX} would be 3 dB. In summary, the total ΔNF_{RX} can be computed as

$$\Delta NF_{RX} = 10 \log \left(1 + \frac{NR_{RX}}{NR_{AUX}} + \frac{NR_{RX}}{DNR} \right). \quad (1)$$

Since NR_{RX} is a given, DNR and NR_{AUX} should be maximized. To ensure less than 0.1 dB of ΔNF_{RX} due to the residual TX noise, more than 28 dB of DNR is required. To maximize NR_{AUX} and avoid compression in the AUX, a broadband attenuator (with gain Att [dB]) is placed in front of it and the minimum required Att is chosen, as determined by the maximum blocker handling capability of the AUX, i.e., the power in dBm that degrades its NF by 1 dB (blocker NF BNF_{AUX}). The calculated ΔNF_{RX} with DNR for different TX power levels is shown in Fig. 4 for an AUX NF (NF_{AUX}) of 7 dB and $BNF_{AUX} = 5$ dBm. ΔNF_{RX} is lower than 1 dB up to the full TX power of 23 dBm. Notice that, even if PSD_{TXn} was raised to -144 dBc/Hz, ΔNF_{RX} would increase by only 1 dB.

III. DIVERSITY RECEIVER DESIGN

As shown in Fig. 2, the receiver must have a very high IIP3. The introduction of bandpass and band-reject N-path filters in front of the receiver can yield very high linearity by attenuating blockers and TX leakage [17], [33]–[35], [55]. However, they introduce large LO leakage, degrade the NF and, to achieve high dynamic range, have large power dissipation. For these reasons, a highly linear broadband current-mode receiver is introduced. To further improve its linearity without increasing power dissipation, a passive RF canceller is utilized.

A. Low-Noise Transconductance Amplifier (LNTA) Design

In [11], a highly linear common-gate (CG) LNTA was presented. The LNTA, reported in Fig. 5(b), has complementary (p-n) cross-coupled CG amplifiers working in class-AB for high 1-dB gain compression point. Gate cross-coupling lowers the CG amplifier noise factor to $1 + \gamma/2$ and rejects the third-order inter-modulation products (IM3) due to the MOS second-order non-linear transconductance, improving IIP3. Better noise and IIP3 can be obtained if the CG LNTA source impedance is increased above its input impedance [11] by making noise/distortion terms recirculate within the transistor that creates them. In a loss-less network, this also leads to impedance mismatch, but considering transformer losses together with RF canceller loading impedance, acceptable impedance matching is reached.

A transformer with one primary and two secondaries with $k = 0.7$ implements the balun and broadband source impedance boosting on the secondary. The inductive impedance seen at the transformer primary resonates with the 3.2 pF series capacitor and the canceller capacitor to attain input impedance matching. The three-winding transformer was optimized for minimum overall noise when the antenna impedance is 50 Ω . LNTA simulation results are reported in Fig. 6. The LNTA IIP3 is 28 dBm and its NF, including transformer losses, is below 2.5 dB between 1.5 and 2.5 GHz while drawing only 8 mA from the 1.8 V supply. Notice that the NMOS and PMOS input transistors are sized to obtain a $g_m/I_d = 10$ mS/mA and no derivative superposition is used to improve linearity.

B. Mixer and Transimpedance Amplifier (TIA)

The LNTA is ac coupled to a passive mixer driven by a 25% duty-cycle LO, followed by a transimpedance amplifier (TIA) with a real pole at 20 MHz [Fig. 5(c)]. The TIA three-stage amplifier is compensated exploiting the passive feedback network to achieve 1.6 GHz unity-gain loop bandwidth while drawing 3 mA from 1.8 V [45]. At the output of the mixer 20 pF capacitors to ground provide low impedance at frequencies above 600 MHz.

C. RF Canceller

Passive cancelers enable low power and high linearity [16]. Without internal amplification, minimization of fixed losses is key, especially at low ISO_{TX-RX} , in order to maximize the input impedance and minimize the noise injected in the RX. For this reason, in the proposed canceller, instead of cascading a magnitude control stage and a phase control stage, two parallel variable attenuators are used (R-DAC and C-DAC) that generate quadrature output currents to be injected directly at the LNTA input [Fig. 5(a)]. This is advantageous also in terms of precision. With the chosen topology, 5-bit precision in the two DACs is sufficient to ensure 27 dB of cancellation. Alternatively, error less than 4% and a phase error less than 2° would be required. In the test chip, a transformer is used to convert the canceller input signal to differential. In a fully integrated solution, the transformer is not needed since the TX signal is typically available in differential form at the output of the transmitter [20], [21]. Moreover, since a relatively

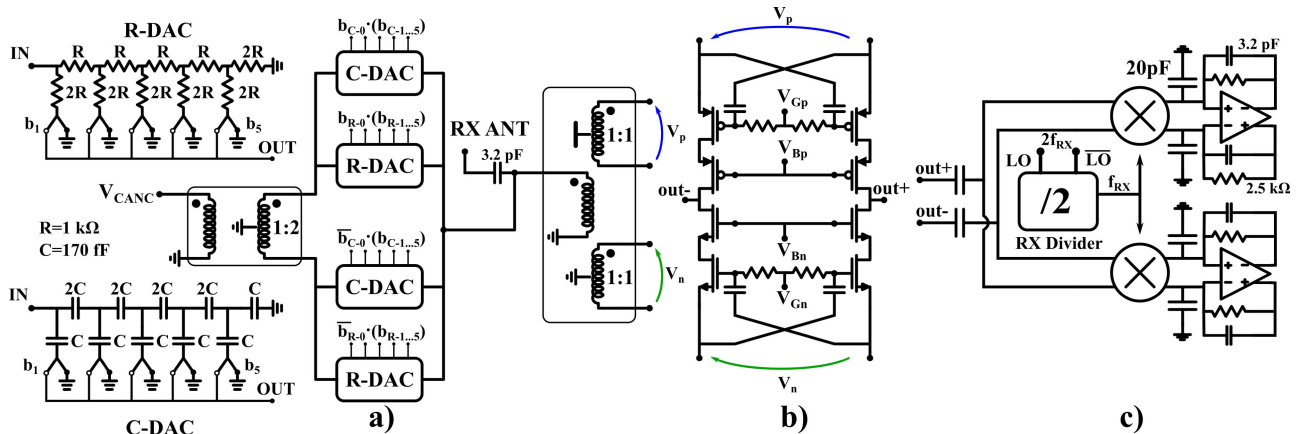


Fig. 5. Complete RX schematic with (a) SIC, (b) LNTA, and (c) four-phase passive mixer and baseband stages.

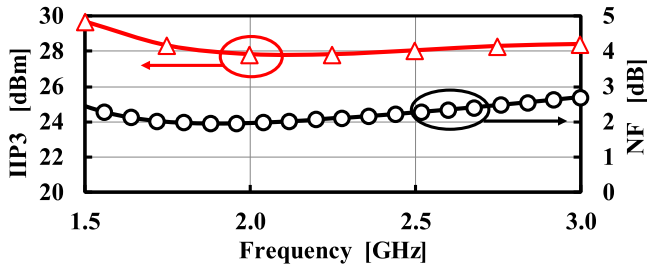


Fig. 6. Simulated LNTA NF (circles) and IIP3 (triangles).

low-cancellation level is targeted, it is not crucial to fully capture power amplifier non-linearity. Hence, the canceller may be tapped at the output of the transmitter before the PA, where a large voltage swing is available [49], which would greatly simplify system integration. R-DAC and C-DAC are independently controlled with 6 bits (5 bits for modulus plus one for sign). The high impedance of the R/C ladder protects the NMOS control switches from the large TX input signal, ensuring reliability and good linearity. Each switch is implemented with $L = 28$ nm and floating gate control, through a large (10 kΩ) resistor to distribute the residual voltage swing across the gate-source and gate-drain [59]. The differential input impedance of the DACs is 1 kΩ in parallel to 170 fF.

IV. AUXILIARY PATH DESIGN

The aim of the AUX is to provide a baseband replica of the TX noise that falls into the RX band. This signal is then converted into the digital domain, processed through the digital equalizer and subtracted from the diversity output to reduce the TX noise in the diversity path. As explained before, the AUX DR needs to be as high as possible to reduce ΔNF_{RX} . For this reason, an input band-reject filter (BRF) based on a N-Path architecture is proposed with a very high DR, thus reducing the DR required for the following blocks. Moreover, the N-Path filter is embedded in an active circuit thus reducing LO leakage and loading effects since it is not power matched to the source.

A. Active Band-Reject Filter

The schematic of the active BRF is shown in Fig. 7. The fully differential P-N common source input stage is

degenerated with a N-Path filter. The filter can be modelled as an RLC tank [32] providing a large degeneration impedance at the frequency of the LO and a much smaller one far away from it [Fig. 8(a)]. Employing the TX LO, the transconductance gain of the BRF is $G_m = g_m / (1 + g_m R_{deg})$, where R_{deg} is equal to R_{sw} in the RX band and $R_{sw} + R_p$ at f_{TX} . The value of the parallel resistance R_p is determined by the driving impedance of the N-Path filter ($R_d = 1/g_m + R_{sw}$), the number of clock phases (N_{ph}) and the clock duty cycle [32]. As N_{ph} increase, R_p and thus filter rejection (TX_{rej}) increase, relaxing the DR requirement of the following blocks. However, as the number of parallel paths increases, the parasitic capacitances (C_{par} in Fig. 7) also grow, down shifting the resonance frequency and degrading the peak rejection. This is modelled by C_{eff} and R_{eff} [30] in Fig. 8(a). For $N_{ph} = 8$ $C_{eff} \approx C_{par}$, hence increasing the number of phases N_{ph} beyond eight does not significantly improve the rejection. To avoid the degradation of the in-band gain for a TX-RX spacing of 50 MHz or higher, the size of the baseband capacitances C_{bb} was set to 8 pF. The input transistors are biased at 2 mA each giving a single-ended transconductance of 40 mS. The filtered output signal current is absorbed by two folded cascode transistors biased at a reduced current of 0.5 mA, and is then fed to a four-phase passive down-conversion mixer.

B. Baseband TIA and LO Phase Generators

The baseband TIAs provides a first-order filtering with a pole at 15 MHz. The TIA OpAmps have the same structure of the RX ones but, thanks to the reduced blocking requirements, the dc current is reduced to 2 mA. The clock for the BRF and for the passive mixers is obtained through on-chip dividers clocked from external generators at $4f_{TX}$ and at $2f_{RX}$, respectively. The eight phases at f_{TX} are generated as shown in Fig. 7 [29]. The first-frequency divider by two drives the second one with 50% duty-cycle waveforms. The final 12.5% duty-cycle clocks are generated ANDing three 50% duty-cycle waveforms at $4f_{TX}$, $2f_{TX}$, and f_{TX} , so that the edges of the output clock are determined by the input signal ones, minimizing phase noise and consequently reciprocal mixing in the BRF. Increasing the TX frequency, the finite BRF clock rise and fall time lower the duty cycle [32]. This can be modelled as an additional series resistance [R_{duty} in Fig. 8(a)]

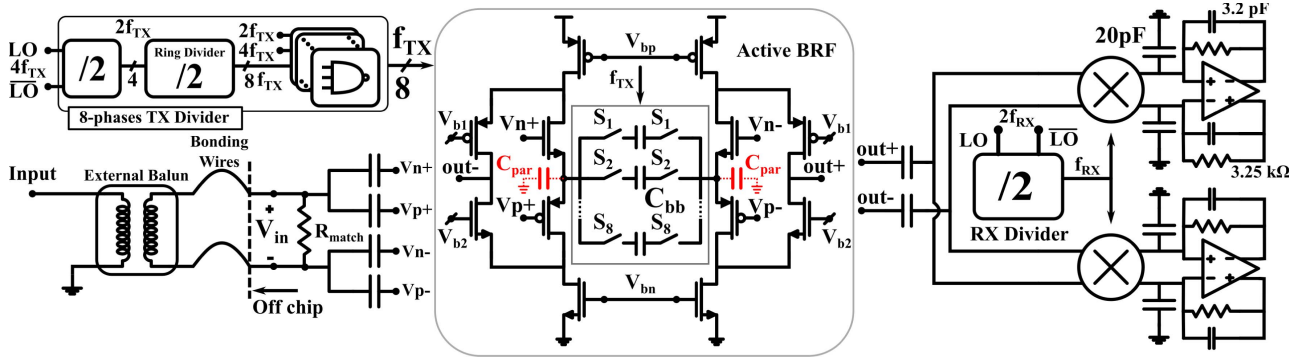


Fig. 7. Complete auxiliary path schematic.

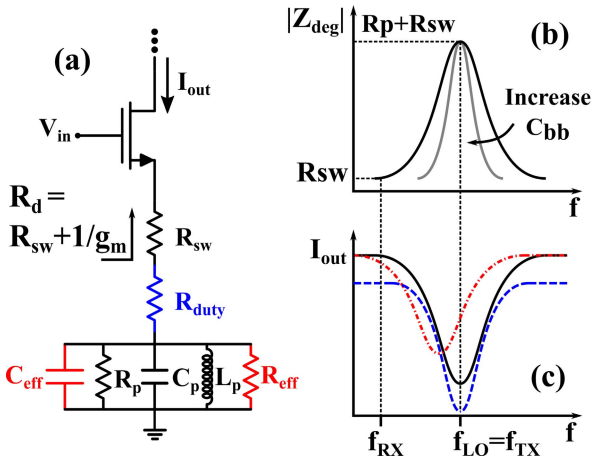
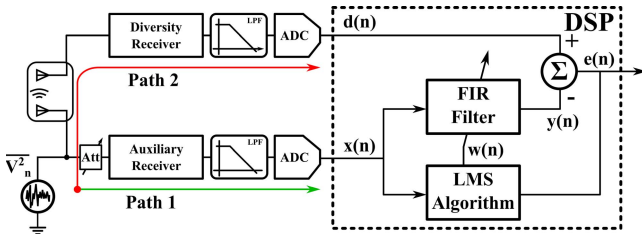

 Fig. 8. (a) Active BRF input stage model. (b) Ideal degeneration impedance versus frequency. Ideal transconductance (black curve), effect of parasitic capacitance C_{par} (red curve), and effect of reduced duty cycle (blue curve).


Fig. 9. Simplified system model. The digital path must equalize the difference between Path1 and Path2 to reduce the TX noise in the RX band.

that increases TX_{rej} , but also lowers the gain and increases $NFAUX$ [Fig. 8(c)].

V. DIGITAL NOISE REDUCTION

To understand the digital algorithm working principle in an intuitive way, a simplified block diagram of the system (Fig. 9) is used. The TX noise in the RX band is modelled as a white noise generator, connected to the AUX through an attenuator and coupled to the RX. The receivers down-convert a signal located in a frequency interval of 20 MHz around the RX carrier and the analog-to-digital converters (ADCs) converts it into digital. In this scenario, the finite-impulse response (FIR) filter must equalize the difference between Path1 and Path2, as shown in Fig. 9. Although the receivers

provide unequal in-band gain, the real asymmetry comes from the transfer function of the antennas coupling: while showing almost flat magnitude over the working bandwidth, a delay (δ) in the order of 2–3 ns introduces a sharp-phase variation in the leakage path. Therefore, the equalizer main task is to provide delay control of the signal coming from the AUX. Moreover, the interaction of the antennas with the external environment changes the coupling transfer function over time. For these reasons, the equalizer is implemented through a FIR filter and a LMS algorithm iteratively updates the filter coefficients.

A. LMS FIR Equalizer

In the proposed architecture (Fig. 9), the final output of the system is the instantaneous error $e(n)$ that is the difference between the signal coming from the RX $d(n)$ and the equalized AUX output $y(n)$. It can be demonstrated [53] that the Wiener filter represents the optimal solution [i.e., minimum $e(n)$] to which the LMS algorithm converges in an iterative way. From the Wiener theory, the minimum mean square error (MSE) is

$$\xi_{\min} = \sigma_d^2 - \mathbf{p}^H \mathbf{w}_0 = \sigma_d^2 - \mathbf{p}^H \mathbf{R}^{-1} \mathbf{p} \quad (2)$$

where H is the Hermitian transposition, σ_d^2 the variance (i.e., power) of $d(n)$, \mathbf{w}_0 is the vector of the optimum filter coefficients, \mathbf{p} is the cross-correlation vector of the two receivers' outputs, and \mathbf{R} is the autocorrelation matrix of $x(n)$. The DNR was defined in the previous section as the ratio between the TX noise power at the output of the RX (i.e., σ_d^2) and the TX noise power after digital equalization (i.e., ξ_{\min}). Therefore, from (2), the DNR in dB can be found normalizing the steady-state MSE over the input signal power, obtaining

$$DNR[dB] = 10 \log_{10} (1 - \mathbf{p}_n^H \mathbf{R}_n^{-1} \mathbf{p}_n) \quad (3)$$

where \mathbf{p}_n and \mathbf{R}_n are the cross correlation vector and correlation matrix normalized to the input signal power. This expression highlights that the DNR depends on the statistical parameter of the input signals: the higher is the correlation, the lower is the steady-state MSE. Since the TX noise bandwidth is inherently much larger than the RX channel, the resulting poor correlation is the main DNR limitation [56].

However, the analog filters in the two paths limit the bandwidth of the TX noise, spreading the signals autocorrelation (and cross correlation) over a larger time interval. For an ideal

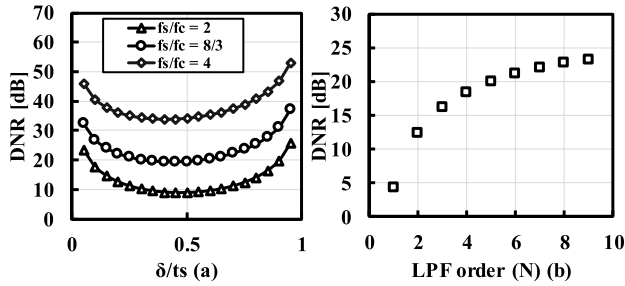


Fig. 10. Computed DNR versus (a) normalized group delay δ/t_s for different sampling/cutoff frequency ratios and (b) LPF order N .

low-pass filter (LPF) with cutoff frequency f_c and transfer function $H_{id} = \text{rect}(f/2f_c)$, the computed DNR with a fourth-order Wiener filter versus the normalized antenna group delay (δ/t_s) for different frequency ratios (f_s/f_c) is reported in Fig. 10(a). From these results, it can be noticed that the main limitation comes from the fact that the group delay between the antennas is only a fraction of the sampling period, limiting the DNR for low f_s/f_c to 10–20 dB. Moreover, the finite-analog LPF order affects the DNR, lowering the correlation between the sampled signals with respect to the ideal LPF case. For example, setting $f_s = 40$ MHz, $f_c = 15$ MHz ($f_s/f_c = 8/3$), and $\delta = 3$ ns ($\delta/t_s = 1.2$), the total DNR is 5 dB with a first-order Butterworth LPF and converges toward the value previously computed when the filter order becomes very large [Fig. 10(b)].

B. System Simulations

A MATLAB Simulink model was developed to simulate the performance of the digital path. The antenna's coupling is modelled as a broadband attenuation of 25 dB and a constant group delay of 3 ns. The cutoff frequency of the baseband LPFs is set to $f_c = 15$ MHz considering the LTE 20 RF channel bandwidth. To minimize the power consumption, ADCs oversampling ratio of 2 is used ($f_s = 40$ MHz). The LPFs order N is chosen equal to 5 to guarantee enough correlation between the sampled signal and a minimum DNR of 20 dB [Fig. 10(b)]. As digital equalizer, a fourth-order complex LMS-FIR filter is implemented. The FIR filter order is set considering the delay in the antenna coupling, the sampling frequency and the signal correlation resulting from the analog filtering. Since the sampling frequency is only twice the RF bandwidth, only few samples show a significant correlation and hence increasing the number of filters taps over four does not significantly improve the DNR.

Fig. 11 shows the spectra at the output of the system with the digital algorithm turned on and off: the noise is reduced by 20 dB over the whole frequency range [−20–20 MHz] and by ~ 25 dB in-band [−10–10 MHz] where the signal is stronger. However, as previously said, the DNR depends on the group delay between the antennas. In Fig. 12, the simulated DNR versus δ is reported for different cases; the LMS equalizer (triangles) is compared with the Wiener implementation (dashed curve) showing that the performance degradation introduced by the LMS approximation is essentially negligible. The other curve (circles) refers to the in-band [−10–10 MHz]

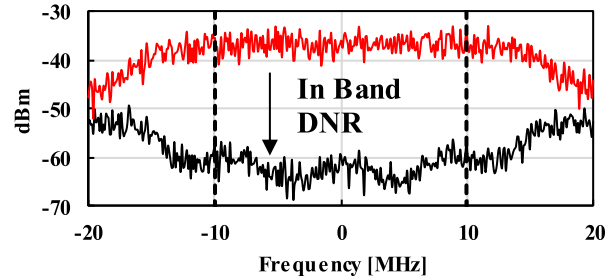


Fig. 11. Simulated spectra before (black line) and after (red line) the noise reduction with $\delta = 3$ ns.

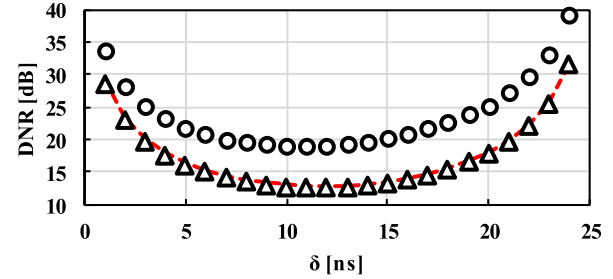


Fig. 12. DNR versus antenna group delay. The total DNR is compared for Wiener (red dashed line) and LMS (triangles) implementations. The in-band DNR (circles) considers only the noise power within −10–10 MHz.

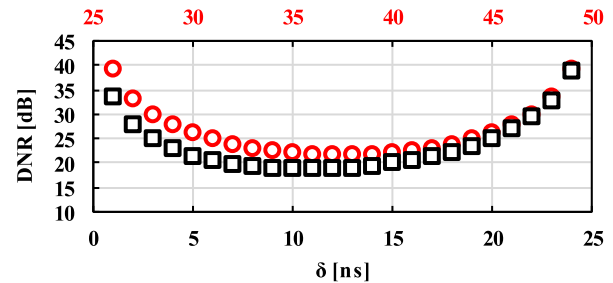


Fig. 13. DNR versus antenna group delay for δ between 0 and t_s (squares) and δ between t_s and $2t_s$ (circles).

power reduction, that is the real DNR of interest for the intended application. Moreover, it can be noticed that the DNR is maximized when δ is zero or a multiple of the sampling period since the AUX output signal is equal to the RX one simply delayed by a multiple of the sampling time (fully correlated). This suggests that the trend of the DNR is periodic with respect to δ , as shown in Fig. 13. When δ is between t_s and $2t_s$, the noise reduction is higher because the filter can exploit also the correlation of the signal with the previous more correlated sample. For this reason, in the final implementation of the LMS-FIR filter (Fig. 14), an additional delay tap is added in the RX path, improving the DNR for small δ (0–10 ns).

Additional simulations were performed for wider signal bandwidths, up to 80 MHz, to evaluate the applicability of the technique to future systems and the results are reported in Table I. For the same antenna delay, with a small increase in the number of FIR filter taps, improved DNR would be achieved.

Up to now, only direct coupling between the antennas has been considered. To take into account also a possible

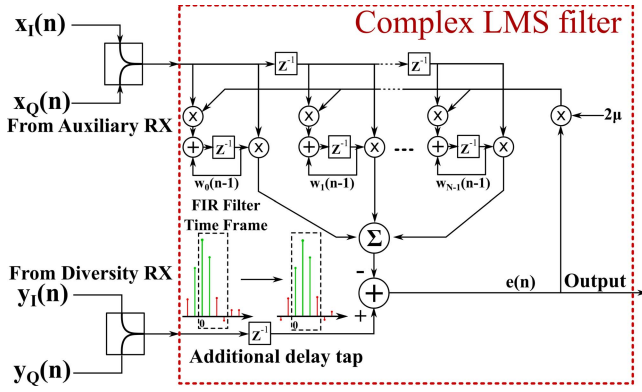


Fig. 14. Block diagram of the digital path. The added delay tap improves the DNR exploiting the most correlated samples of the noise signal.

TABLE I
DNR PERFORMANCE VERSUS RF BANDWIDTH

RF BW [MHz]	f_s [MHz]	LMS-FIR Taps	Delay Taps	In Band DNR [dB]
20	40	4	1	30
40	80	8	2	39
80	160	16	4	42

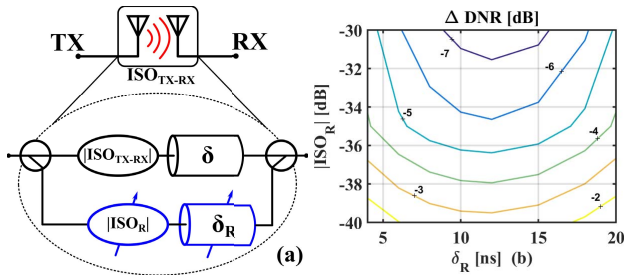


Fig. 15. (a) Antenna-coupling model with main (black) and reflected (blue) path. (b) Δ DNR versus attenuation ($|ISO_R|$) and delay (δ_R).

reflection, a second path with attenuation $|ISO_R|$ and group delay δ_R was added in parallel to the main one [Fig. 15(a)]. Fig. 15(b) shows the DNR degradation (Δ DNR) considering different delays/attenuations. In all cases, Δ DNR stays between -7 and -2 dB corresponding to an additional ΔNF_{RX} of 0.35 – 0.06 dB with respect to the value showed in Fig. 4 for $P_{TX} = 23$ dBm.

The above considerations have been done assuming noiseless receivers. However, the simulations confirm that the noise generated by the two down-conversion paths does not limit the final value of the DNR, since it is uncorrelated with the TX one. For the same reason, the algorithm is able to restore the RX sensitivity also in the presence of a modulated RX signal coming from the diversity antenna without performance degradation.

VI. EXPERIMENTAL MEASUREMENTS

The diversity [46] and auxiliary [47] receivers were fabricated in 28-nm CMOS technology, while the digital algorithm was implemented on an field-programmable gate

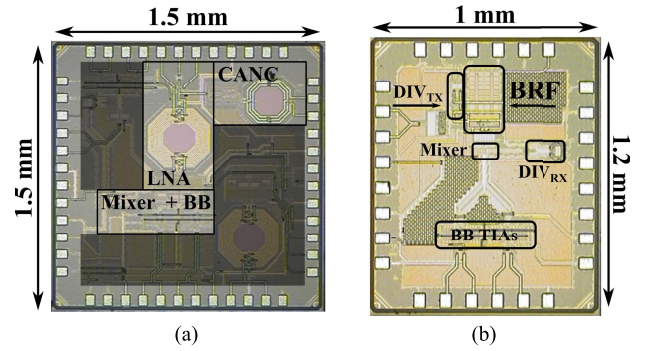


Fig. 16. (a) Diversity and (b) auxiliary chip photographs.

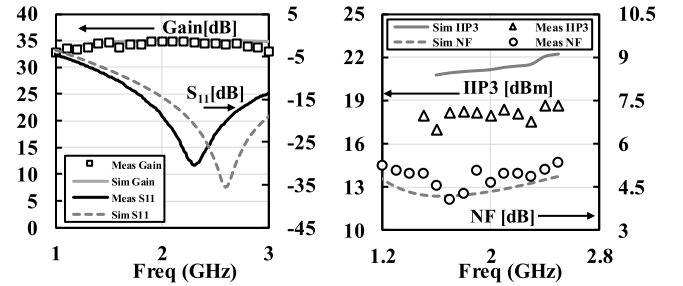


Fig. 17. Receiver down-conversion gain, S_{11} versus input frequency (left). NF and OOB IIP3 versus input frequency (right).

array (FPGA). The chip microphotograph is shown in Fig. 16. The active area occupied by the diversity RX is 0.51 mm^2 while the AUX takes 0.12 mm^2 . In this section, the performance of each chip and the measurements of the whole system are provided.

A. Diversity RX Performance

The main receiver has been characterized first with the canceler disabled. Gain, return loss, and noise measurements were carried out with an RF probe for better accuracy. The results are reported in Fig. 17, showing good agreement with simulations. The gain ranges from 32.8 to 34.9 dB between 1.2 and 3 GHz and S_{11} is below -10 dB from 1.5 to >3 GHz. The double-sideband NF is 4.6 dB at 2 GHz and varies from 4 to 5.4 dB between 1.2 and 2.5 GHz. Turning on the canceler degrades the NF by 0.4 – 0.8 dB depending on the canceler phase setting. The receiver IIP3 is 9 dBm IB and 18 dBm OOB at 2 GHz. The measured OOB IIP3 is close to the post-layout simulation results but is significantly lower than the LNA IIP3 reported in Fig. 6. This difference is due to two effects. First, even at very large frequency offsets, the TIA inter-modulation is not negligible. Second, the LNA requires a very low load impedance.

Even though in this design the mixer switches were designed for 10Ω on-resistance, due to a poor layout, their interconnect resistance increases the LNA load to over 40Ω . The normalized vector gain for all configurations of sign bit plus three MSBs for R-DAC and C-DAC is reported in Fig. 18(b), showing a noticeable constellation distortion. This issue was traced back to the signal un-balancing due to the connection of the canceler balun secondary winding center tap to the primary ground, configuration B in Fig. 18(a). If the

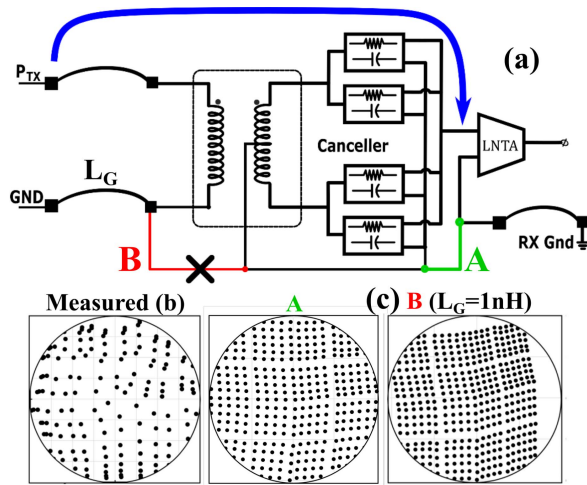


Fig. 18. Effect of different canceller grounding schemes on constellation. (a) Grounding configurations: A and B. (b) Measurement (configuration B). (c) Simulations.

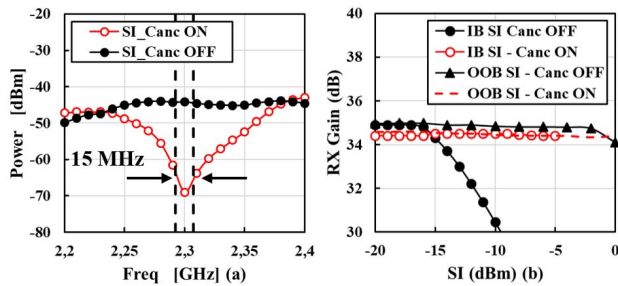


Fig. 19. (a) SI Power with a pair of PIFA. (b) IB gain compression with and without SIC.

secondary center-tap was connected instead to the receiver common-ground [configuration A in Fig. 18(a)], the correct canceller vector gain constellation is restored, as shown by the simulations in Fig. 18(c). Cancellation bandwidth for an antenna pair [planar inverted-F antenna (PIFA) from [14]], with a -25 dB coupling and 2.8 ns group delay is shown in Fig. 19(a). Minimum relative cancellation across 15 MHz bandwidth is 20 dB. When the canceller is disabled, the input-referred receiver 1 dB IB gain compression point ($P_{1\text{dB}}$) is -15 dBm with an IB blocker and 0 dBm with OOB blocker, as shown in Fig. 19(b). When the canceller is enabled IB $P_{1\text{dB}}$ goes to -5 dBm, while no compression was observed with OOB TX leakage up to the maximum available power level of 0 dBm [Fig. 19(b)]. Effective IIP3 due to inter-modulation between a continuous wave (CW) blocker and the TX leakage is reported in Fig. 20(a) and (b) versus cancellation for the halved FDD frequency spacing (HFS) and full FDD frequency spacing (FFS) scenarios. IIP3 improves by 1/2 dB (1 dB) for every dB of cancellation in HFS (FFS) scenario up to 29 dBm (25 dBm). Beyond these levels, IIP3 saturates due to canceller nonlinearity. The effective receiver IIP3 for IB SI goes from 9 dBm without cancellation to 25 dBm for 16 dB of cancellation. Beyond this point, the effective IIP3 is again limited by the canceller. Simulations indicate that canceller linearity is limited by the chosen grounding scheme. In fact, the large signal present at the canceller primary modulates the

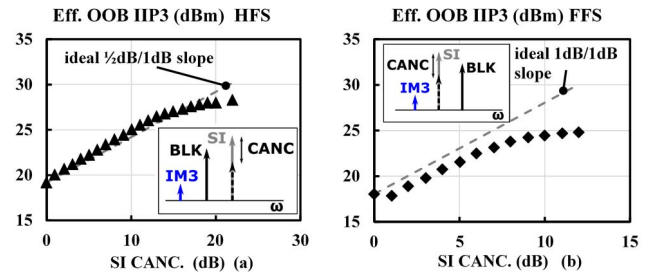


Fig. 20. Effective OOB IIP3 in HDS/FDS scenarios (a) and (b) and IB IIP3.

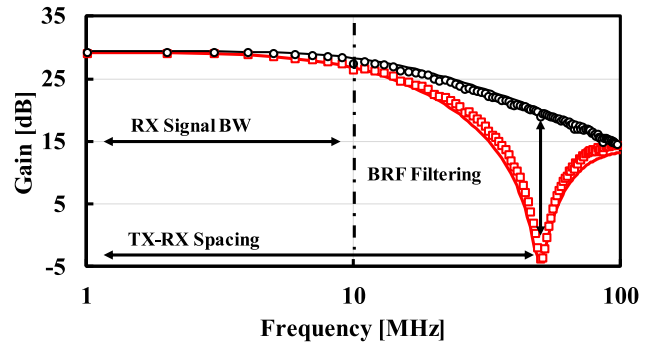


Fig. 21. Measured (dots) and simulated (lines) BRF attenuation versus baseband output frequency for a fixed RX frequency offset (50 MHz).

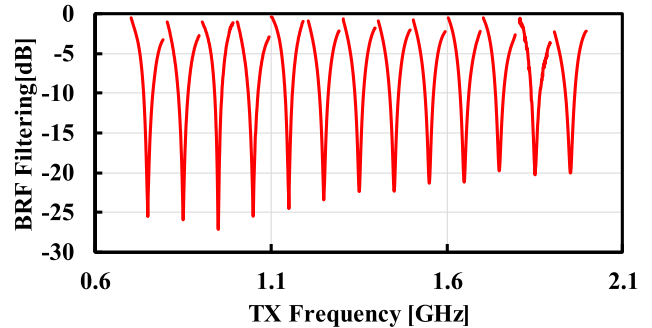


Fig. 22. Measured BRF attenuation versus f_{TX} for a fixed duplex spacing (50 MHz).

switches on-resistance leading to distortion. From simulations, connecting canceller ground to receiver ground, where ground bounce due to the TX is much lower, the effective IIP3 in FFS for 20-dB cancellation reaches 35 dBm.

B. AUX Performance

As for the RX, basic measurements were performed on the auxiliary receiver. An external balun with 50- Ω on-chip resistors are used to provide a differential input signal (Fig. 7). The losses of the balun and of the matching network are de-embedded from measurements since they will not be present in when the circuit is integrated with the main TX. Setting $f_{\text{TX}} = 1.15$ GHz and $f_{\text{RX}} = 1.1$ GHz, the measured down-conversion gain versus the baseband output frequency is shown in Fig. 21: the active BRF provides additional 24.5 dB of filtering at the TX frequency while not degrading the RX in-band gain. The BRF attenuation is then measured over a broad frequency range (Fig. 22). The peak attenuation goes

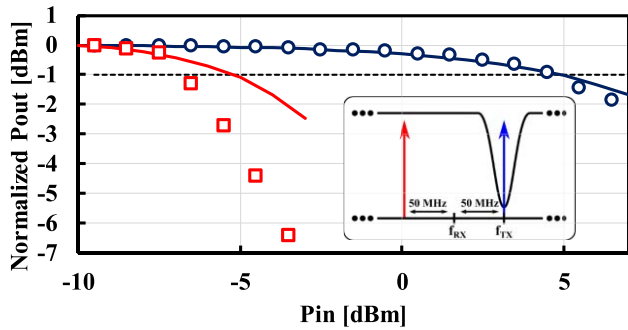


Fig. 23. Measured (dots) and simulated (lines) in-band gain compression with a CW blocker placed at $f_{RX} + 50$ MHz (circles) and at $f_{RX} - 50$ MHz (squares) with $f_{RX} = 1$ GHz and $f_{TX} = 1.05$ GHz.

from 26 to 20 dB at high frequencies due to the parasitic capacitances effect explained in Section IV-A. For the same reason, a negative frequency shift in the peak attenuation is observed that goes from 4 MHz for $f_{TX} = 750$ MHz to around 10 MHz at 2 GHz. To test the effective enhancement of the active BRF to the large signal handling capability of the auxiliary path, the 1-dB compression point was measured in two different cases: a CW signal was placed 50 MHz above and below the RX frequency ($f_{RX} = 1$ GHz), setting $f_{TX} = 1.05$ GHz (Fig. 23). In the first case, the CW passed unfiltered from the first stage, resulting in $B_{1dB} = -7$ dBm; in the other case, the signal is filtered by the active BRF and the B_{1dB} is improved up to 5 dBm. The enhancement is not equal to the peak attenuation of the filter because two different compression mechanisms are involved: when the blocker is unfiltered, the compression comes from the BB TIA stage, while limited LO swing driving the BRF switches causes the compression when the blocker is at f_{TX} . As long as the attenuation is kept above 19 dB, the B_{1dB} is nearly constant at 5 dBm. This allows to achieve high compression even with modulated TX signals and to accommodate for the unavoidable frequency shift caused by parasitic capacitors. With a 20 MHz modulated signal, the BRF provides an average attenuation of 18 dB over the bandwidth and the B_{1dB} is equal to 4 dBm. The in-band gain and NF were measured versus RX frequency for a fixed $f_{TX} = 800$ MHz (Fig. 24). The NF is nearly constant at 6.8 dB and the gain is 29.6 dB. Keeping constant the RX frequency ($f_{RX} = 1.95$ GHz), the TX frequency was swept between 0.7 and 2 GHz. The simulation results with ideal TX clock divider show a constant NF and gain around 6.2 and 30 dB, respectively. However, the effect of the reduced duty cycle at high frequencies degrades both NF and gain measurements. In fact, NF goes from 6.2 to 9.6 dB and the gain varies between 30 and 27 dB. Finally, the measured and simulated NF degradation due to a blocker at f_{TX} is reported in Fig. 25. To perform this measurement, SAW filters and duplexers were used to filter out the generators noise floor. With $f_{TX} = 950$ MHz and $f_{RX} = 1.05$ GHz, the NF degrades by 1.1 dB when the blocker power reaches 5 dBm thanks to the conservative design of the clock generation circuits.

In a fully integrated solution, the BRF would be clocked with the same noisy LO as the TX. Based on the analysis

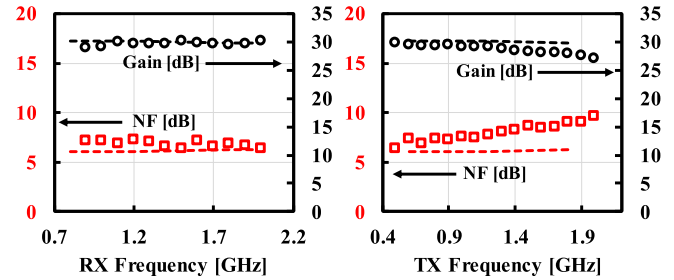


Fig. 24. Measured (dots) and simulated (lines) gain (circles) and NF (squares) versus (a) f_{RX} with $f_{TX} = 0.8$ GHz and (b) TX frequency with $f_{RX} = 1.95$ GHz.

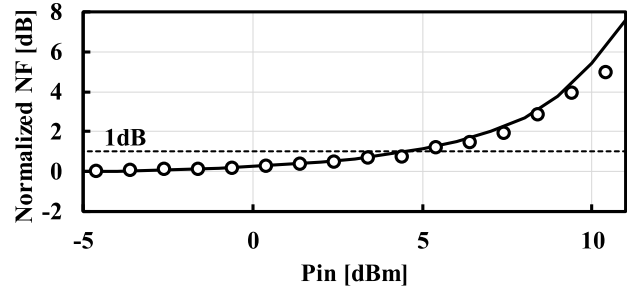


Fig. 25. Measured (circles) and simulated (line) NF degradation versus blk power.

in [52], it is easy to show that this introduces an additional noise due to reciprocal mixing in the BRF that will not be cancelled in the digital domain. Considering f_{TX} between 1 and 2 GHz, with the Class-B oscillator proposed in [51] for a power of 10 mW, a phase noise below -173 dBc/Hz at 50 MHz offset is expected. With reference to Fig. 4, this contribution would increase ΔNF_{RX} by 0.7 dB at $P_{TX} = 23$ dBm.

C. Digital Equalization Performance

The block diagram of the complete system measurement setup is shown in Fig. 26. The diversity and auxiliary receiver prototype chips are bonded on two dedicated printed circuit boards (PCBs), and they are biased through a National Instrument CRio-9014. A HP ESG-400A signal generator provides the RX clock to both chips while an Anritsu MG3692A signal generator is used for the TX clock. A QPSK/16-QAM 20-MHz modulated RX signal is produced through a R&S SMU 200A Vector Signal Generator and the broadband white noise is generated through a HP 364B noise source. The coupling between the antennas is emulated using a delay line that provides a group delay of 2–3 ns in the frequency range between 1 and 2 GHz. The output of the diversity and auxiliary receiver is connected to the input of two separate PCBs that are used to implement additional filtering and analog-to-digital conversion. Each board includes two fourth-order Butterworth LPFs (one for the I and one for the Q path) implemented with off-the-shelf components and two commercial 10-bit ADC (Analog Devices AD9215). Finally, the DNR algorithm is implemented on a Cyclone IV EP4CE115F29C7 Altera FPGA, which also provides the clock for the ADCs. The processed data are then acquired from an FPGA through the SignalTap II logic analyzer tool of Quartus.

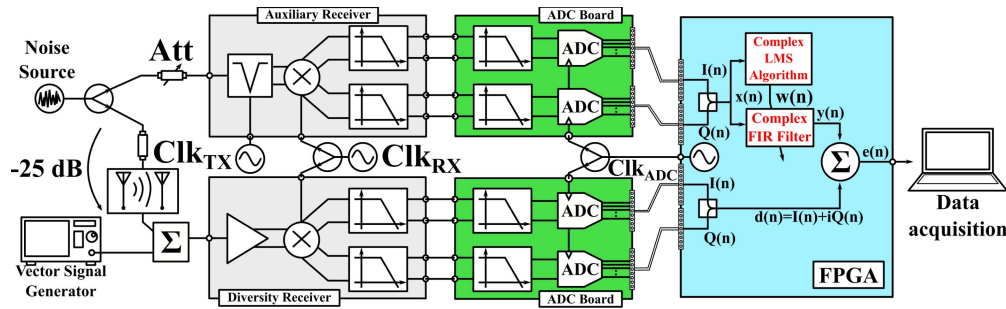


Fig. 26. Block diagram of the complete system measurement setup.

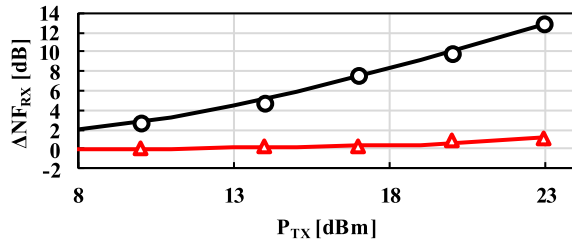


Fig. 27. Simulated (lines) and measured (dots) ΔNF_{RX} versus transmitter power with (triangles) and without (circles) DNR.

To test the digital algorithm performance, a broadband white noise source is used and its output is sent to both receivers, as shown in Fig. 26. For this preliminary test, the RX signal generator is disconnected, meaning that in the RX band only the TX noise is present. The RX LO frequency (f_{RX}) is set to 1.2 GHz and the TX frequency (f_{TX}), driving the active BRF in the AUX, to 1.1 GHz. In the band of interest (± 10 MHz around f_{RX}), the delay line used to emulate the coupling between the antennas provides a group delay of 3.2 ns and an attenuation of 2 dB. To reproduce the nominal $ISO_{TX-RX} = 25$ dB, the remaining attenuation is obtained through RF attenuator between the source and the RX. With a TX noise power $PSD_{TXn} = -153$ dBc/Hz, the ΔNF_{RX} is first measured when the DNR is turned off. The measurement results are reported in Fig. 27 and reveal that, with a $PSD_{TXn,RX} = -130$ dBm/Hz, corresponding to a TX power of 23 dBm, the diversity NF is degraded by almost 13 dB, which is in good agreement with the simulated and computed value. The theory and simulations developed in Section V suggest that, with a delay in the order of 3 ns, the resulting DNR is around 30 dB, meaning that the TX noise will be reduced well below the RX noise floor. Therefore, we expect that most of the contribution to ΔNF_{RX} comes from of the AUX. Both computation and simulation predict that the dynamic range of the auxiliary path should be sufficiently high to give a ΔNF_{RX} of only 1 dB when the TX noise is referred to a full power TX signal. The measurements are reported in Fig. 27 and follow the computed and simulated values very well. The spectra of the output signals with and without the noise reduction at full TX power are shown in Fig. 28: the TX noise power is uniformly reduced within the bandwidth restoring the RX sensitivity.

It is interesting to notice that, increasing PDS_{TXn} , the NRs in the RX and AUX side increase by the same amount, keeping

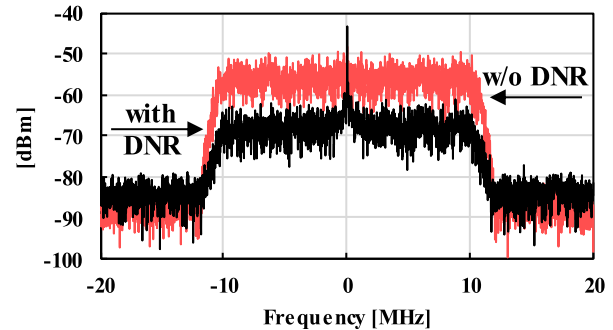


Fig. 28. Measured spectra with (black line) and without (red line) noise reduction with full power TX.

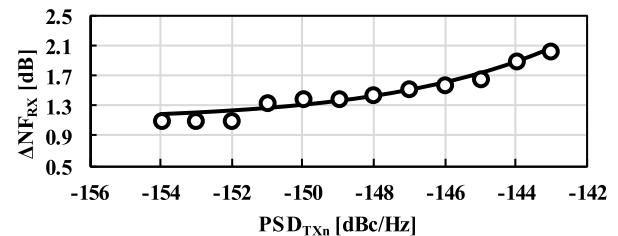


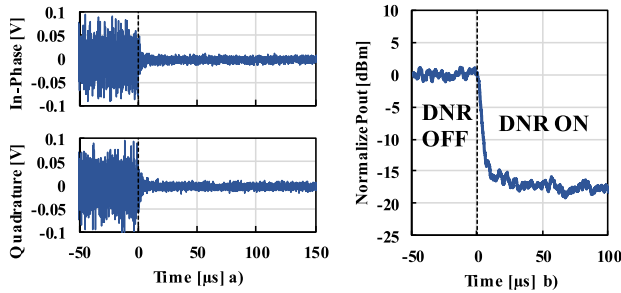
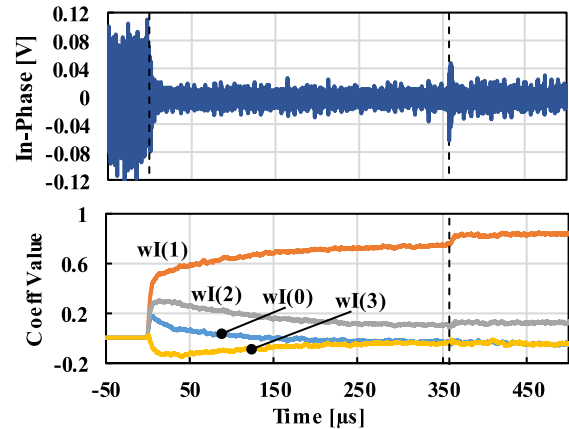
Fig. 29. Simulated (line) and measured (circles) ΔNF_{RX} versus transmitter noise power, increasing by 10-dB PSD_{TXn} degrades only by only 1 more dB ΔNF_{RX} .

their ratio (NR_{RX}/NR_{AUX}) constant. Therefore, the additional NF_{RX} degradation comes only from the residual TX noise after the cancellation, as per (1). Moreover, given the good DNR achievable, this is not the dominant component and its effect on the final degradation is limited. This was verified experimentally increasing the TX noise level, as shown in Fig. 29, and noticing that the performance of the system degrades by 1 dB only when PSD_{TXn} reaches -144 dBc/Hz. This result can be further improved increasing the LPF order or the sampling frequency as explained in the previous sections.

To test the convergence time of the proposed adaptation algorithm, a white noise with PSD equal to -148 dBm/Hz referred to the RX input was used. Fig. 30 shows the time waveforms of the output signals. At $t = 0$, the DNR is turned on, and in few microseconds, the output power is near the final value. This is more than enough to track the antenna variations, occurring on a time scale of milliseconds [44], [54]. The tracking mechanism of the algorithm was tested modifying the $|ISO_{TX-RX}|$ value to emulate a change in the environmental

TABLE II
 PERFORMANCE COMPARISON WITH THE STATE OF THE ART

		This work	JSSC 2014 [15]	JSSC 2015 [19]	JSSC 2015 [18]	
Architecture		RF Canceller + Auxiliary RX	Active Two-Point Cancellation	Wideband SIC RF equalization	Mixer-First RX + SIC VM-mixer	
FDD/FD		FDD	FDD	FDD FD	FD	
Antenna Interface		Antenna pair	Antenna pair 1 Ant. + duplexer	1 Ant. + duplexer Antenna pair	Antenna pair	
CMOS Tech.		28nm	65 nm	65 nm	65 nm	
Frequency [GHz]		1-2	0.3-1.7	0.8-1.4	0.15-3.5	
RX Gain [dB]		35	N/A	27-42	24	
NF w/o SIC [dB]		4-5	4.2-5.6	4.2-5.8	6.3	
NF Degradation with SIC [dB]		RF SIC	<0.8	0.6	1.1-1.3	
		Aux RX				
IIP3 OOB [dBm]		+18	+12 (c)	+17	+22	
Eff. IIP3 OOB [dBm]		+25 / +29	+33	+25 / +27	N/A	
IIP3 IB [dBm]		+9	N/R	-20	+9	
Eff. IIP3 IB [dBm]		+25	N/R	+2	+21.5	
SINDR [dB]		+78	N/R	+62.5	+71.5	
SI Cancellation		Canc [dB]	> 20	N/R 20	20 20	21
		BW [MHz]	15	N/R 1-7	24 25	16
External TX-RX Isolation		Mag [dB]	25	30 41-51	30 35	25
		Del [ns]	3	2-4 ~20	<11 5-9	4
Max IB TX Leak. [dBm]		-5	N/A	-8	+1.5	
Max TX Power [dBm]		+23	N/R	N/R	N/R	
TX Noise Reduction [dB]		≥ 29	13	N/R N/A	N/A	
Max OOB TX Leak. [dBm]		0 (b)	+2 (c)	-4	N/A	
Power [mW]		RX	32-40	74.6-83	63-69	22-46
		Canc.	Main	0	13-72	91/path
Aux RX						
Area [mm ²]		0.63	1.2	4.8	2	

 a) With $P_{TX}=23\text{dBm}$; b) 100 MHz Offset; c) 60 MHz Offset;

 Fig. 30. (a) Time waveforms of the baseband signals. (b) Normalized output power. At $t = 0$ the digital algorithm is turned on, converging in few microseconds.

 Fig. 31. Time waveform of the baseband signal and real FIR coefficients. At $t \approx 350 \mu\text{s}$, the ISOTX-RX is changed by 3 dB.

condition. Fig. 31 shows the time output waveform when at $t \approx 350 \mu\text{s}$ the coupling is changed by 3 dB; also in this case, the LMS algorithm updates the filter coefficients in few microseconds, restoring the RX sensitivity.

The vector signal generator is used to produce a 20 MHz PSK modulated signal emulating a wanted RX signal coming into the diversity RX. Since it is completely uncorrelated with the TX noise that falls in the same band, the LMS algorithm

should be able to find the correct coefficients to reduce the TX interference without degrading the wanted signal. This is experimentally demonstrated injecting a -82 dBm 20 MHz QPSK modulated signal at the RX input (the RX

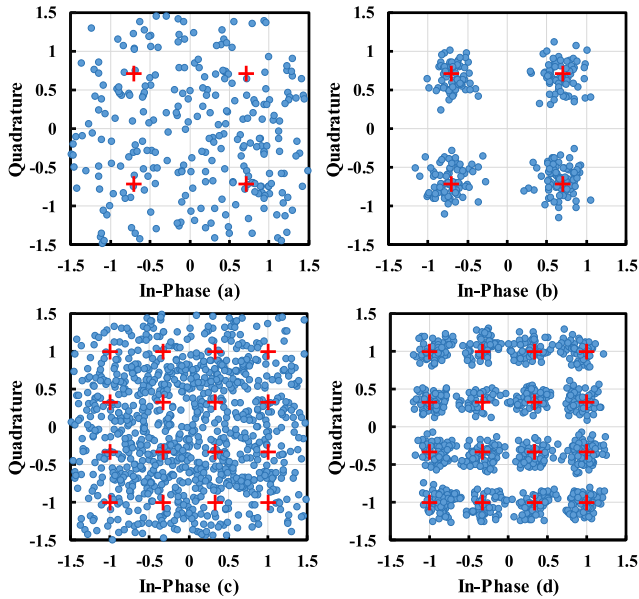


Fig. 32. Measured 20-MHz QPSK and 16-QAM signal constellation (b) and (d) with and (a) and (c) without TX noise reduction.

noise level is -95 dBm) together with a noise power density of -156 dBm/Hz, that corresponds to an in-band noise power of -83 dBm. Without the equalization process, the RX signal is almost completely covered by the TX noise and its constellation is shown in Fig. 32(a) and (b). When the algorithm is turned on, the signal can be correctly demodulated with a measured modulation error ratio (MER) of 12 dB. Finally, the same test was performed with a -77 dBm 16-QAM modulated signal, as shown in Fig. 32(c) and (d), with a measured MER of 17 dB.

A challenging aspect that has not been addressed in this paper is the selectivity requirement. The TX leakage reaching the RX/AUX is in the order of $-20/-15$ dBm after the SIC/BRF. In our implementation, only a single real pole was integrated in each receiver, which is not enough to achieve sufficient selectivity. An efficient solution to this problem is to merge the anti-alias filter into an oversampling ADC architecture [58]. Sufficient selectivity and DR to withstand OOB blockers as high as -20 dBm while dissipating only 8 mW has been reported in [58]. Notice that the same level of filtering that preserves sensitivity also ensures that the DNR algorithm will not be impacted by the TX signal leakage.

A comparison with other SIC receivers is reported in Table II. Considering the RX with the RF canceller, this paper achieves lower power dissipation and equal or better NF. When the TX noise leakage is considered, this paper outperforms [15], which is the only SIC receiver that reports dual-band TX leakage cancellation. Very good IB IIP3 and effective IIP3 were achieved, as shown by the improved SI-to-noise and distortion ratio (SINDR) [18]. Effective OOB IIP3, which is comparable to [19], is limited by canceler nonlinearity. Simulation results indicate that an improved canceler grounding scheme could boost the effective OOB IIP3 up to 35 dBm. Finally, area occupation is reduced compared to other works.

VII. CONCLUSION

A diversity receiver for FDD systems with transmitter leakage cancellation in both TX and RX bands was presented. Due to the antenna-coupling group delay, typically on the order of 2–3 ns, SIC bandwidth is limited to 25 MHz or less, which makes it difficult to ensure isolation in both TX and RX bands. To overcome this limitation, an auxiliary receiver senses the TX noise in the RX band, and a dedicated DSP performs broadband TX noise cancellation in the digital domain. The complete SIC system includes a current-mode main RX path with a highly linear CG LNTA, a passive RF canceller for improved TX leakage tolerance, and the AUX that ensures noise suppression also in the RX band. In this way, large TX–RX frequency spacing can be accommodated. For 25-dB antenna isolation, TX power levels up to 23 dBm and broadband TX transmitter noise of up to -144 dBc/Hz are handled with less than 1.8-dB NF degradation. Experimental results demonstrate an effective OOB IIP3 of 25–29 dBm, limited by canceler non-linearity. Simulations show that, with an improved canceler grounding scheme, the effective IIP3 should reach 35 dBm.

ACKNOWLEDGMENT

The authors would like to thank Marvell for chip fabrication and support and Integrand Software for EMX software donation.

REFERENCES

- [1] S. Hong *et al.*, “Applications of self-interference cancellation in 5G and beyond,” *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 114–121, Feb. 2014.
- [2] D. Bharadia, E. McMillin, and S. Katti, “Full duplex radios,” in *Proc. ACM SIGCOMM*, 2013, pp. 375–386.
- [3] A. Sabharwal, P. Schniter, D. Guo, D. W. Bliss, S. Rangarajan, and R. Wichman, “In-band full-duplex wireless: Challenges and opportunities,” *IEEE J. Sel. Areas Commun.*, vol. 32, no. 9, pp. 1637–1652, Sep. 2014.
- [4] N. A. Estep, D. L. Sounas, J. Soric, and A. Alù, “Magnetic-free non-reciprocity and isolation based on parametrically modulated coupled-resonator loops,” *Nature Phys.*, vol. 10, no. 12, pp. 923–927, Dec. 2014.
- [5] J. Zhou, N. Reiskarimian, and H. Krishnaswamy, “Receiver with integrated magnetic-free N-path-filter-based non-reciprocal circulator and baseband self-interference cancellation for full-duplex wireless,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 178–180.
- [6] N. A. Estep, D. L. Sounas, and A. Alù, “Magnetless microwave circulators based on spatiotemporally modulated rings of coupled resonators,” *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 502–518, Feb. 2016.
- [7] N. Reiskarimian and H. Krishnaswamy, “Magnetic-free non-reciprocity based on staggered commutation,” *Nature Commun.*, vol. 7, no. 4, Apr. 2016.
- [8] N. Reiskarimian, M. B. Dastjerdi, J. Zhou, and H. Krishnaswamy, “Highly-linear integrated magnetic-free circulator-receiver for full-duplex wireless,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2017, pp. 316–317.
- [9] N. Reiskarimian, J. Zhou, and H. Krishnaswamy, “A CMOS passive LPTV nonmagnetic circulator and its application in a full-duplex receiver,” *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1358–1372, May 2017.
- [10] M. Mikhemar, H. Darabi, and A. Abidi, “A tunable integrated duplexer with 50 dB isolation in 40 nm CMOS,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2009, pp. 386–387, 387a.
- [11] I. Fabiano, M. Ramella, D. Manstretta, and R. Castello, “A +25-dBm IIP3 1.7–2.1-GHz FDD receiver front end with integrated hybrid transformer in 28-nm CMOS,” *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4677–4688, Nov. 2017.

- [12] B. van Liempd, B. Hershberg, B. Debaillie, P. Wambacq, and J. Craninckx, "An electrical-balance duplexer for in-band full-duplex with <-85 dBm in-band distortion at +10 dBm TX-power," in *Proc. 41st Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 176–179.
- [13] B. van Liempd *et al.*, "A +70-dBm IIP3 electrical-balance duplexer for highly integrated tunable front-ends," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4274–4286, Dec. 2016.
- [14] D. Montanari, L. Silvestri, M. Bozzi, and D. Manstretta, "Antenna coupling and self-interference cancellation bandwidth in saw-less diversity receivers," in *Proc. EuMC*, London U.K., Oct. 2016, pp. 731–734.
- [15] J. Zhou, A. Chakrabarti, P. R. Kinget, and H. Krishnaswamy, "Low-noise active cancellation of transmitter leakage and transmitter noise in broadband wireless receivers for FDD/Co-existence," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3046–3062, Dec. 2014.
- [16] T. Zhang, A. R. Suvarna, V. Bhagavatula, and J. C. Rudell, "An integrated CMOS passive self-interference mitigation technique for FDD radios," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1176–1188, May 2015.
- [17] C. Luo, P. S. Gudem, and J. F. Buckwalter, "0.4–6 GHz, 17-dBm B1dB, 36-dBm IIP3 channel-selecting, low-noise amplifier for SAW-less 3G/4G FDD receivers," in *Proc. IEEE RFIC*, May 2015, pp. 299–302.
- [18] D.-J. van den Broek, E. A. M. Klumperink, and B. Nauta, "An in-band full-duplex radio receiver with a passive vector modulator downmixer for self-interference cancellation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3003–3014, Dec. 2015.
- [19] J. Zhou, T.-H. Chuang, T. Dinc, and H. Krishnaswamy, "Integrated wideband self-interference cancellation in the RF domain for FDD and full-duplex wireless," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3015–3031, Dec. 2015.
- [20] T. Zhang, A. Najafi, C. Su, and J. C. Rudell, "A 1.7-to-2.2 GHz full-duplex transceiver system with >50 dB self-interference cancellation over 42 MHz bandwidth," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2017, pp. 314–315.
- [21] T. Zhang, Y. Chen, C. Huang, and J. C. Rudell, "A low-noise reconfigurable full-duplex front-end with self-interference cancellation and harmonic-rejection power amplifier for low power radio applications," in *Proc. 43rd IEEE Eur. Solid State Circuits Conf. (ESSCIRC)*, Leuven, Belgium, Sep. 2017, pp. 336–339.
- [22] A. Kiayani, L. Anttila, and M. Valkama, "Active RF cancellation of nonlinear TX leakage in FDD transceivers," in *Proc. IEEE Global Conf. Signal Inf. Process. (GlobalSIP)*, Washington, DC, USA, Dec. 2016, pp. 689–693.
- [23] J. Tamminen *et al.*, "Digitally-controlled RF self-interference canceller for full-duplex radios," in *Proc. 24th Eur. Signal Process. Conf. (EUSIPCO)*, Budapest, Hungary, Aug. 2016, pp. 783–787.
- [24] T. Huusari, Y.-S. Choi, P. Liikkanen, D. Korpi, S. Talwar, and M. Valkama, "Wideband self-adaptive RF cancellation circuit for full-duplex radio: Operating principle and measurements," in *Proc. IEEE 81st Veh. Technol. Conf. (VTC Spring)*, Glasgow, U.K., May 2015, pp. 1–7.
- [25] S. Ramakrishnan, L. Calderin, A. Niknejad, and B. Nikolić, "An FD/FDD transceiver with RX band thermal, quantization, and phase noise rejection and >64 dB TX signal cancellation," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Honolulu, HI, USA, Jun. 2017, pp. 352–355.
- [26] L. Calderin, S. Ramakrishnan, A. Puglielli, E. Alon, B. Nikolić, and A. M. Niknejad, "Analysis and design of integrated active cancellation transceiver for frequency division duplex systems," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2038–2054, Aug. 2017.
- [27] H. Hedayati, V. Aparin, and K. Entesari, "A +22 dBm IIP3 and 3.5 dB NF wideband receiver with RF and baseband blocker filtering techniques," in *Symp. VLSI Circuits Dig. Tech. Papers*, Honolulu, HI, USA, Jun. 2014, pp. 1–2.
- [28] H. Hedayati, W.-F. A. Lau, N. Kim, V. Aparin, and K. Entesari, "A 1.8 dB NF blocker-filtering noise-canceling wideband receiver with shared TIA in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1148–1164, May 2015.
- [29] J. W. Park and B. Razavi, "Channel selection at RF using miller bandpass filters," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3063–3078, Dec. 2014.
- [30] M. Darvishi, R. van der Zee, and B. Nauta, "Design of active N-path filters," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2962–2976, Dec. 2013.
- [31] Y. Lien, E. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "A highly-linear CMOS receiver achieving +44 dBm IIP3 and +13 dBm B1dB for SAW-less LTE radio," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2017, pp. 412–413.
- [32] A. Ghaffari, E. A. M. Klumperink, and B. Nauta, "Tunable N-path notch filters for blocker suppression: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1370–1382, Jun. 2013.
- [33] C.-K. Luo, P. S. Gudem, and J. F. Buckwalter, "A 0.4–6-GHz 17-dBm B1dB 36-dBm IIP3 channel-selecting low-noise amplifier for SAW-less 3G/4G FDD diversity receivers," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1110–1121, Apr. 2016.
- [34] M. N. Hasan, Q. J. Gu, and X. Liu, "Tunable blocker-tolerant on-chip radio-frequency front-end filter with dual adaptive transmission zeros for software-defined radio applications," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4419–4433, Dec. 2016.
- [35] G. Qi, B. van Liempd, P. I. Mak, R. P. Martins, and J. Craninckx, "A 0.7 to 1 GHz switched-LC N-Path LNA resilient to FDD-LTE self-interference at ≥ 40 MHz offset," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Honolulu, HI, USA, Jun. 2017, pp. 276–279.
- [36] S. H. Abdelhalem *et al.*, "Tunable CMOS integrated duplexer with antenna impedance tracking and high isolation in the transmit and receive bands," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2092–2104, Sep. 2014.
- [37] B. Hershberg, B. van Liempd, X. Zhang, P. Wambacq, and J. Craninckx, "A dual-frequency 0.7-to-1GHz balance network for electrical balance duplexers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2016, pp. 356–357.
- [38] B. van Liempd, A. Visweswaran, S. Ariumi, S. Hitomi, P. Wambacq, and J. Craninckx, "Adaptive RF front-ends using electrical-balance duplexers and tuned saw resonators," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4621–4628, Nov. 2017.
- [39] E. Roverato *et al.*, "All-digital RF transmitter in 28 nm CMOS with programmable RX-band noise shaping," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2017, pp. 222–223.
- [40] R. Bhat, J. Zhou, and H. Krishnaswamy, "Wideband mixed-domain multi-tap finite-impulse response filtering of out-of-band noise floor in watt-class digital transmitters," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3405–3420, Dec. 2017.
- [41] E. Roverato *et al.*, "All-digital LTE SAW-less transmitter with DSP-based programming of RX-band noise," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3434–3445, Dec. 2017.
- [42] *Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) Radio Transmission and Reception Version 12.6.0*, document 3GPP TS 36.610, Release 12, 2015.
- [43] S. H. Abdelhalem, P. S. Gudem, and L. E. Larson, "Hybrid transformer-based tunable differential duplexer in a 90-nm CMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1316–1326, Mar. 2013.
- [44] G. Castellano, D. Montanari, D. De Caro, D. Manstretta, and A. G. M. Strollo, "An efficient digital background control for hybrid transformer-based receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 12, pp. 3068–3080, Dec. 2017.
- [45] G. Pini, D. Manstretta, and R. Castello, "Analysis and design of a 20-MHz bandwidth, 50.5-dBm OOB-IIP3, and 5.4-mW TIA for SAW-less receivers," *IEEE J. Solid-State Circuits*, to be published.
- [46] E. Kargaran, S. Tijani, G. Pini, D. Manstretta, and R. Castello, "Low power wideband receiver with RF self-interference cancellation for full-duplex and FDD wireless diversity," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Honolulu, HI, USA, Jun. 2017, pp. 348–351.
- [47] D. Montanari, D. Manstretta, R. Castello, and G. Castellano, "A 0.7–2 GHz auxiliary receiver with enhanced compression for SAW-less FDD," in *Proc. 43rd IEEE Eur. Solid State Circuits Conf. (ESSCIRC)*, Leuven, Belgium, Sep. 2017, pp. 27–30.
- [48] H. Yüksel *et al.*, "A wideband fully integrated software-defined transceiver for FDD and TDD operation," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1274–1285, May 2017.
- [49] N. Codega, P. Rossi, A. Pirola, A. Liscidini, and R. Castello, "A current-mode, low out-of-band noise LTE transmitter with a class-A/B power mixer," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1627–1638, Jul. 2014.
- [50] M. Garampazzi *et al.*, "An intuitive analysis of phase noise fundamental limits suitable for benchmarking LC oscillators," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 635–645, Mar. 2014.
- [51] M. Garampazzi, P. M. Mendes, N. Codega, D. Manstretta, and R. Castello, "Analysis and design of a 195.6 dBc/Hz peak FoM P-N class-B oscillator with transformer-based tail filtering," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1657–1668, Jul. 2015.

- [52] T. Tapen, Z. Boynton, H. Yüksel, A. Apse and A. Molnar, "The impact of LO phase noise in N-path filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 5, pp. 1481–1494, May 2018.
- [53] S. Haykin, *Adaptive Filter Theory*, 3rd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 1996.
- [54] L. Laughlin, M. A. Beach, K. A. Morris, and J. L. Haine, "Electrical balance duplexing for small form factor realization of in-band full duplex," *IEEE Commun. Mag.*, vol. 53, no. 5, pp. 102–110, May 2015.
- [55] C.-K. Luo, P. S. Gudem, and J. F. Buckwalter, "A 0.2–3.6-GHz 10-dBm B1dB 29-dBm IIP3 tunable filter for transmit leakage suppression in SAW-Less 3G/4G FDD receivers," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 10, pp. 3514–3524, Oct. 2015.
- [56] G. Castellano, "SAW-less digitally assisted receivers," Ph.D. dissertation, Dept. Elect. Eng. Technol., Univ. Naples Federico II, Naples, Italy, 2018.
- [57] Y. Lien, E. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "A mixer-first receiver with enhanced selectivity by capacitive positive feedback achieving +39 dBm IIP3 and <3 dB noise figure for SAW-less LTE Radio," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Honolulu, HI, USA, Jun. 2017, pp. 280–283.
- [58] X. Liu *et al.*, "A 65 nm CMOS wideband radio receiver with $\Delta\Sigma$ -based A/D-converting channel-select filters," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1566–1578, Jul. 2016.
- [59] M. Ramella, I. Fabiano, D. Manstretta, and R. Castello, "A 1.7–2.1 GHz +23 dBm TX power compatible blocker tolerant FDD receiver with integrated duplexer in 28 nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Xiamen, China, Nov. 2015, pp. 1–4.



Daniele Montanari (S'16) was born in Pavia, Italy, in 1991. He received the B.S. and M.S. (*summa cum laude*) degrees in electronic engineering from the University of Pavia, Pavia, in 2013 and 2015, respectively, where he is currently pursuing the Ph.D. degree.

His current research interests include radio frequency circuits and systems.



Gerardo Castellano was born in Avellino, Italy in 1988. He received the M.S. degree (Hons.) in electronic engineering and the Ph.D. degree in information technology and electrical engineering from the University of Naples "Federico II," Naples, Italy, in 2014 and 2017, respectively.

Since 2018, he has been a Digital Designer at STMicroelectronics. His current research interests include the analysis and design of mixed-signal systems and real-time signal processing.



Ehsan Kargaran was born in Abarkouh, Iran, in 1984. He received the B.S. and M.Sc. degrees in electronic engineering from the Sadjad University of Technology, Mashhad, Iran, in 2007 and 2011, respectively, and the Ph.D. degree from the University of Pavia, Pavia, Italy, in 2017.

From 2011 to 2014, he was a Lecturer with the Electronic Engineering Department, Sadjad University of Technology. From 2015 to 2016, he was an Intern at Marvell Semiconductor, Pavia. He was also an RF Intern at MediaTek, U.K., where he was

involved in the design of ultra low power (ULP) RX for BTLE in 2017. He is currently a Post-Doctoral Fellow with the University of Pavia. His current research interests include high performance and ULP RF integrated-circuit designs.

Dr. Kargaran was chosen as the Best Student for Research Work by the Dean of the Sadjad University of Technology in 2011.



Giacomo Pini (S'16) was born in Pavia, Italy, in 1990. He received the M.Sc. degree (*cum laude*) in microelectronic engineering from the University of Pavia, Pavia, in 2015, where he is currently pursuing the Ph.D. degree.

His current research interests include base-band filters for broadband wireless receivers.



Saheed Tijani received the B.Eng. degree (First Class Hons.) in electrical and electronics engineering from the Federal University of Technology, Akure, Nigeria, in 2010, and the M.Sc. degree (*summa cum laude*) in electronics engineering and the Ph.D. degree in microelectronics from the University of Pavia, Pavia, Italy, in 2014 and 2017, respectively.

From 2015 to 2016, he was an Intern at Marvell Semiconductor, Pavia, working on the design of Self-interference cancellation techniques for SAW-less transceivers. He is currently a Research Associate

with the Microelectronics Laboratory Group, University of Pavia. His current research interests include RF/analog circuits for wireless communications.



Davide De Caro (M'05–SM'09) received the M.S. degree (Hons.) in electronic engineering and the Ph.D. degree in electronic engineering and computer science from the University of Naples "Federico II," Naples, Italy, in 1999 and 2003, respectively.

He worked in the area of digital integrated very large scale integration circuit design for the last 19 years. Since 2014, he has been an Associate Professor with the Department of Electrical Engineering and Information Technology, University of Naples "Federico II." He has authored over 80 technical papers.



Antonio Giuseppe Maria Strollo (M'05–SM'06) received the M.S. (*cum laude*) and Ph.D. degrees in electronic engineering from the University of Napoli Federico II, Naples, Italy, in 1988 and 1992, respectively.

Since 2002, he has been a Full Professor with the University of Napoli Federico II, where he was the Head of the Department of Electronic and Telecommunication Engineering from 2005 to 2008.

He has authored or co-authored over 130 papers in international journals and refereed conferences. His

research interests included power electronics. His current research interests include the design and analysis of VLSI circuits. In this field, he is working on high-performance arithmetic circuits, all-digital techniques for clock synthesis in digital ASICs, and approximate circuits for energy-efficient digital systems.

Dr. Strollo was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-Ifrom 2009 to 2012. He is currently an Associate Editor of the *Integration*, the VLSI Journal.



Danilo Manstretta (M'03) received the Laurea (*summa cum laude*) and Ph.D. degrees in electrical engineering and computer science from the University of Pavia, Pavia, Italy, in 1998 and 2002, respectively.

From 2001 to 2003, he was a Technical Staff Member of Agere Systems, working on WLAN transceivers and linear power amplifiers for base stations. From 2003 to 2005, he was with Broadcom Corporation, Irvine, CA, USA, working on RF tuners for TV applications. In 2005, he joined the

University of Pavia as an Assistant Professor and was granted tenure in 2008. His current research interests include analog, RF, and millimeter-wave-integrated circuit designs.

Dr. Manstretta has been a member of the Technical Program Committee of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium since 2006 and of the Steering Committee for the same conference since 2017. He was a co-recipient of the 2003 IEEE JOURNAL OF SOLID-STATE CIRCUITS Best Paper Award. He was a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS 2017 Special Section dedicated to the 2016 RFIC Symposium and a Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES 2018 Mini Special Issue dedicated to the 2017 RFIC Symposium.



Rinaldo Castello (S'78–M'78–SM'92–F'99) received the bachelor's degree (*summa cum laude*) from the University of Genova, Genova, Italy, in 1977, and the M.S. and Ph.D. degrees from the University of California, Berkeley, Berkeley, CA, USA, in 1981 and 1984, respectively.

From 1983 to 19'85, he was a Visiting Assistant Professor at the University of California, Berkeley. In 1987, he joined the University of Pavia, Pavia, Italy, where he is currently a Full Professor. He was a Consultant for ST-Microelectronics, Milan, Italy,

till 2005. In 1998, he started a joint research centre between the University of Pavia and ST, where he was the Scientific Director till 2005. He promoted the establishing of several design centre from multinational IC companies around Pavia, among them he was a Consultant for Marvell from 2005 to 2016. He is currently a Consultant for InvenSense.

Dr. Castello has been a member of the TPC of the European Solid State Circuit Conference (ESSCIRC) since 1987 and of the International Solid State Circuit Conference (ISSCC) from 1992 to 1904. He was a co-recipient of the Best Paper Award at the 2005 Symposium on VLSI of the Best Invited Paper Award at the 2011 CICC and of the Best Evening Panel Award at ISSCC 2012 and 2015. He was the Technical Chairman of the ESSCIRC 1991 and the General Chairman of the ESSCIRC 20'02. He was an Associate Editor of the Europe of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 1994 to 1996 and a Guest Editor of the Europe of the IEEE JOURNAL OF SOLID-STATE CIRCUITS July 1992 special issue. From 2000 to 2007, he has been a Distinguished Lecturer of the IEEE Solid State Circuit Society. He was named one of the outstanding contributors for the first 50 and 60 years of ISSCC. He was one of the two European representatives at the Plenary Distinguished Panel of ISSCC 2013 and the Summer 2014 Issue of the *IEEE Solid State Circuit Magazine* was devoted to him.