Analysis and Design of a 20-MHz Bandwidth, 50.5-dBm OOB-IIP3, and 5.4-mW TIA for SAW-Less Receivers

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***Abstract*— A power-efficient transimpedance amplifier with wide channel bandwidth is proposed to meet the stringent linearity requirements of surface acoustic wave-less frequency-division duplexing receivers. A unity-gain loop bandwidth of 1.6 GHz is achieved with low-power dissipation. This was done without using any internal compensation but relying on zeros, both within the operational transconductance amplifier and in the feedback network, to ensure stability across all parameter variations. A simple non-linear analysis methodology is presented that provides important insights, useful for the design optimization. The prototype, implemented in 28-nm CMOS technology, has 14 dB of gain with 20-MHz bandwidth and achieves 21.1-μV in-band noise together with 33 and 50.5-dBm IIP3 at 6 and 100-MHz offset, respectively, while requiring only 5.4 mW. The corresponding filter figure of merit (FOM) of 183.2 dBJ^{-1} at 100-MHz offset exceeds that of all previous designs. Simulation shows that an even better FOM could be achieved using a larger width (more linear) feedback resistor. Finally, the differential input impedance is less than 33 Ω at all frequencies.**

***Index Terms*— Baseband, frequency-division duplexing (FDD), high linearity, low power, mobile receivers, surface acoustic wave (SAW)-less, transimpedance amplifier (TIA).**

I. Introduction

NEWER communication standards for both cellular and Wi-Fi applications use wider channel bandwidths. At the same time, the attempt to reduce cost by removing some off-chip filters and the need to co-exist with other transceivers on the same board increases the required linearity of the receiver. In either frequency-division duplexing (FDD) or full-duplex (FD) systems, the use of self-interference cancellation techniques can significantly reduce the required linearity [1]–[4]. Nonetheless, residual interference is still larger when using highly selective off-chip filters. Whereas both the IIP3 and compression of the receiver front-end have been extensively studied [5], less attention was given to the baseband (BB) portion. For the universally used current-mode receiver architecture [6], the first block after the passive mixer is either a filtering transimpedance amplifier (TIA) or a higher order filter [6]–[11]. In both cases, very stringent requirements are placed on this circuit. For FDD, it needs to have high out-of-band (OOB) linearity and low input impedance up to very large offset frequencies, while for FD, high in-band (IB) linearity and wide bandwidth are needed. In both cases, low-integrated IB noise and small area with the smallest possible power consumption are desired. Placing a very large capacitor (hundreds of picofarad) on the virtual ground node helps with some of these issues, but it increases area and integrated noise. In the literature, many continuous-time filters with the bandwidth of up to tens of megahertz are presented [12]–[19]. Although some have good dynamic range (DR) [15], they do not always address all the specs of a BB channel filter, e.g., low input impedance. In [20] and [21], a receiver BB TIA is enhanced by placing a negative resistance in parallel with its input nodes. In [21], this is exploited to significantly improve the IB IIP3, but with small benefits on the OOB IIP3 and at the cost of extra noise and power consumption. Lower noise is achieved in a TIA [13] that uses a smaller input capacitance by boosting its value for OOB signals. Furthermore, a second-order filtering is implemented which is beneficial for the following stages, however, its relatively high input impedance may degrade the mixer linearity. These limitations could be overcome if the TIA/filter was able to achieve high IB IIP3 and to maintain both low input impedance and high IIP3 up to high frequencies. Many active-*RC* filters for channel-selection use a simple two-stage operational transconductance amplifier (OTA) with Miller compensation [11], [12], [16], [22], which suffers from a low-gain-bandwidth product when loaded with a large capacitor. In [23], a filtering TIA based on a three-stage OTA showing high gain over a large bandwidth and enabling good virtual ground and high linearity was presented. This was achieved using a non-classical approach to compensation. No Miller capacitors were used but stability was ensured thanks to some additional zero's introduced within both the forward and feedback portions of the loop. In this paper, an OTA non-linearity modeling is proposed, which is then applied to the analysis of the TIA. An extended design section is presented, including a detailed stability analysis. This paper is organized as follows. After this introduction, the key target specifications of the TIA are derived in Section II. Section III describes the design of the uncompensated three-stage OTA. The model used to analyze the non-linearities of the TIA is introduced in Section IV.

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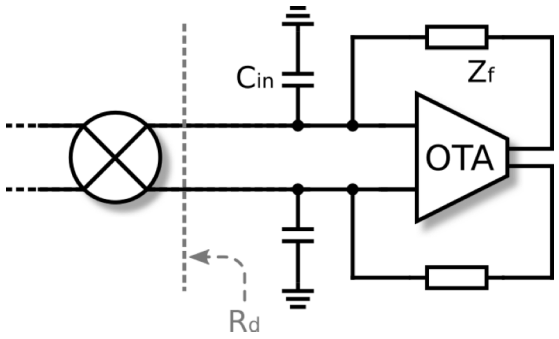

Fig. 1. Typical TIA with big input capacitance.

The design of the uncompensated three-stage OTA is given in Section IV and experimental results on the TIA prototype is given in Section V, with also some insights on a self-interference cancellation receiver the TIA was included in. Some conclusions are drawn in Section VI.

II. TIA Target Specifications

When a TIA is driven by a passive current-switching mixer, a big capacitor C_{in} is always placed at its input nodes [8], [10], [11] (Fig. 1). This serves several purposes: 1) it shunts the signal at the clock harmonics; 2) it maintains low input impedance across frequency to preserve both mixers IIP2 and IIP3 with strong OOB interferers [24]; and 3) it filters the higher frequency down-converted interferers, improving TIA OOB IIP3. To fulfill all these requirements, increasing the value of C_{in} is beneficial and typically C_{in} is of the order of 200 pF [8], [10]. A large C_{in} has, however, the drawback of increasing both area and noise. In fact, the noise transfer function (NTF) of the OTA input-referred (IR) noise voltage is proportional to $|1 + Z_F/Z_{\text{in}}|^2$, where Z_F is the feedback impedance and Z_{in} is the virtual ground impedance, i.e., the parallel of C_{in} and the driving impedance R_d. Hence, C_{in} creates a zero in the OTA NTF at $1/(R_d C_{\text{in}})$ and if this falls within the signal bandwidth, the integrated noise degrades. For example, assuming $R_d = 500\ \Omega$ [25], [26] and that the filter bandwidth ω_0 is 15 MHz, a 20 pF C_{in} produces an NTF zero at ω_0 and 1.2 dB increase in the integrated OTA noise. Beyond this value, however, the integrated noise increases with the square of C_{in}, quickly becoming unacceptable. We, therefore, need to find an optimum value for C_{in}. With respect to point 1 above, we see that the impedance of a 20 pF C_{in} is significantly smaller than the switches on-resistance R_{ON} (typically about 20 Ω) even at the lowest possible harmonic of the local oscillator (LO). Therefore, from this point of view, we have no reason to increase C_{in} beyond 20 pF. With respect to point 2 above, we need to ensure that the TIA input impedance Z_{in} remains below R_{ON} up to the highest blocker frequency (e.g., 400 MHz for long term evolution (LTE) in FDD). Z_{in} is the parallel of C_{in} and the TIA impedance at its virtual ground Z_{VG}. Since 20 pF correspond to 20 Ω at 400 MHz, a much higher C_{in} or a very broadband OTA is required to satisfy the above requirement at all frequencies. In this paper, we target a sufficiently wideband OTA to achieve low Z_{in} at all frequencies with a C_{in} of 20 pF, to avoid noise penalties. With respect to point 3 above, if the impedance of C_{in} is lower than Z_{VG} at the blocker frequency, only a fraction of the blocker current is absorbed by the OTA. On the other hand, with a C_{in} of 20 pF, all the blockers are absorbed by the OTA, making OTA IIP3 much more critical. To design a highly linear OTA, we need a model of the distortion associated with its different stages.

TABLE I
OTA Design Parameters

Parameter	Value
M1,M2	140/0,08
Mc1, Mc2	20/0,04
Mc3, Mc4	8/0,04
M3, M4	20/0,2
M5,M6	20/0,06
M7,M8, M9, M10	2/0,08
M11, M12	6/0,08
MPo+, MPo-	36/0,08
MNo+, MNo-	16/0,08
M13, M14	12/0,08
C_c	300 fF
R_c	500 Ω
R_{deg}	250 Ω
R_z	1 kΩ
C_z	100 fF

III. OTA Design

In order to extend OTA bandwidth and achieve low TIA input impedance over a broad bandwidth with 20 pF C_{in}, an unconventional approach was adopted to ensure loop stability. In traditional general-purpose OTA design, where purely capacitive load is assumed, Miller compensation schemes are often used. Miller capacitors create one dominant pole in the OTA transfer function and push nondominant poles above the unity gain bandwidth (GBW), increasing phase margin and guaranteeing OTA stability. In the design of BB TIAs such approach has the main drawback of producing a low-frequency pole, limiting OTA bandwidth and making TIA input impedance increase. In fact, the GBW is limited to about one half of the nondominant pole, which is given by the ratio between the last stage transconductance and the effective load capacitance C_{in}. To gain a quantitative insight, targeting a GBW of 1.6 GHz with a 20-pF load capacitance would require an unpractically high transconductance of 400 mS. In our solution no Miller capacitors are used. Stability is instead achieved by placing some additional zeros in the TIA loop gain, both in OTA and feedback network transfer functions, close to GBW to improve phase margin. This approach allows achieving much wider OTA bandwidth than a Miller compensation. In the following, a detailed OTA description is provided. The OTA architecture is given in Fig. 2 and design parameters are given in Table I. The first stage consists of a PMOS Telescopic-Cascode, with R_c and C_c providing an output impedance $Z_{O,1} = r_{\text{out},1}//(1/j\omega C_{L,1})//(1 + j\omega R_c C_c)/j\omega C_c(1 + G_{m,L} R_c)$, where $r_{\text{out},1}$ is the output resistance at low frequency, $C_{L,1}$ is the output capacitance, and $G_{m,L}$ is the equivalent transconductance of the load transistors M3/4 degenerated by R_{deg}. The third term is associated with R_c and C_c and corresponds to the series combination

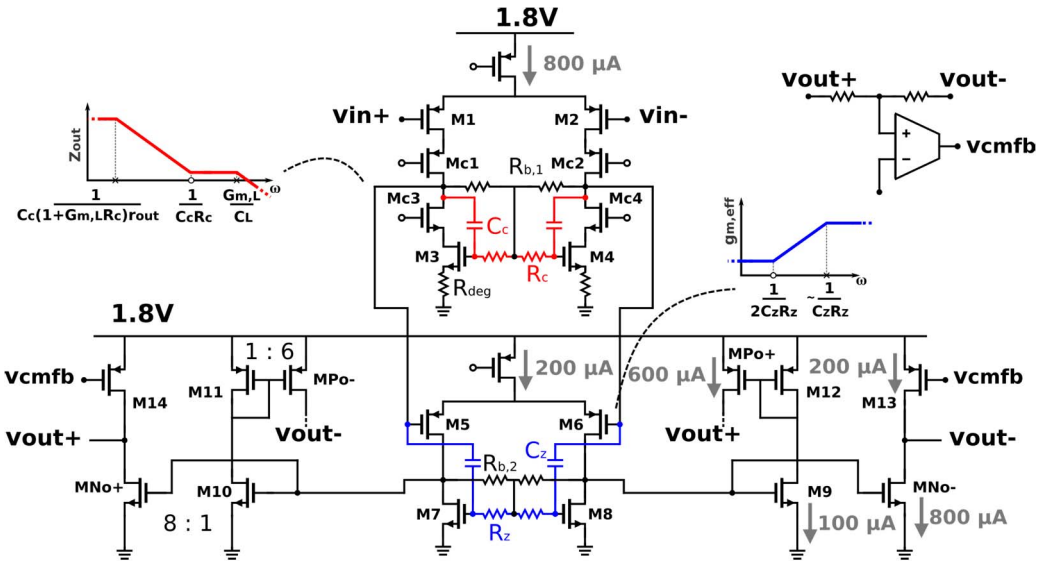

Fig. 2. Schematic of the proposed OTA.

of capacitance $C_c(1 + G_{m,L}R_c)$ and resistance $R_c/(1 + G_{m,L}R_c)$.$Z_{o,1}(\omega)$ has a low-frequency pole $\omega_{p,OTA,1} = 1/C_c(1+G_{m,L}R_c)\cdot r_{out,1}$ and a high-frequency zero $\omega_{z,OTA,1} = 1/(R_cC_c)$ that is placed before the TIA GBW to improve phase margin. At very high-frequency, $C_{L,1}$ produces a second pole $\omega_{p,OTA,2} \approx G_{m,L}/C_{L,1}$. The common-mode (CM) output voltage is set by the local feedback made, at low frequency, by $R_{b,1}$ and, at high frequency, by C_c. The second stage is a PMOS differential pair, with the boosting network R_z, C_z which produces a zero-pole doublet $\omega_{z,OTA,2} = 1/(R_zC_z(1 + g_{m,7/8}/g_{m,5/6}))$ and $\omega_{p,OTA,3} = 1/(R_zC_z)$. This is because above $\omega_{p,OTA,3}$, capacitance C_z shorts the gate of $M_{5/6}$ and $M_{7/8}$ approximately doubling the stage g_m. In addition, there is a pole $\omega_{p,OTA,4} = 1/r_{o,2}C_{L,2}$, where $r_{o,2}$ and $C_{L,2}$ are the resistance and capacitance at the output which is, however, cancelled placing $\omega_{z,OTA,2}$ on top of it. In this way the stage shows a single pole at $\omega_{p,OTA,3}$. The CM voltage of the second stage and the dc current in the output stage are set through $R_{b,2}$. The output stage is based on a crossed current mirror where the nMOS transistors ($M_{O,N+/-}$) are driven directly while the pMOS ($M_{O,P+/-}$) are driven through the mirror made of M9/10 and M11/M12. In this design, the output stage was enlarged compared with what would be required in normal operation, to directly drive the big off-chip capacitance (C_L), without using a buffer. The output CM is set to 900 mV with a CM feedback loop that controls the P-side current in the output branches (transistors M13/M14) via a resistor divider and a simple OTA.

A. TIA Stability

The complete TIA is reported in Fig. 3(a). Even if it was implemented in differential form, single-ended representation of the TIA is used here for simplicity. C_L represents the testing probe input capacitance, which is about 2 pF (differential) and is represented here as a single-ended 4-pF capacitance. In a real receiver, the actual load seen by the TIA would be drastically smaller, i.e., below 100 fF. A smaller load results in a better linearity for the same OTA since the output stage needs to deliver less current. This means that the measured IIP3 is smaller than the one achievable in the real receiver. Through simulation 6 dB improvement in OOB IIP3 was demonstrated with 100-fF load capacitance. R_{in} in series with C_{in} and R_L in series with C_L are added to improve stability, as discussed below. However, to filter out clock harmonics, the input signal is injected below R_{in}. The loop gain is computed breaking the loop at the input of the OTA, injecting a test signal v_t and observing the return signal v_r, as shown in Fig. 3(b). The singularities of the OTA first and second stage were derived previously and the simulated transfer functions of these stages are reported in Fig. 4(a), where poles and zeros were highlighted for clarity. The high-frequency zero of the first stage $\omega_{z,OTA,1}$ is placed before the second stage pole $\omega_{p,OTA,3}$ to improve phase margin. Poles and zeros introduced by third stage and feedback network are listed below assuming R_L and R_{in} are much smaller than all other resistances and $C_{in} \gg C_F, C_L$. In Fig. 4(b), the simulated transfer function of the output stage and passive feedback network, i.e., $v_r/v_{o,2}$ in Fig. 3(b), is reported. A low-frequency pole is produced by C_{in} at frequency $\omega_{p,4} = 1/(R_d//(R_F + r_o)C_{in})$, R_{in} gives a high-frequency zero at

TABLE II
TIA DESIGN PARAMETERS

Parameter	Value
R_d	500 Ω
C_{in}	20 pF
R_{in}	13 Ω
C_F	3 pF
R_F	2.5 kΩ
C_L	4 pF
R_L	50 Ω

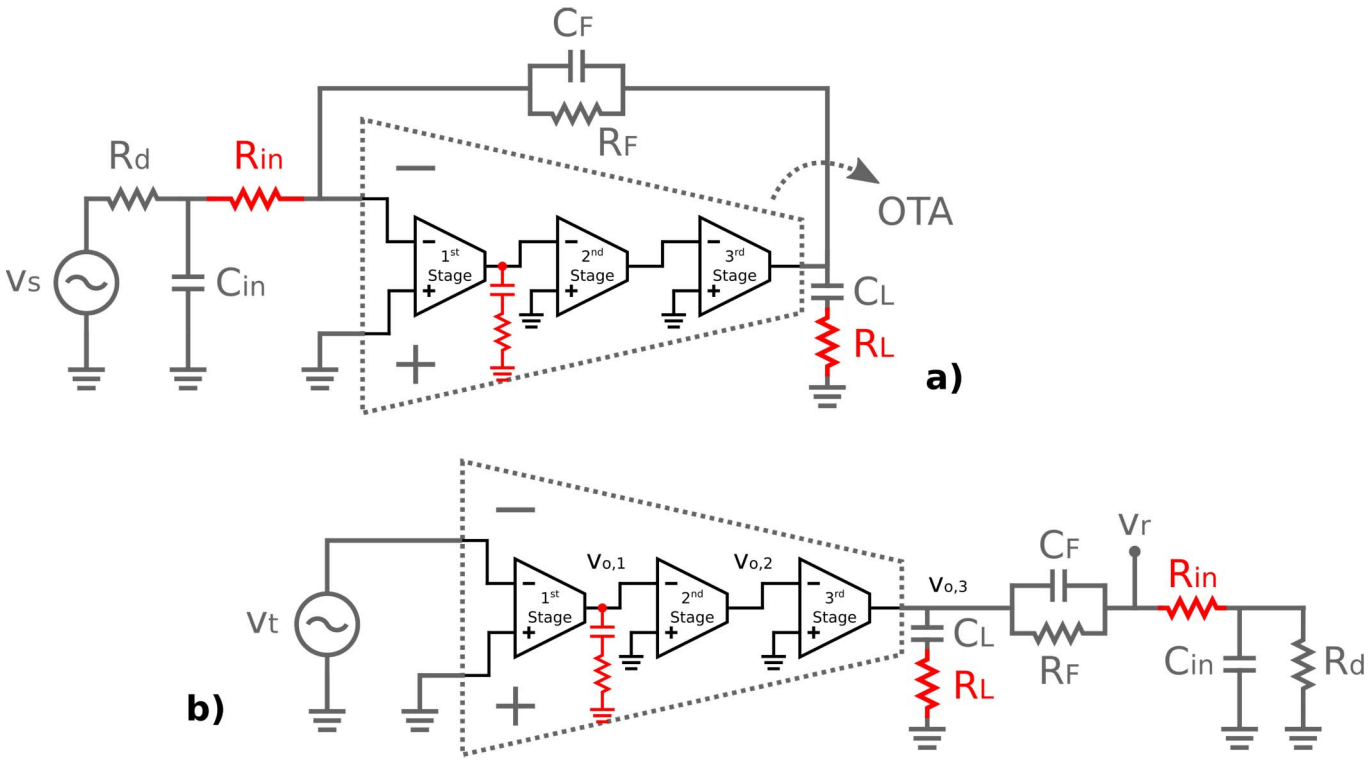

Fig. 3. (a) Simplified single-ended representation of the proposed TIA Architecture. (b) Open-loop circuit used to compute the loop gain.

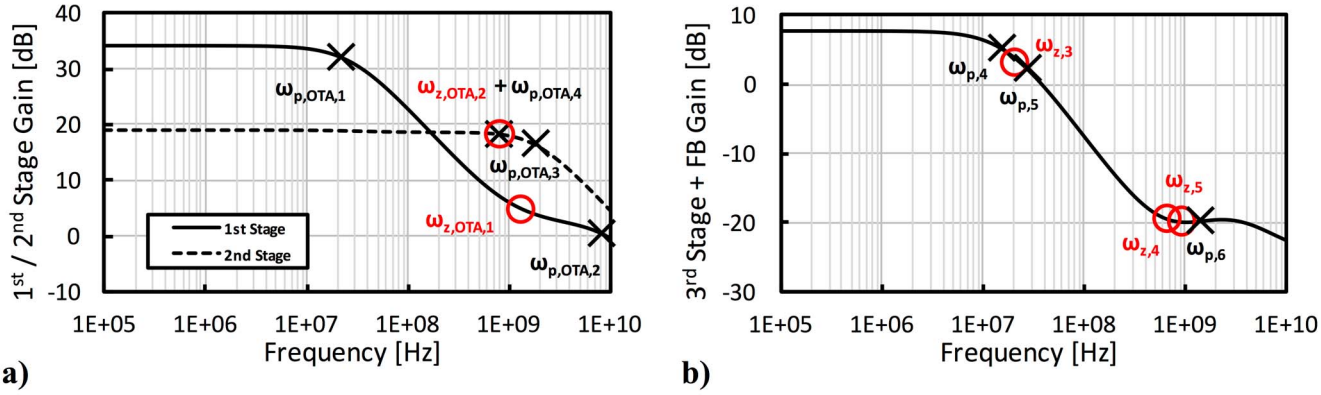

Fig. 4. (a) Gain of 1st (solid line) and 2nd (dashed line) stages. (b) Gain of 3rd stage and passive feedback network.

$\omega_{z,4} = 1/R_{\text{in}}C_{\text{in}}$, which is placed before the GBW. This is key to ensure stability, given the two low-frequency poles ($\omega_{p,\text{OTA},1}$, $\omega_{p,4}$). Feedback components create a zero at $\omega_{z,3} = 1/R_F C_F$ and a pole at $\omega_{p,5} = 1/(R_f//r_o)(C_F + C_L)$, near the cutoff frequency. The large external load capacitance C_L significantly reduces $\omega_{p,5}$. Increased OTA bandwidth could be achieved using an on-chip buffer or additional filtering stage as load. R_L creates a high-frequency zero-pole doublet at $\omega_{z,5} = 1/(R_L C_L)$ and $\omega_{p,6} = (C_F + C_L)/(C_F C_L(R_{\text{in}} + R_L))$. For the components given in Table II, the post-layout simulated magnitude and phase of the loop transfer function are shown in Fig. 5 (black curve). The loop has a gain of nearly 60 dB at dc which remains flat up to the feedback pole $\omega_{p,4}$, located around 18 MHz. Next, we find the first stage pole $\omega_{p,\text{OTA},1}$, at 20 MHz, followed by the zero-pole pair $\omega_{z,3}$–$\omega_{p,5}$, near 20 and 32 MHz, respectively. Beyond 32 MHz, the curve starts decreasing with a slope of 40 dB/decade. Above $\omega_{z,4}$, located at 670 MHz, 20 dB/decade slope is resumed. Since $\omega_{z,\text{OTA},1}$ (at about 1.1 GHz) is very close to $\omega_{p,\text{OTA},3}$ the plot crosses the 0-dB axis with slightly less than 20-dB/decade slope at 1.5-GHz GBW, in the vicinity of the zero-pole doublet given by R_L and C_L ($\omega_{z,5}$ and $\omega_{p,6}$). At GBW the phase is close to its maximum, giving 57° of phase margin. TIA stability was simulated over all process corners and for different operating temperatures, including passive components variations. Singularity position is affected by the MOM capacitors and poly-silicon resistors used in the feedback network and within the OTA. Having such passives, low temperature coefficients (few hundreds parts per million per degree Centigrade), PM and GBW are stable across temperature as shown

TABLE III
TIA CORNER STABILITY

Corner	TT			FF			SS			FS			SF		
Temperature [°C]	-50	25	100	-50	25	100	-50	25	100	-50	25	100	-50	25	100
GBW [GHz]	1.55	1.53	1.5	1.17	1.09	1.03	2.01	1.98	1.9	1.31	1.28	1.27	1.94	1.85	1.76
PM [deg]	58.1	57.6	57.6	50	52	54.5	45.3	42.5	41.3	59.3	60.5	61.6	51.5	51	51.5

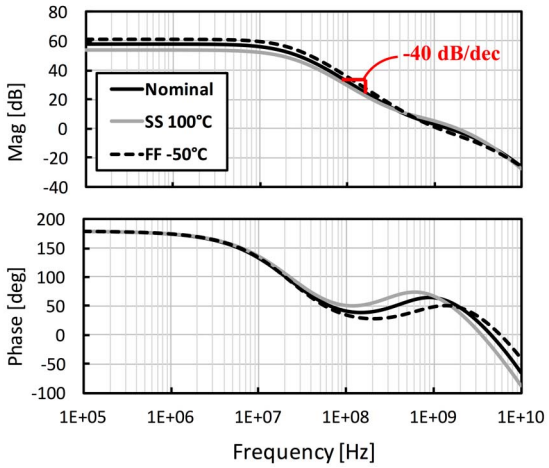

Fig. 5. Loop gain magnitude and phase on nominal corner (black line), SS corner at 100 ° C (gray Line) and fast–fast corner at −50 °C (dashed Line).

TABLE IV
MODEL COEFFICIENTS FOR THE PROPOSED OTA

Stage	Coefficient	Value
1st	$(3/4) \times g_{mNL3.1}$	$3{,}22 \times 10^{-2}$ A/V^3
	$(3/4) \times g_{dsNL3,1}$	$3{,}58 \times 10^{-6}$ A/V^3
	$Z_{o,OL,1}$(1 MHz)	16,4 kΩ
	$TF_{1\rightarrow OUT}$(1 MHz)	41,1 dB
2nd	$(3/4) \times g_{mNL3,2}$	$9{,}32 \times 10^{-3}$ A/V^3
	$(3/4) \times g_{dsNL3,2}$	$-7{,}11 \times 10^{-6}$ A/V^3
	$Z_{o,OL,2}$(1 MHz)	10,4 kΩ
	$TF_{2\rightarrow OUT}$(1 MHz)	22 dB
3rd	$(3/4) \times g_{mNL3,3}$	$1{,}19 \times 10^{-3}$ A/V^3
	$(3/4) \times g_{dsNL3,3}$	$2{,}32 \times 10^{-5}$ A/V^3
	$Z_{o,OL,3}$(1 MHz)	2,1 kΩ
	$TF_{3\rightarrow OUT}$(1 MHz)	0 dB
	G_{LOOP}(1 MHz)	61,4 dB

in Table III, reporting simulated PM and GBW over all process corners and for different temperatures. Fig. 5 shows the phase and magnitude response of the loop for extreme values of temperature and process demonstrating stability robustness. The most critical corner is slow–slow (SS) where salicided poly-silicon resistor R_{in} strong variations lower $\omega_{z,4}$, increasing GBW to give 42° of PM. Montecarlo simulation over 500 samples defines the effect of the mismatch. A standard deviation of 176 MHz in GBW and of 2.5° PM is obtained. From the point of view of the mixer load, we see that the virtual ground impedance stays below the switches Ron up to 400 MHz as required since the OTA gain is higher than 30 dB up to such a frequency. The only open point is the linearity of the TIA itself in the band of interest (i.e., up to 400 MHz) when 20 pF are used at its input.

IV. NON-LINEARITY ANALYSIS

This section presents the non-linearity analysis of the proposed TIA. We introduce a relatively simple model of the closed-loop OTA 3rd order intermodulation (IM3), which is the critical spec in a receiver. The 2nd order intermodulation is neglected, assuming a differential structure for the OTA. The model provides three key pieces of information versus tone frequencies and IM3 frequency (f_{IM3}):1) the total closed-loop intermodulation; 2) the stages that dominate distortion in a frequency range; and 3) the mechanism that dominates distortion within a stage. Two key concepts are identified: distortion injection and distortion compression. The former represents the distortion a stage injects in the circuit, which depends on the voltage swing at the intermediate nodes at the frequency of the input tones. The latter, quantifies by how much the distortion is reduced by the loop, which depends on the loop gain at the IM3 frequency. The approach is based on the one proposed in [27]–[30], where the linearized circuit response is used to extract the non-linear terms injected at the various nodes, which are then referred to the output. A single-ended representation of the loop for a three-stage-OTA with no internal feedbacks[1] is given in Fig. 6. Each OTA stage is modeled as a transconductor ($g_{m,i}$), loaded by $Z_{o,i}$, which includes both output resistance and capacitance. To simplify the analysis, the non-linearity is modeled at the OTA stage level, as opposed to the transistor level as in [27]–[29]. Furthermore, only two distortion terms are considered, the first due to the transconductance $g_{m\text{NL3},i}$ and the second due to the output conductance $g_{\text{dsNL3},i}$. The procedure to get the output intermodulation is represented by the flowchart of Fig. 7 and will be applied to the OTA in Fig. 2. Some parameters must be first computed for each stage by either simulation or computation. In Step 1.a, the non-linear coefficients $g_{m\text{NL3},i}$ and $g_{\text{dsNL3},i}$ are found simulating each stage separately, as described in the Appendix, giving the results reported in Table IV.[2] In Step 1.b, the closed-loop swing

[1]The same methodology can be easily applied to other common OTA topologies.

[2]In multi-stage and feedback amplifiers, 2nd order non-linearities coming from two stages may interact, resulting into 3rd order non-linearity. In this design, however, since the first two stages are fully differential, at least up to very high frequencies, this effect is negligible.

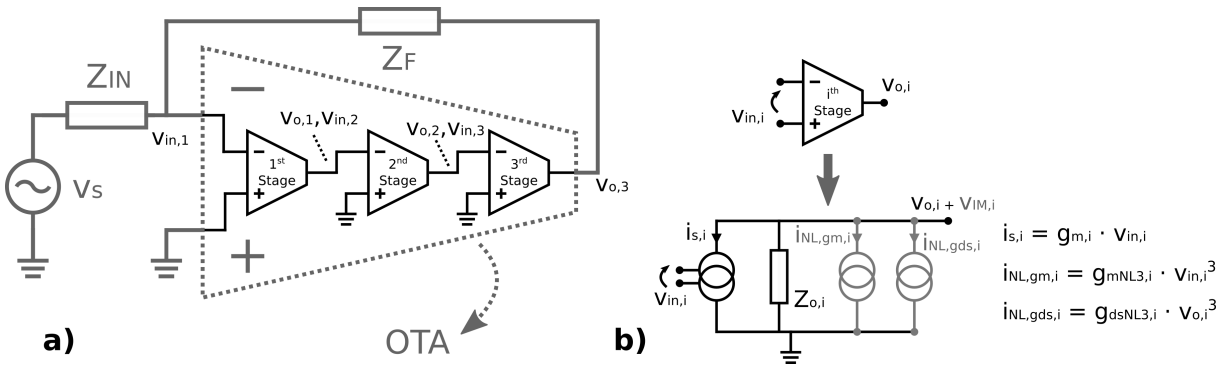

Fig. 6. Simplified single-ended representation of the proposed model. (a) Overall loop. (b) Single OTA stage.

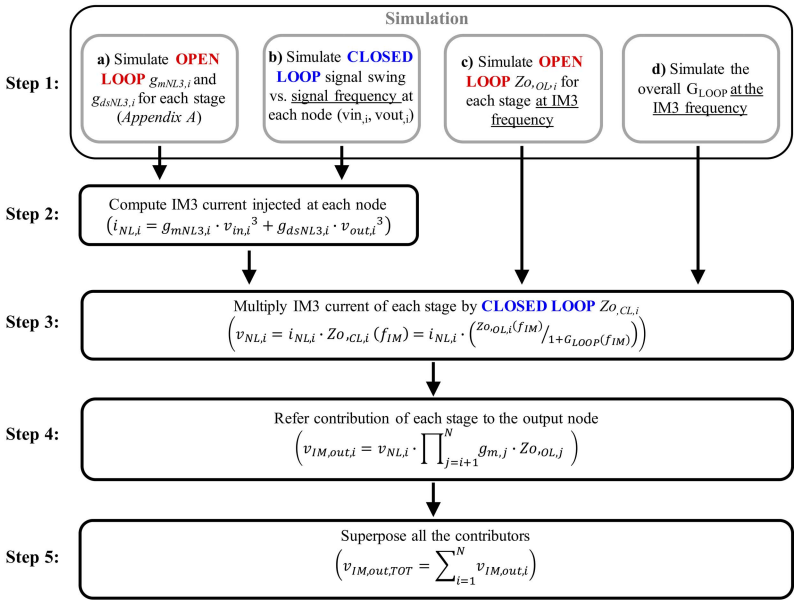

Fig. 7. Schematic representation of the adopted procedure for computation of output intermodulation of an OTA closed in feedback loop.

versus frequency at the input and output of each stage is obtained. Finally, the closed-loop output impedance $Z_{o,\mathrm{CL},i}$, at the IM3 frequency (f_{IM3}) is computed by dividing the open-loop output impedance $Z_{o,\mathrm{OL},i}$ by the loop gain.[3] The output intermodulation contributed by each stage is computed in Steps 2 to 5. In Step 2, the intermodulation injection is found. Applying two sinusoids of amplitude $A_{1,i}$ and $A_{2,i}$ and frequency ω_1 and ω_2, the two IM3 components in the ith stage output current are located at $2\omega_1$–ω_2 and have strengths that depend on the signal amplitude at the input and output of the ith stage as given in the following:

$$i_{\mathrm{gm},i}^{\mathrm{NL}} = \frac{3}{4} g_{m\mathrm{NL3},i} A_{1,i}^2 A_{2,i} \sin((2\omega_1 - \omega_2)t) \quad (1)$$

$$i_{\mathrm{gds},i}^{\mathrm{NL}} = \frac{3}{4} g_{\mathrm{dsNL3},i} (A_{1,i} \cdot |G_i(\omega_1)|)^2 \cdot (A_{2,i} \cdot |G_i(\omega_2)|) \times \sin((2\omega_1 - \omega_2)t + 2\angle G_i(\omega_1) - \angle G_i(\omega_2)) \quad (2)$$

where $G_i(\omega_k)$ is the gain of the stage at frequency ω_k and $g_{m\mathrm{NL3},i}$ and $g_{\mathrm{dsNL3},i}$ are the third-order non-linear coefficients associated with g_m and g_{ds}. In Step 3, the IM3 voltage ($v_{\mathrm{IM},i}$) at the output of each stage is found by multiplying the total injected current $i_{,\mathrm{NL,gm},i} + i_{,\mathrm{NL,gds},i}$ by the closed-loop output impedance $Z_{o,\mathrm{CL},i}$ at f_{IM3}, as given in (3). In (3), we add the two non-linear terms, without considering their relative phase, assuming that one term dominates in each frequency interval. In Step 4, all $v_{\mathrm{IM},i}$ are referred to the output by multiplying them by $\mathrm{TF}_{i\to\mathrm{out}}$, i.e., the open-loop transfer function from the ith stage output to the OTA output. $\mathrm{TF}_{i\to\mathrm{out}}$ is equal to the product of $g_{m,j} \times Z_{o,\mathrm{OL},j}$ at the IM3 frequency for all stages following ith stage, as given in (4). In Step 5, all output-referred terms are summed as in (5)

$$v_{\mathrm{IM},i} \cong \left(\frac{3}{4} g_{m\mathrm{NL3},i} A_{1,i}^2 A_{2,i} + \frac{3}{4} g_{\mathrm{dsNL3},i} (A_{1,i} \cdot |G_i(\omega_1)|)^2 \cdot (A_{2,i} \cdot |G_i(\omega_2)|)\right) \cdot \frac{|Z_{o,\mathrm{OL},i}(2\omega_1 - \omega_2)|}{|1 + G_{\mathrm{LOOP}}(2\omega_1 - \omega_2)|} \cdot \sin((2\omega_1 - \omega_2)t) \quad (3)$$

[3]Notice that $Z_{o,\mathrm{OL},3}$ also includes the loading of the feedback network.

$$v_{\mathrm{IM,out},i} = v_{\mathrm{IM},i} \cdot \mathrm{TF}_{i\to\mathrm{OUT}} = v_{\mathrm{IM},i} \cdot \prod_{j=i+1}^{N} g_{m,j} \cdot Z_{o,\mathrm{OL},j} \quad (4)$$

$$v_{\mathrm{IM,out,TOT}} = \sum_{i=1}^{N} v_{\mathrm{IM,out},i}. \quad (5)$$

Fig. 8 shows IM3 versus the first tone frequency for two −20 dBm input signals when the IM3 falls at 1 MHz. The difference between calculations and simulations is typically around 1 dB and always below 4 dB. Fig. 8 shows also the calculated IM3 of each stage. We see the following.

1) The last stage dominates distortion up to 400 MHz.
2) Beyond this the first stage dominates.
3) When the first stage starts to dominate, the overall IM3 starts to decrease with frequency.
4) The second stage never dominates distortion.

This behavior can be intuitively understood as follows. For the last stage, whose $v_{\mathrm{IM,out},3}$ is given in (6), the injected distortion depends only on the output stage itself and not on any other OTA characteristic. This is because both the swing and the current at the output node are set only by the feedback network and the load impedance. The output distortion $v_{\mathrm{IM,out},3}$ is obtained by multiplying the injected distortion by the closed-loop output impedance at f_{IM3}

$$v_{\mathrm{IM,out},3} = \left(i^{\mathrm{NL}}_{\mathrm{gm},3} + i^{\mathrm{NL}}_{gds,3}\right) \cdot \frac{Z_{o,\mathrm{OL},3}(f_{\mathrm{IM}})}{1+G_{\mathrm{LOOP}}(f_{\mathrm{IM}})} \cong \left(i^{\mathrm{NL}}_{\mathrm{gm},3} + i^{\mathrm{NL}}_{gds,3}\right) \cdot \frac{1 + Z_F/Z_{\mathrm{in}}}{g_{m,3} \cdot g_{m,1} Z_{o,\mathrm{OL},1}(f_{\mathrm{IM}}) \cdot g_{m,2} Z_{o,\mathrm{OL},2}(f_{\mathrm{IM}})}. \quad (6)$$

We conclude that to improve the closed-loop intermodulation distortion of the output stage, it is the key to enhance the gain of the OTA at the IM3 frequency, i.e., up to TIA cutoff frequency ω_0 since intermodulation is increasing the noise floor when it falls within the signal bandwidth. Since the second stage has a broadband gain of about 20 dB, the swing at its input stays low and constant with frequency, making its distortion always negligible compared to that of the last stage.[4] The first stage distortion is given by

$$v_{\mathrm{IM,out},1} = \left(i^{\mathrm{NL}}_{\mathrm{gm},1} + i^{\mathrm{NL}}_{gds,1}\right) \cdot \frac{Z_{o,\mathrm{OL},1}(f_{IM}) \cdot g_{m,2} Z_{o,\mathrm{OL},2}(f_{IM}) \cdot g_{m,3} Z_{o,\mathrm{OL},3}(f_{\mathrm{IM}})}{1+G_{\mathrm{LOOP}}(f_{\mathrm{IM}})} \cong \left(i^{\mathrm{NL}}_{\mathrm{gm},1} + i^{\mathrm{NL}}_{gds,1}\right) \cdot \frac{1}{g_{m,1}} \cdot \left(1+\frac{Z_F}{Z_{\mathrm{IN}}}\right). \quad (7)$$

The first stage distortion starts from a very small value and rises beyond the first OTA pole at 20 MHz with a 60-dB/decade slope since, as the gain $A(\omega_{1,2})$ drops, the virtual ground signal increases as $1/A(\omega_{1,2})$ and the distortion increases as $1/(A^2(\omega_1)A(\omega_2))$. Since OTA gain at 400 MHz is still 30 dB, OTA input swing stays small enough to prevent excessive distortion injection in this range. The situation is the dual of the output stage. For a given input stage, distortion

[4]This applies directly to g_m nonlinearity. From the data in Table IV it can be observed that, with a gain of about 10, the second stage g_{ds} nonlinearity is of the same order of magnitude of its g_m nonlinearity. Hence, g_{ds} nonlinearity is also always negligible.

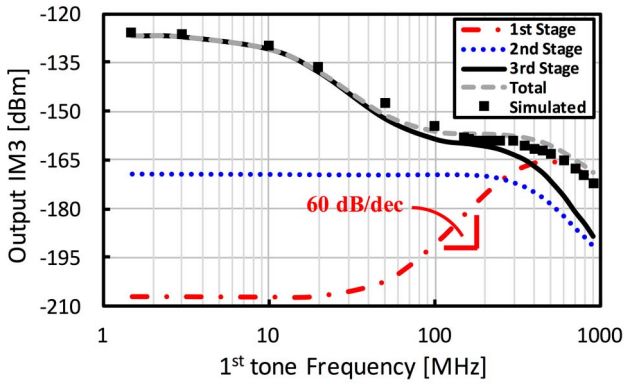

Fig. 8. Simulated and computed IM3 at the TIA output as a function of the input tones frequency, with the proposed OTA and contribution of single OTA stages.

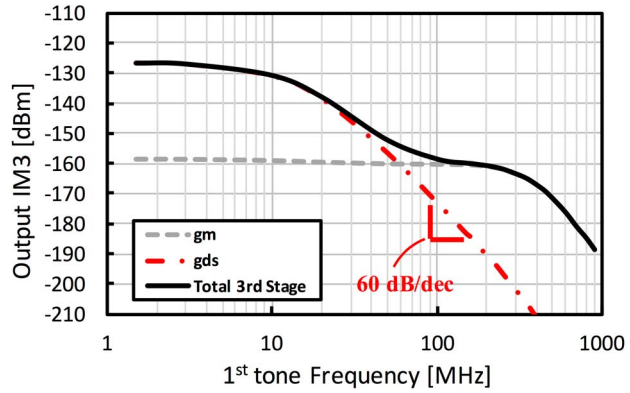

Fig. 9. Non-linear contributors of the output stage.

compression by the loop is independent of any characteristic of the OTA. On the contrary, distortion injection decreases by increasing the OTA gain at the tone frequency. We conclude that to improve the closed-loop intermodulation distortion of the input stage, it is key to enhance the gain of the OTA at the frequency of the OOB tones, i.e., up to maximum frequency distance between TX and RX band. Alternatively, C_{in} can achieve the same goal thanks to its low-pass filtering effect at the OTA input. Notice, however, that C_{in} cannot be increased arbitrarily since this may not only degrade noise but can also have an adverse effect on output stage linearity. In fact, when C_{in} is large enough to lower Z_{in} before the TIA cutoff frequency ω_0, the loop gain starts to decrease in-band due to a reduction of the feedback factor and the IM3 of the output stage increases as its frequency nears ω_0. In this design, C_{in} starts diverting the current from the OTA around 400 MHz, making overall IM3 to decrease with frequency.

Our method allows also to find which distortion mechanism dominates within a stage. This information is difficult to obtain even using sophisticated distortion simulations [31]. Focusing on the output stage, we see from Fig. 9 that, at low frequency, the large output swing makes g_{ds} non-linearity dominant. As a result, the output IM3 follows the frequency response of the TIA, i.e., beyond ω_0 it decreases with a slope of 60 dB/decade, leading to a sharp rise in the IIP3. Around 60 MHz, the g_m non-linearity takes over and IM3 flattens out, leading to a plateau in the IIP3. This is because up to 400 MHz, the input current is completely absorbed by the OTA, hence both the

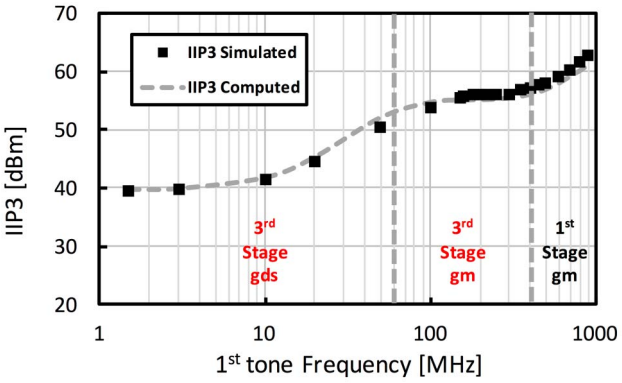

Fig. 10. Simulated IIP3 of the TIA, with the proposed OTA and dominating contributors.

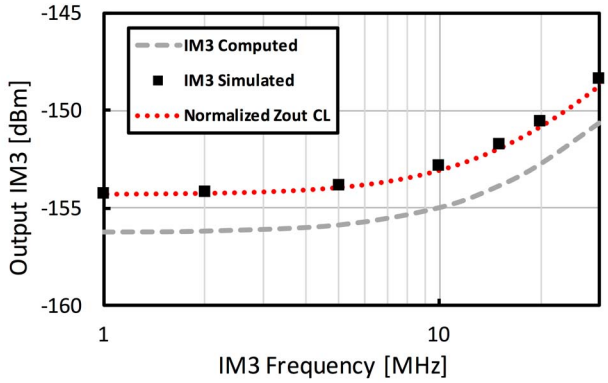

Fig. 11. IM3 as function of IM3 frequency and closed-loop output impedance frequency shape.

swing at the input of the last stage and the g_m non-linearity are frequency independent. On the other hand, at higher frequency C_{in} absorbs part of the input current, lowering all types of distortion including the one due to the output g_m. The above IM3 behavior corresponds to the IIP3 shown in Fig. 10, where the dominant source of distortion in each frequency range is indicated. Lowering the TIA transimpedance gain would lower IM3 injection and improve IIP3 up to 60 MHz, i.e., where the third stage g_{ds} non-linearity dominates. Beyond this frequency, a larger output stage or higher gain in front of it are needed to further boost IIP3. Our method allows also to compute IM3 versus f_{IM3} to find the worst case IB distortion energy due to blockers at different relative frequencies. To do this, we place the first tone at 100 MHz and move the second so that f_{IM3} is swept within the TIA band. In Fig. 11 we see that, as opposed to what generally happens, IM3 remains flat over almost all the TIA passband. This can be explained as follows.

1) In the frequency range considered output stage non-linearity is the main contributor.

2) The two tones are sufficiently beyond ω_0 that the g_m non-linearity dominates.

3) The non-linearity injection at f_{IM3} is independent of the position of the tones and the non-linear current is directly injected into the output node.

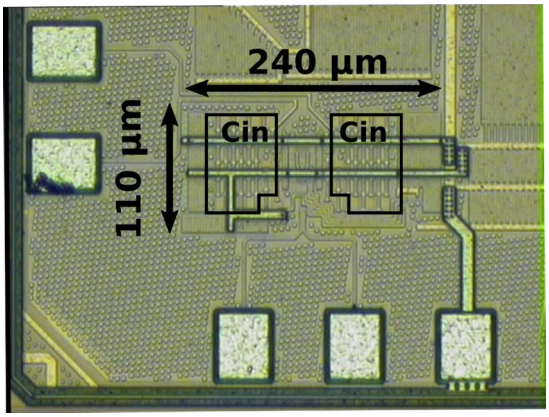

Fig. 12. Chip photograph.

4) The IM3 follows the frequency shape of the closed-loop output impedance, which is almost flat IB since the first OTA pole is near 20 MHz.

Combining the results derived for both output and input stage we come to the following overall conclusions. To improve IIP3 we need to increase the OTA gain at the highest OOB blocker frequency for low input stage distortion and at ω_0 for low output stage distortion. This involves in general maximizing the OTA bandwidth but also shaping its frequency response to have a larger than 20-dB/decade slope up to as near as possible the OTA unity gain frequency while preserving TIA stability. The latter technique is especially necessary to cope with the input stage distortion. We notice that the presence of a wideband second stage is critical to achieve low IM3. In fact, it helps compressing the distortion from the output stage by increasing the IB loop gain and it strongly reduces distortion injection from the first stage by reducing the OTA input signal.

V. Experimental Measurements

The photograph of the prototype TIA implemented in CMOS 28 nm is shown in Fig. 12. Thanks to the reduced input capacitance, area is only 0.026 mm^2. The measurement setup is shown in Fig. 13. An external balun converts the signal to differential while two 500-Ω resistors ($R_{d,\text{SE}}$) perform V–I conversion emulating the driving resistance of the passive mixer estimated from the LTE receiver in which the TIA is embedded. The output signal is detected with a differential active probe with a 2-pF differential load. The TIA frequency response, given in Fig. 14, has 20-MHz cutoff frequency and 14-dB IB gain to represent an LTE channel. The output noise power spectral density (PSD), measured with 20-dB probe gain to overcome the spectrum analyzer noise, given in Fig. 15 shows no IB noise increase due to C_{in}. Main noise contributors are driving resistors, OTA, and feedback resistors. The IR noise $P_{N,\text{In}}$ integrated up to 16 MHz is 21.1 μV_{RMS}. The differential TIA input impedance ($Z_{\text{in,diff}}$) was derived from s_{11} measurements with the 500 Ω driving resistances substituted with 50-Ω ones. From Fig. 16, the low-frequency value is 25 Ω, almost entirely due to R_{in}, while the resistance at the virtual ground is only a few Ohms. At higher

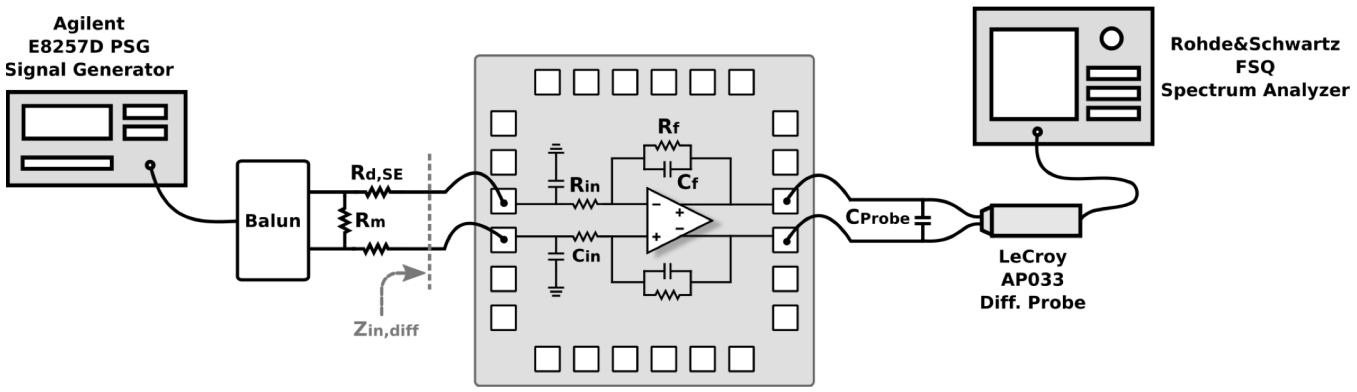

Fig. 13. Measurement setup.

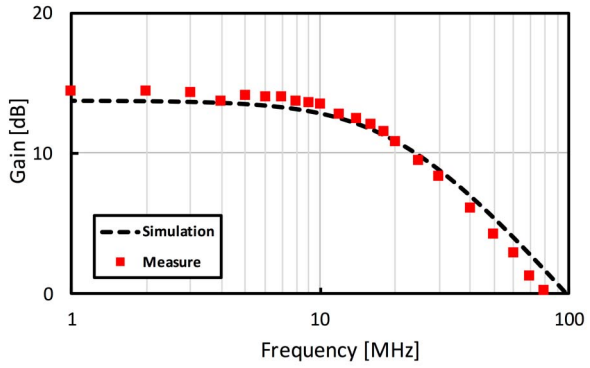

Fig. 14. Measured TIA gain.

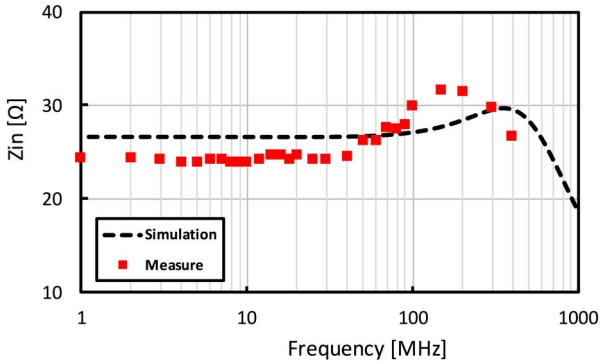

Fig. 16. Measured TIA differential input impedance ($Z_{\text{in,diff}}$).

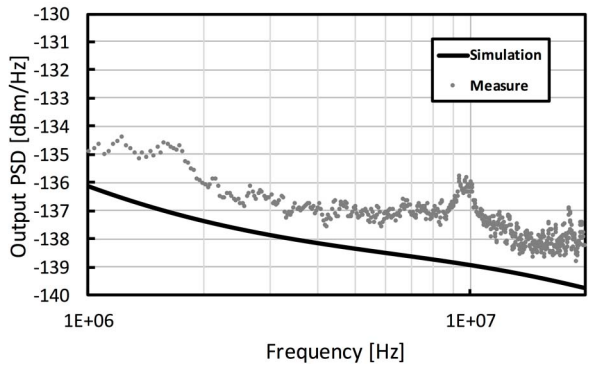

Fig. 15. Measured TIA output noise PSD.

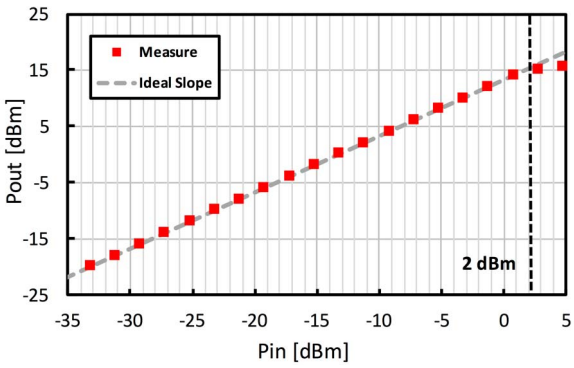

Fig. 17. Measured TIA 1-dB compression.

frequency, due to OTA gain reduction, $Z_{\text{in,diff}}$ increases but stays always below 32 Ω, thanks to the large OTA bandwidth. For very high-frequency C_{in} shunts the input, lowering $Z_{\text{in,diff}}$ again. Fig. 17 shows a 1-dB compression point of almost 2 dBm at 5 MHz, corresponding to an output swing very close to the supply. Linearity was tested through a two-tone intermodulation test. A passive first-order 3-MHz low-pass filter is used after the TIA, to limit the intermodulation of the probe for high-frequency tones, where low IM3 signals have to be detected. Figs. 18 and 19 show the IIP3 for IB (5–9 MHz) and OOB (100–199 MHz) tones, respectively. Fig. 20 is a plot of measured and simulated IIP3 versus the first tone frequency, with IM3 always at 1 MHz. IIP3 starts from 31.5 dBm IB, it increases moving OOB and reaches 50.5 dBm at 100 MHz.[5] IB IIP3 is around 9-dB smaller than expected (solid curve) when ideal feedback resistors are used in the TIA. Including the effect of poly-silicon feedback resistors non-linearity into the model (dashed curve) gives good correspondence. Multiplying by 3 the width of the poly resistors (dotted curve) less than 3 dB of in-band degradation is incurred, showing that this is not a fundamental limit. The OOB IIP3 corresponds to an intermodulation-free DR defined as $\text{IMFDR}_{3|\text{dB}} = (2/3)(\text{IIP3} - P_{N,\text{In}})$ of 87.5 dB [15]. OOB IIP3 was also tested versus IM3 frequency, by moving

[5]In [23], IR-noise and IIP3 were referred to the primary of the balun, performing a 1:3 impedance transformation.

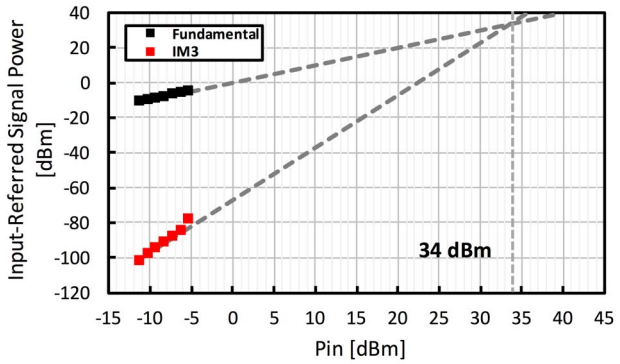

Fig. 18. IIP3 with input signals at 5–9 MHz.

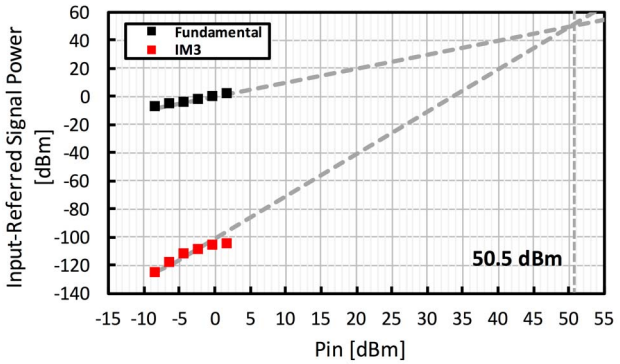

Fig. 19. IIP3 with input signals at 100–199 MHz.

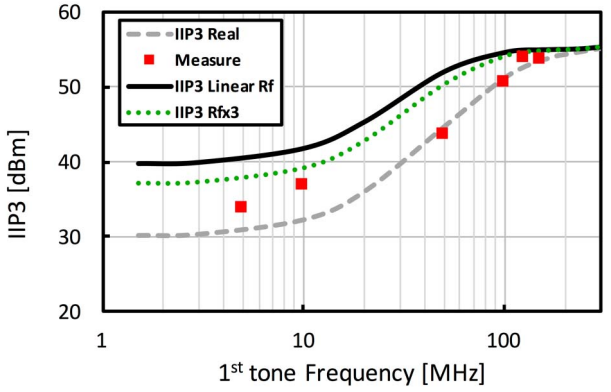

Fig. 20. IIP3 versus first tone frequency.

the second-tone while keeping the first one at 100 MHz (Fig. 21). IM3 remains flat over almost all the filter band. This is consistent with the analysis of Section IV. TIA performance is summarized and compared with other state-of-the-art filter implementations in Table V. Both figure of merit (FoM) given in [15] and reported in Table V are used for comparison. The proposed TIA has conventional and modified FOM's 2 and 6 dB above the previous best one [13], which has 7 times lower bandwidth. FOMs provide a useful way to compare different solutions given that high DR is the key goal in a filter. This, however, assumes that noise and distortion can be freely traded with each other by changing the gain in front of the filter. On the other hand, in practical cases,

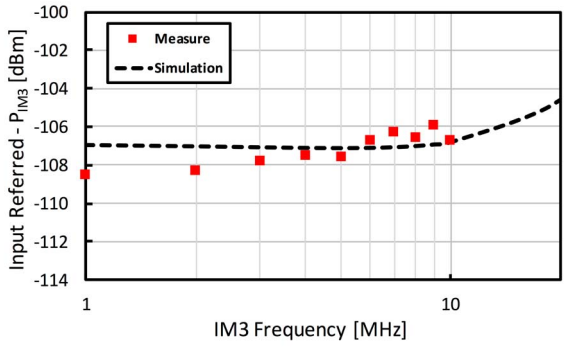

Fig. 21. IM3 versus IM3 frequency.

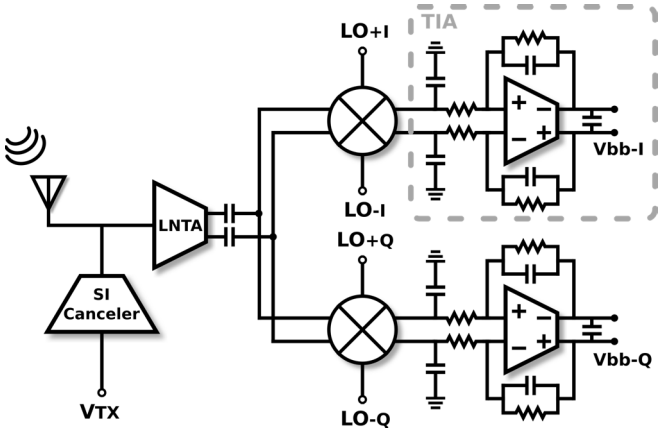

Fig. 22. Schematic of the SI-Cancellation RX reported in [33].

there may be a maximum gain that can be achieved before other limitations occur. The TIA described in this paper is part of a highly linear wideband receiver for FD and FDD wireless diversity [33] that includes a passive interference cancellation circuit and is conceptually shown in Fig. 22. The receiver low-noise trans-conductance amplifier (LNTA) is made of two complementary (p-n) cross-coupled common-gate amplifiers working in class-AB. The quadrature down-converter uses a passive mixer driven by a 25% duty-cycle LO, followed by the TIA, having a real pole at 20 MHz. The TIA ensures a low loading impedance ($<32\ \Omega$) at the mixer output, while 20-pF capacitors to ground give a low impedance at very high frequencies (above 400 MHz). The chip, fabricated in 28-nm CMOS, has a 0.51-mm^2 active area. The receiver s_{11} is below -10 dB from 1.5 to 3 GHz. At 2 GHz, the gain and double-sideband (DSB) NF are 4.6 and 35 dB, respectively. The receiver 1-dB compression point and IIP3 (without self-interference cancellation) are -15 and 9.5 dBm, respectively, IB while OOB (at 100-MHz offset) increase to 0 and 19 dBm, respectively. To assess the performance of the TIA in its real operating environment, we refer its noise and IIP3 to the receiver input. The TIA noise, referred to the receiver input corresponds to a DSB NF of 1.9 dB. It follows that the TIA contribution to the receiver NF is small. On the other hand, Fig. 23 (solid line) shows the impact of the TIA on the receiver IIP3, for the case of a perfectly linear LNTA and mixer. IIP3 starts from

TABLE V
TIA PERFORMANCE SUMMARY

Parameters	**This Work**	[12] RFIC '13	[13] ISSCC '16	[13] ISSCC '16	[14] JSSC '09	[15] JSSC '15	[32] JSSC '09	[32] JSSC '09
Technology [nm]	***28***	65	130	130	130	180	90	90
Area [mm^2]	***0.026***	0.29	0.45	0.45	1.53	0.14	0.5	0.5
Supply Voltage [V]	***1.8***	1.2	1.2	1.2	1	1.8	2.5	1.8
Power [mW]	***5.4***	3.4	1.92	1.92	7.5	1.38	1.26	0.15
f_0 [MHz]	***20***	14	2.8	12	5	33	2.8	2.8
N	***1***	5	2	2	5	4	4	4
OOB IIP3 [dBm]	***50.5***	20.6	48.5	36.1	52.8	18	35.6	48.5
Noise Vin [μV_{RMS}]	***21.1***	122	18.4	33.1	170	45	32	273
OOB IFDR [dB]	***87.5***	57.2	86.8	75.1	76.8	61.3	75	71.2
FOM_{conv} [dB(J^{-1})]	***183.2***	160.4	181.5	176.1	172	171.1	174.5	179.9
FOM_{IM3} [dB(J^{-1})]	***180.2***	155.9	174	172.3	165	155.9	167	172.4

$FoM_{conv} = IMFDR3|_{dB} + 10\log(N \cdot f_0/P_w)$ $FoM_{IM3} = FoM_{conv} + 10\log(f_{IM3}/f_0)$

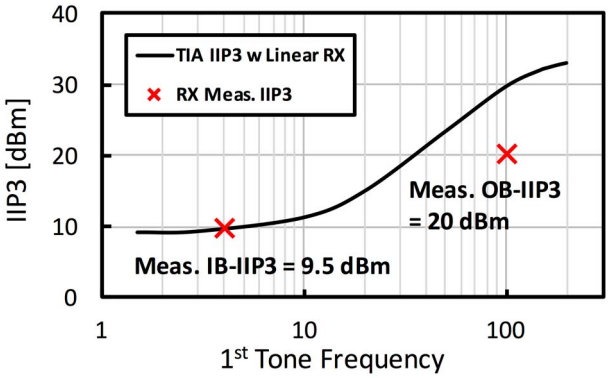

Fig. 23. RX IIP3 with perfectly linear LNTA and mixer (solid line) and measure IB and OOB RX IIP3.

around 10-dBm IB and reaches 29 dBm at 100-MHz offset. The much lower value of the TIA IIP3 when referred to the RX input is due to the >20 dB difference between the gain from RX input to TIA output and the TIA gain. Fig. 23 clearly shows that the TIA is dominating IB receiver IIP3.

VI. CONCLUSION

A TIA for wireless receivers has been designed and tested. Avoiding any Miller capacitance but relying on zeros in both the OTA and the feedback, an outstanding bandwidth of 1.6 GHz was achieved. This allowed reducing the capacitance at the TIA input from hundreds of picofarad to 20. The result is a better noise, a lower input impedance and a smaller distortion up to 400 MHz giving an FOM that exceeds that of all previous designs. Linearity optimization was made possible by a simple model capable to predict the IM3 of each stage and of each distortion mechanism within a stage.

APPENDIX

This Appendix describes how to extract the non-linear coefficients of each OTA stage. Equation (8) is derived from (3) with the gain $G(\omega)$ of each stage rewritten as $g_{m,i} \cdot |Z_{o,i}(\omega)|$. From (8), we see that when a stage is loaded by a low impedance, its g_m non-linearity is dominant since this reduces the output swing. On the contrary, when the load impedance is high, the large output swing makes the g_{ds} non-linearity dominant. With a 1-Ω load resistance at the stage output, (8) can be approximated by (9). Simulating the circuit intermodulation magnitude ($|v_{IM,out,i}|$) with two input tones of amplitude $A_{1,i}$ and $A_{2,i}$, the $g_{mNL3,i}$ coefficient can be extracted by inversion of (9), as shown in (10)

$$v_{IM,out,i} = \left(\frac{3}{4} g_{mNL3,i} A_{1,i}^2 A_{2,i} + \frac{3}{4} g_{dsNL3,i} (A_{1,i} \cdot g_{m,i} |Z_{o,i}(\omega_1)|)^2 \cdot (A_{2,i} \cdot g_{m,i} |Z_{o,i}(\omega_2)|)\right) \cdot |Z_{o,i}(2\omega_1 - \omega_2)| \cdot \sin((2\omega_1 - \omega_2)t) \quad (8)$$

$$v_{IM,out,i} \cong \frac{3}{4} g_{mNL3,i} A_{1,i}^2 A_{2,i} \cdot (1\ \Omega) \cdot \sin((2\ \omega_1 - \omega_2)t) \quad (9)$$

$$g_{mNL3,i} \cong \frac{4}{3} \frac{|v_{IM,out,i}|}{A_{1,i}^2 A_{2,i} \cdot (1\ \Omega)}. \quad (10)$$

The same simulation is performed with no explicit load. At sufficiently low frequency, $Z_{o,i}(\omega)$ is the parallel of the r_{out} of the output transistors, which is typically in the order of kiloohm. Putting the result of (10) in (8) we get $g_{dsNL3,i} = ((4|v_{IM,out,i}|/3r_{o,i}) - g_{mNL3,i} A_{1,i}^2 A_{2,i})/A_{1,i}^2 A_{2,i} (g_{m,i} r_{o,i})^3$.

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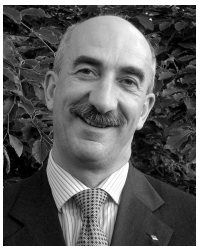

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