64-QAM 60-GHz CMOS Transceivers for IEEE 802.11ad/ay

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***Abstract*— This paper presents 64-quadrature amplitude modulation (QAM) 60-GHz CMOS transceivers with four-channel bonding capability, which can be categorized into a one-stream transceiver and a two-stream frequency-interleaved (FI) transceiver. The transceivers are both fabricated in a standard 65-nm CMOS technology. For the proposed one-stream transceiver, the TX-to-RX error vector magnitude (EVM) is less than −23.9 dB for 64-QAM wireless communication in all four channels defined in the IEEE 802.11ad/WiGig. The maximum communication distance with the full rate can reach 0.13 m for 64 QAM, 0.8 m for 16 QAM, and 2.6 m for QPSK using 14-dBi horn antennas. A data rate of 28.16 Gb/s is achieved in 16 QAM by four-channel bonding. The transmitter, receiver, and phase-locked loop consume 186, 155, and 64 mW, respectively. The core area of the transceiver is 3.9 mm^2. For the proposed two-stream FI transceiver, four-channel bonding in 64 QAM is realized with a data rate of 42.24 Gb/s and an EVM of less than −23 dB. The front end consumes 544 mW in transmitting mode and 432 mW in receiving mode from a 1.2-V supply. The core area of the transceiver is 7.2 mm^2.**

***Index Terms*— 60 GHz, 64 quadrature amplitude modulation (QAM), CMOS, four-channel bonding, I/Q mismatch calibration, transceiver, wideband.**

I. Introduction

With the fast development of wireless communication technologies, nowadays, we are experiencing tremendous growth of data traffic in radio access networks. It is predicted that the required wireless communication capacity will become 1000 times higher every ten years. Many wireless standards are under discussion to satisfy the unprecedented capacity requirement. For example, the IEEE 802.11ay standard is targeting over 100-Gb/s data rate by using 60-GHz band. Unfortunately, the channel bandwidth of 2.16 GHz for the 60-GHz band is not wide enough to realize such high data rate. A channel-bonding capability as well as the high-order modulation support is strongly demanded to boost the data rate. For instance, a four-channel bonding in 64 quadrature amplitude modulation (QAM) can achieve 42.24-Gb/s data rate (7.04 GS/s × 6 b/S).

To realize four-channel bonding operation with 64 QAM, there are several challenges, such as wideband gain characteristics, wide dynamic range, low local oscillator (LO) phase noise, fine and wideband I/Q mismatch calibration, and small LO leakage. A direct-conversion architecture is widely used for the 60-GHz CMOS transceivers due to its low power consumption and wideband characteristic [1], [2]. The direct-conversion 60-GHz transceivers reported in [3] and [4] achieve 4 Gb/s in QPSK and 7 Gb/s in 16 QAM, respectively. However, the low-pass nature of the baseband amplifiers limits the full use of the 60-GHz band with reasonable power consumption. Furthermore, an injection-locking technique is employed for the 60-GHz transceivers [5], [6], which realizes low phase noise with wide frequency tuning range in 60-GHz quadrature LO synthesis. Nevertheless, a method for the fine and wideband I/Q mismatch calibration is still desired to accomplish the four-channel bonding operation with 64 QAM. In addition, an 8-bit 14.08-GS/s analog-to-digital converter (ADC) is normally required to support 42.24 Gb/s in 64 QAM, which is usually realized by a massive time-interleaved ADC, and needs unreasonably large power consumption. In this condition, a baseband signal bandwidth of 3.52 GHz is assumed. The Nyquist rate is 7.04 GS/s. Considering an oversampling ratio of 2, which can ease the implementation of the baseband filtering [7], the sampling rate of the ADC is 14.08 GS/s. With such a high sampling rate, the signal-to-noise-and-distortion ratio (SNDR) of an 8-bit ADC may be less than 36 dB [8], which leaves around 10-dB margin to tolerate the impairments mentioned earlier.

In this paper, a one-stream 64-QAM 60-GHz CMOS transceiver is presented, which achieves a TX-to-RX error vector magnitude (EVM) of −26.3 dB and can transmit 10.56 Gb/s in all four channels defined in the IEEE 802.11ad/WiGig standard [9]. By using a four-bonded channel, 28.16 Gb/s can be transmitted in 16 QAM. The front end consumes 251 mW in transmitting mode and 220 mW in receiving mode from

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TABLE I
LINK BUDGET FOR SHORT-RANGE HIGH-SPEED COMMUNICATION

Carrier frequency	61.56 GHz	
Distance	0.2 m	0.1 m
Bandwidth	1.76 GHz	7.04 GHz
TX output power	3 dBm	
TX/RX antenna gain	2 dBi	
LOS loss	−54.2 dB	−48.2 dB
Implementation loss	−3 dB	
Received level	−50.3 dBm	−44.3 dBm
Thermal noise	−81.4 dBm	−75.4 dBm
NF	6 dB	
Received SNR	25.1 dB	
Modulation	64QAM	
Required SNR	22.5 dB	

a 1.2-V supply. The core area of the transceiver is 3.9 mm^2. Furthermore, a frequency-interleaved (FI) architecture is employed for a 60-GHz transceiver to mitigate the wideband I/Q mismatch issue and the ADC requirement [10]. The transceiver achieves 42.24-Gb/s data rate in 64 QAM by operating two FI transceivers at the same time. Each FI transceiver uses two-channel bonded spectrum with different carrier frequencies, which realizes the TX-to-RX EVM of −24.1 and −23.0 dB, respectively. The transmitters, receivers, and phase-locked loops (PLLs) consume 412, 300, and 132 mW from a 1.2-V supply, respectively.

This paper is organized as follows. The design challenges and considerations for realizing high-data-rate 60-GHz transceivers are discussed in Section II. The proposed architecture and the detailed circuit implementation for several key blocks are introduced in Section III. Section IV presents the FI architecture to achieve four-channel bonding in 64 QAM. The measurement results are shown in Section V. Finally, this paper is concluded in Section VI.

II. DESIGN CHALLENGES AND CONSIDERATIONS

Table I shows a link budget example of the 60-GHz transceiver, which includes the communication of one-channel (1.76 GHz) and four-channel bonding (7.04 GHz) in 64 QAM. The output power of the transmitter is 3 dBm. The target communication distances are 0.2 and 0.1 m, respectively. The transmitter and receiver antennas have a gain of 2 dBi. A noise figure of 6 dB is assumed for the receiver. It can be seen that the received signal-to-noise ratio (SNR) has about 3-dB margin from the required SNR of 22.5 dB.

However, there are many other factors (especially for the 64 QAM and four-channel bonding case) that will degrade the quality of the received signal. First, the wideband gain characteristics are required for both transmitter and receiver. At RF side, a wide-and-flat gain roughly from 57 to 66 GHz is needed. On the other hand, a 5-GHz bandwidth is necessary at baseband side, which is very power-consuming because of the low-pass nature of baseband amplifiers. Fig. 1 shows the MATLAB simulation results of EVM in 16 QAM considering the influence of the TRX gain flatness. The

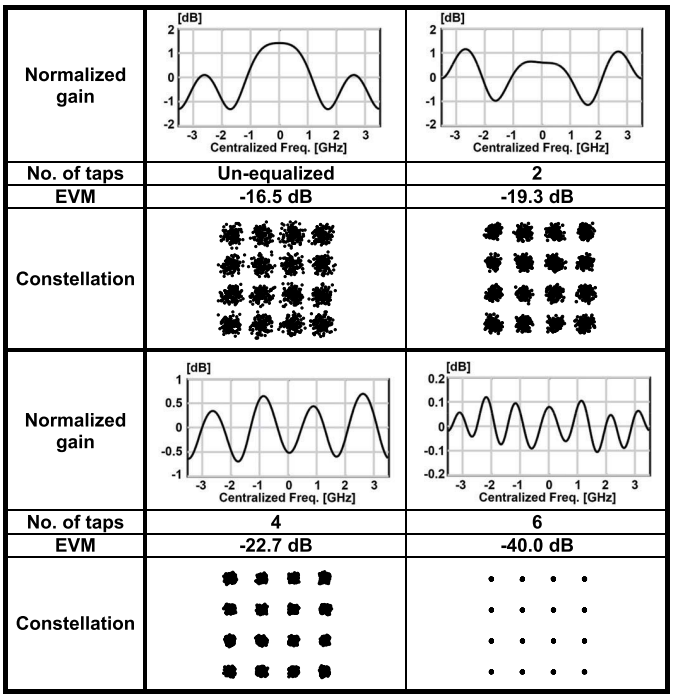


Fig. 1. Simulated EVM in 16 QAM with 7.04-GS/s symbol rate at different equalization conditions.

symbol rate is 7.04 GS/s on single carrier (SC) mode. The frequency response of a fourth-order finite impulse response (FIR) filter is assumed for modeling the gain flatness of the TRX. A recursive least square (RLS) linear equalizer is used for demonstrating the influence of the gain flatness and equalization. It is observed that the maximum gain variation of the un-equalized TRX within the 7.04-GHz bandwidth is about ±1.4 dB, which corresponds to an EVM of −16.5 dB. When the number of the equalizer taps increases, the maximum gain variation is reduced, and the EVM performance is improved. A gain variation of less than ±0.7 dB (four-tap equalizer) over the frequency band of interest is needed to achieve 16 QAM and four-channel bonding considering about 6-dB margin from the required EVM of −16.5 dB. As for 64 QAM and four-channel bonding, a larger number of taps with smaller gain variation (such as six taps, ±0.1-dB gain variation) may be required, considering over 10-dB margin from the required EVM of −22.5 dB. In practical implementation, the actual required number of taps and the corresponding gain variations should be estimated by both the value and shape of the TRX gain characteristics.

Furthermore, the wide dynamic range has to be maintained considering linearity and noise with the 5-GHz baseband bandwidth. In addition, the phase noise of the LO, image rejection, and LO leakage is also critical [7], [11]. All those impairments can disturb the signal constellation and degrade the system EVM. The relationship between the TX/RX EVM and impairments can be expressed as [12], [13]

$$\mathrm{EVM_{tot}} \approx \sqrt{\frac{1}{\mathrm{SNDR}^2} + \varphi_{\mathrm{RMS}}^2 + \mathrm{EVM_{IMRR}^2} + \mathrm{EVM_{LOFT}^2} + \mathrm{EVM_{GF}^2}} \quad (1)$$

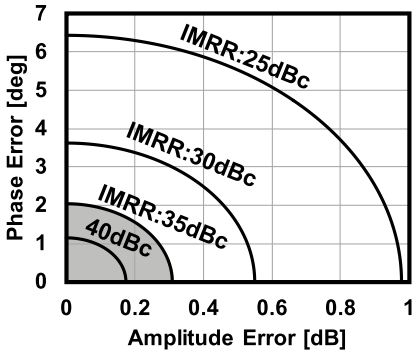


Fig. 2. Calculated IMRR versus gain and phase error.

where SNDR is the signal-to-noise-and-distortion ratio, which considers the effects of the front-end noise and non-linearity, such as AM–AM and AM–PM distortion [14]. φ_{RMS} is the integrated double-sideband (DSB) phase noise of a carrier. $\mathrm{EVM_{IMRR}}$, $\mathrm{EVM_{LOFT}}$, and $\mathrm{EVM_{GF}}$ represent the degraded EVM due to I/Q mismatch, LO leakage, and gain flatness, respectively. It should be indicated that (1) is a simplified expression, which emphasizes several dominant effects for the 60-GHz transceivers. In actual transceivers, many other effects could influence the EVM performance, such as the correlated effects between AM–AM/AM–PM distortion and phase noise, the resolution and clock jitter of the ADC/digital-to-analog converter (DAC) [15], [16], and so on. Thorough system analysis and simulations should be conducted to identify the major performance limiters.

As we know, the phase noise is one of the major performance limiters for the EVM of the 60-GHz CMOS transceivers [17]. To support 64 QAM, a phase noise of −96 dBc/Hz at 1-MHz offset is required, considering a 400-kHz bandwidth for the carrier tracking [12], [17]. The carrier tracking is a common technique in baseband, which can suppress the phase noise effects within the tracking bandwidth. For the SC mode, because the tracking bandwidth can be wider than the loop bandwidth of the PLL, the in-band phase noise is not a critical issue. Therefore, the out-of-band phase noise requirement is discussed as mentioned before. However, in orthogonal frequency-division multiplexing (OFDM) cases, the tracking bandwidth is generally smaller than the loop bandwidth. Both in-band and out-of-band phase noises are dominant issues, which leads to a more stringent phase noise requirement. It has been demonstrated that the required phase noise performance can be achieved by using 60-GHz quadrature injection-locked oscillators (QILOs) and a 20-GHz PLL [6]. As shown in (1), the I/Q mismatch has significant influence on the EVM performance of the 60-GHz transceiver, which is normally evaluated by the image rejection ratio (IMRR). The IMRR can be expressed as the function of gain and phase imbalance

$$|\mathrm{IMRR}| = \left| \frac{10^{\frac{\Delta A}{10}} + 2 \cdot 10^{\frac{\Delta A}{20}} \cos \Delta\theta + 1}{10^{\frac{\Delta A}{10}} - 2 \cdot 10^{\frac{\Delta A}{20}} \cos \Delta\theta + 1} \right| \tag{2}$$

where ΔA is the gain error in decibel. $\Delta\theta$ is the phase error in degree. For 64-QAM communication, $|\mathrm{IMRR}| \geq 35$ dBc should be satisfied in consideration of other impairment degradations. It is corresponding to less than 0.3-dB gain mismatch and less than 2° phase mismatch, as shown in Fig. 2. Therefore, fine calibrations of I/Q gain and phase errors are desired to obtain the high IMRR. Moreover, the IMRR of more than 35 dBc needs to be maintained over wide bandwidth for the channel-bonding cases, which further increases the design difficulty.

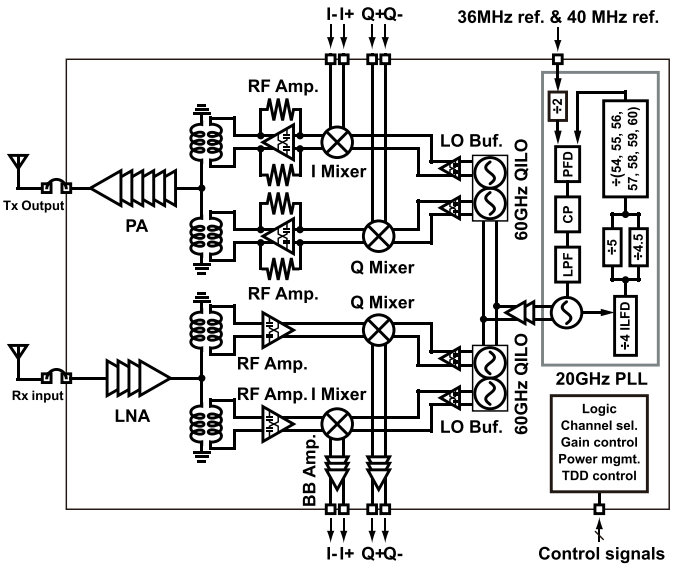


Fig. 3. Block diagram of the proposed 60-GHz one-stream transceiver.

III. 60-GHz TRX Architecture and Circuit Implementation

A. Transceiver Architecture

Fig. 3 shows the block diagram of the 60-GHz one-stream front end. A direct-conversion architecture is employed for both TX and RX because of wide-bandwidth and low-power capability [19]. The transmitter adopts the mixer-first topology for achieving wideband gain characteristics with low power consumption. It consists of a six-stage power amplifier (PA), differential pre-amplifiers, I/Q double-balanced passive mixers, and a QILO. To realize the wideband and linear characteristics, the receiver employs an open-loop baseband amplifier based on the flipped voltage follower (FVF) and a current-bleeding mixer. The receiver is composed of a four-stage low noise amplifier (LNA), differential RF amplifiers, I/Q current-bleeding mixers, a QILO, and baseband amplifiers. The LO consists of the 60-GHz QILO and a 20-GHz PLL. The 60-GHz QILO works as a frequency tripler with the integrated 20-GHz PLL. It can generate seven carrier frequencies with a 36/40-MHz reference, 58.32 GHz (ch.1), 60.48 GHz (ch.2), 62.64 GHz (ch.3), and 64.80 GHz (ch.4) defined in the IEEE 802.11ad/WiGig, and 59.40 GHz (ch.1 and ch.2), 61.56 GHz (ch.2 and ch.3 or ch.1–ch.4), and 63.72 GHz (ch.3 and ch.4) aiming for channel bonding in the IEEE 802.11ay, as shown in Fig. 4.

B. Transmitter

Starting from the TX topology consideration, Fig. 5(a) shows a conventional design of the 60-GHz direct-conversion transmitter. The 5-GHz baseband bandwidth requires large

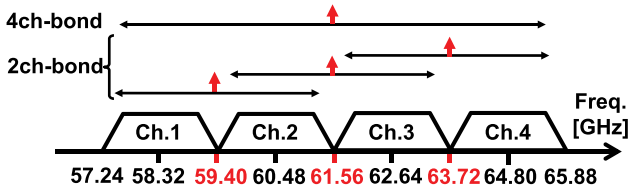


Fig. 4. Channels defined by the IEEE 802.11ad/WiGig standard.

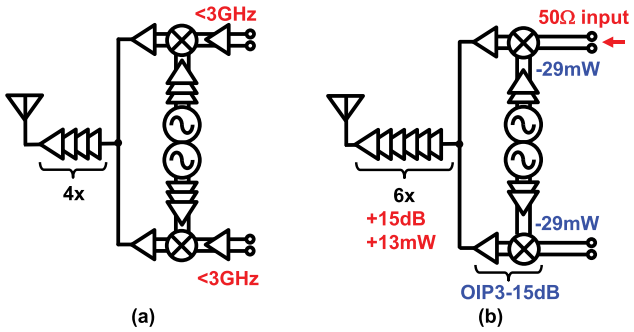


Fig. 5. Block diagram of (a) conventional 60-GHz direct-conversion transmitter [18] and (b) proposed mixer-first transmitter.

power consumption for this topology because of low-pass nature of baseband amplifiers. For example, each baseband amplifier consumes 11 mW while achieving less than 3-GHz bandwidth in [18]. Therefore, in this paper, the wide 5-GHz baseband bandwidth for both gain and input impedance is maintained by the proposed mixer-first topology. The detailed circuit implementation will be explained later in this section. Basically, this topology contributes to improving baseband gain characteristics and reducing power consumption. In addition, as shown in Fig. 5(b), increasing RF gain by adding more stages for the PA and decreasing baseband gain by removing baseband amplifiers, the linearity requirement for the mixer block is relaxed. For instance, a 15-dB increase in the PA gain leads to a 15-dB reduction of the required output third-order intercept point for the mixer and RF amplifier group. Consequently, the number of LO buffer stages can be reduced. The LO buffers have to amplify four paths of 60-GHz signals in case of differential topology, which are very power-hungry. Even through a 13-mW increase in RF path is considered, the reduction of the LO buffers contributes to saving 45-mW power consumption in total. As a result, the mixer-first topology achieves wider bandwidth and reduces power consumption.

It is well known that in software-defined radios, the mixer-first receiver can be used to realize tunable RF characteristics with high linearity [20], [21]. The baseband low-pass characteristics can be up-converted by a passive mixer. Thus, the RF bandpass characteristics is controlled by baseband circuitry, as shown in Fig. 6(a). In this paper, the mixer-first topology is applied to a millimeter-wave transmitter for realizing wide baseband characteristics. A wide-and-flat gain characteristic, such as 57–66 GHz, is realized at the RF side, which is down-converted by a passive mixer. Hence, a 4.5-GHz wide-and-flat gain at baseband side can be obtained, as shown in Fig. 6(b). In addition, the 50-Ω input impedance is also maintained by the mixer-first topology.

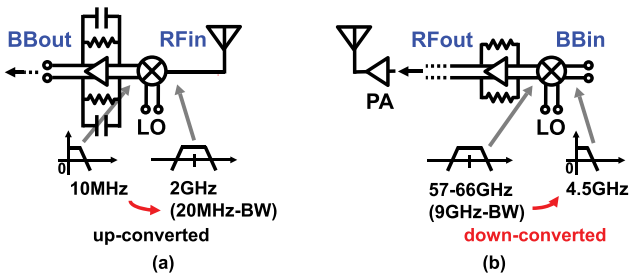


Fig. 6. Simplified block diagram of (a) mixer-first receiver and (b) proposed mixer-first transmitter.

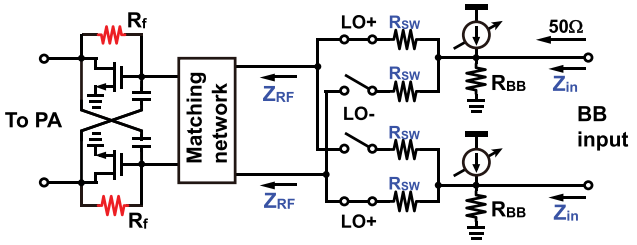


Fig. 7. Circuit schematic of the mixer-first transmitter.

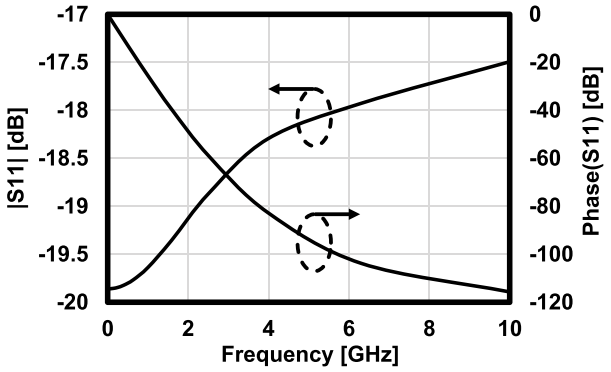


Fig. 8. Simulated S11 seen at the baseband input port of the TX mixer.

Fig. 7 shows the detailed circuit schematic of the mixer-first transmitter (I or Q path). It consists of a double-balanced passive mixer and a differential resistive-feedback RF amplifier with a matching network. The baseband input impedance ($Z_{\rm in}$) can be roughly calculated as [22]

$$Z_{\rm in}(\omega_{\rm BB}) = R_{\rm BB} /\!\!/ \left\{ R_{\rm SW} + \frac{4}{\pi^2}[Z_{\rm RF}(\omega_{\rm BB}+\omega_{\rm LO}) + Z_{\rm RF}(\omega_{\rm BB}-\omega_{\rm LO})] \right\} \quad (3)$$

where $\omega_{\rm BB}$ and $\omega_{\rm LO}$ represent the baseband frequency and LO frequency, respectively. $Z_{\rm RF}$ is the input impedance of the RF amplifier including the matching network. $R_{\rm SW}$ is the ON-resistance of the switch. To achieve a wide-and-flat impedance characteristic at RF side, a resistive-feedback topology is applied to a differential amplifier with a capacitive-cross coupling neutralization. The matching block is used to compensate an imaginary part of $Z_{\rm RF}$. The shunt resistors $R_{\rm BB}$ are also used for maintaining 50-Ω input impedance over the four channels. Fig. 8 shows the simulated S11 seen at the baseband

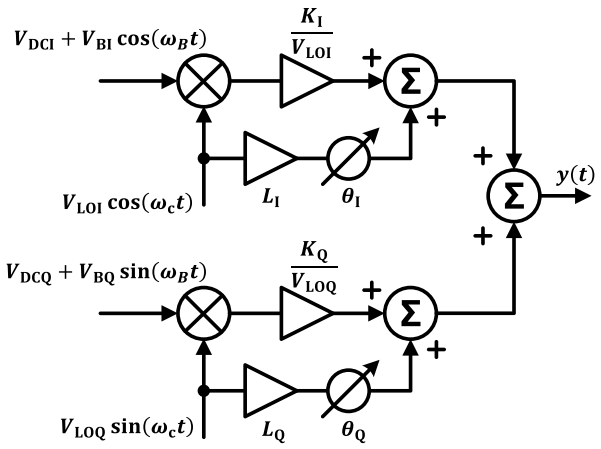


Fig. 9. Analysis model of the TX quadrature mixer LO leakage.

input port of the TX mixer. The magnitude of S11 is lower than −17 dB over 10-GHz bandwidth, which demonstrates the wideband characteristic. This will ease the implementation of the matching network between the baseband input of the mixer and the output of the low-pass filter (LPF) in baseband circuitry, since the output of the LPF generally has a 100-Ω (differential) interface.

The current sources at the baseband input are used for LO leakage calibration. It is known that the LO leakage of the quadrature mixer can be minimized by adding the DC offset voltage at the baseband input [23], [24]. Its principle is explained using the analysis model shown in Fig. 9. V_{DCI} and V_{DCQ} are DC offset voltages applied at the baseband input of I path and Q path, respectively. The baseband signal has a frequency of ω_B and an amplitude of V_B. The frequency of the carrier signal is ω_c with an amplitude of V_{LO}. The LO leakage for each mixer is modeled as a scaled (L_I and L_Q) and phase-shifted (θ_I and θ_Q) signal of each LO input. K represents the conversion gain of the mixer. Therefore, the combined output signal is expressed as

$$y(t) = y_{leak}(t) + y_{sig}(t) \tag{4}$$

where $y_{leak}(t)$ is the LO leak at the combined output

$$y_{leak}(t) = A\cos(\omega_c t + \alpha) + B\sin(\omega_c t + \beta) \tag{5}$$

$$A = \sqrt{K_I^2 V_{DCI}^2 + V_{LOI}^2 L_I^2 + 2K_I V_{DCI} V_{LOI} L_I \cos\theta_I} \tag{6}$$

$$\alpha = \arctan\left(\frac{V_{LOI} L_I \sin\theta_I}{K_I V_{DCI} + V_{LOI} L_I \cos\theta_I}\right) \tag{7}$$

$$B = \sqrt{K_Q^2 V_{DCQ}^2 + V_{LOQ}^2 L_Q^2 + 2K_Q V_{DCQ} V_{LOQ} L_Q \cos\theta_Q} \tag{8}$$

$$\beta = \arctan\left(\frac{V_{LOQ} L_Q \sin\theta_Q}{K_Q V_{DCQ} + V_{LOQ} L_Q \cos\theta_Q}\right) \tag{9}$$

and $y_{sig}(t)$ contains the desired signal and image signal (if $K_I V_{BI} \neq K_Q V_{BQ}$)

$$y_{sig}(t) = \frac{K_I V_{BI} + K_Q V_{BQ}}{2}\cos[(\omega_c - \omega_B)t] + \frac{K_I V_{BI} - K_Q V_{BQ}}{2}\cos[(\omega_c + \omega_B)t]. \tag{10}$$

Hence, the relative LO leakage is calculated using the following equation:

$$\eta|_{dBc} = 20\log\frac{2C}{K_I V_{BI} + K_Q V_{BQ}} \tag{11}$$

where

$$C = \sqrt{A^2 + B^2 - 2AB\sin(\alpha - \beta)}. \tag{12}$$

The required DC offset voltages and voltage tuning resolution ($V_{DC,res}$) can be estimated by solving (11). In CMOS implementation, the leakage phase shift is very close to zero ($\theta_I \approx \theta_I \approx 0°$). Then, (11) has a simplified formation

$$\eta|_{dBc} = 10\log\frac{4K_I^2\left(V_{DCI} + \frac{V_{LOI}L_I}{K_I}\right)^2 + 4K_Q^2\left(V_{DCQ} + \frac{V_{LOQ}L_Q}{K_Q}\right)^2}{(K_I V_{BI} + K_Q V_{BQ})^2}. \tag{13}$$

It is interesting to know that (13) is an ellipse equation in V_{DCI}–V_{DCQ} plane with the semimajor axis of a and semiminor axis of b (or vice versa). The center point of the ellipse is ($V_{DCI,opt}$, $V_{DCQ,opt}$), which corresponds to $\eta = 0$

$$a = 10^{\frac{\eta}{20}}\frac{(K_I V_{BI} + K_Q V_{BQ})}{2K_I} \tag{14}$$

$$b = 10^{\frac{\eta}{20}}\frac{(K_I V_{BI} + K_Q V_{BQ})}{2K_Q} \tag{15}$$

$$V_{DCI,opt} = -\frac{V_{LOI} L_I}{K_I} \tag{16}$$

$$V_{DCQ,opt} = -\frac{V_{LOQ} L_Q}{K_Q}. \tag{17}$$

Therefore, $V_{DC,res}$ is determined by the minimum values among a, b, $|V_{DCI,opt}|$, and $|V_{DCQ,opt}|$

$$V_{DC,res} = \min(a, b, |V_{DCI,opt}|, |V_{DCQ,opt}|). \tag{18}$$

Consequently, the optimum offset current ($I_{DCx,opt}$) and required current resolution ($I_{DC,res}$) are expressed as

$$I_{DCx,opt} = \frac{V_{DCx,opt}}{Z_{in}(\omega_{BB})|_{\omega_{BB}=0,x}} \tag{19}$$

$$I_{DC,res} = \frac{V_{DC,res}}{Z_{in}(\omega_{BB})|_{\omega_{BB}=0,x}} \tag{20}$$

where the footnote x is I or Q. To obtain some quantitative values, the following design parameter is used. The conversion gain of the I/Q mixer is −10 dB. The baseband input power of each path is 0 dBm. The LO amplitude is 1.2 V for I and Q path. L_I and L_Q are both −30 dB. The target η is −50 dBc. In this condition, $V_{DC,res}$ is dominated by $a(= b)$, which is about 1.4 mV. The corresponding $I_{DC,res}$ is around 24 μA with the baseband input resistance of 59 Ω. In practical implementation, $I_{DCx,opt}$ and $I_{DC,res}$ fluctuate under process, voltage, and temperature (PVT) variation. It should be taken into consideration that re-calibration schemes and enough design margin for the offset current tuning range and resolution are prepared.

Fig. 10 shows the circuit schematic of the six-stage PA. A transmission-line (TL)-based design is employed to achieve

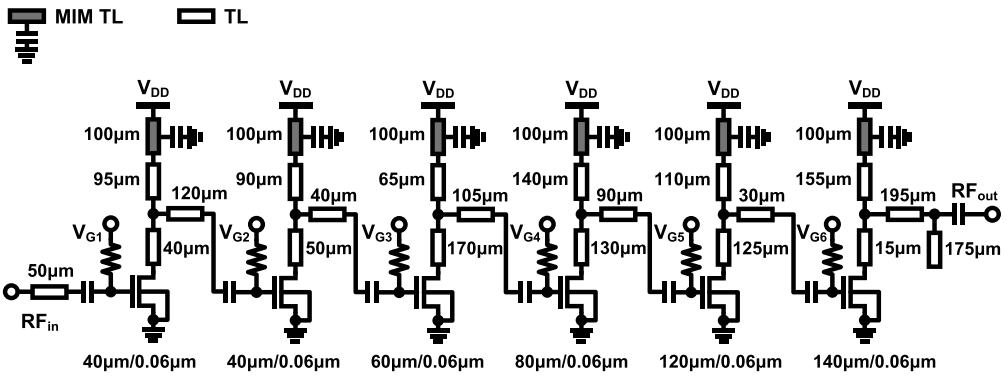


Fig. 10. Schematic of the 60-GHz PA.

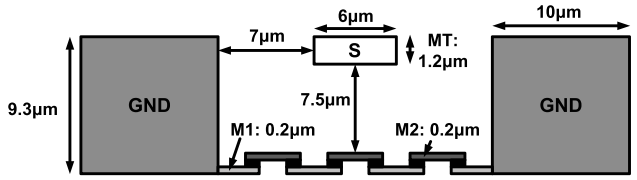


Fig. 11. Cross-sectional view of the TL.

a reliable simulation and flexible layout [25]. The structure of the TL is shown in Fig. 11. Only the top metal layer (MT) is used for the signal line. The signal line is isolated from the substrate by two metal layers (M1 and M2). A MIM TL with the MIM capacitors shunt-connected alongside the TL is used for the de-coupling of the power supplies. A common-source topology is chosen for each gain stage due to its high linearity. The transistor size is gradually increased from the input stage to the output stage of the PA with the consideration of power consumption and linearity. The multistage gain peaking technique [6] is adopted for realizing wide and flat gain characteristics. Fig. 12 shows the simulated gain of the PA at different temperatures and supply voltages. The maximum gain difference within the 8.64-GHz bandwidth is kept around 1.3 dB over temperature and voltage variation. However, the absolute gain of the PA varies obviously, which necessitates the use of compensation and calibration techniques, such as constant-g_m biasing, low-ripple voltage regulators, gain calibration loop, and so on, in practical implementation.

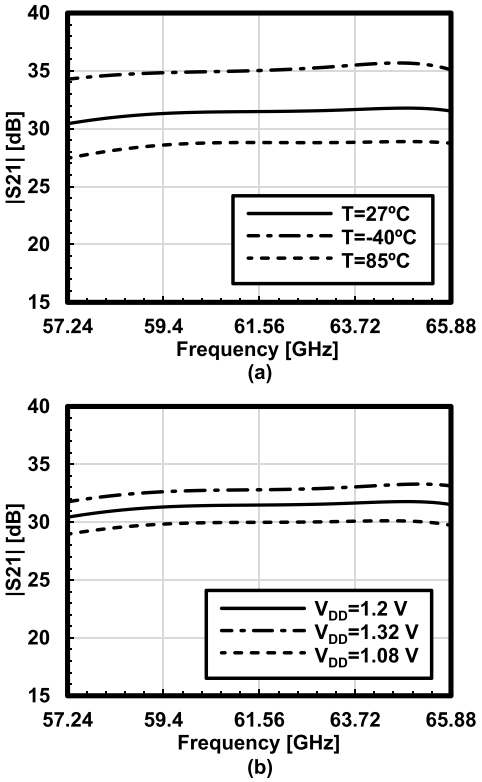


Fig. 12. Simulated gain of the PA versus frequency at (a) different temperatures with 1.2-V supply and (b) temperature of 27 °C with different supply voltages.

C. Receiver

For the mm-Wave receiver design, the noise figure, linearity, gain flatness, and frequency-dependent I/Q mismatch should be considered. Especially for the four-channel bonding condition, the noise floor becomes at least 98 dB higher from −174 dBm/Hz. The peak SNDR of the RX also suffers from the non-linearity of the receiver chain. In addition, it is difficult to use a close-loop baseband amplifier for improving linearity and gain flatness due to the wide bandwidth. Thus, in this paper, an open-loop baseband amplifier based on the FVF [26] is employed to maintain both gain flatness and linearity with reasonable power consumption.

Fig. 13 shows the detailed circuit schematic of one unit cell used for the first and second stage of the baseband amplifier. The unit cell consists of two amplifier stages. The first stage is a modified FVF amplifier with resistors R_s and capacitors C_s connected between the source terminals of M1 and M2. The voltage gain of the first stage can be expressed as

$$A_{V,1\text{st}}(\omega) \approx \frac{1}{g_{m3} \cdot [r_{ds3} /\!/ R_s /\!/ (1/j\omega C_s)]}. \quad (21)$$

The second stage is an active-load common-source amplifier with common-mode feedback loop. The voltage gain of the second stage is

$$A_{V,2\text{nd}}(\omega) \approx g_{m7} \cdot [r_{ds7} /\!/ r_{ds9} /\!/ R_L /\!/ (1/j\omega C_L)] \quad (22)$$

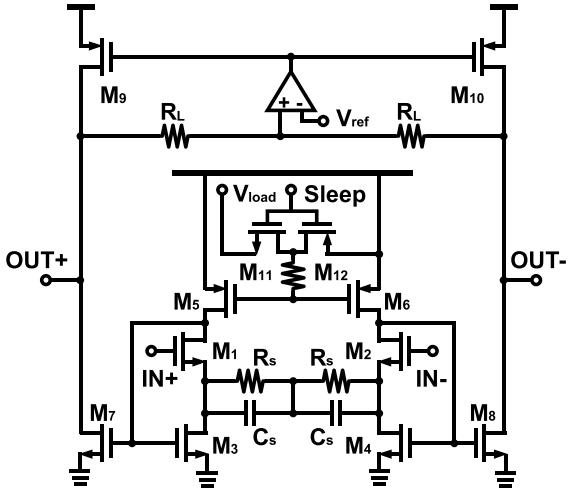


Fig. 13. Circuit schematic of one unit cell for the first and the second stage of the baseband amplifier.

where C_L represents the capacitor between the output node of the second stage and ground. Assuming that $r_{ds3} \gg R_s$, $r_{ds7} \gg R_L$, and $r_{ds9} \gg R_L$, the voltage gain of the unit cell is

$$A_{V,\mathrm{BB}}(\omega) = A_{V,1\mathrm{st}}(\omega) \cdot A_{V,2\mathrm{nd}}(\omega) \approx \frac{g_{m7} \cdot [R_L \,/\!/\, (1/j\omega C_L)]}{g_{m3} \cdot [R_s \,/\!/\, (1/j\omega C_s)]} \tag{23}$$

where g_{m3} and g_{m7} are the transconductance of M3 and M7, respectively. Basically, the voltage gain is determined by the g_m ratio and resistance ratio. The non-linearity of the amplifier is reduced because of the similar bias conditions for M3 (M4) and M7 (M8). The capacitor C_s is used for a gain peaking at high frequencies. So, a flat-and-linear characteristic can be realized by an open-loop amplifier. Considering that M3 (M4) and M7 (M8) have the same channel length and bias conditions, (23) can be simplified as the following equation at low frequency:

$$A_{V,\mathrm{BB}} \approx N\frac{R_L}{R_s}, \quad N = \frac{W_{\mathrm{M7}}}{W_{\mathrm{M3}}} = \frac{W_{\mathrm{M8}}}{W_{\mathrm{M4}}}. \tag{24}$$

Fig. 14 shows the simulated voltage gain of the baseband amplifier versus frequency. A −3-dB bandwidth of 4.6 GHz is achieved at 27 °C with 1.2-V supply voltage. As will be discussed later in Section IV, a mismatch in cutoff frequencies of baseband amplifiers can cause frequency-dependent I/Q mismatch. This FVF-based amplifier can relax the influence of the mismatch due to its high cutoff frequency. However, the variation of the supply voltage and temperature causes the change of the gain flatness and −3-dB bandwidth as shown in Fig. 14. It is mainly because the transistors deviate from the designed operation condition with constant-voltage biases when the temperature and supply voltage change. In practical uses, it is better to employ temperature-insensitive bias techniques and on-chip voltage regulators to mitigate those effects. Fig. 15 shows the Monte Carlo simulation results of the baseband amplifier, which estimates the influence of the random mismatch between transistors M3 (M4) and M7 (M8) on the linearity of the baseband amplifier. A ±10% random

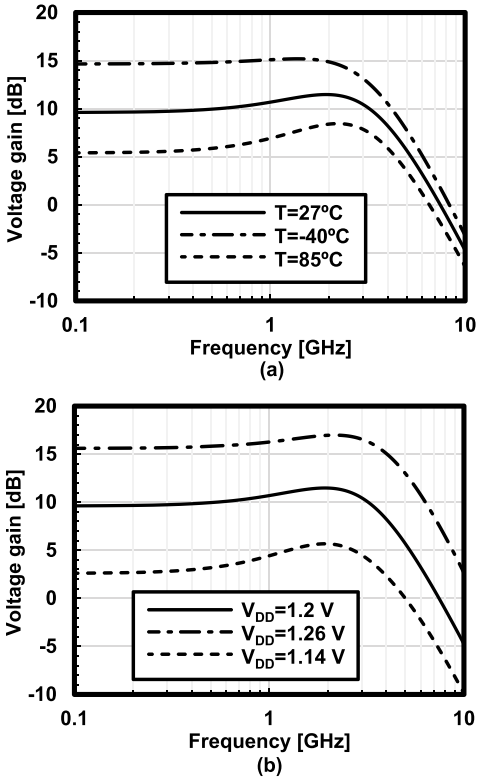


Fig. 14. Simulated voltage gain of the baseband amplifier versus frequency at (a) different temperatures with 1.2-V supply and (b) temperature of 27 °C with different supply voltages.

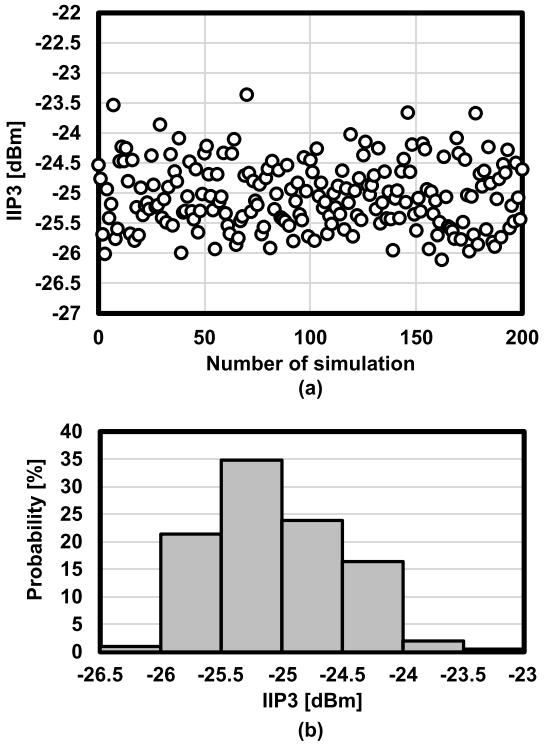


Fig. 15. Monte Carlo simulation results of the baseband amplifier. (a) Simulated IIP3 versus number of simulation. (b) Calculated probability histogram of IIP3.

mismatch among the transistors M3, M4, M7, and M8 of the second FVF stage is applied in the simulation. The simulated input third-order intercept point (IIP3) varies between

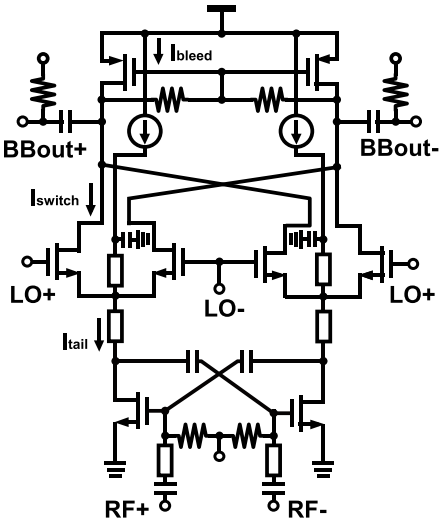


Fig. 16. Circuit schematic of the current-bleeding down-conversion mixer.

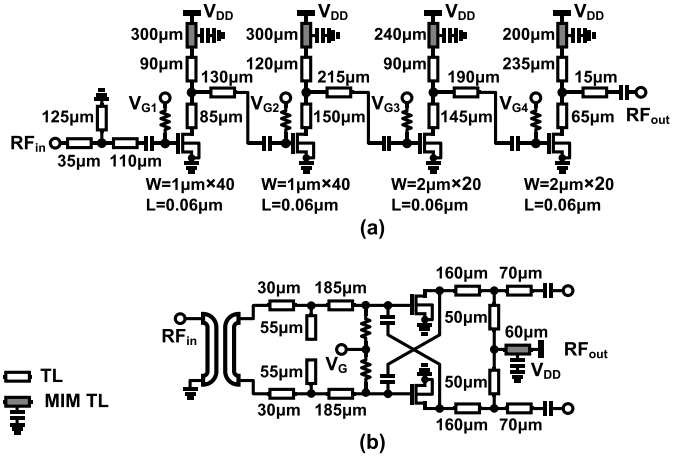


Fig. 17. Circuit schematic of (a) 60-GHz LNA and (b) RF amplifier.

−23 and −26.5 dBm considering the random mismatch, while the simulated IIP3 is around −25 dBm without the mismatch.

Fig. 16 shows the circuit schematic of the double-balanced down-conversion mixer. The input stage has a capacitive-cross-coupling for higher gain. To reduce the required LO power, a known technique called current bleeding [27] is applied, which contributes to reducing power consumption of LO buffers. The TLs are placed between the neutralized mixer input stage and the switching stage to maximize the power transfer. In the current-bleeding paths, the series TLs and shunt capacitors are used to form a high impedance at the RF frequency. The simulated IIP3 and noise figure of the mixer are −7.5 dBm and 17 dB, respectively. The estimated (averaged) input second-order intercept point from the Monte Carlo simulation is about 12.4 dBm. In this condition, the estimated SNDR at the output of the mixer is around 31 dB for a typical input power of −30 dBm, which has enough margin (about 9 dB) for the 64-QAM communication. The LNA uses a four-stage common-source topology as shown in Fig. 17(a). The input matching block of the LNA has a shunt-grounded structure for electrostatic discharge protection. The matching block

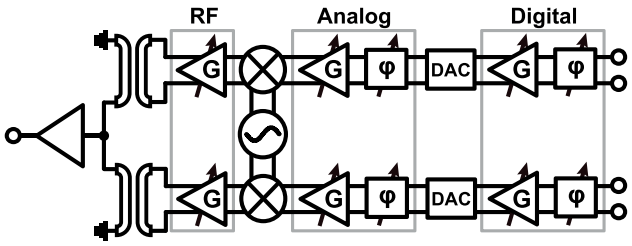


Fig. 18. Conventional I/Q mismatch calibration method.

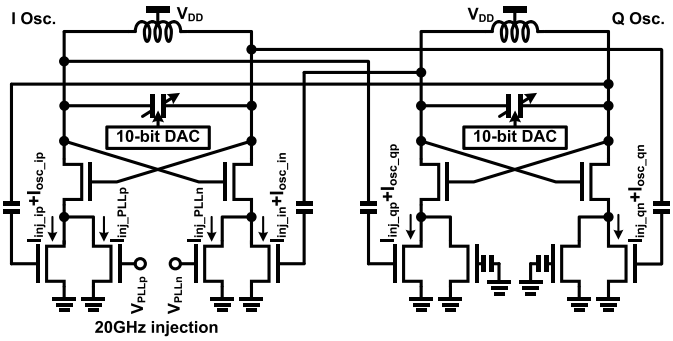


Fig. 19. Circuit schematic of the 60-GHz QILO.

is designed with low-impedance MIM TLs, 50-Ω TLs, and parallel-line transformers. The differential mismatch of the transformer is compensated by the common-mode rejection of the RF amplifiers shown in Fig. 17(b).

D. I/Q Mismatch and LO Leakage Calibration

It is known that the I/Q mismatch has significant influence on the EVM performance of the 60-GHz transceiver. Unfortunately, as shown in Fig. 18, conventional tunable RF/analog amplifiers cannot realize individual and fine-tuning for the gain and phase mismatch. Even though digital-baseband techniques can achieve fine and separate calibration of the gain and phase error, they require extra high-speed baseband circuitry with large power consumption and area penalty. A mm-Wave phase shifter using an injection-locked oscillator is reported for a phased-array receiver [28], and this technique can be applied to a QILO. A fine I/Q phase calibration is realized by adjusting free-running frequency of the QILO, and a 10-bit DAC is used for a DC-domain fine tuning of the control voltage of the QILO varactor [11], [12]. The schematic of the 60-GHz QILO implemented in this paper is shown in Fig. 19. To satisfy the phase tuning requirement, the free-running frequency of the QILO is designed to cover from 58 to 66 GHz, which is wider than the required carrier frequency range (58.32–64.8 GHz). The frequency tuning is implemented by a 3-bit switched capacitor bank and a varactor controlled by the 10-bit DAC.

Fig. 20 shows the I/Q mismatch-calibration technique used in this paper, which can realize the fine phase calibration and compensate the I/Q gain and phase errors separately. The variable-gain RF amplifiers are used for the I/Q gain calibration. A 10-bit DAC is used to tune the gate bias voltage of the RF amplifier for gain adjusting. The QILO is used as a very-fine phase shifter for the fine I/Q phase calibration.

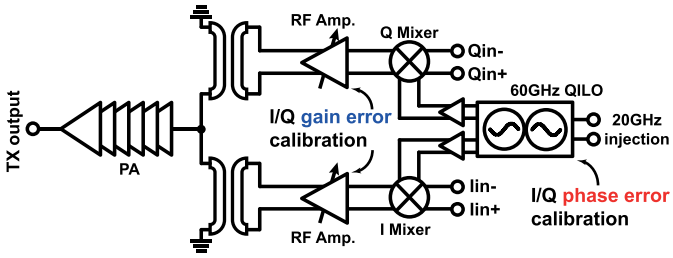


Fig. 20. Proposed I/Q mismatch calibration method.

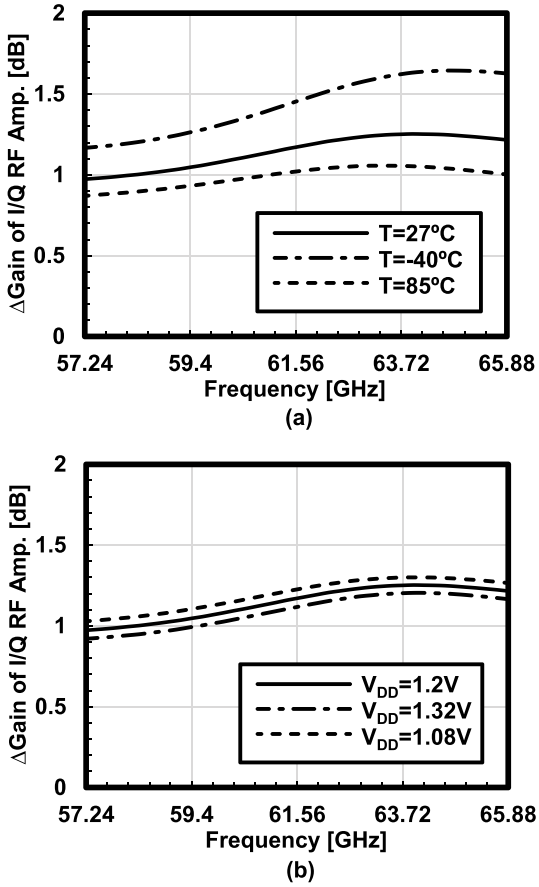


Fig. 21. Simulated gain difference of the I/Q RF amplifier when the gate bias of the I and Q amplifier is 0.6 and 0.55 V, respectively, at (a) different temperatures with 1.2-V supply and (b) temperature of 27 °C with different supply voltages.

Because the proposed phase tuning has negligible influence on the gain characteristic, individual tuning for the gain and phase mismatch can be realized. The LO leakage is minimized by adjusting the DC level at the baseband input of the TX through the current sources and shunt resistors. The whole transceivers can be calibrated by the following order: TX LO leakage, TX I/Q gain mismatch, TX I/Q phase mismatch, RX I/Q gain mismatch, and RX I/Q phase mismatch. It is worthy of knowing that the performance of the calibrated (I/Q mismatch and LO leakage) transceiver may be degraded over corners. Fig. 21 shows the simulated gain difference of the I/Q RF amplifiers, which are used for the I/Q gain mismatch calibration. The I-path amplifier is biased at 0.6 V.

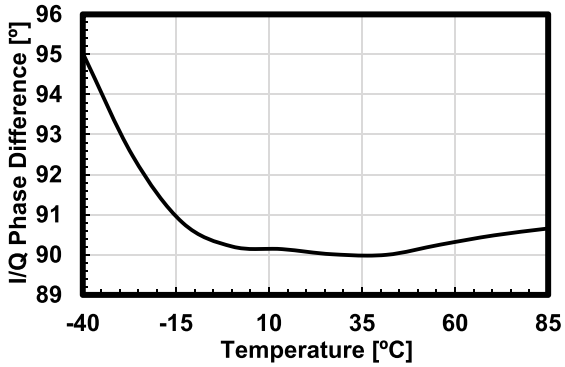


Fig. 22. Simulated phase difference between I output and Q output of the QILO at different temperatures.

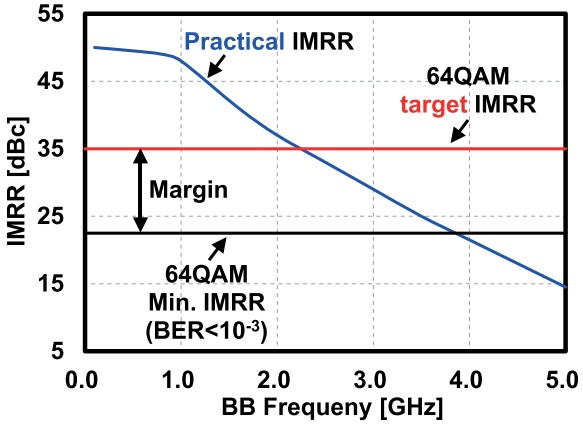


Fig. 23. Wideband I/Q mismatch challenge.

The Q-path amplifier is biased at 0.55 V. This imitates the bias-tuning operation during the calibration. It is shown that the gain difference between I and Q path is not kept the same over temperature and supply voltage variations. In the simulation, the varied gain difference can be over 0.4 dB, which causes an IMRR of worse than 33 dBc. Fig. 22 shows the simulated phase difference between I output and Q output of the QILO at different temperatures. The phase difference is optimized to 90° around the temperature of 27 °C, while, in the worst case, the phase difference is shifted to 95°, which corresponds to an IMRR of 27 dB. Therefore, a PVT-variation tolerant design [29] and automatic detection and calibration technique [30] are necessary for maintaining the system performance.

IV. Frequency-Interleaved 60-GHz Transceiver

By utilizing the techniques discussed earlier, the implemented transceiver can realize four-channel bonding with 16 QAM, which will be shown in Section V. However, it is still difficult to realize four-channel bonding with 64 QAM achieving 42.24-Gb/s data rate. One of the dominant issues is the frequency-dependent I/Q mismatch, as shown in Fig. 23. For 64-QAM four-channel-bonding applications, an IMRR of more than 35 dBc should be satisfied over 4.32-GHz bandwidth in consideration of other impairment degradations.

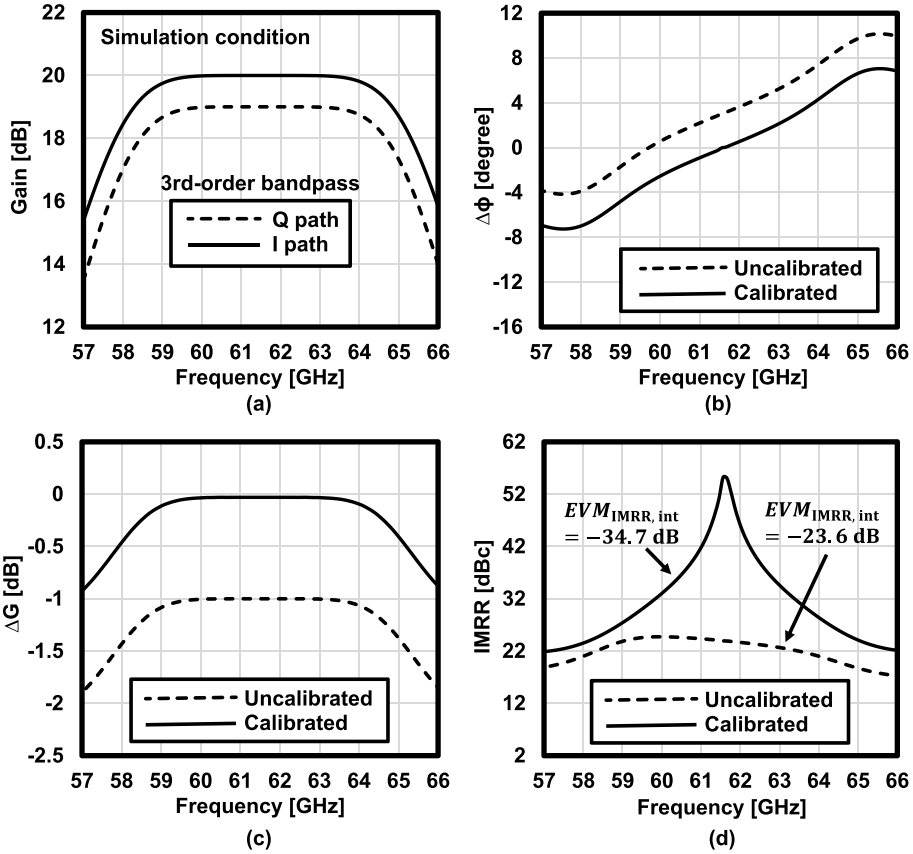


Fig. 24. Example of frequency-dependent I/Q mismatch dominated by baseband parts. (a) Un-calibrated gain characteristic of I path and Q path versus frequency. (b) Phase difference between I path and Q path versus frequency. (c) Gain difference between I path and Q path versus frequency. (d) Calculated IMRR versus frequency and $\mathrm{EVM}_{\mathrm{IMRR,int}}$ within 4.32-GHz bandwidth.

Unfortunately, the IMRR will be degraded along with the frequency even using the proposed calibration technique.

To gain more detailed insight of this issue, (2) can be extended to a frequency-dependent formation. Note that the analysis and discussion presented in the following are mainly for the SC mode. Since the I/Q mismatch can be compensated for individual sub-carriers in OFDM mode, the frequency-dependent IMRR has less effects on the system EVM.

$$|\mathrm{IMRR}(\omega)| = \left|\frac{P_{\mathrm{sig}}(\omega)}{P_{\mathrm{img}}(\omega)}\right| = \left|\frac{\gamma^2(\omega) + 2\gamma(\omega)\cos[\Delta\phi(\omega)]+1}{\gamma^2(\omega) - 2\gamma(\omega)\cos[\Delta\phi(\omega)]+1}\right| \tag{25}$$

where

$$\gamma(\omega) = \frac{\alpha(\omega)}{\beta(\omega)} \tag{26}$$

$$P_{\mathrm{sig}}(\omega) = \frac{1}{8}\left\{\alpha^2(\omega) + 2\alpha(\omega)\beta(\omega)\cos[\Delta\phi(\omega)] + \beta^2(\omega)\right\} \tag{27}$$

$$P_{\mathrm{img}}(\omega) = \frac{1}{8}\left\{\alpha^2(\omega) - 2\alpha(\omega)\beta(\omega)\cos[\Delta\phi(\omega)] + \beta^2(\omega)\right\} \tag{28}$$

where $\alpha(\omega)$ is the gain of the in-phase path. $\beta(\omega)$ is the gain of the quadrature-phase path. $\Delta\phi(\omega)$ is the phase difference between in-phase path and quadrature-phase path. $P_{\mathrm{sig}}(\omega)$ represents the desired signal power. $P_{\mathrm{img}}(\omega)$ denotes the un-wanted image power.

Therefore, an integrated EVM ($\mathrm{EVM}_{\mathrm{IMRR,int}}$) induced by the frequency-dependent I/Q mismatch can be evaluated using the following equation:

$$\mathrm{EVM}_{\mathrm{IMRR,int}} = \frac{1}{\mathrm{SNR}_{\mathrm{IMRR,int}}} = \frac{\int P_{\mathrm{img}}(\omega)d\omega}{\int P_{\mathrm{sig}}(\omega)d\omega}. \tag{29}$$

$\mathrm{SNR}_{\mathrm{IMRR,int}}$ is the ratio of the integrated desired signal power to the integrated image power over the frequency band of interest. It should be pointed out that the integrated EVM is calculated, assuming the signal tones are not correlated. This assumption gives a handy expression for a quantitative but rough estimation of the frequency-dependent IMRR issues. More accurate results should be obtained by the comprehensive system simulation and measurement.

The main cause of the frequency-dependent I/Q mismatch is the mismatch in cutoff frequencies, especially at baseband paths. Fig. 24 shows an example how the baseband mismatch and proposed calibration technique influence the IMRR and EVM of the system. It is assumed that the I path and Q path both exhibit a third-order low-pass characteristic at baseband side, which is a bandpass response referred to RF frequencies. The −3-dB bandwidth of I path is 4.1 GHz, while that of Q path is 3.9 GHz. This models the cutoff frequency mismatch, which generally occurs in baseband paths.

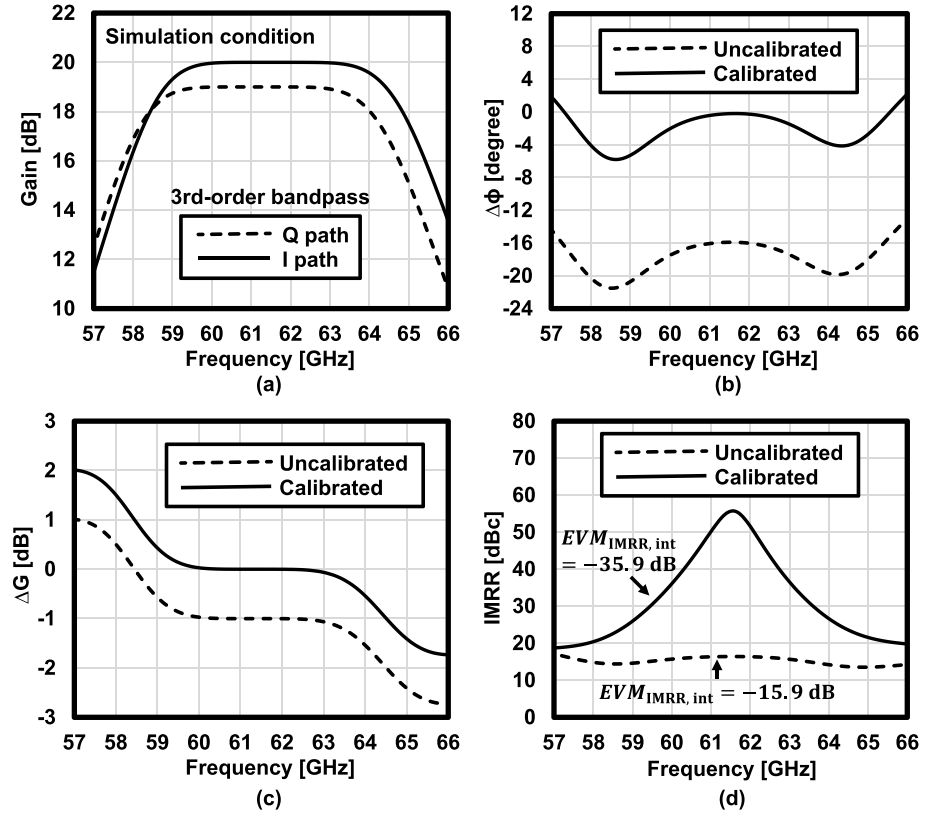


Fig. 25. Example of frequency-dependent I/Q mismatch dominated by RF parts. (a) Un-calibrated gain characteristic of I path and Q path versus frequency. (b) Phase difference between I path and Q path versus frequency. (c) Gain difference between I path and Q path versus frequency. (d) Calculated IMRR versus frequency and $\mathrm{EVM_{IMRR,int}}$ within 4.32-GHz bandwidth.

The carrier frequency is 61.56 GHz. In this example, the un-calibrated I/Q phase mismatch includes a constant phase error of 3° and phase errors caused by the cutoff frequency mismatch shown in Fig. 24(b). The un-calibrated I/Q gain mismatch is also composed of a constant gain error of 1 dB and gain errors due to the cutoff frequency mismatch shown in Fig. 24(c). It can be observed in Fig. 24(d) that the IMRR is less than 25 dBc over the 4.32-GHz frequency band of interest (two channel bonding) without calibration. The corresponding $\mathrm{EVM_{IMRR,int}}$ is about −23.6 dB, which is far from the target value of −35 dB. For demonstration simplicity, the following assumptions are made for the calibration applied in Figs. 24 and 25: 1) the phase error and gain error calibration have no mutual influence on each other and 2) the gain tuning value and phase tuning value are constant over the frequency band of interest. The calibration is performed at 61.66 GHz, where a peak IMRR is observed in Fig. 24(d). The corresponding $\mathrm{EVM_{IMRR,int}}$ is −34.7 dB over the 4.32-GHz band. It should also be pointed out that the calibrated $\mathrm{EVM_{IMRR,int}}$ is degraded to −28.1 dB if the bandwidth is extended to 8.64 GHz (four channel bonding). This gives a quantitative demonstration of the critical frequency-dependent I/Q mismatch issue for four channel bonding.

Similarly, the influence of the cutoff frequency mismatch at RF paths is modeled and exemplified in Fig. 25. Both I path and Q path show the third-order bandpass characteristic with the −3-dB bandwidth of 7 GHz at RF paths. The top-side and bottom-side cutoff frequencies of the Q path are 400-MHz lower than those of the I path. The un-calibrated I/Q phase mismatch consists of a constant phase error of 3° and phase errors caused by the cutoff frequency mismatch shown in Fig. 25(b). The un-calibrated I/Q gain mismatch is composed of a constant gain error of 1 dB and gain errors due to the cutoff frequency mismatch shown in Fig. 25(c). An obvious improvement of IMRR and $\mathrm{EVM_{IMRR,int}}$ (within 4.32-GHz bandwidth) can be observed when the calibration is conducted at 61.66 GHz. It is also shown that the frequency-dependent I/Q mismatch limits the achievable IMRR at the frequency away from the calibration point. Furthermore, 8-bit 14.08-GS/s ADCs are normally required to support the four-channel bonding in 64 QAM, which are usually realized by massive time-interleaved ADCs. The ADC may consume several hundreds of mW power, as summarized in Fig. 26 [31].

In this paper, to cope with the wideband I/Q mismatch issue and the ADC requirement, the FI architecture is implemented for the 60-GHz transceiver. Fig. 27 shows the proposed FI front-end design. The transceiver is composed of two direct-conversion FI transceivers. Each FI transceiver consists of an individual FI transmitter, FI receiver, and LO. A control-logic block is integrated to manage the operation of both FI transceivers. The two FI transceivers operate simultaneously within different frequency bands. One of the TRX is working in the low band (LB; 57.24–61.56 GHz),

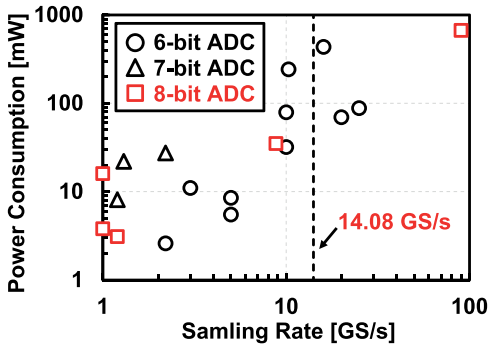


Fig. 26. Summarized ADC power consumption versus sampling rate.

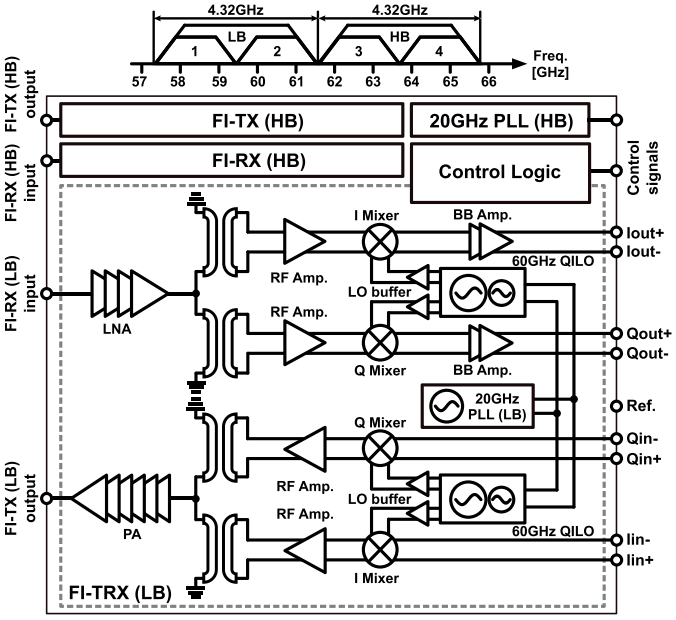


Fig. 27. Proposed 60-GHz two-stream FI transceiver topology.

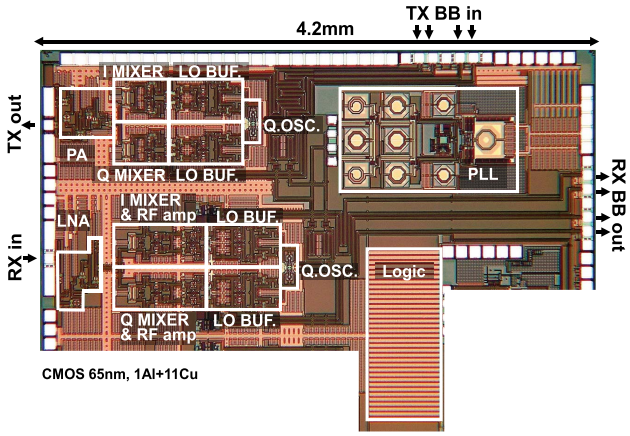


Fig. 28. Die micrograph of the 60-GHz one-stream transceiver.

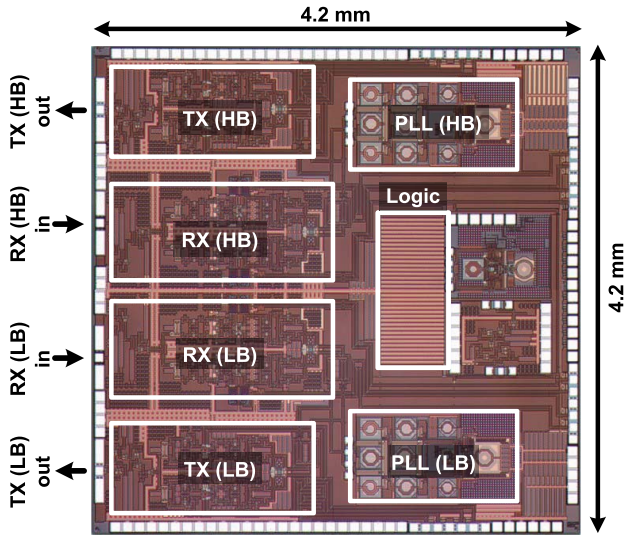


Fig. 29. Die micrograph of the 60-GHz two-stream FI TRX.

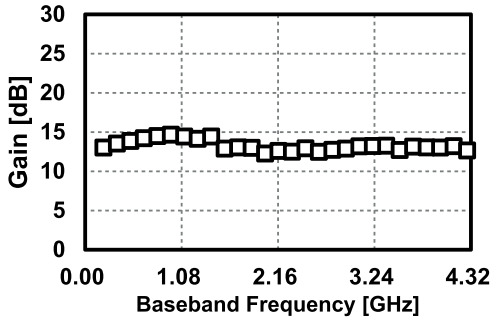


Fig. 30. Measured conversion gain of the transmitter (bottom sideband) versus baseband frequency with $f_{LO} = 61.56$ GHz.

while the other one is working in the high band (HB; 61.56–65.88 GHz). Therefore, the required bandwidth of individual FI transceiver for $EVM_{IMRR,int} < -35$ dBc is reduced from 8.64 to 4.32 GHz. The corresponding sampling rate of the ADC is also reduced to 7.04 GS/s. The architecture of each FI transceiver is similar to that of the one-stream transceiver, except the asymmetric QILO used for enhancing the locking range [10], the PA with higher P_{1dB}, the injection-locked frequency divider with wider locking range, and the baseband amplifier with improved linearity.

V. Measurement Results

Figs. 28 and 29 show the die micrographs of the 60-GHz one-stream transceiver and two-stream FI transceiver, respectively. Both RF chips are fabricated in the standard 65-nm CMOS technology. The core area of each transceiver chip is 3.85 and 7.18 mm^2, respectively. Tables II and III summarize the power consumption and area breakdown of the transceivers.

Fig. 30 shows the measured conversion gain of the transmitter. The LO frequency (f_{LO}) is 61.56 GHz, which is the center frequency of the four channels. The wide-and-flat gain characteristic is implemented by the proposed mixer-first transmitter. Fig. 31 shows the measured conversion gain of the receiver. The LO frequency (f_{LO}) is 61.56 GHz. Because the output nodes of the mixers have DC-cut capacitors, the measured bottom-side cutoff frequency is 0.27 MHz. The top side is more than 4 GHz. A very wide-and-flat gain characteristic can be observed.

TABLE II
POWER CONSUMPTION BREAKDOWN SUMMARY

		Power consumption	
		1-stream	FI (LB)
20-GHz PLL		64 mW	66 mW
TX	PA	115 mW	113 mW
	RF amplifier +Mixer	16 mW	16 mW
	QILO	19 mW	40 mW
	LO buffer	37 mW	37 mW
Total in TX mode		251 mW	272 mW
RX	LNA	41 mW	29 mW
	RF amplifier	19 mW	31 mW
	Mixer	23 mW	14 mW
	BB amplifier	30 mW	11 mW
	QILO	15 mW	35 mW
	LO buffer	28 mW	30 mW
Total in RX mode		220 mW	216 mW

TABLE III
CORE AREA BREAKDOWN SUMMARY

	Core area [mm^2]			
	TX	RX	PLL	logic
1-stream TRX	1.03	1.25	0.90	0.67
FI TRX (LB & HB)	2.03	2.56	1.93	0.66

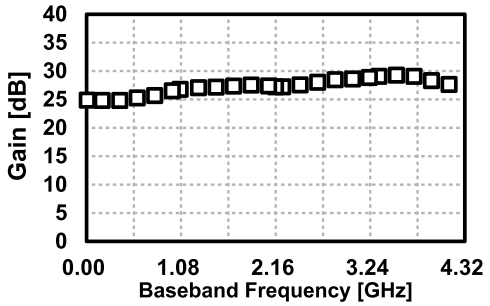


Fig. 31. Measured conversion gain of the receiver (bottom sideband) versus baseband frequency with $f_{LO} = 61.56$ GHz.

Fig. 32 shows the measured characteristics of the one-stream transceiver. Both TX and RX cover four channels. The TX conversion gain is about 15 dB, excluding the PCB loss. The saturated output power is 10.3 dBm at the center frequency of 61.56 GHz. The output power is measured for both a stand-alone PA and a transceiver chip implemented on a PCB. The PCB loss is estimated from the difference between these saturated output powers. The LO leakage is less than -47 dBc as shown in Fig. 33. The IMRR of more than 41 dB is achieved at the 0.5-GHz offset after the I/Q calibration. The PA consumes 115 mW, and the two differential amplifiers and mixers consume 16 mW. The RX conversion gain is more than 20 dB, excluding the PCB loss. The SNDR at the center frequency of 61.56 GHz is estimated from the measured third-order intermodulation (IM3) and noise figure of the RX PCB. A peak SNDR is 30.3 dB excluding the PCB loss. The power consumptions of LNA, two differential amplifiers, two mixers, and two BB amplifiers are 41, 19, 23, and 30 mW, respectively.

The phase noise measured at the TX output is -96.5 dBc/Hz@1-MHz offset from the center frequency of 61.56 GHz, as shown in Fig. 34. The measured free-running frequency of the QILO covers from 58 to 66 GHz. The 20-GHz PLL consumes 64 mW. The QILOs for TX and RX consume 19 and 15 mW, and I/Q LO buffers consume 37 and 28 mW, respectively.

Fig. 35 shows the measured TX EVM as a function of the averaged output power. An SC 16 QAM is applied with 7.04-Gb/s data rate in channel 3. The EVM approaches the optimum value of -28.4 dB around 5.4-dBm output power. It also can be observed that the TX EVM is lower than -21 dB (16-QAM requirement) for a wide output power range.

The measurement setup for the TX-to-RX performance of the one-stream TRX is shown in Fig. 36(a) and (b). Two PCBs with 14-dBi horn antennas are used. One is for TX mode and the other is for RX mode with on-board 36-MHz TCXOs. The modulated I/Q signals are generated by an arbitrary waveform generator (Tektronix AWG70002A) with the symbol rates of 1.76 GS/s (for one channel) and 7.04 GS/s (for four-bonded channel), and a roll-off factor of 25%. The TX output spectrum is measured with a spectrum analyzer and a down-conversion mixer. An oscilloscope (Tektronix DSA73304D) with an adaptive RX equalizer is used to evaluate the constellation and EVM as shown in Fig. 36(c). To estimate the required number of equalizer taps for the implemented transceiver, MATLAB simulations similar to Fig. 1 are performed. The TRX gain characteristic is modeled by the frequency response of a fourth-order FIR filter with about 10-dB variation within 7.04-GHz bandwidth. It is observed that the gain flatness of this assumption is worse than the measured TX/RX gain characteristics in Figs. 30 and 31. An RLS linear equalizer is used in the receiver for the estimation. The symbol rate is 7.04 GS/s in 64 QAM on SC mode. It can be seen that with ten taps, the equalizer can successfully suppress the gain variation between -0.4 and 0.2 dB, which leads to an EVM of -34.9 dB. Furthermore, from the literature [32], it is known that a 15-tap 28-Gb/s equalizer can be implemented in CMOS processes with reasonable power consumption and area. Therefore, the equalizer setting in the measurement equipment could be a realistic model for the baseband circuitry, which will not influence the observations and conclusions made in this paper. In this measurement, a maximum distance is defined by a TX-to-RX EVM of -9.8 dB for QPSK, -16.5 dB for 16 QAM, and -22.5 dB for 64 QAM for a theoretical BER of 10^{-3}. Figs. 37–39 show the measured constellation with spectrum, EVM, and maximum communication distance. The measured TX-to-RX EVM ($= -$SNR) in 64 QAM is less than -23.9 dB

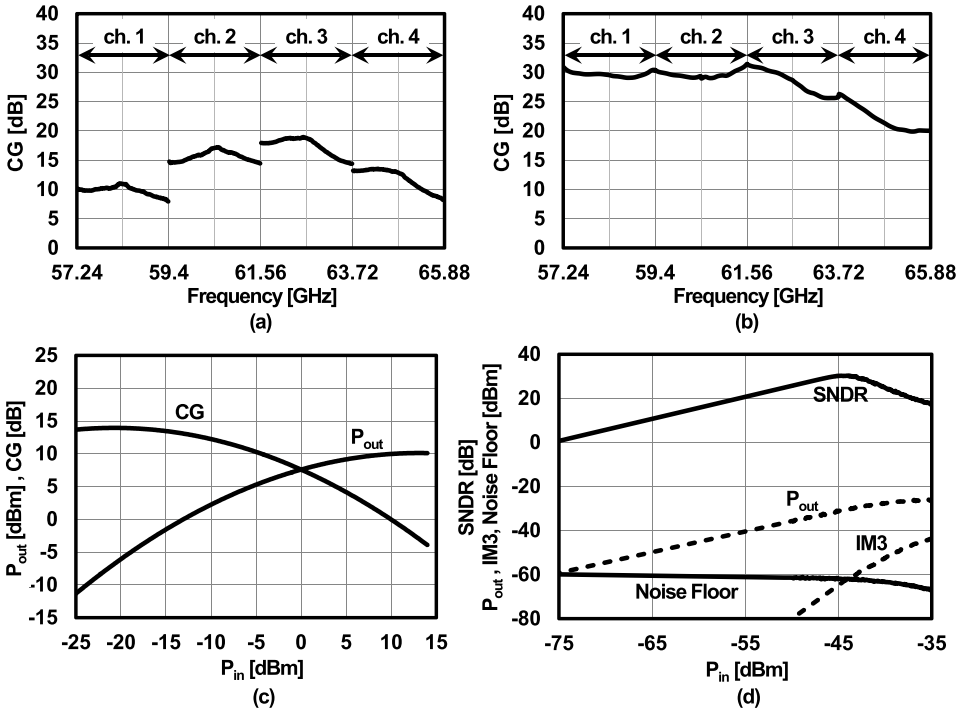


Fig. 32. Measured characteristics of the one-stream TRX front end. (a) Conversion gain of TX. (b) Conversion gain of RX. (c) Output power of TX. (d) Output power, IM3, noise floor, and SNDR of RX for channel 1.

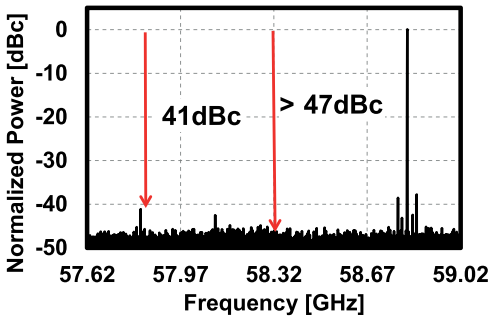


Fig. 33. Measured spectrum of the TX output with 0.5-GHz baseband input signal.

Fig. 34. Measured phase noise at the TX output with $f_{LO} = 61.56$ GHz.

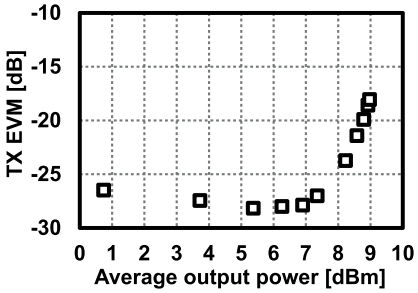


Fig. 35. Measured TX EVM with 16 QAM in channel 3.

for every channel with a data rate of 10.56 Gb/s, and −26.3 dB is achieved at channel 4. By using the four-bonded channel, 14.08 Gb/s in QPSK and 28.16 Gb/s in 16 QAM have been achieved within a BER of 10^{-3}. The maximum communication distances with 14-dBi horn antennas are 2.4, 2.0, 2.6, and 0.9 m in QPSK, 0.7, 0.6, 0.6, and 0.4 m in 16 QAM, and 0.08, 0.08, 0.13, and 0.06 m in 64 QAM for channels 1–4, respectively. All the spectrum meets the mask requirement defined in the IEEE 802.11ad/WiGig standard.

Recalling to (1), it would be interesting to have a breakdown of the measured TRX EVM and discuss the limiting factor. The measurement results for the four-channel bonding in 16 QAM are chosen as an example, since most of the required data for the breakdown have already been obtained. It is known that the measured TX-to-RX EVM and TX EVM are −17.2 and −20.0 dB, respectively. The estimated RX EVM is around −17.9 dB. Obviously, the impairments in the receiver limit the transceiver performance. Similar to Fig. 32(d), the calculated maximum RX SNDR for four-channel bonding is about 26.6 dB. The measurement equipment shows the gain

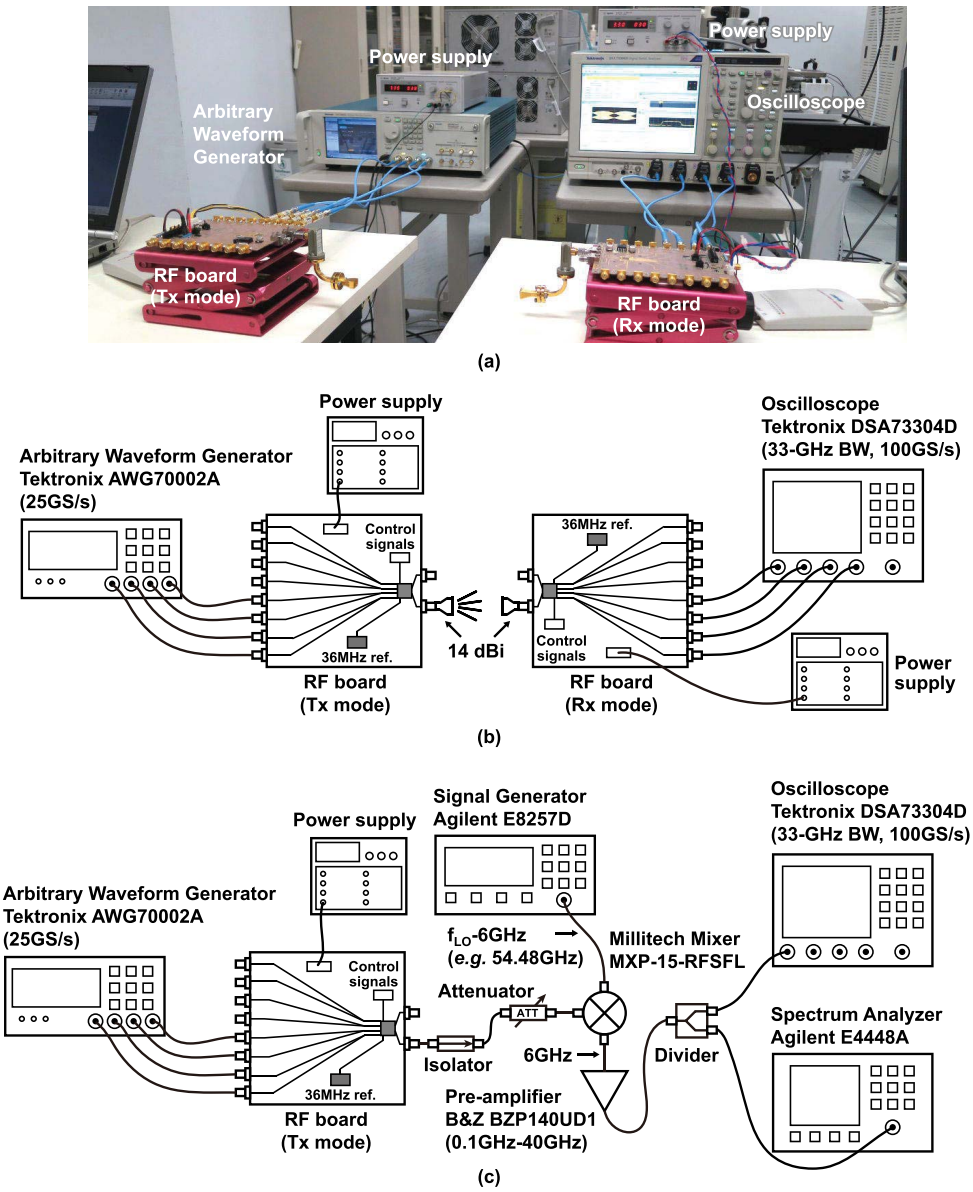


Fig. 36. (a) Photograph of measurement setup for TX-to-RX performance. (b) Measurement setup for TX-to-RX performance. (c) Measurement setup for TX performance (one-stream TRX).

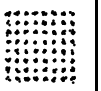
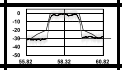
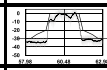
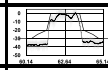
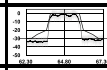
Channel/ Carrier freq.	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz
Modulation	64QAM			
Data rate	10.56Gb/s	10.56Gb/s	10.56Gb/s	10.56Gb/s
Constellation				
Spectrum				
TX output power	-0.2dBm	0.1dBm	1.8dBm	0.1dBm
TX EVM	-27.1dB	-27.5dB	-28.0dB	-28.8dB
TX-to-RX EVM	-24.6dB	-23.9dB	-24.4dB	-26.3dB
Distance	0.08m	0.08m	0.13m	0.06m

Fig. 37. Measured TX-to-RX performance in 64 QAM.

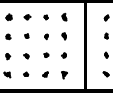
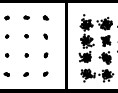
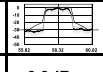
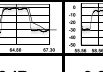
Channel/ Carrier freq.	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz	ch.1-ch.4 Channel bond
Modulation	16QAM				
Data rate	7.04Gb/s	7.04Gb/s	7.04Gb/s	7.04Gb/s	28.16Gb/s
Constellation					
Spectrum					
TX output power	6.3dBm	6.5dBm	5.4dBm	5.8dBm	3.2dBm
TX EVM	-27.8dB	-27.6dB	-28.4dB	-28.8dB	-20.0dB
TX-to-RX EVM	-24.6dB	-24.1dB	-24.6dB	-27.0dB	-17.2dB
Distance	0.7m	0.6m	0.8m	0.4m	0.07m

Fig. 38. Measured TX-to-RX performance in 16 QAM.

and phase imbalance of the received signal are 0.74 dB and 0.26°, respectively. It corresponds to an IMRR of 27.4 dB. The integrated phase noise of the carrier is −28.7 dB, considering a 400-kHz carrier tracking bandwidth. Because the influence of the LO feed-through is trivial for the receiver, it is omitted in the analysis. Therefore, the unknown impairment in (1),

Channel/ Carrier freq.	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz	ch.1-ch.4 Channel bond
Modulation	QPSK				
Data rate	3.52Gb/s	3.52Gb/s	3.52Gb/s	3.52Gb/s	14.08Gb/s
Constellation					
Spectrum					
TX output power	6.3dBm	7.3dBm	8.7dBm	6.9dBm	3.2dBm
TX EVM	-28.1dB	-27.7dB	-29.0dB	-29.7dB	-20.1dB
TX-to-RX EVM	-25.3dB	-24.5 dB	-24.5dB	-26.6dB	-17.9dB
Distance	2.4m	2.0m	2.6m	0.9m	0.3m

Fig. 39. Measured TX-to-RX performance in QPSK.

MCS	Modulation		Data rate [Mb/s]	TX EVM [dB]	
				Spec.	Meas.
9	QPSK	SC	2502.5	-15	-27.1
12	16QAM	SC	4620	-21	-27.0
24	64QAM	OFDM	6756.75	-26	-26.5

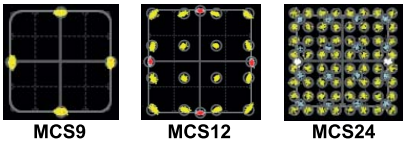


Fig. 40. Measured performance using the IEEE 802.11ad/WiGig packets in channel 3.

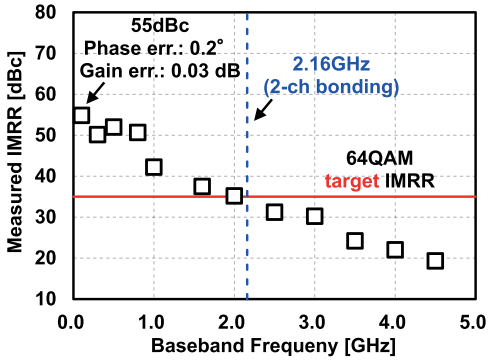


Fig. 41. Measured FI-TX (LB) IMRR versus baseband frequency.

EVM_{GF}, is estimated to be −18.0 dB, which indicates that the gain flatness of the receiver finally limits the transceiver performance.

The measurement result by using the IEEE 802.11ad/WiGig packets in channel 3 is demonstrated in Fig. 40. For MCS 9 and 12, the TX EVM is −27.1 and −27.0 dB, respectively. For OFDM MCS 24, the TX EVM is −26.5 dB, and the TX-to-RX cascaded EVM is −21.3 dB.

To demonstrate the frequency-dependent I/Q mismatch, the measured IMRR of the FI transmitter (LB) versus the baseband frequency is shown in Fig. 41. The IMRR is calibrated with 100-MHz baseband input. The optimum IMRR at the calibration frequency is 55 dBc, which corresponds to a phase error of 0.2° or a gain error of 0.03 dB. A wideband IMRR

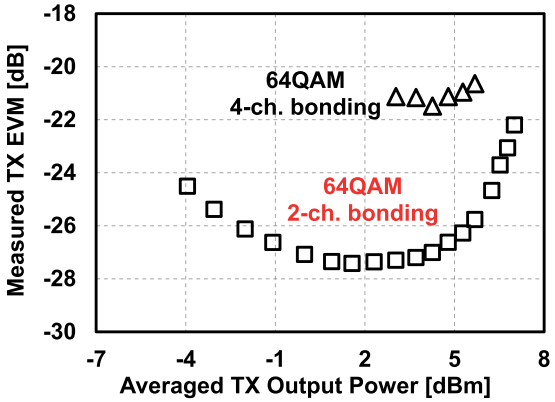


Fig. 42. Measured FI-TX (LB) EVM versus output power.

Channel/ Carrier freq.	ch.1-2 (LB) 59.40GHz	ch.3-4 (HB) 63.72GHz
Modulation	64QAM	
Data rate	21.12Gb/s	21.12Gb/s
Constellation		
Spectrum	[dB] 10 0 -10 -20 -30 -40 -50; [GHz] 55.08 57.24 59.40 61.56 63.72 65.88 68.04	
TX EVM	-27.6 dB	-27.2 dB
TX-to-RX EVM	-24.1 dB	-23.0 dB

Fig. 43. Measured constellation and performance summary of the FI TRX.

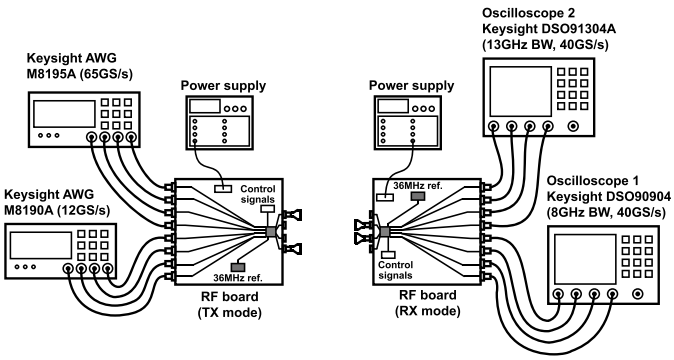


Fig. 44. Measurement setup for TX-to-RX performance of the FI TRX.

characteristic (≥35 dBc for around 2-GHz bandwidth) is also observed. However, the measured IMRR degrades prominently with the increasing of the baseband frequency, which indicates the degradation of EVM performance for direct four-channel bonding. The measured EVM of the FI-TX (LB) shows that the optimum EVM for two-channel bonding (ch.3 and ch.4) in 64 QAM is −27.4 dB, while it is only −21.5 dB for four-channel bonding, as shown in Fig. 42.

Fig. 43 shows the measured constellation and performance summary of the FI transceiver. Two PCB boards are used in the measurement, as shown in Fig. 44. One is for TX mode and the other is for RX mode. All the FI-transmitters on the PCB board in TX mode are operating during the measurement,

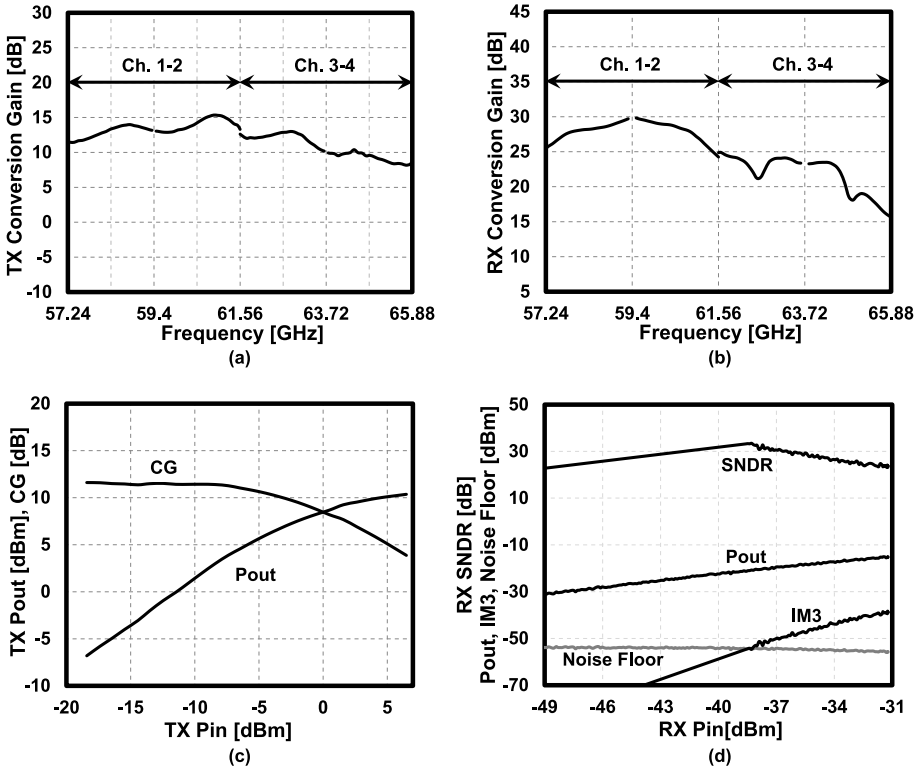


Fig. 45. Measured characteristics of the FI TRX front end. (a) Conversion gain of TX. (b) Conversion gain of RX. (c) Output power of TX. (d) Output power, IM3, noise floor, and SNDR of RX for ch.3 and ch.4 bonding.

while the FI-receivers are working on the PCB board in RX mode. The modulated baseband signals are generated by two AWGs (Keysight M8190A and M8195A) with a symbol rate of 3.52 GS/s (for two-channel bonding) and a roll-off factor of 25%. Two oscilloscopes (Keysight DSO90904 and DSO91304A) are used to evaluate the constellation and EVM performance. Horn antennas with 14-dBi gain are utilized in the TX-to-RX EVM measurement. The horizontal distance is 3 cm. The measured TX-to-RX EVM in 64 QAM is −24.1 dB for LB and −23.0 dB for HB, which satisfy the required EVM of less than −22.5 dB for a BER of 10^{-3}. The data rates for both FI-transceiver pairs are 21.12 Gb/s, which demonstrates a total data rate of 42.24 Gb/s by the FI four-channel bonding. The spectrum for each TX channel is measured using an external down-conversion mixer and the oscilloscope.

The measured RF front-end characteristics of the FI transceiver are shown in Fig. 45. Both FI-TX and FI-RX realize two-channel bonding. The conversion gain of the TX is around 10 dB excluding the PCB loss. The saturated output power is 10.4 dBm at the center frequency of 63.72 GHz. The output power at 1-dB compression point is 6.1 dBm. The RX conversion gain is over 24 dB for LB and about 20 dB for HB, excluding PCB loss. The estimated SNDR at the center frequency of 63.72 GHz for two-channel bonding is calculated from the measured output power, IM3, and noise figure of the RX PCB. The peak SNDR is 32.9 dB. The estimated sensitivity of the FI-RX is −66 and −49.3 dBm for one-channel QPSK and two-channel bonding 64 QAM, respectively. Table IV summarizes the RF front-end performance of both the one-stream transceiver and two-stream FI transceiver.

TABLE IV
RF FRONT-END PERFORMANCE SUMMARY

		1-stream	2-stream FI
TX			
	Conversion gain	13.5 dB	11.6 dB
	P_{sat}	10.3 dBm (@61.56 GHz)	10.4 dBm (@63.72 GHz)
	P_{1dB}	2.6 dBm (@61.56 GHz)	6.1 dBm (@63.72 GHz)
RX			
	Conversion gain	16 dB	18 dB
	NF	5.7 dB	5.7 dB
	IIP3	-30 dBm	-21 dBm
	Sensitivity	-66 dBm* -53 dBm†	-66 dBm* -52 dBm†
	Maximum SNDR (1-ch)	30.3 dB	35.3 dB

* For 1-ch QPSK, SNDR=9.8 dB

† For 1-ch 64QAM, SNDR=22.5 dB

Table V shows a performance comparison of the state-of-the-art 60-GHz CMOS transceivers. This paper realizes the first-reported four-channel bonding in 16 QAM and 64 QAM, which achieves the data rate of 28.16 and 42.24 Gb/s, respectively. The front end also covers all of the four channels and achieves full data rates for QPSK, 16 QAM, and 64 QAM with the best EVM.

TABLE V
PERFORMANCE COMPARISON OF 60-GHz CMOS RF FRONT ENDS

Ref.	Data rate (Modulation)	P_{out} [dBm] /antenna path	TX-to-RX EVM [dB]	Integration level	Core [mm^2]	Power consumption
This work (Tokyo Tech)	28.16 Gb/s[3] (16QAM)	8.5 @TX EVM=-21dB	-27 (1-ch.) -17 (4-ch.)	65 nm, direct conversion, TX, RX, LO (**1-stream**)	3.9	TX:251mW RX:220mW
	42.24 Gb/s[3] (64QAM)	7 @TX EVM=-22dB	-24 (LB[4]) -23 (HB[4])	65 nm, direct conversion, 2TX, 2RX, 2LO (**2-stream FI**)	7.2	TX:544mW RX:432mW
[1] Panasonic	2.5 Gb/s (QPSK)	2 @TX EVM=-22dB[5]	N/A	90 nm, direct conversion, TX, RX, LO	13.5[2]	TX:347mW RX:274mW
[2] NEC	2.6 Gb/s (QPSK)	5.2 @TX P_{1dB}	N/A	90 nm, direct conversion, TX, RX	3.4	TX:133mW RX:206mW
[3] UCB	4 Gb/s (QPSK)	N/A	N/A	90 nm, direct conversion, TX, RX, LO, BB	6.9[2]	TX:170mW RX:138mW
[4] IMEC	7 Gb/s (16QAM)	7.3[1] @TX-to-RX EVM=-15dB	-15 (1-ch.)	40 nm, direct conversion, TX, RX, LO	11.5[2]	TX:584mW RX:397mW 4 × 4 array
[5] IMEC	7 Gb/s (16QAM)	6[1] @TX EVM=-23dB	-20 (1-ch.)	28 nm, direct conversion, TX, RX, LO	7.9[2]	TX:670mW RX:431mW 4 × 4 array
[33] Broadcom	4.6 Gb/s (16QAM)	-4[1,6] @TX EVM=-23dB[5]	-20[5] (1-ch.)	40 nm, heterodyne, TX, RX, LO	26.3[2]	TX:1190mW RX:960mW 16 × 16 array
[34] SiBEAM	7.14 Gb/s (16QAM)	-2[1] @TX EVM=-19dB	-19 (1-ch.)	65 nm, heterodyne, TX, RX, LO	149.9[2]	TX:1820mW RX:1250mW 32 × 32 array
[35] Toshiba	2.6 Gb/s (QPSK)	2.6[6] @TX P_{1dB}	N/A	65 nm, heterodyne, TX, RX, LO	2.9	TX:160mW RX:233mW
[36] CEA-LETI	3.9 Gb/s (16QAM)	5 @TX P_{1dB}	-20 (1-ch.)	65 nm, heterodyne, TX, RX, LO	9.2[2]	TX:357mW RX:454mW

[1] Estimated from literature [2] Chip area [3] 4-channel bonding [4] 2-ch.
[5] Measured with integrated ADC/DAC [6] Measured with integrated TX/RX switch

VI. CONCLUSION

This paper is the first report of 64-QAM 60-GHz CMOS transceivers with four-channel bonding. The proposed one-stream TRX achieves 28.16-Gb/s data rate with an EVM of −17 dB by using a four-bonded channel in 16 QAM. A best TX-to-RX EVM of −26 dB in 64 QAM is achieved within the channel defined by the IEEE 802.11ad/WiGig standard. This performance is supported by flat gain characteristics, fine calibration of I/Q mismatch and LO leakage, and low phase noise. Moreover, with the help of the FI architecture, four-channel bonding in 64 QAM is viable for the 60-GHz transceiver, which realizes 42.24 Gb/s with reasonable power consumption.

REFERENCES

[1] T. Tsukizawa *et al.*, "A fully integrated 60 GHz CMOS transceiver chipset based on WiGig/IEEE802.11ad with built-in self calibration for mobile applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 230–231.

[2] M. Tanomura *et al.*, "TX and RX front-ends for 60 GHz band in 90 nm standard bulk CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 558–559.

[3] C. Marcu *et al.*, "A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry," in *IEEE ISSCC Dig. Tech. Papers*, Dec. 2009, pp. 314–315.

[4] V. Vidojkovic *et al.*, "A low-power radio chipset in 40 nm LP CMOS with beamforming for 60 GHz high-data-rate wireless communication," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 236–237.

[5] G. Mangraviti *et al.*, "A 4-antenna-path beamforming transceiver for 60 GHz multi-Gb/s communication in 28 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 246–247.

[6] K. Okada *et al.*, "A 60-GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE 802.15.3c," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2988–3004, Dec. 2011.

[7] K. Okada *et al.*, "Full four-channel 6.3-Gb/s 60-GHz CMOS transceiver with low-power analog and digital baseband circuitry," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 46–65, Jan. 2013.

[8] L. Kull *et al.*, "A 90 GS/s 8 b 667 mW 64× interleaved SAR ADC in 32 nm digital SOI CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 378–379.

[9] K. Okada *et al.*, "A 64-QAM 60 GHz CMOS transceiver with 4-channel bonding," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 346–347.

[10] R. Wu *et al.*, "A 42 Gb/s 60 GHz CMOS transceiver for IEEE 802.11ay," in *IEEE ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 248–249.

[11] S. Kawai *et al.*, "A digitally-calibrated 20-Gb/s 60-GHz direct-conversion transceiver in 65-nm CMOS," in *IEEE RFIC Symp. Dig. Papers*, Jun. 2013, pp. 137–140.

[12] T. Siriburanon *et al.*, "A low-power low-noise mm-wave subsampling PLL using dual-step-mixing ILFD and tail-coupling quadrature injection-locked oscillator for IEEE 802.11ad," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1246–1260, May 2016.
[13] D. Zhao and P. Reynaert, "A 40 nm CMOS E-band transmitter with compact and symmetrical layout floor-plans," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2560–2571, Nov. 2015.
[14] J. H. Kim, J. H. Jeong, S. M. Kim, C. S. Park, and K. C. Lee, "Prediction of error vector magnitude using AM/AM, AM/PM distortion of RF power amplifier for high order modulation OFDM system," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2005, pp. 2027–2030.
[15] S. Kundu *et al.*, "A 1.2 V 2.64 GS/s 8 bit 39 mW skew-tolerant time-interleaved SAR ADC in 40 nm digital LP CMOS for 60 GHz WLAN," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 8, pp. 1929–1939, Aug. 2015.
[16] Y. Tan *et al.*, "A 2.4 GHz WLAN transceiver with fully-integrated highly-linear 1.8 V 28.4 dBm PA, 34 dBm T/R switch, 240 MS/s DAC, 320 MS/s ADC, and DPLL in 32 nm SoC CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2012, pp. 76–77.
[17] K. Okada, "60 GHz WiGig frequency synthesizer using injection locked oscillator," in *IEEE RFIC Symp. Dig. Papers*, Jun. 2014, pp. 109–134.
[18] K. Okada *et al.*, "A full 4-channel 6.3 Gb/s 60 GHz direct-conversion transceiver with low-power analog and digital baseband circuitry," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 218–219.
[19] K. Okada *et al.*, "A 60 GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver," in *IEEE ISSCC Dig. Tech. Papers*, Nov. 2011, pp. 160–161.
[20] C. Andrews and A. C. Molnar, "A passive-mixer-first receiver with baseband-controlled RF impedance matching, <6 dB NF, and >27 dBm wideband IIP3," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 46–47.
[21] M. C. M. Soer, E. A. M. Klumperink, Z. Ru, F. E. van Vliet, and B. Nauta, "A 0.2-to-2.0 GHz 65 nm CMOS receiver without LNA achieving >11 dBm IIP3 and <6.5 dB NF," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 222–223.
[22] C. Andrews and A. C. Molnar, "Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 12, pp. 3092–3103, Dec. 2010.
[23] E. Nash, "Correcting imperfections in IQ modulators to improve RF signal fidelity," Analog Devices, Norwood, MA, USA, Appl. Note AN-1039, 2009. [Online]. Available: http://www.analog.com/media/en/technical-documentation/application-notes/AN-1039.pdf
[24] J. G. Baldwin and D. F. Dubbert. (May 2002). "Quadrature mixer LO leakage suppression through quadrature DC bias," Sandia Nat. Lab., Albuquerque, NM, USA, Tech. Rep. SAND2002-1316. [Online]. Available: http://prod.sandia.gov/techlib/access-control.cgi/2002/021316.pdf
[25] T. Suzuki, Y. Kawano, M. Sato, T. Hirose, and K. Joshin, "60 and 77 GHz power amplifiers in standard 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 562–563.
[26] R. G. Carvajal *et al.*, "The flipped voltage follower: A useful cell for low-voltage low-power circuit design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 7, pp. 1276–1291, Jul. 2005.
[27] W. L. Chan and J. R. Long, "A 60-GHz band 2 × 2 phased-array transmitter in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2682–2695, Dec. 2010.
[28] L. Wu, A. Li, and H. C. Luong, "A 4-path 42.8-to-49.5 GHz LO generation with automatic phase tuning for 60 GHz phased-array receivers," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2309–2322, Oct. 2013.
[29] T. Tsukizawa *et al.*, "A PVT-variation tolerant fully integrated 60 GHz transceiver for IEEE 802.11ad," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 123–124.
[30] J. Pang *et al.*, "A 128-QAM 60 GHz CMOS transceiver for IEEE 802.11ay with calibration of LO feedthrough and I/Q imbalance," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 424–425.
[31] B. Murmann. (Jul. 2016). *ADC Performance Survey 1997–2016*. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html
[32] J. F. Bulzacchelli *et al.*, "A 28-Gb/s 4-tap FFE/15-tap DFE serial link transceiver in 32-nm SOI CMOS technology," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3232–3248, Dec. 2012.
[33] M. Boers *et al.*, "A 16TX/16RX 60 GHz 802.11ad chipset with single coaxial interface and polarization diversity," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 344–345.
[34] S. Emami *et al.*, "A 60 GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 164–165.
[35] T. Mitomo *et al.*, "A 2 Gb/s-throughput CMOS transceiver chipset with in-package antenna for 60 GHz short-range wireless communication," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 266–267.
[36] A. Siligaris *et al.*, "A 65 nm CMOS fully integrated transceiver module for 60 GHz wireless HD applications," in *IEEE ISSCC Dig. Tech. Papers*, Mar. 2011, pp. 162–163.

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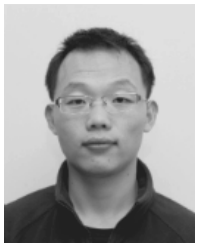

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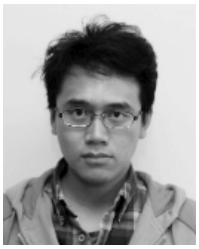

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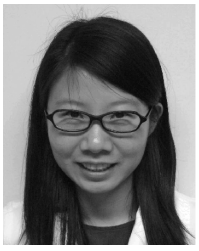

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