A 2 × 70 W Monolithic Five-Level Class-D Audio Power Amplifier in 180 nm BCD

Mikkel Høyerby, *Member, IEEE*, Jørgen Kragh Jakobsen, *Member, IEEE*, Jesper Midtgaard, *Member, IEEE*, and Thomas Holm Hansen, *Member, IEEE*

***Abstract*— A 2 × 70 W from 24 V into 4 Ω class-D audio power amplifier in 30/40 V 180 nm bipolar CMOS DMOS is presented. The device employs a flying capacitor (FC) three-level half bridge topology to reduce switching frequency and filter/load power losses in near-idle operation. This is combined with a fourth-order analog feedback system for shaping noise introduced by the digital FC voltage control loop. A power-efficient gate drive scheme suitable for power converters with multiple floating switching devices is also presented, including a compact fast low-power *dV/dt* robust high-voltage level shifter circuit. Power-efficient operation from idle to full-power operation is demonstrated along with a very high audio performance of 0.003% THD + N at 10 W/1 kHz into 4 Ω.**

***Index Terms*— Audio power amplifier, bipolar CMOS DMOS (BCD), gate drivers, multilevel, multiphase.**

I. Introduction

THE class-D audio power amplifier market and technology has matured over the last 15–20 years following the initial push to bring viable products to the mass market [1]–[9]. With the audio bandwidth remaining a constant 20 Hz–20 kHz in combination with the high-efficiency numbers (more than 90% at full load) and more than adequate audio performance (total harmonic distortion, THD, and noise) available from first-generation integrated circuit products, the motivation for improving the core amplifier technology shifts to different parameters. One performance parameter that has gained importance is the near-idle power consumption of the amplifier, especially in the relatively newly introduced wireless battery-powered loudspeaker product class, and of course in the now-ubiquitous smartphone application.

Compactness of the overall amplifier solution (IC and support passives) is also gaining importance due to the continuously shrinking form factors of consumer electronics. The physical footprint of first generation amplifier solutions in the 20 W+ power class tends to be dominated by output EMI filter inductors. Some effort has been done in prior art to improve in first-generation technology (shift from AD to BD [10], [11] and ternary [12], [13] modulation), but room for improvement remains.

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The authors are with Merus Audio, 2730 Herlev, Denmark (e-mail: mh@merus-audio.com).

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This paper hence (in expansion of [14]) presents an integrated class-D audio amplifier solution that aims to maintain the good properties of first-generation products while significantly improving on near-idle power loss and solution footprint. To this end, a multilevel power stage is adopted, to provide design room for improvement through fundamentally reduced high-frequency content in the pulsewidth-modulated (PWM) output waveform and inherent multiplication of device switching frequency [15]. This is combined with digital management of operation parameters, a solution afforded by the availability of relatively high logic density in a contemporary bipolar-CMOS-DMOS (BCD) process.

II. Power Topology

The three-level flying capacitor (FC) half bridge topology [14]–[20] adopted for the work presented in this paper is illustrated in Fig. 1(a). Interestingly, the first report [16] of this topology predates the proliferation of the class-D audio power amplifier.

The effective functionality of this half bridge (two sub-bridges and a summation element) is also illustrated in [Fig. 1(b)]. For the bridge-tied load (BTL) application in Fig. 1(c), a total of four PWM phases are used, leading to the five-level output capability illustrated in Fig. 1(d). Fig. 1(a) also shows the almost-dc output pattern in near-idle operation, which under such conditions ensures near-zero power loss in the speaker and/or output filter shown in Fig. 1(c). Most prior art [5], [8], [20] uses the ripple current in the output filter inductor for achieving soft switching of the output stage during dead time in near-idle operation, an exactly opposite approach to the zero-ripple solution presented in this paper. Some prior art [13] adopts reduced-ripple modulation schemes to reduce idle loss, at the cost of adding significant common-mode content to the output PWM pattern, degrading audio performance due to finite common-mode rejection ratio (CMRR) of the analog feedback system. In soft-switching (auto commutating) prior art, the ripple current in the filter inductor is significant, leading to a tradeoff between size and core loss [21] due to hysteresis losses in the core material. This issue is relieved in the presented amplifier, allowing physically small filter inductors to be used with a reduced idle loss penalty. Another benefit of the multilevel power stage is the fourfold switching frequency multiplication seen from the BTL output. As an example, 660 kHz switching across the load is realized with only 165 kHz switching of each output transistor, limiting the power loss impact of output transistor capacitances.

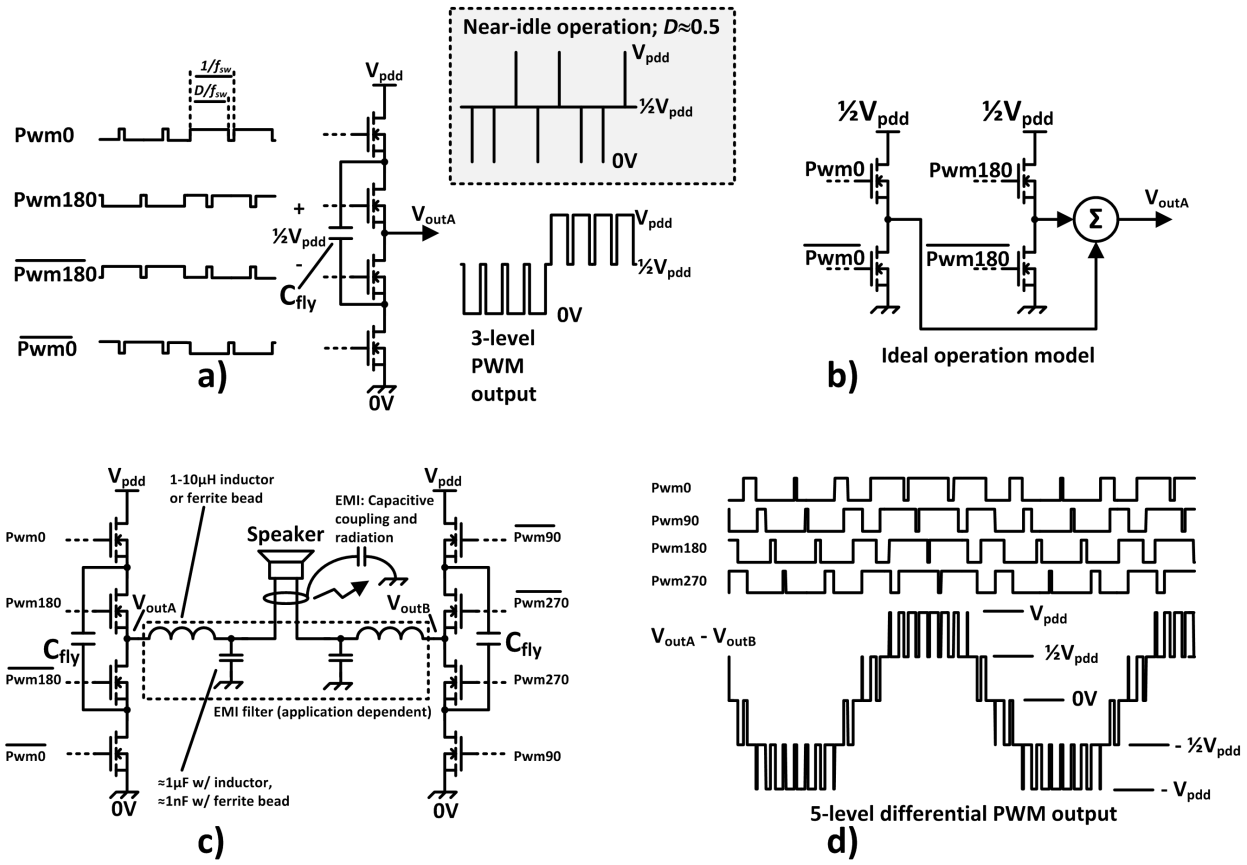

Fig. 1. Three-level FC half bridge, its operation, and application in a BTL class-D audio power amplifier. (a) Topology. (b) Operation model. (c) BTL power amplifier application. (d) Five-level modulation.

A feature of most proposed high-power multilevel half bridge topologies [15] (including FC, neutral-point clamp, and cascade) is the systematic sharing of switch voltage stress. In a lower powered integrated device, this can be put to use by allowing the output transistors to be rated at less than the power rail voltage V_{pdd}. Depending on technology, this reduces the area penalty otherwise incurred for increasing the number of output switching devices. In the used 180 nm 30/40 V BCD technology from Dongbu Hitek, the specific on-resistance differs by a factor of around three between a 30 V NLDMOS and a 16 V NLDMOS, leading to a manageable area penalty of +33% for a half bridge with four half-resistance 16 V NLDMOS devices instead of the usual two 30 V NLDMOS devices at nominal resistance.

The greatest penalty from using an FC half bridge is thus not necessarily area, but rather the presence of an FC. It turns out that the FC can be an SMT component of manageable size (0805 or smaller), provided that its voltage is balanced by an effective control system, which becomes one of the main challenges in creating a viable and compact design.

III. Resampling Noise Analysis

In this paper, FC voltage balancing is achieved using the redundant state selection (RSS) [22], [23] method. In this scheme, a controller is inserted to modify the usage of the (redundant) switch states [see Fig. 2(a)] that generate the same output level. To control the assignment of switch states without glitches, the presented design (like prior art [22], [23]) uses synchronous digital logic. In an analog PWM amplifier, this necessitates resampling (synchronization) of the analog PWM stream to a much faster digital clock. This introduces time quantization errors, adding white quantization noise to the PWM stream.

For a single-phase analog PWM stream $V_{\text{pwm},A}$ of frequency f_{sw}, resampled by calculation clock f_s, assuming no correlation between PWM and clock transitions, the resampling error of each PWM transition leads to a uniformly distributed error with the range $0–f_s^{-1}$, as illustrated in Fig. 3. The sampling of the analog PWM signal can be considered a quantization process with a quantization step Q of

$$Q = \frac{2f_{\text{sw}}}{f_s}.$$

The power of the quantization error within a bandwidth of f_a is

$$p_e = \frac{Q^2}{12} \times \frac{f_a}{f_{\text{sw}}} = \frac{f_{\text{sw}} f_a}{3f_s^2}.$$

Assuming 100% usable modulation range in the PWM stream, sinusoidal audio signal power p_s is up to 1/8. This leads to a signal-to-quantization noise ratio (SQNR) of

$$\text{SQNR} = 10\log_{10}\left(\frac{p_s}{p_e}\right) = 10\log_{10}\left(\frac{3f_s^2}{8f_{\text{sw}}f_a}\right).$$

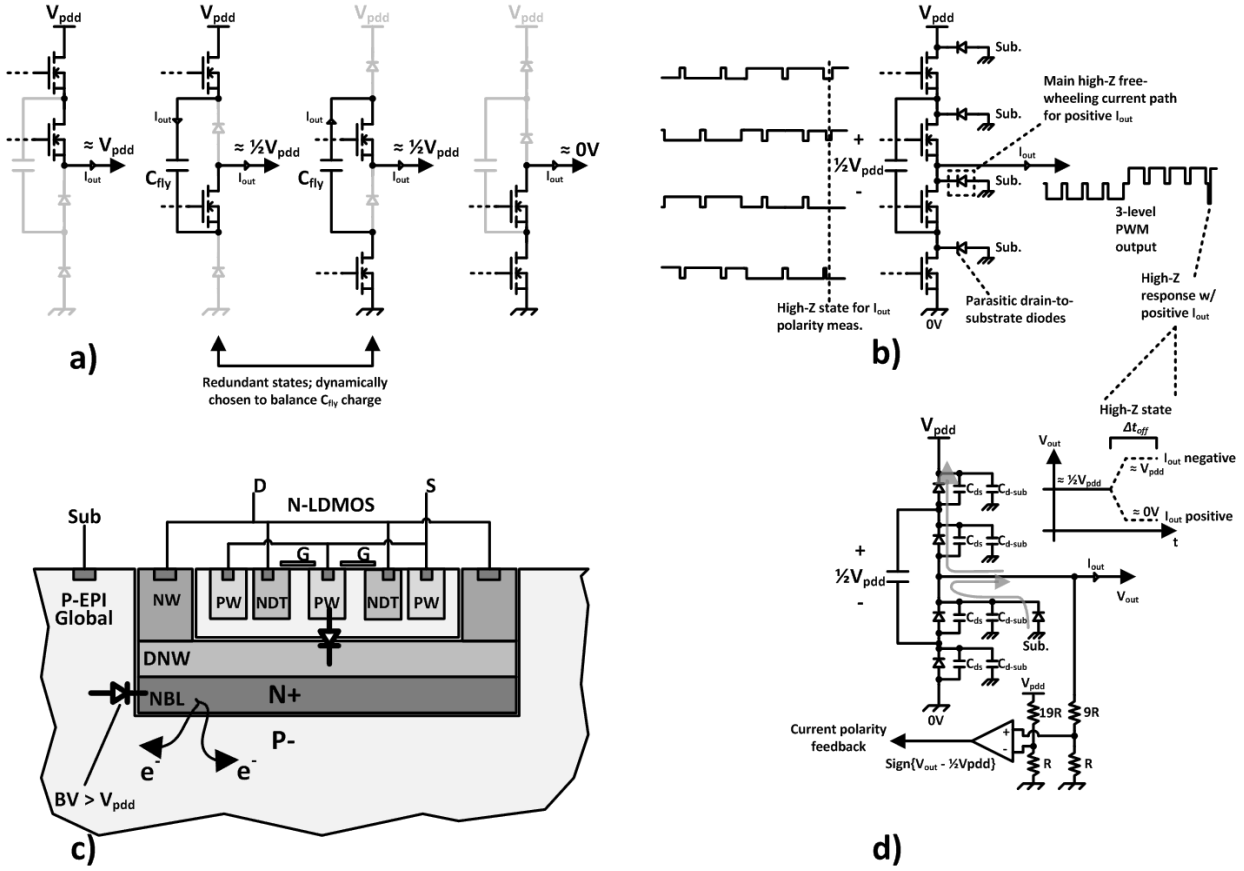

Fig. 2. Redundant-state selection scheme and output current polarity measurement scheme. (a) Four main power stage states. (b) High-impedance (high-Z) state insertion scheme. (c) Drain-substrate parasitic diode in N-LDMOS. (d) Output current polarity sensing during high-Z state.

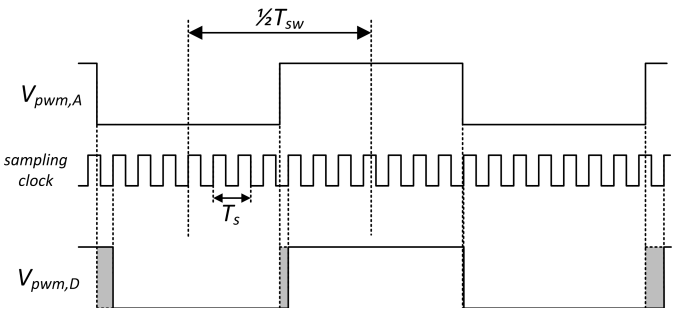

Fig. 3. Quantization noise introduced by digital sampling of analog PWM stream.

In a system with N-phase PWM, the quantization noise of the N parallel quantization processes is uncorrelated, whereas the signal power is 100% correlated. This leads to

$$\mathrm{SQNR}(N) = 10\log_{10}\left(\frac{3Nf_s^2}{8f_{\mathrm{sw}}f_a}\right).$$

For the design choices of $f_s = 100$ MHz, $f_{\mathrm{sw}} = 150$ kHz, and $N = 4$ for five-level modulation, and given the audio bandwidth $f_a = 20$ kHz, SQNR evaluates to 67 dB. This means that a significant (but realistic) amount of analog feedback loop error suppression (33 dB or more) is required to bring the unweighted amplifier SNR above 100 dB.

IV. Output Current Polarity Sensing

An important part of the RSS decision process is knowledge of the amplifier output current polarity (assumed constant over a switching cycle), since this determines the mapping between redundant states and FC current polarity [as illustrated in Fig. 2(a)].

Due to the inductive character of a typical loudspeaker and the fact that only ac current is to be driven into the loudspeaker, the polarity of the amplifier output current can only be known by measurement. Using a voltage sensed across a resistive element (a physical resistor or a power transistor in the triode region) has the drawback of producing a relatively small voltage for small output currents, making sensor offset a nuisance. A more digital-centric scheme, which is compatible with sensors used for FC voltage sensing, is the introduction of high-Z (all-off) events in the output stage, along with observation of the freewheeling potential of the output node. The scheme is illustrated in Fig. 2(b). A key feature of this scheme is the potential for accurate determination of the polarity of small output currents. If we consider the half bridge with all four output transistors turned off [as in Fig. 2(d)], the amount of capacitance seen from the output node is

$$C_{\mathrm{out}} = C_{ds} + C_{d\text{-sub}}.$$

Now, when output current I_{out} flows from the output node for a high-Z event duration of Δt_{OFF}, the output node voltage

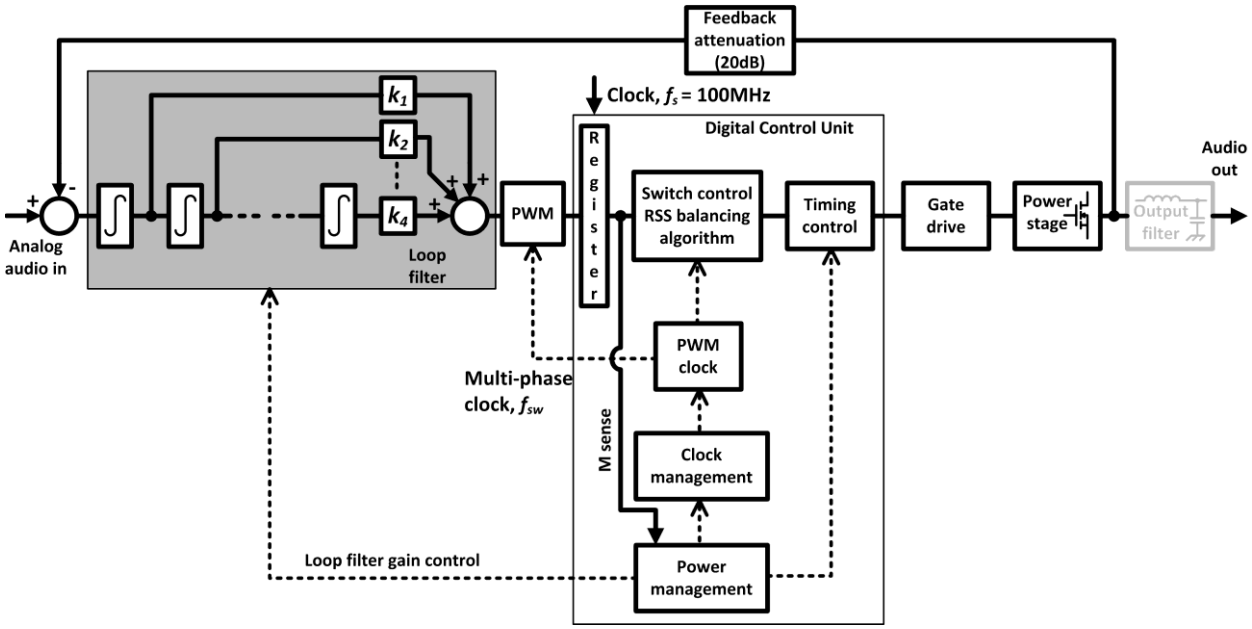

Fig. 4. Overall amplifier architecture with audio feedback loop and semidigital forward path with power management subsystem.

will (unless clamped) change by voltage ΔV_{out}

$$\Delta V_{\text{out}} = -\frac{\Delta t_{\text{OFF}} I_{\text{out}}}{C_{\text{out}}}.$$

If we assume that a minimum voltage change of $\Delta V_{\text{out}} = 2$ V can be resolved correctly (easy if V_{out} is initially near $(1/2)V_{\text{pdd}}$, which here is ensured by digital control of the switching pattern) along with $C_{\text{out}} = 200$ pF and allow a high-Z duration $\Delta t_{\text{OFF}} = 20$ ns, then output current magnitudes down to 20 mA can be correctly resolved. For a reasonable 50 mΩ (the NLDMOS on-resistance of the presented design) sensing resistor-based solution, such a current would require less than 1 mV sensor offset, which would mandate the use of offset-cancellation techniques. In a junction isolated BCD process, the NLDMOS drain will have a parasitic diode from drain to substrate [see Fig. 2(c)]. When high-Z patterns are inserted, the output current will sometimes be driven though this diode as illustrated in Fig. 2(b) and (d). This creates an extra-large substrate noise problem, which must be dealt with by guard ring insertion, isolation of low-noise circuitry, and careful floorplanning.

V. Power Management Control System

The choice of modulation type, switching frequency, and dead time in two-level half-bridge-based class-D audio power amplifiers involves many tradeoffs between EMI performance, audio performance, idle efficiency, and full-power efficiency. Using an FC half bridge adds the concerns of FC size, ripple, and balancing. The most desirable tradeoff will vary with output power level; as an example, it is desirable to increase switching frequency with output power to avoid excessive FC voltage ripple. The presented design therefore has a digital subsystem for managing switching frequency, modulation type, dead time, loop filter response, and FC balancing parameters based on a detected modulation index M. M is detected and averaged by a counter-based state machine, producing an output sample every 100 μs. A comparison of M against fixed thresholds is performed to select the amplifier operating parameters, with hysteresis added to eliminate chattering between operating regions. As shown in Fig. 4, this subsystem fits well into the already digital PWM forward path.

VI. Multiphase Analog PWM Loop

The three-level FC half bridge can be considered as two two-level half bridges and a summation element [illustrated in Fig. 1(b)], so the applicability of multiphase PWM is obvious, as also observed in prior art. For a full BTL amplifier, four PWM phases can be used. The use of multiple PWM phases provides an increase in the ratio of maximum loop bandwidth to per-phase switching frequency. From a discrete-time perspective [24], [25], this can be attributed to the N-fold increase in sampling rate from using N interleaved PWM streams. Alternatively, the decreased PWM step size (a factor of N when going from 1 to N PWM phases) can be considered to result in N times lower dV/dt in the analog PWM input ripple, allowing the expression of [11] (9) to be modified to

$$f_0 < \frac{N f_{\text{sw}}}{\pi}$$

where f_0 is the unity-gain bandwidth (not taking into account the gain reducing effect of feedback ripple on the comparator sampling gain [24]) and f_{sw} is the per-phase switching frequency. For a minimum f_{sw} of 150 kHz and four PWM phases, this means that feedback loop bandwidth can still be more than 100 kHz, allowing sufficient suppression (>33 dB at 20 kHz) of the PWM resampling noise with a fourth-order loop filter. For the case of three-level modulation, N is reduced to 2, doubling the minimum f_{sw} to 300 kHz for the same f_0 target.

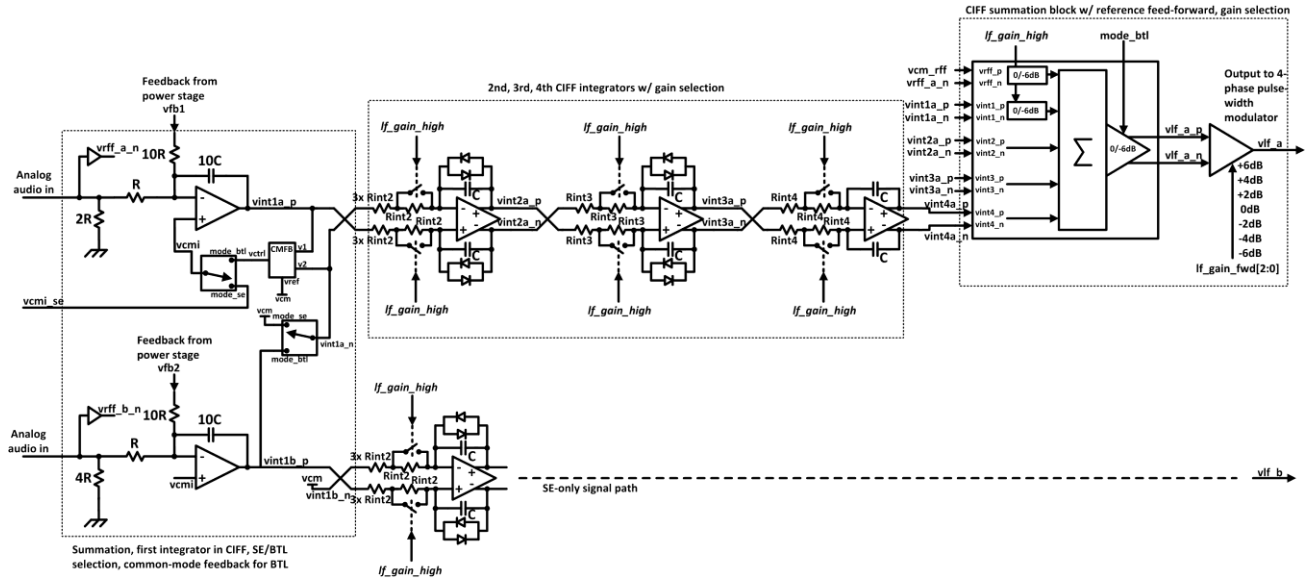

Fig. 5. Fourth-order SE/BTL loop filter with frequency response scalable by lf_gain_high control bit.

VII. Fourth-Order SE/BTL Loop Filter

To facilitate the typical BTL usage case as well as the more rare single-ended (SE) case with minimum area overhead, the designed loop filter (see Fig. 5) uses a first summation/integration stage with two separate operational amplifiers and a switchable common-mode feedback circuit. This allows the loop filter to be configured for differential input (for BTL) or for SE input. Two sets of higher order integrators and summation for the CIFF structure are still needed, but these are each significantly smaller than the first integration stage. To accommodate different loop bandwidths [26] (and audio performance versus power tradeoffs), the frequency response of the loop filter can be shifted (in frequency) by a factor of two by the *lf_gain_high* control bit. This is done by effectively changing all integrator time constants with a factor of two. All integrator time constant changes are implemented by altering the *RC* integrator resistances rather than capacitances, in order to avoid changes to the states of the integrators. For the first integrator, the noise of the feedback resistor is a key part of the system noise performance, and hence it is not desirable to switch its value. The gain change function of integrator 1 is therefore pushed forward to the second integrator and the summation block. By having all gain switching functionality performed without changing integrator states [26], the loop bandwidth of the feedback system can be changed dynamically without audible impact. No effort was made in the loop filter design to avoid aliasing distortion [9], [27], which can be minimized by shaping the loop filter frequency response to produce feedback ripple to triangular shape [28]. In order to make room for variations in forward path gain, a loop filter shape close to that given in [29] was adopted, giving the system error transfer function a nominal Bessel-like response.

VIII. Drain-Scavenging Gate Driver

A key problem introduced with an all-NMOS FC high-voltage power stage is that of driving the gates. In conventional two-level half bridges, only the high-side NMOS [5], [20] requires a floating gate driver and associated power source (classically an external bootstrap capacitor) for the gate charge. In the presented topology, however, three out of four of the NLDMOS devices need a floating gate driver, making the use of bootstrap capacitors in a stereo BTL device unattractive due to pin/component count (12 extra pins and 12 extra capacitors.) Hence, a solution with higher integration is necessary. Prior art [12] has demonstrated the practicality of using a charge pump for generating a single high-voltage supply node that is used by the floating driver cells. The use of a linear regulator for dropping excess voltage presents an additional and substantial power loss. Fortunately, this power loss scales with driver current consumption, which is possible to manipulate by design and architecture. The overall structure of the floating high-side gate driver is shown in Fig. 6.

An add-on solution presented in [14] and [30] and shown in Fig. 7 is to reduce the HV rail current consumption for gate charging by sourcing as much of the gate charge from the drain node of the power transistor. This reduces the system power loss since the voltage drop across the series regulating element is much reduced. The signal processing functions needed to perform the changeover from source gate charge between the available sources is limited to a single comparator (implemented as a dynamically biased common-source amplifier using the device *MP* in Fig. 7) and a state machine. Thus, the average power consumption of this subsystem scales with switching frequency. It was found by simulation that a near-idle ($I_{\text{out}} \approx 0$ A) reduction in gate turn-on power of 25% was achieved with the drain-scavenging approach.

IX. High-Voltage Level Shifter

The use of complex multilevel half bridge topologies invariably leads to an increase in the number of floating gate driver channels. A good portion of the area of a floating gate driver is occupied by high-voltage level shifters, where the high-voltage

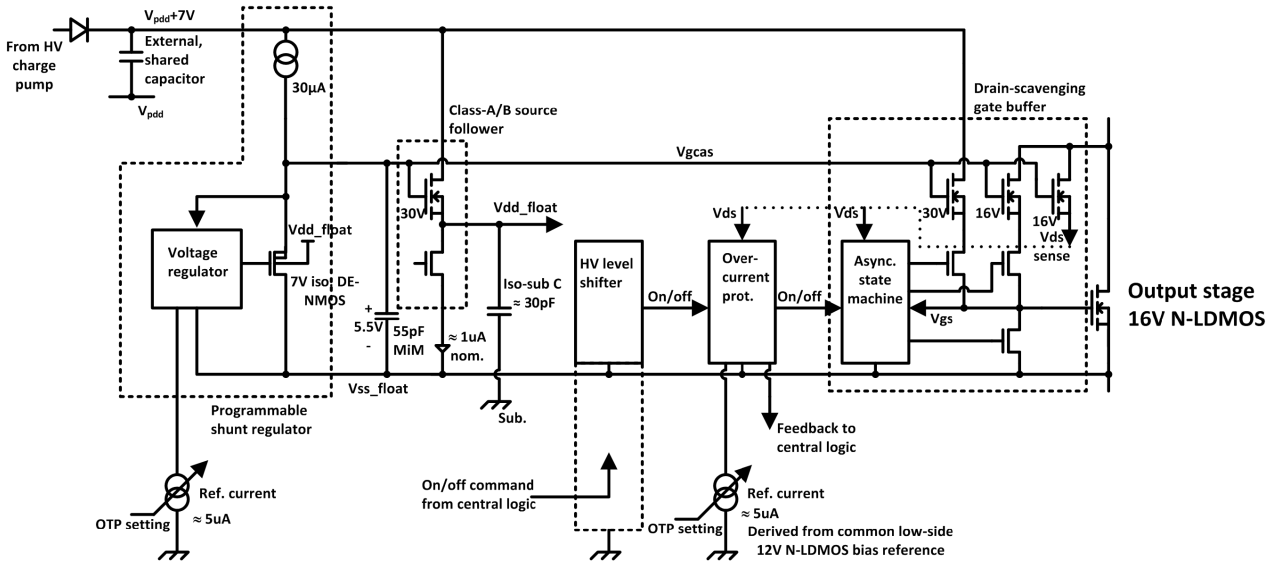

Fig. 6. Floating gate driver with local supply regulator and drain-scavenging gate buffer.

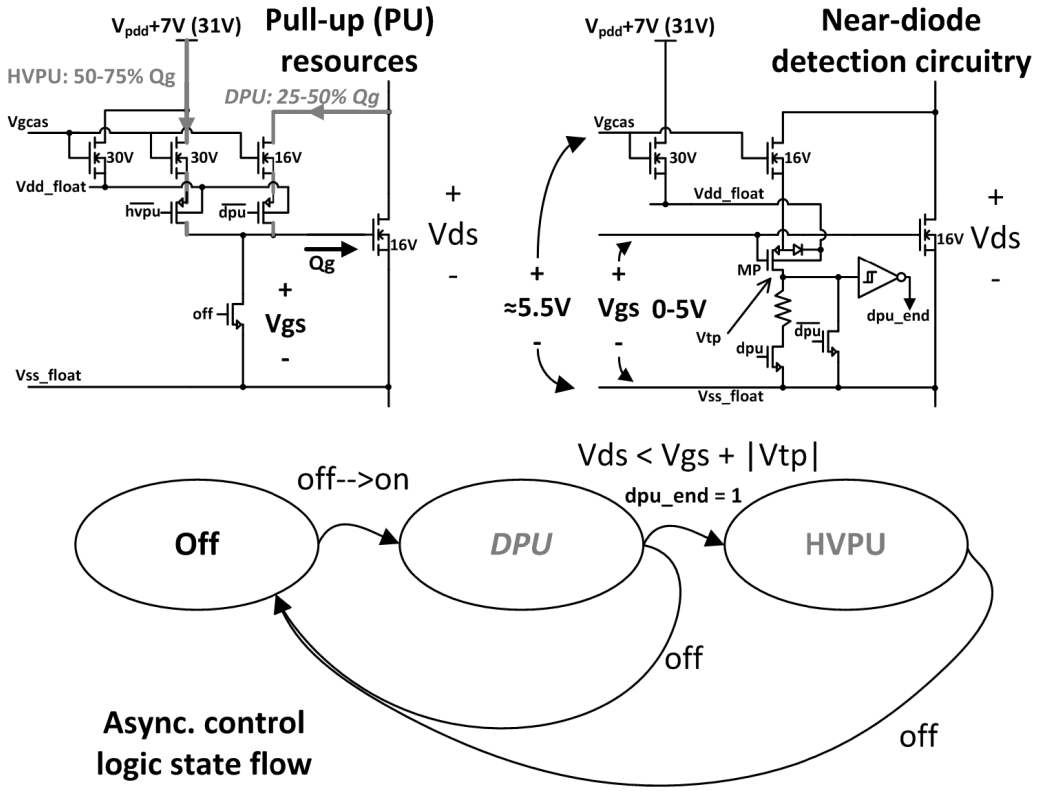

Fig. 7. Drain-scavenging gate buffer and control scheme.

devices (due to high-voltage spacing rules) easily take up 50% of the total area. For this design, a high-voltage level shifter using only two high-voltage devices was created, as shown in Fig. 8.

Unlike the conventional digital-style level shifter [5], both drain nodes of the low-side DE-NMOS devices are always at low impedance (due to diode-wired high-side receiver devices), speeding up transitions. In order to reject disturbances (electron injection from the power stage to the exposed drain of the DE-NMOS or displacement currents caused by switching of the Vss_float node), the current signaling scheme is differential, and signaled currents are subtracted to cancel out disturbances. For symmetry, two current outputs are provided and for maximum supply range. The supply range (Vss versus Vss_float) is maximized by having a low signal swing on the high-side current receiver, which is operating near the Vdd_float potential. Thus, for a high-side floating supply of 5 V, the circuit is capable of operating even with

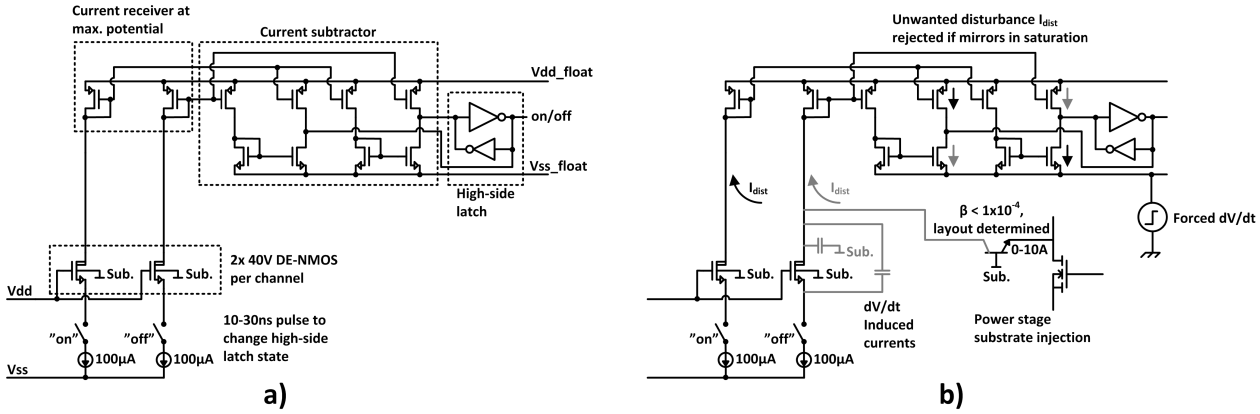

Fig. 8. High-voltage level shifter and rejection of injected disturbances. (a) Circuit subelements. (b) Disturbance injection and rejection.

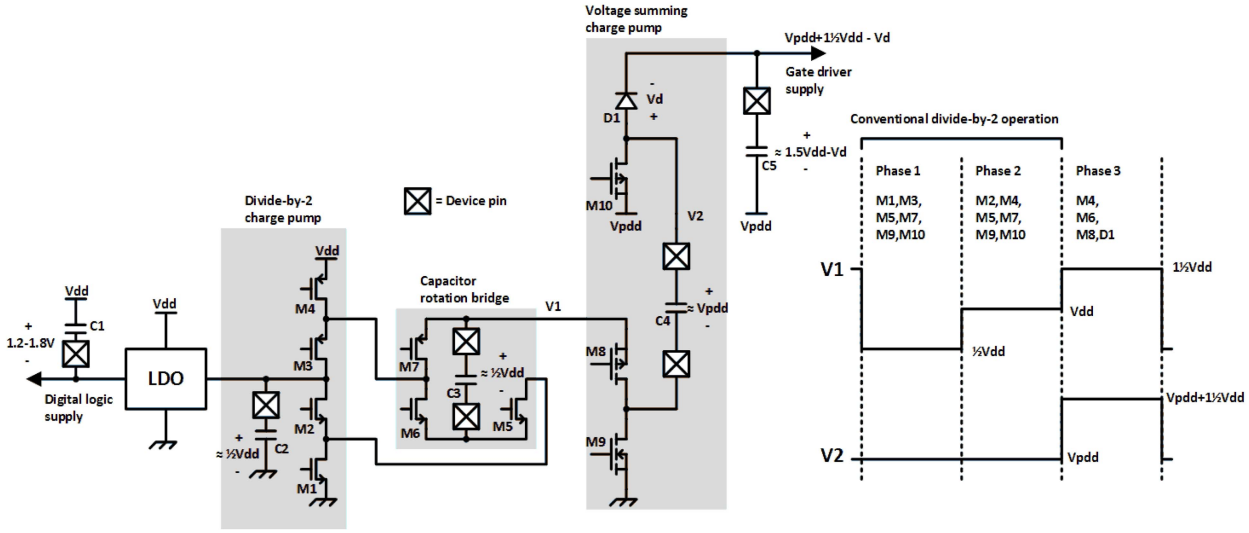

Fig. 9. Auxiliary supply generation subsystem.

Vss_float 2–3 V below Vss, ensuring operation even during ringing events from power stage switching. The current outputs of the subtraction circuit are used to drive a latch implemented as a set of inverters in positive feedback configuration, akin to an SRAM cell. Not shown in Fig. 9 is the necessary (for system reliability) power-on-reset function for the high-side latch. Propagation delay of the design was (by simulation) found to be in the range of 5–15 ns across process, voltage, and temperature, significantly less than the power stage commutation delay. Area of the level shifter (including isolation spacing between LV and HV sections) was 30×90 μm^2 (0.0027 mm^2).

X. Auxiliary Supply Generation

Generation of the high-voltage supply for the gate driver is performed by the multistage charge pump illustrated in Fig. 9. In order to provide headroom for gate driver reference bias current sources, the generated HV supply rail voltage must exceed V_{pdd} by more than the voltage target for the driver of 5 V. To facilitate this from a 5 V supply, while at the same time solving the problem of efficiently generating a low-voltage (1.2–1.8 V) supply for the digital core logic, the designed charge pump structure is based on a conventional divide-by-two charge pump that is modified to provide outputs of (1/2)Vdd and 1(1/2)Vdd. The (1/2)Vdd (around 2.5 V) output supplies an LDO that generates the logic supply. The 1(1/2)Vdd output *V1* is valid in only one phase of the charge pump switching cycle (phase 3 in Fig. 10) and is used for supplying a second charge pump that adds Vpdd for 1(1/2)Vdd. A total of four external capacitors (excluding inevitable Vdd decoupling) and five extra device pins are used for the charge pump structure. Efficiency of the charge pump was simulated to near 90% with 10 mA load of the gate drive supply and 20 mA load on the digital supply. ESD protection of the charge pump structure was a challenge due to the many pins and voltage levels.

XI. Silicon Evaluation Results

The 13.4 mm^2 design stereo BTL (or four-channel SE) device die is depicted in Fig. 10. The packaged device is shown with (nonfilter) supporting passives in Fig. 11. Power performance of the device is shown in Fig. 12, where 90% peak efficiency (at 70 W into 4 Ω) is combined with 45%

TABLE I
MEASURED TWO-CHANNEL BTL V_{pdd} IDLE CURRENT AND POWER FOR DIFFERENT OUTPUT FILTERS

PM system setting	No filter	Ferrite-C filter Wurth 74279245 +1nF/50V/0603/NP0	L-C filter 3.3µH Coilcraft MSS1246-332 + 0.47uF/50V/0805/X7R
High-efficiency f_{sw}=165kHz/330kHz	5.6mA 130mW	7.2mA 170mW	5.9mA 140mW
High-performance f_{sw}=330kHz/660kHz	7.3mA 180mW	9.4mA 230mW	8.9mA 210mW

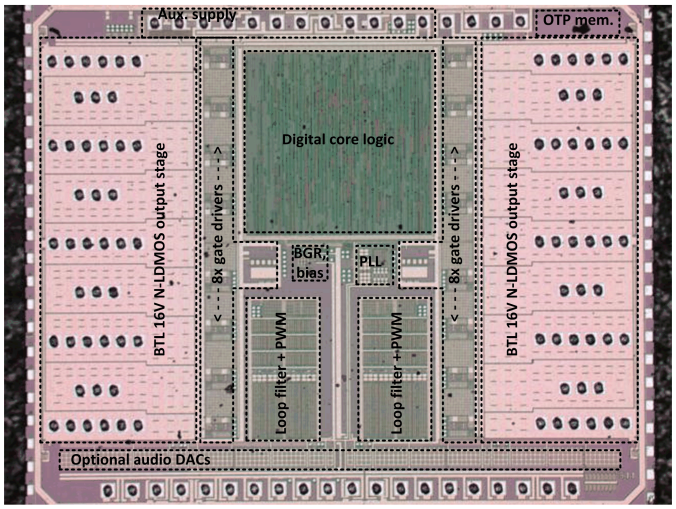

Fig. 10. Photo of the 13.4 mm^2 die.

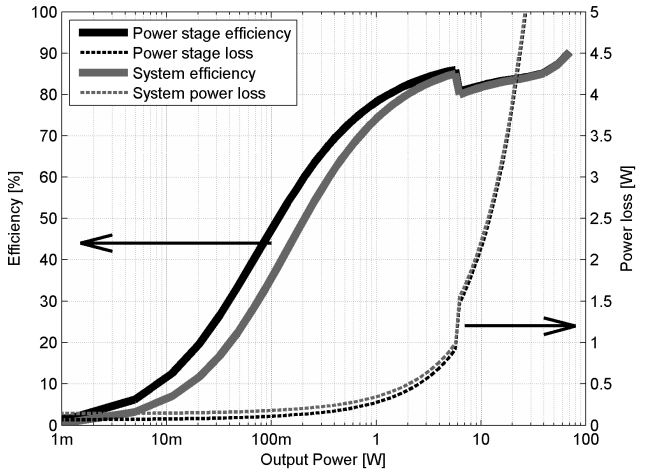

Fig. 12. Measured power efficiency and power loss for filterless operation into a 22 μH + 4 Ω in "high-efficiency" PM system setting. Switching frequency changes from 165 to 330 kHz at 6 W.

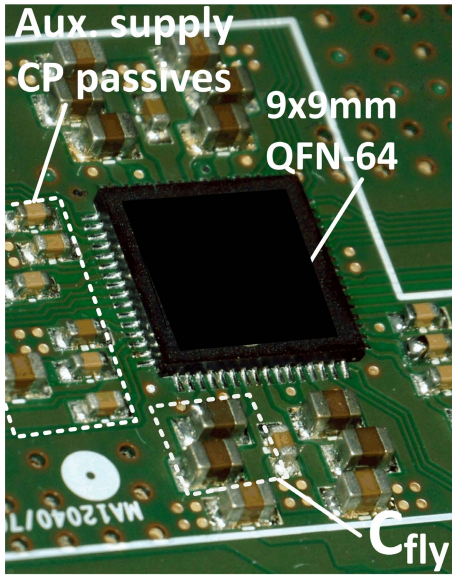

Fig. 11. Packaged device with external passives.

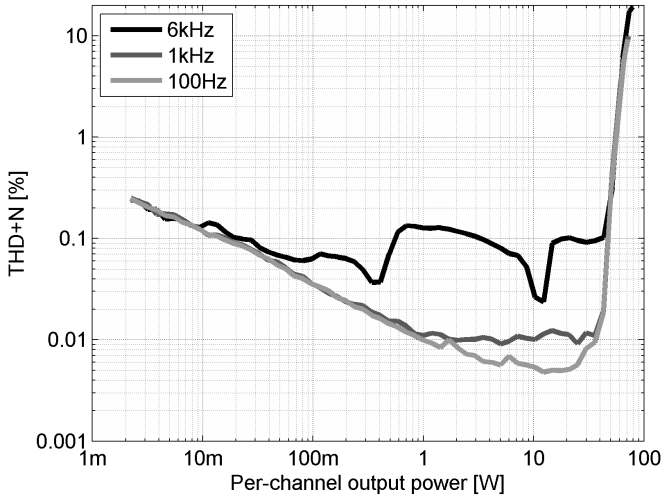

Fig. 13. Measured audio performance for filterless operation into 22 μH + 4 Ω load in "high-efficiency" PM system setting.

efficiency at 100 mW. Efficiency of the power stage itself (V_{pdd} power to output power) is plotted along with full system (5 V rail consumption included) to allow comparison with available prior art. In near-idle operation, the balance between V_{pdd} (24 V) and 5 V rail consumption is near 1:1 (both in the area of 130–150 mW), illustrating the need for power conscious design of signal processing circuitry to accompany the multilevel power stage. (Near-) idle V_{pdd} losses for three different output filtering conditions in two different power management (PM) system setups are given in Table I; a good degree of invariance to filter particularities is evident. The

TABLE II
COMPARISON OF THE PRESENTED WORK AND PRIOR ART IN THE SAME POWER CLASS

Parameter	This work, effcy. opt.	This work, perf. opt.	[20]	[8]	[5]	[13]
Half bridge topology	3-level FC		2-level	2-level	2-level	2-level
Modulation	5-level		2-level	2-level	2-level	3-level (ternary)
Power stage supply V_{pdd}	24V		80V	50V	60V	24V
Max. output power per channel	70W		45W	240W	100W	50W @21V
V_{pdd} idle cons. per channel	70mW (w. output filter)	110mW (w. output filter)	360mW (w. output filter)	2100mW (w. output filter)	1600mW (w. output filter)	380mW (w/o output filter)
Max/idle power ratio	1kW/W	630W/W	125W/W	115W/W	63.5W/W	132W/W
Efficiency at max. output power	90%	88%	91%	?	>90%	88%
THD+N	0.03% @10W, 1kHz	0.003% @10W, 1kHz	0.015% @ 9VA, 100Hz	0.04% @ 10W	0.03% @ 10W, 1kHz	0.04% @ 10W
Dynamic range	108dB	110dB	?	110dB	103dB	102dB
Feedback topology	Analog		Analog	None	Analog	Analog
Max. total output power	140W		45W	240W	200W	100W
Die size	13.4mm^2		8.5mm^2	?	22mm^2	7.04mm^2 (from X-ray)
Power/area ratio	10.4W/mm^2		5.3W/mm^2	?	9.1W/mm^2	14.2W/mm^2
Process	180nm BCD, dual-oxide		140nm SOI BCD	400nm BCD	?nm SOI BCD	?

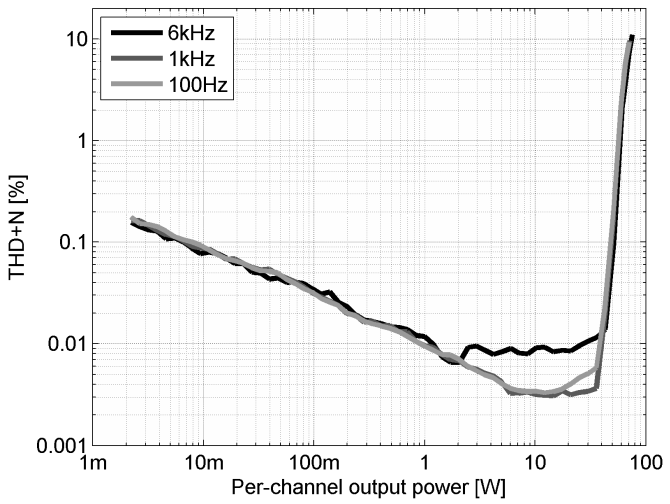

Fig. 14. Measured audio performance for filterless operation into 22 μH+4 Ω load in "high-performance" PM system setting.

variation in loss is due to the fluctuating nonzero width of output pulses due to noise shaping activity in the analog feedback loop, which causes power loss in the filter. Additional power loss data with a low-impedance loudspeaker customized for filter-free operation are given in [31].

Audio performance for the same two configurations is given in Figs. 13 (efficiency optimized) and 14 (audio performance optimized); performance levels are very adequate and excellent (on par with integrated circuit state of the art), respectively. Measurements were done with an Audio Precision APX-515 using the industry-standard AUX-0025 prefilter and AES-20 measurement filter. A summary of key device parameters and comparison with prior art in the same power/voltage area is given in Table II.

XII. CONCLUSION

A class-D audio power amplifier design with several architectural upgrades over prior art has been presented. The design uses a multilevel power stage to drive down size and power loss in external filtering components as well as reducing switching frequency. In combination with a power management scheme that adjusts operational parameters in accordance with output power level, this leads to a design that achieves state-of-the-art idle power loss in the power stage, as well as small physical size of supporting passive components. The design is further shown to be flexible enough to support applications with demanding audio performance requirements, through audio performance datum that is on par with the state of the art. Finally, a suite of solutions to solve challenges that arise from integration of the multilevel power

stage was presented, making for a fully rounded device that is drop-in compatible with first-generation class-D audio power amplifier devices.

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Mikkel Høyerby (M'06) received the M.Sc. degree in electrical engineering from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2004, and the industrial Ph.D. degree from the Technical University of Denmark in co-operation with Motorola, in 2010, working in-between as a Research Assistant in the field of power electronics.

From 2009 to 2010, he was a Research Engineer in the field of radio frequency (RF) power amplifier linearization with Motorola Solutions, Copenhagen, Denmark. In 2010, he co-founded the Copenhagen-based startup Merus Audio, Herlev, Denmark, as the Chief Technology Officer and Analog/Digital/Power IC Designer/Architect. He holds seven patents in the areas of switching power conversion and RF power amplification. His current research interests include feedback systems, power conversion/amplification, and mixed-signal integrated circuitry.

Jørgen Kragh Jakobsen (M'16) received the B.Sc. degree in electrical engineering from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1998.

From 1999 to 2003, he was involved in Radio Frequency/Baseband/ phase-locked loop designs for integrated Bluetooth transceivers in the Copenhagen-based startup Silicide. From 2003 to 2010, he was with the hearing aid company Oticon, Denmark, designing integrated electronics for low-power wireless communication links. In 2010, he joined the startup Merus Audio, Virum, Denmark, as the first employee and has been a Senior Integrated Circuit designer in the fields of analog and digital frontend/backend design, design management, device interface software, and automated test development.

Jesper Midtgaard (M'15) received the M.S. degree in electronical engineering from the Centre for Physical Electronics Ørsted, Technical University of Denmark (DTU), Kongens Lyngby, Denmark, in 2004.

From 2004 to 2005, he was a Research Assistant with the Centre for Physical Electronics, DTU. From 2005 to 2012, he was an Analog Design Engineer with Oticon, Denmark, where he was involved in the design of ultra-low power wireless systems for hearing aids. In 2012, he joined the startup company Merus Audio, Hvidovre, Denmark, where he is currently involved in low-power mixed-signal frequency synthesis and analog loop filter- and pulsewidth modulator design for advanced multilevel switching amplifiers, with a focus on voltage-controlled oscillators and phase-locked loops.

Thomas Holm Hansen (M'15) received the M.Sc. degree in electrical engineering from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2000, the industrial Ph.D. degree in algorithms and signal processing from the IT University of Denmark in co-operation with the Technical University of Denmark and Texas Instruments in 2003.

From 2000 to 2005, he was with Texas Instruments, where he was involved in audio power amplifier ICs. From 2005 to 2013, he was with DK-Technologies, Herlev, Denmark, developing instruments for audio and video signal analysis. Since 2013, he has been a Senior Research & Development Engineer at Merus Audio, Værløse, Denmark, researching and developing concepts for audio power amplifier ICs in the field of signal processing, algorithms, digital design, and system level architecture. He holds six patents related to audio amplifier IC technology.