A 300 GHz CMOS Transmitter With 32-QAM 17.5 Gb/s/ch Capability Over Six Channels

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***Abstract*— A 300 GHz transmitter (TX) fabricated using a 40 nm CMOS process is presented. It achieves 17.5 Gb/s/ch 32-quadrature amplitude modulation (QAM) transmission over six 5 GHz-wide channels covering the frequency range from 275 to 305 GHz. With the unity-power-gain frequency f_{max} of the NMOS transistor being below 300 GHz, the TX adopts a power amplifier-less QAM-capable architecture employing a highly linear subharmonic mixer called a cubic mixer. It is based on and as compact as a tripler and enables the massive power combining necessary above f_{max} without undue layout complication. The frequency-dependent characteristics of the cubic mixer are studied, and it is shown that even higher data rates of up to 30 Gb/s are possible at certain frequencies, where the channel signal-to-noise ratio is high. The design and the operation of the power-splitting and power-combining circuits are also described in detail. The measurements reported herein were all made "wired" via a WR3.4 waveguide.**

***Index Terms*— Power combiner, power splitter, quadrature amplitude modulation (QAM), subharmonic mixing, terahertz (THz) transmitter (TX).**

I. Introduction

According to Shannon's theorem, the speed of a wireless link is proportional to its spectral bandwidth. Therefore, the availability of wide bandwidths is an important factor in achieving very high speeds. The recent interest in terahertz (THz) wireless communication [1]–[4] is certainly motivated by the availability of wide bandwidths, which are required to cope with the burgeoning demand for high data rates. Research into photonics-based [5]–[9] and solid-state-circuit-based [10]–[21] THz wireless systems is currently very active.

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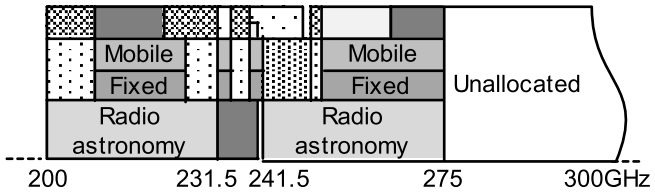


Fig. 1. Frequency allocations above 200 GHz in the U.S.

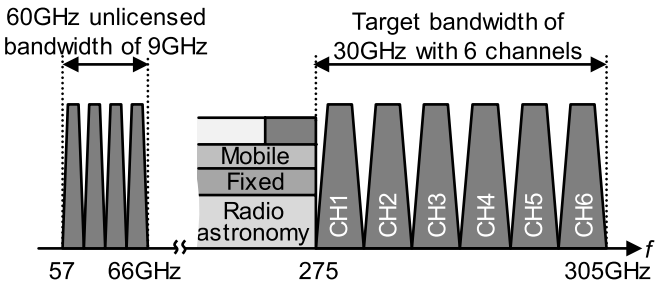


Fig. 2. Target band plan and channel allocation for 300 GHz ultrahigh-speed wireless communication.

In the latter approach, it is technically more challenging to use CMOS technology to build THz circuits than to use compound semiconductor technology because of the lower unity-power-gain frequency, f_{max}, of Si MOSFETs. In spite of the rather optimistic projections for the future growth of CMOS f_{max} in ITRS [22], the actual f_{max} tends to be significantly lower. THz CMOS technology is, therefore, less fueled by technology scaling than the conventional digital and RF CMOS evolution [10]. The role of design as well as the characterization and modeling of devices is assuming ever greater importance [10], [23]. Given the apparent slowdown in the growth of CMOS f_{max}, the development of near-f_{max} [12], [24] and above-f_{max} circuit design techniques will be a key to the successful takeoff of THz CMOS.

In this paper, we present a 300 GHz CMOS transmitter (TX) reported previously in [25]. It covers the currently unallocated frequency range from 275 to 305 GHz (Fig. 1) with six 5 GHz-wide channels, as shown in Fig. 2. The overall bandwidth is more than three times the 60 GHz unlicensed bandwidth

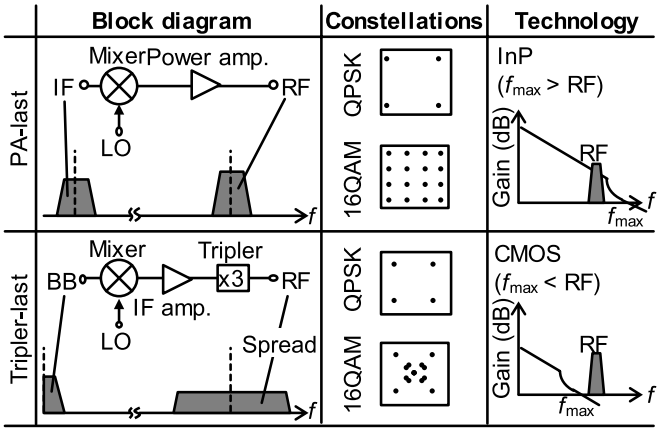


Fig. 3. Possible architectures of THz TXs and corresponding output power spectra, output signal constellations, and frequency dependence of transistor gain.

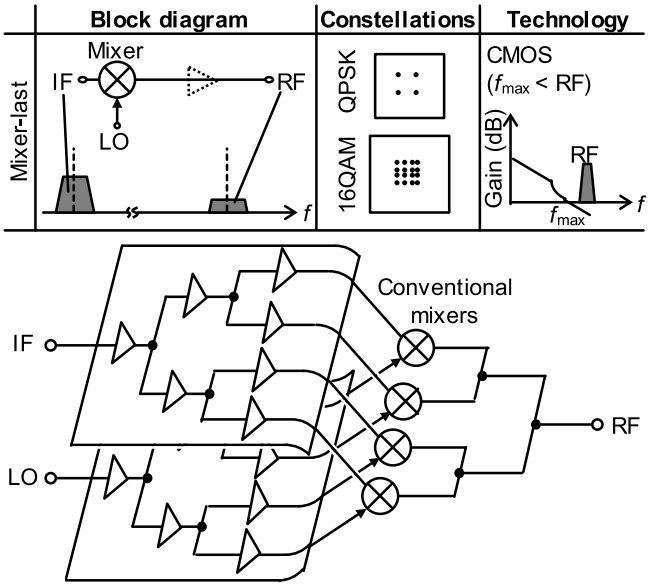


Fig. 4. Easily conceivable mixer-last architecture. It is difficult to realize in practice, because the layout would become extremely complicated with a large number of crossovers.

of 9 GHz. According to the process design kit provided by the foundry, NMOS f_{max} for the 40 nm CMOS process that we used is about 280 GHz. The measured f_{max} values were somewhat lower. Our TX, therefore, is an above-f_{max} TX. While quadrature amplitude modulation (QAM) signal transmission at 300 GHz or above has already been reported [26], [27], achieving this using a CMOS technology has been a tremendous challenge, as will be discussed in Section II. Our TX is capable of 32-QAM 17.5 Gb/s/ch signal transmission.

The rest of this paper is organized as follows. In Section II, we discuss the choice of the architecture in view of the transistor f_{max} and clarify the technical challenges faced while building an above-f_{max} TX. Section III explains the designs of the constituent blocks and the overall TX. Section IV analyzes the characteristics of the key enabling component, a highly linear subharmonic mixer called a *cubic mixer*. Section V presents the measured performance of the TX. Finally, Section VI concludes this paper.

II. Architectural Consideration

Fig. 3 shows the possible architectures of THz TXs based on state-of-the-art above-200 GHz TXs. The choice of the architecture strongly depends on the transistor f_{max}. Above f_{max}, the transistor gain falls below unity and the transistor becomes passive. If f_{max} is sufficiently higher than the transmitted signal frequency, RF, as is typical when using InP technology (Fig. 3, first row), the ordinary power amplifier (PA)-last architecture [11]–[14] is the most suitable. In this architecture, the IF signal is upconverted to RF by a mixer and the signal is amplified at RF. Complex modulation formats such as QAM can be used, provided that the signal path has sufficient linearity. Since f_{max} should be very high when this architecture is adopted, the conversion gain of the mixer should also be reasonably high. The presence of a PA is not a requirement [28], [29].

If f_{max} is comparable with or lower than RF, as is typical when using CMOS technology, a PA-less architecture must be adopted. The state-of-the-art CMOS TXs adopt a tripler-last [20] (Fig. 3, second row) or quadrupler-last architecture [21]. A drawback of these architectures is their low spectral efficiency due to signal bandwidth spreading caused by frequency tripling or quadrupling. Another drawback is that the use of multibit digital modulation is very difficult, if not impossible. An exception to this is quaternary phase shift keying (QPSK) combined with frequency tripling. When a QPSK-modulated IF signal undergoes frequency tripling, the resulting signal constellation remains that of QPSK with some symbol permutation. Such a tripler-last QPSK TX has been reported [30]. However, a 16-QAM constellation, for example, would suffer severe distortion upon frequency tripling (Fig. 3, second row). If the 300 GHz band is to be seriously considered as a platform for ultrahigh-speed wireless communication, QAM capability will be a requisite, because a wide bandwidth alone is not sufficient for achieving very high data rates.

Fig. 4 shows a possible PA-less, mixer-last architecture that has the PA removed from the PA-last architecture (Fig. 3, first row). In this configuration, signal bandwidth spreading should not occur and QAM should work, except that the amplitude will be much smaller than that in the PA-last case. However, no PA-less, mixer-last CMOS TXs operating above f_{max} appear to have been reported, presumably because the layout would become too complicated, as shown in the schematic of Fig. 4. Our goal here is to develop a 300 GHz CMOS TX operating above f_{max}. The output power from a single mixer is inevitably very low. That means that massively parallel power combining is necessary at RF. However, if we attempted to achieve this using ordinary three-port mixers, as in Fig. 4, the layout would become extremely complicated with a large number of crossovers. The mixers would typically be double-balanced mixers, thus doubling the number of wires. It would be extremely difficult to achieve the correct phase relationship between different branches.

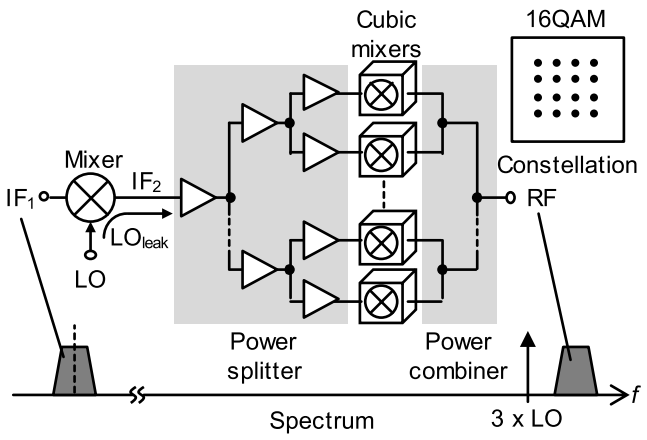


Fig. 5. QAM-capable cubic-mixer-last architecture. Its layout is as simple as that of the tripler-last architecture. There is no bandwidth spreading at RF.

In contrast, the tripler-last architecture (Fig. 3, second row) allows massive power combining with a much simpler layout, because it does not require LO signal paths.

To summarize, the main technical challenges faced when building an above-$f_{\max}$ PA-less TX in CMOS are as follows.

1) Giving the QAM capability required to achieve high data rates. That means that frequency multipliers should not be used because they badly distort QAM signals.
2) Performing massive power combining to obtain sufficient output power without undue layout complication and/or die area explosion.

We reconcile these conflicting requirements by introducing a mixer-last architecture that employs a tripler-based, highly linear subharmonic mixer, which we call the *cubic mixer* (Fig. 5). Since it is a mixer, not a tripler, the TX is QAM-capable and there is no signal bandwidth spreading. The layout of the cubic mixer is as simple as that of a tripler, and this simplicity is vital for realizing massive power combining without undue layout complication.

III. Circuit Design

As shown in Fig. 5, the 300 GHz CMOS TX consists of a double-balanced mixer, a power splitter, cubic mixers, and a power combiner. Since the cubic mixer is the key component of this TX, we start this section with a description of it. We then introduce the power splitter and power combiner. Finally, we explain the overall design of the TX.

A. Cubic Mixer

The cubic mixer is used to upconvert a digitally modulated IF signal at IF_2 to RF with high linearity (Fig. 5). As the name suggests, it uses the cubic nonlinearity of the MOSFET and is essentially a tripler. It receives a two-tone-like signal composed of modulated IF_2 and pure LO. When the two-tone-like input is cubed by a tripler, first- to third-order signals are generated in accordance with

$$(\mathrm{LO}+\mathrm{IF}_2)^3 = \mathrm{LO}^3 + 3\mathrm{LO}^2\cdot\mathrm{IF}_2 + 3\mathrm{LO}\cdot\mathrm{IF}_2^2 + \mathrm{IF}_2^3 \quad (1)$$

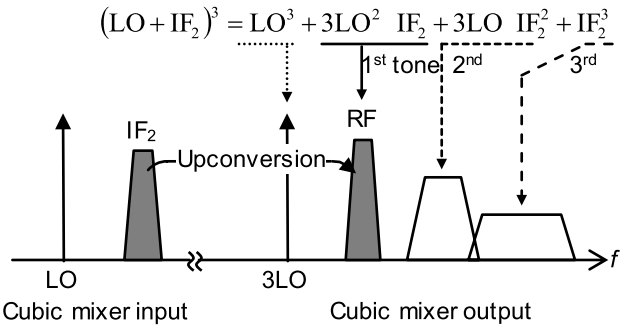


Fig. 6. Operation principle of the cubic mixer. The second subharmonic mixing term, $3\mathrm{LO}^2\cdot\mathrm{IF}_2$, is used for linear upconversion. LO < IF_2 in this example.

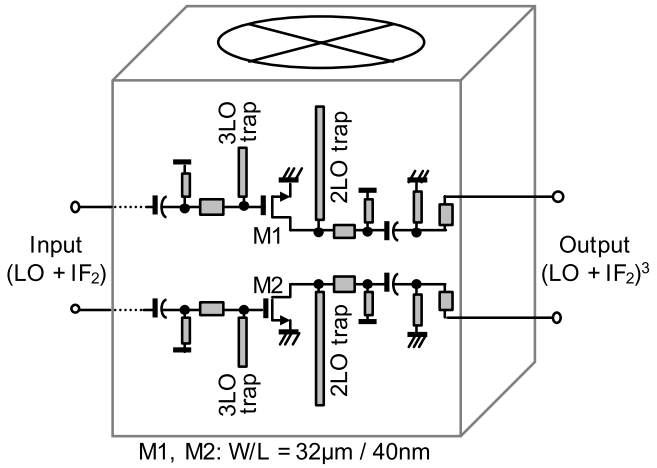


Fig. 7. Schematic of the cubic mixer.

as shown in Fig. 6. To be exact

$$\begin{aligned}(\cos\omega_{\mathrm{LO}}t + \cos\omega_{\mathrm{IF2}}t)^3 &= \frac{3}{4}[3\cos\omega_{\mathrm{LO}}t + \cos(2\omega_{\mathrm{LO}} - \omega_{\mathrm{IF2}})t \\ &\quad + \cos(\omega_{\mathrm{LO}} - 2\omega_{\mathrm{IF2}})t + 3\cos\omega_{\mathrm{IF2}}t] \\ &\quad + \frac{1}{4}[\cos 3\omega_{\mathrm{LO}}t + 3\cos(2\omega_{\mathrm{LO}} + \omega_{\mathrm{IF2}})t \\ &\quad + 3\cos(\omega_{\mathrm{LO}} + 2\omega_{\mathrm{IF2}})t + \cos 3\omega_{\mathrm{IF2}}t]. \quad (2)\end{aligned}$$

The last four terms of (2) are the high-frequency (near $3\omega_{\mathrm{LO}}$) components and are shown in Fig. 6. By appropriately tuning the power levels of LO and IF_2, the second subharmonic mixing term, $3\mathrm{LO}^2\cdot\mathrm{IF}_2$ in (1), becomes the dominant output. We use this term for linear signal upconversion. The optimal LO-power-to-IF_2-power ratio is $P_{\mathrm{LO}}/P_{\mathrm{IF2}} = 2$ [31]. Fig. 7 shows a schematic of the cubic mixer, which is a tripler with a differential input and output. As shown in the circuit simulation result in Fig. 8, upconversion is accomplished with good linearity. The desired first tone is the dominant output at frequencies of interest, as shown in Fig. 9.

A more detailed analysis of the frequency-dependent characteristics of the cubic mixer is given in Section IV.

B. Power Splitter

Since the NMOS $f_{\max}$ of the 40 nm CMOS process that we used is at most 280 GHz, the cubic mixer acts as a passive

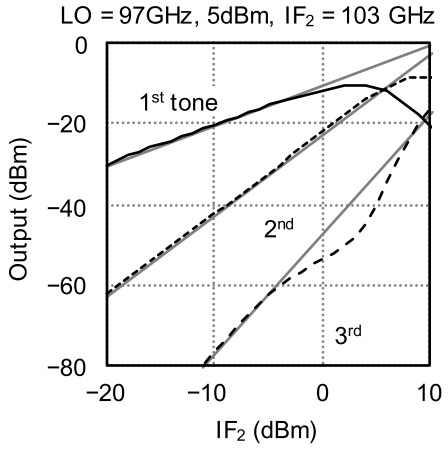


Fig. 8. Simulated output power of the cubic mixer as a function of input IF_2 power.

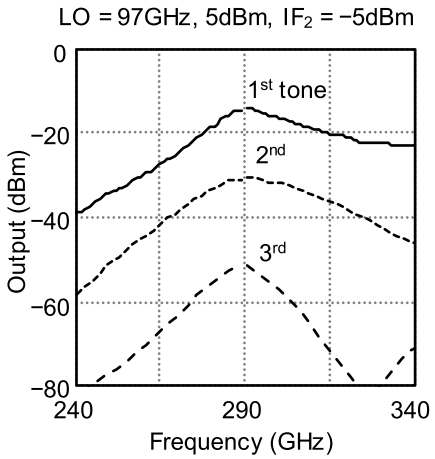


Fig. 9. Simulated output power of the cubic mixer as a function of frequency.

mixer with a rather low conversion gain. Massively parallel amplification at IF_2 and power combining at RF are required, and we perform 32-way power combining.

An orthodox approach to power splitting and amplification without introducing layout crossovers is to use passive baluns and differential amplifiers [12]. However, passive baluns operating at 100 GHz occupy a large area, and the area required for 32-way power splitting would become excessive if we adopted a passive-balun-based network. As shown in Fig. 10, we perform crossover-free 32-way power splitting using differential-amplifier-based active baluns with single-ended feeding.

Fig. 11 shows a schematic of the active balun. It is a capacitively neutralized differential amplifier with a single-ended input and a differential output. This type of balun is known to have some limitations compared with passive baluns, including the inherent imbalance between the two outputs [32]. However, it can be designed to perform reasonably well over a not-so-wide bandwidth.

Fig. 12 shows the differential- and common-mode half circuits of the core amplifier. The capacitor C_n functions as a neutralizing capacitor only in the differential mode, and it lowers the gain in the common mode. Fig. 12 also shows the gain and the stability factor K [33] of the half circuits as

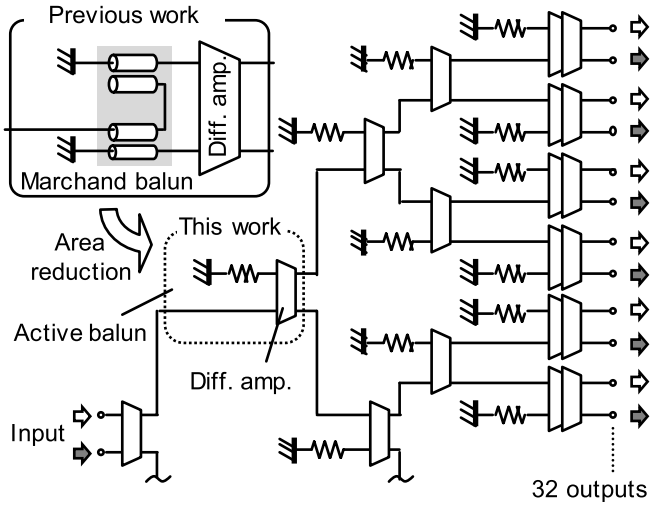


Fig. 10. 32-way power-splitting network composed of differential-amplifier-based active baluns. The area is significantly smaller than a passive-balun-based network [12].

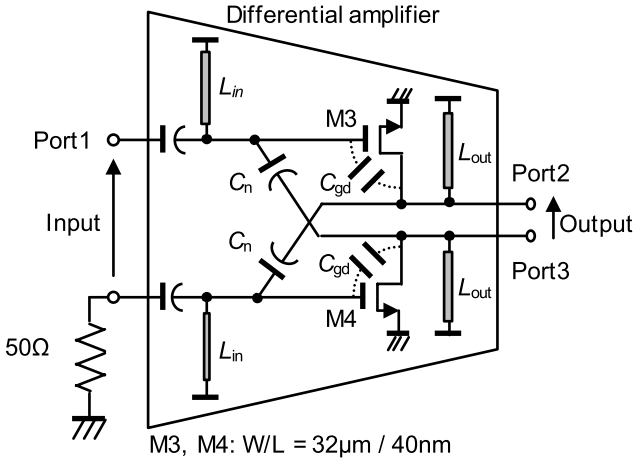


Fig. 11. Schematic of the active balun.

a function of the capacitance C_n. If the design goal is high gain, a value of C_n could be chosen from an *over-neutralized region* [12], in which the maximum available gain (MAG) [33] has a local maximum. The interrelationship between the MAG and K can be visualized and the design space be further explored using a graphical chart called the *MAG-K chart*, discussed elsewhere [24], [34]. The graphs in Fig. 12 can be understood as cross-sectional gain and K profiles along a Y (shunt–shunt)-feedback circle on an MAG-K chart [34]. Here, we choose a value of C_n, such that the highest reverse isolation is achieved (within the limited design space spanned only by C_n), because we must be able to tune L_{in} and L_{out} in Fig. 11 independently to optimize the balun characteristics. Fig. 13 shows the frequency-dependent characteristics of the active balun. Because of the high isolation between the input and output ports, we can select the lengths of the shunt stubs implementing L_{in} and L_{out} independently to obtain good input and output matching. We tuned the stub lengths such that the phase difference between the output ports

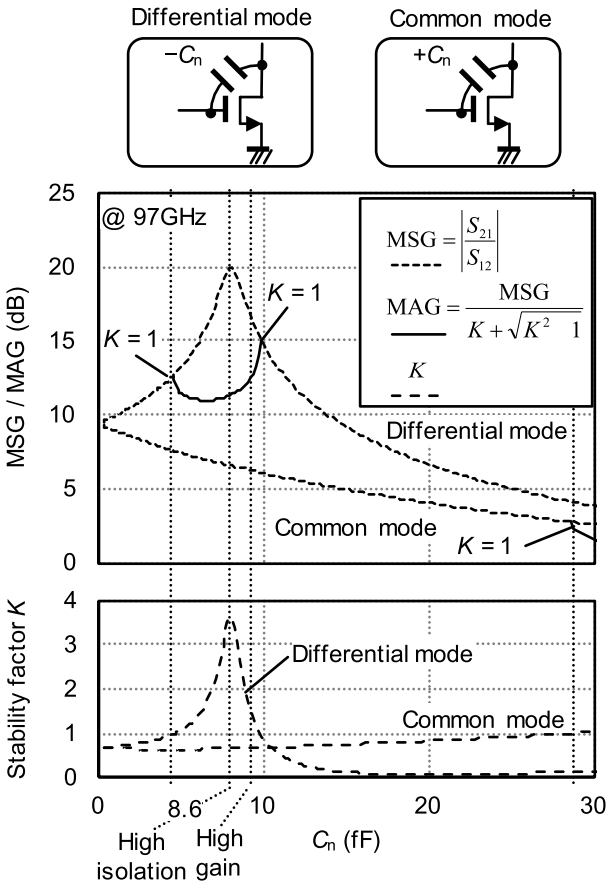


Fig. 12. Differential- and common-mode half-circuit characteristics of the active balun (Fig. 11) at 97 GHz as a function of feedback (neutralization) capacitance C_n. The top graph shows the maximum stable gain and MAG. The bottom graph shows the stability factor K.

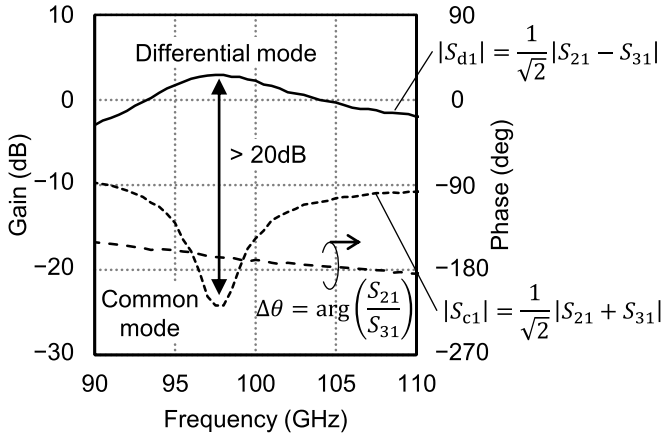


Fig. 13. Simulated differential-mode gain $|S_{d1}|$, common-mode gain $|S_{c1}|$, and phase balance $\Delta\theta$ for the active balun (Fig. 11).

is $\Delta\theta \simeq \arg(S_{21}/S_{31}) = 180°$ at around 100 GHz. The common-mode rejection ratio is maximized near this frequency, as shown in Fig. 13.

C. Power Combiner

We performed 32-way power splitting at IF_2 and fed 16 cubic mixers differentially. We must, therefore, perform 32-way power combining at RF. We introduce a passive eight-way combiner called the *quad-rat-race*, shown in Fig. 14, and use four quad-rat-races to perform 32-way power combining. The quad-rat-race is an extension of the ordinary rat-race balun [35], shown in Fig. 15(a). The circumference of the rat-race is 1.5λ. According to circuit theory, if the access transmission lines have a characteristic resistance [36]–[38] of R_0, the line constituting the ring should have a characteristic resistance of $\sqrt{2}R_0$ [35]. Then, all the diagonal elements of the S-matrix of the rat-race balun become zero ($S_{ii} = 0$), as shown in Fig. 15(a). This can be understood by recognizing that port 3 (port 2) becomes a virtual ground node when port 2 (port 3) is the driving port and that each of the $\lambda/4$-sections of the ring serves as a $\lambda/4$-transformer.

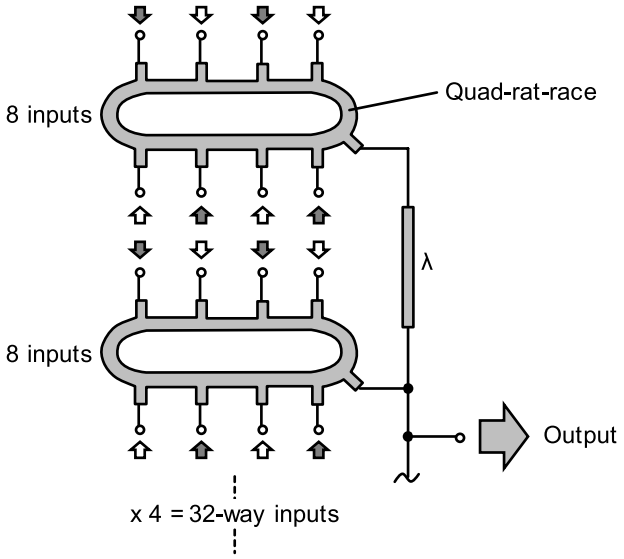


Fig. 14. 32-way power combining network consisting of four quad-rat-races and two sections of transmission line of length λ.

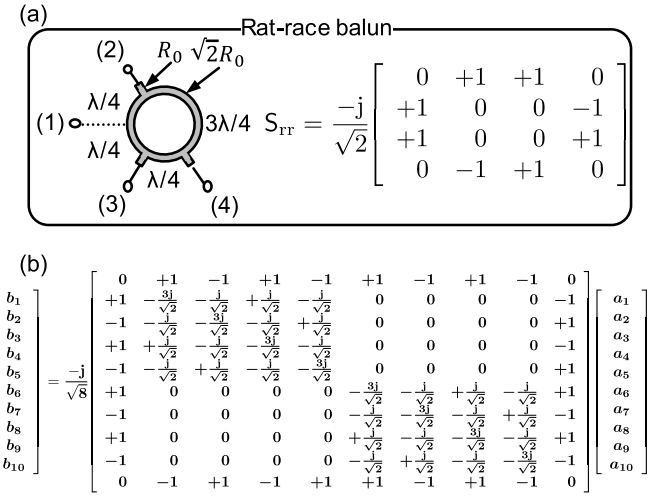


Fig. 15. (a) Rat-race balun and its S-matrix in the ideal lossless case. R_0 is the characteristic resistance of the access line. Port numbers are indicated in parentheses. (b) S-matrix of the quad-rat-race in an ideal case, where the ring has a characteristic resistance of $R_0/\sqrt{2}$. Port numbers are shown in Fig. 16(a).

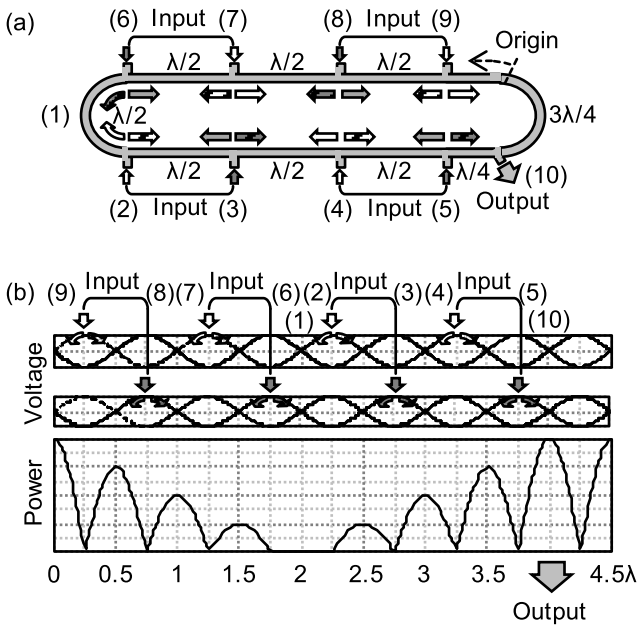


Fig. 16. (a) Quad-rat-race. Port numbers are indicated in parentheses. (b) Traveling-wave voltages and the power available along the ring.

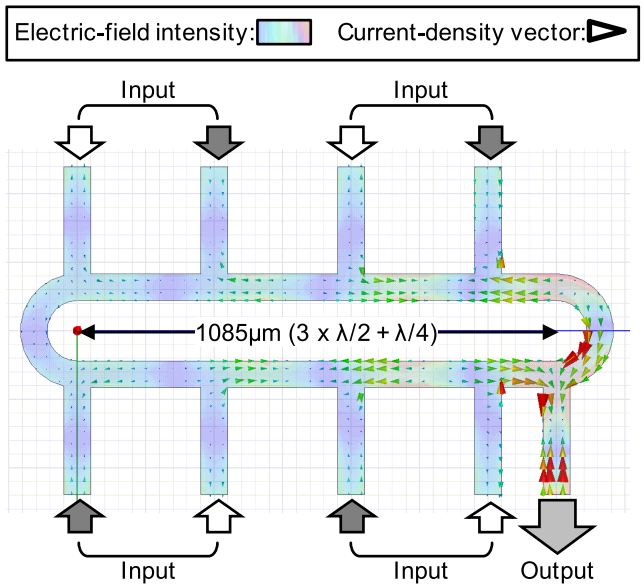


Fig. 17. Simulated electric field intensity and current density vectors in a lossless quad-rat-race having a simpler layout than the actual design (in Fig. 20), provided as an illustration of the basic operation.

The quad-rat-race has four differential input ports or eight single-ended input ports, as shown in Fig. 16(a). It performs differential-to-single-ended conversion and eight-way power combining. A differential input port consists of a pair of single-ended ports. These input ports are placed $\lambda/2$ apart from each other. The circumference of the ring is 4.5λ. A signal injected into a single-ended port splits into clockwise and counterclockwise traveling waves, each having half the input power. The first (second) graph in Fig. 16(b) shows the traveling-wave voltages along the ring originating from the positive (negative) ports. A pair of counter-rotating traveling waves originating from an input port cancel each other when they reach other input ports, that is, the input ports become virtual ground nodes. On the other hand, a pair of counter-rotating traveling waves are superposed constructively at the output port. The power available along the ring is plotted in the bottom graph of Fig. 16(b). Altogether, 16 traveling waves are summed at the output port and eight-way power combining is achieved.

Fig. 15(b) shows the S-matrix of a quad-rat-race when the characteristic resistance of the ring is $R_0/\sqrt{2}$. If the inputs to the quad-rat-race are four ideally differential signals, the S-matrix can be simplified by the following substitution:

$$\begin{cases} a_2' = (a_2 - a_3 + a_4 - a_5)/2 \\ a_6' = (a_6 - a_7 + a_8 - a_9)/2 \\ b_2' = (b_2 - b_3 + b_4 - b_5)/2 \\ b_6' = (b_6 - b_7 + b_8 - b_9)/2. \end{cases} \tag{3}$$

The result is

$$\begin{bmatrix} b_1 \\ b_2' \\ b_6' \\ b_{10} \end{bmatrix} = \mathsf{S}_{\mathrm{rr}} \begin{bmatrix} a_1 \\ a_2' \\ a_6' \\ a_{10} \end{bmatrix} \tag{4}$$

where S_{rr} is the S-matrix of the rat-race given in Fig. 15(a). Equation (4) clearly shows that the quad-rat-race is an extension of the rat-race.

Fig. 17 shows the E-field intensity and current density in a lossless quad-rat-race having a simpler layout than the actual design. In practice, the electromagnetic (EM) design of a quad-rat-race (and also an ordinary rat-race) involves taking account of reflections at the T-junctions, losses, and the imaginary parts of characteristic impedances of the transmission lines, not usually considered in ideal circuit theoretic treatment. In our final design, the access lines and the ring are implemented using the same type of microstrip transmission line having a characteristic impedance close to 50 Ω. Its signal strip width is 9 μm. We did not use a 35 Ω line for the ring, because only the 50 Ω line was experimentally characterized and modeled for circuit simulation. The model was used to predict the characteristics of the quad-rat-race before the actual layout was done. EM-simulated characteristics of the actual design are shown in Fig. 18. The somewhat high reflection as seen from 50 Ω-referenced ports can be attributed to the use of the 50 Ω line for the ring. We designed matching networks taking that into consideration.

D. Overall TX Design

Fig. 19 shows the overall schematic of the 300 GHz CMOS TX. It receives a modulated IF signal at IF_1 and a W-band LO signal. The modulated signal is upconverted to IF_2 (around 100 GHz) by a double-balanced mixer. At this point, we must superpose IF_2 and LO, so that we can feed the cubic mixers with $(\mathrm{IF}_2 + \mathrm{LO})$. However, a large area would be required if we used another passive device to superpose IF_2 and LO. Instead, we designed the double-balanced mixer, such that the LO and $\overline{\mathrm{LO}}$ ports are very close to

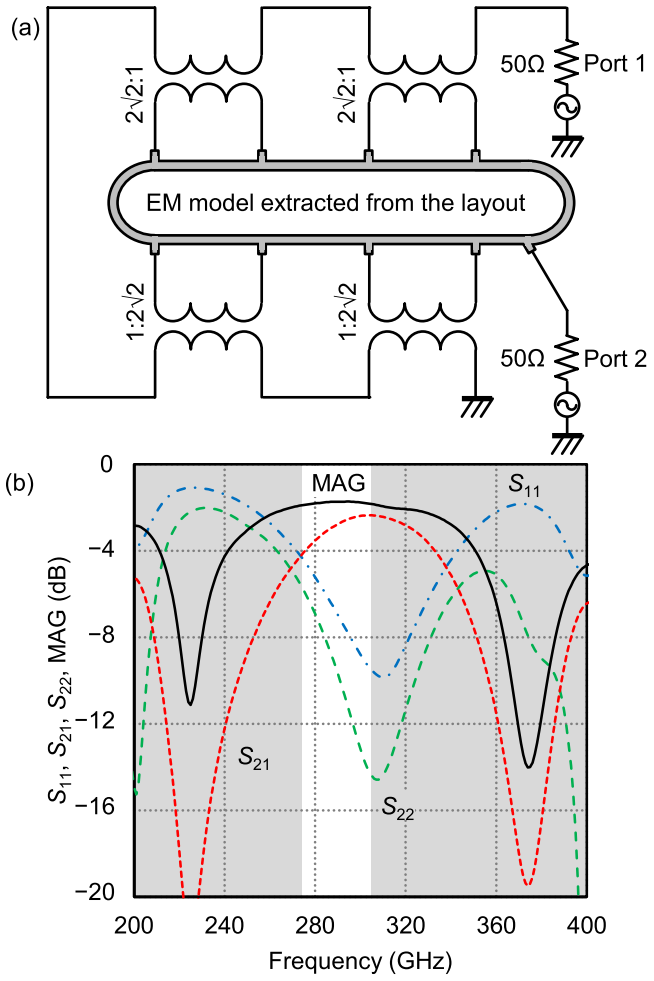


Fig. 18. (a) Simulation setup for bundling together the input ports of a quad-rat-race. (b) Simulated frequency response of the quad-rat-race (actual design).

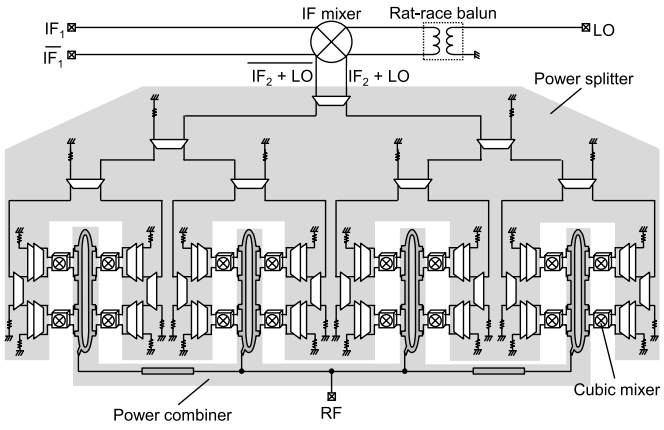


Fig. 19. Schematic of the 300 GHz CMOS TX.

the output ports. The intentional capacitive coupling thus introduced provides an LO leakage path and results in the desired superposition of IF_2 and LO at the output of the mixer.

After 32-way power splitting (Fig. 10), the signal is upconverted to 300 GHz by 16 cubic mixers (Fig. 7). The power combiner consists of four quad-rat-races and transmission

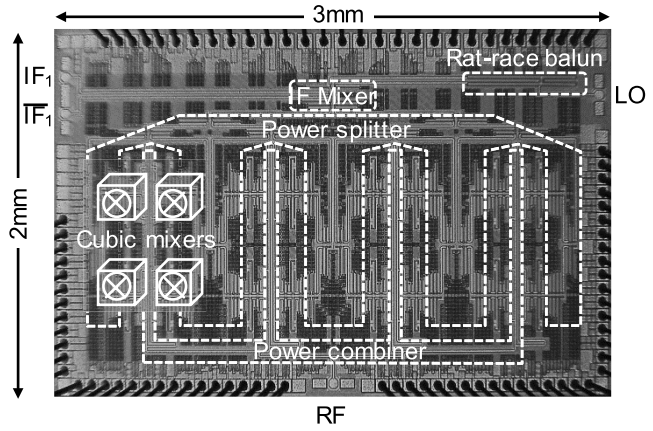


Fig. 20. Die micrograph of the 300 GHz CMOS TX.

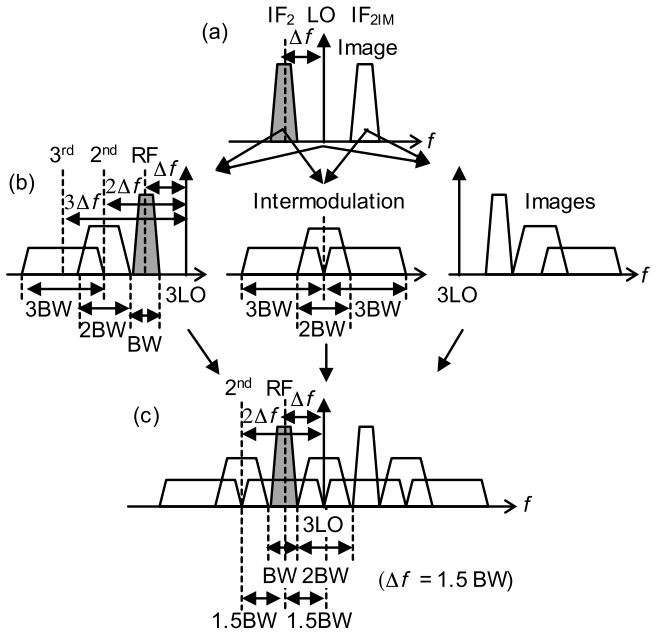


Fig. 21. (a) Input power spectrum fed into the cubic mixer. IF_2 < LO < IF_{2IM} in this example. (b) Spectral components generated by the cubic mixer. (c) Output power spectrum of the cubic mixer obtained by superposing all the components shown in (b).

lines (Fig. 14). Fig. 20 shows a die micrograph of the TX. The die size is 2 mm × 3 mm.

IV. Analysis of Cubic Mixer

The cubic mixer generates unused spectral components, as is clear from (1). Currently, no particular care is exercised to filter out these unused components. It is thus natural that they will adversely affect the desired signal and degrade the TX performance. In this section, we examine the frequency-dependent signal-to-noise ratio (SNR) of the cubic mixer.

Let the frequency separation between IF_2 and LO be Δf

$$\Delta f = |\mathrm{LO} - \mathrm{IF}_2|. \tag{5}$$

In the present implementation, the output from the first upconversion mixer (Fig. 19) contains not only IF_2 and LO but also the image of IF_2 at IF_{2IM}. If IF_2 < LO, as shown in Fig. 21(a)

$$\mathrm{IF}_{2\mathrm{IM}} = \mathrm{IF}_2 + 2\Delta f. \tag{6}$$

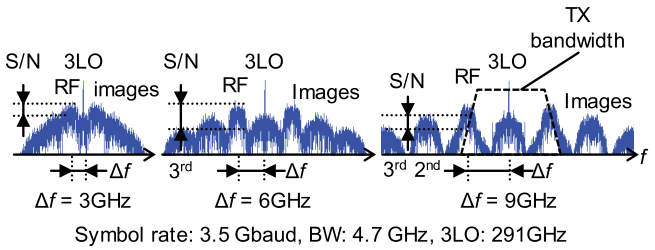


Fig. 22. Simulated output spectrum of the cubic mixer for $\Delta f = 3$, 6, and 9 GHz. A root-raised-cosine filter with a roll-off factor of 0.35 was applied to the input signal. "S/N" in the figure indicates that the height is related to the SNR, but it has no quantitative meaning. The result for $\Delta f = 6$ GHz gives the highest SNR.

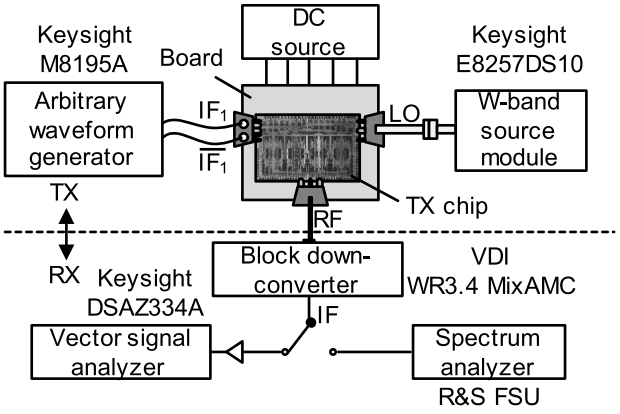


Fig. 23. Measurement setup.

Thus, the cubic mixer generates the spectral components shown in Fig. 21(b) [39], including the terms in (1) from IF_2 and IF_{2IM} [Fig. 21(b) (left and right)], and the intermodulation products from IF_2 and IF_{2IM} [Fig. 21(b) (center)].

If Δf is too small, the desired signal, RF, may interfere with the second-order term, $3LO \cdot IF_2^2$, from (1). This can be avoided by making $\Delta f \gtrsim 1.5$ BW, where BW is the bandwidth of RF. Fig. 22 shows system simulation results with three different values of Δf. The SNR of the cubic mixer degrades if $\Delta f \lesssim 1.5$ BW. Of course, Δf cannot be increased indefinitely, and its upper bound is dictated by the overall TX bandwidth [Fig. 22 (right)].

Another more fundamental noise source is the lower-side, third-order intermodulation product [Fig. 21(b) (center)]. It always interferes with RF itself, regardless of the value of Δf, as shown in Fig. 21(c). In addition, as is clear from Fig. 22, other spurious components interfere with neighboring channels. The present configuration, therefore, does not allow multiple channels to be used simultaneously. A fundamental solution would be to design a TX such that IF_{2IM} does not exist in the input to the cubic mixer. This can be achieved, for example, by using a quadrature modulator. Another less complete but easier fix applicable to this TX is to choose LO and IF_2 in such a way that IF_{2IM} is driven outside the bandwidth of the IF amplifiers for IF_2 in the power-splitting network (Fig. 5) [40]. This will allow higher data rates to be achieved over all six channels [40].

V. Transmitter Performance

Fig. 23 shows the measurement setup. The arbitrary waveform generator generates a digitally modulated IF signal at IF_1

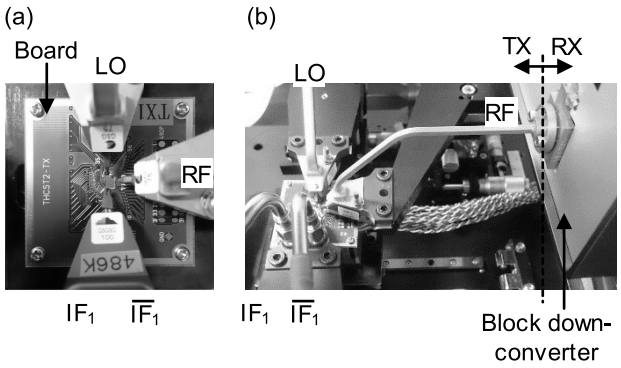
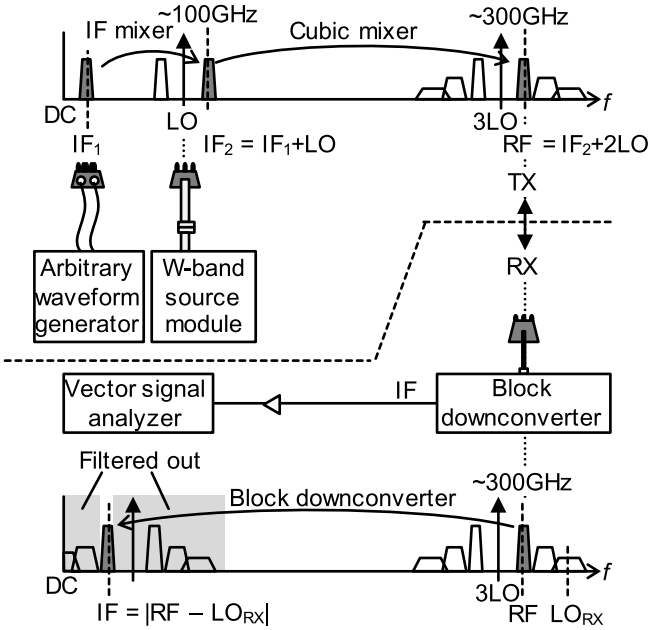


Fig. 24. (a) TX PCB. (b) Waveguide connection to the block downconverter.



	CH1	CH2	CH3	CH4	CH5	CH6
BW (GHz)	4.7	4.7	4.7	4.7	4.7	4.7
Δf, IF_1 (GHz)	13	8	3	3	8	13
LO (GHz)	97	97	97	97	97	97
IF_2 (GHz)	84	89	94	100	105	110
3LO (GHz)	290	290	290	290	290	290
RF (GHz)	277	282	287	293	298	303
LO_{RX} (GHz)	271	276	281	299	304	309
IF (GHz)	6	6	6	6	6	6

Fig. 25. Frequency upconversion in the TX and downconversion in the measurement system.

and feeds the TX chip differentially. The W-band source module supplies the LO signal. The output RF signal at 300 GHz is led to a block downconverter through a WR3.4 waveguide probe. The downconverted signal is fed either to a vector signal analyzer or to a spectrum analyzer.

Fig. 24 shows the snapshots of the TX and the measurement system. The chip is mounted on a printed circuit board (PCB). DC power is supplied through bond wires, and high-frequency signals are supplied or measured via RF probes. Fig. 25 shows the frequency up/downconversion taking place in the TX and the measurement system. The first IF, IF_1, fed to the chip is upconverted to the second IF, IF_2, at around 100 GHz. The values of IF_1 and IF_2 are given in Fig. 25. Then, the signal

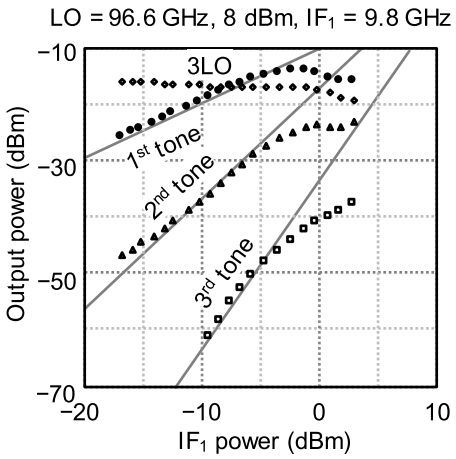


Fig. 26. Output power as a function of IF_1 power.

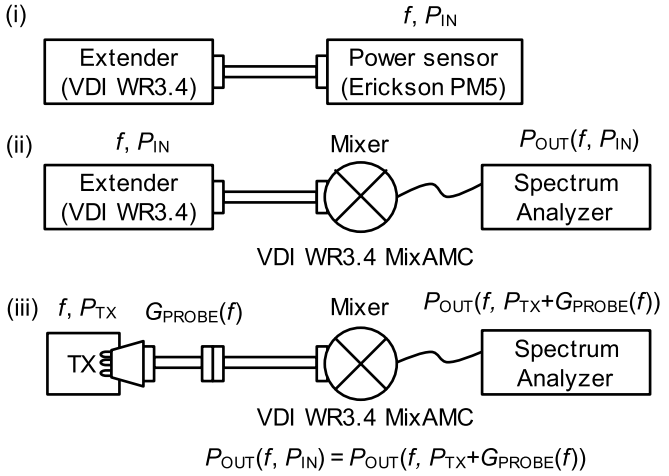


Fig. 27. Calibration procedure for the output power measurement. (i) Output power, P_{IN}, of a WR3.4-band frequency extender is measured as a function of frequency f. (ii) Frequency-dependent conversion loss of the block downconverter (mixer) is measured and tabulated as $P_{OUT}(f, P_{IN})$. (iii) TX output power P_{TX} (in dBm) is found from $P_{OUT}(f, P_{TX} + G_{PROBE}(f))$. The probe loss, $G_{PROBE}(f)$ (in dB), is characterized by another measurement.

is upconverted by the cubic mixer to about 300 GHz. The 300 GHz RF signal is downconverted to 6 GHz by the block downconverter. Unwanted spectral components that reach the vector signal analyzer are filtered out before demodulation.

The measured output RF power (Fig. 26), calibrated by the procedure shown in Fig. 27, clearly shows linear dependence on the input IF_1 power as intended. This linearity is crucial to successful QAM signal transmission. The peak output power was −14.5 dBm. The frequency dependence of the output power shown in Fig. 28 indicates that RF transmission is possible for all six channels (Fig. 2). Fig. 29 shows the output power spectra of a 3.5 GBd 32-QAM signal for the six channels. Each channel spectrum was measured separately with the spectrum analyzer [25]. The corresponding 32-QAM signal constellations are shown in Fig. 30. All channels achieved 17.5 Gb/s with 32 QAM. The gross aggregate data rate reached $17.5 \times 6 = 105$ Gb/s. The TX consumes 1.4 W of dc power.

Fig. 30 shows that the SNR depends strongly on the channel. This is because of the frequency-dependent characteristics

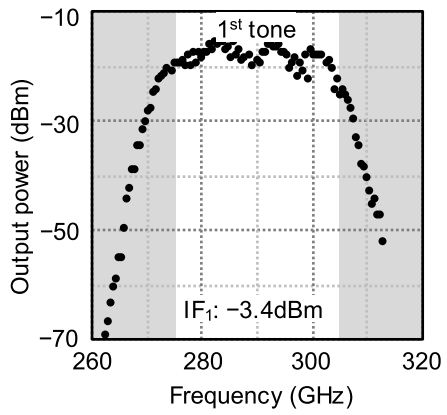


Fig. 28. Output RF power as a function of frequency.

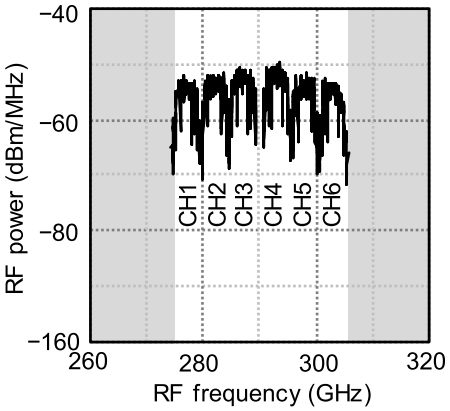


Fig. 29. Channel power spectra of a 3.5 GBd 32-QAM signal for the six channels (Fig. 2).

Channel RF Freq. (GHz)	CH1 275 – 279	CH2 280 – 284	CH3 285 – 289
Constellation (Equalized)			
EVM	8.9%rms	4.8%rms	7.0%rms
Data rate	17.5Gb/s	17.5Gb/s	17.5Gb/s
Channel RF Freq. (GHz)	CH4 291 – 295	CH5 296 – 300	CH6 301 – 305
Constellation (Equalized)			
EVM	7.1%rms	6.4%rms	5.9%rms
Data rate	17.5Gb/s	17.5Gb/s	17.5Gb/s

Fig. 30. 32-QAM signal constellations and EVMs at 17.5 Gb/s.

of the cubic mixer, discussed in Section IV. Fig. 31 shows the measured error-vector magnitude (EVM) and estimated SNR of a 3.5 GBd QPSK signal as a function of the center frequency of RF. The SNR was calculated from the following

TABLE I
PERFORMANCE COMPARISON OF THz TXs

Ref.	Technology	Freq. (GHz)	Modulation	Data rate (Gb/s)	$P_{\rm out}$ (dBm)	$P_{\rm dc}$ (W)
[12]	32-nm SOI CMOS	210	OOK	20	4.6	0.24
[13]	250-nm InP DHBT	298	NA	NA	−2.3	0.45
[14]	130-nm SiGe BiCMOS	240	64QAM	1.02	7	0.54
[15]	35-nm GaAs mHEMT	240	8PSK	96	−3.5	NA
[16]	35-nm GaAs mHEMT	240	QPSK	64	−3.6	NA
[19]	130-nm SiGe HBT	314	NA	NA	−8	0.13
[20]	130-nm SiGe BiCMOS	434	ASK	10	−18.5	0.12
[21]	65-nm CMOS	260	OOK	NA	5 (EIRP)	0.69
[26]	SBD mixer	300	64QAM	0.032	−15	NA
[27]	SBD mixer	340	16QAM	3	−17.5	NA
[28]	130-nm InP HBT	630	NA	NA	−30	0.65
[29]	250-nm InP HBT	300	QPSK	50	NA	NA
[30]	65-nm CMOS	240	QPSK	16	0	0.22
This work	40-nm CMOS	275–305 282	32QAM	17.5 × 6 30	−14.5	1.4

EIRP: Equivalent isotropically radiated power; SBD: Schottky-barrier diode.

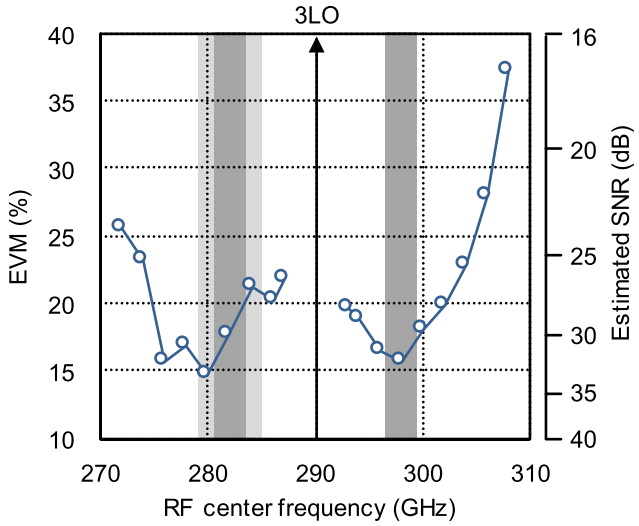


Fig. 31. Measured EVM of a 3.5 GBd QPSK signal and estimated SNR plotted against the center frequency of RF. The shaded regions have a high SNR.

rough approximate formula [41]:

$$\text{SNR} \simeq \frac{1}{\text{EVM}^2} \tag{7}$$

or

$$\text{SNR (dB)} \simeq -20\log_{10}\frac{\text{EVM (\%)}}{100}. \tag{8}$$

The measurement was made with a fixed LO (3LO = 290 GHz), and $\Delta f = |3\text{LO} - \text{RF}|$ was swept. The result is consistent with the discussion in Section IV. SNR degrades when Δf is either too small or too large. Fig. 31 explains why CH2 gave the lowest EVM in Fig. 30. In addition, the per-channel data rate of 17.5 Gb/s is limited by the noisiest channel. Higher per-channel data rates should, therefore, be achievable in the shaded regions in Fig. 31. With 3LO = 290 GHz and RF = 282 GHz (Δf = 8 GHz), we achieved 30 Gb/s signal transmission with 32QAM.

Table I shows a summary of performances of the state-of-the-art THz TXs. GaAs and InP technologies provide a very high $f_{\rm max}$ and hence high performance. Conventional CMOS TXs adopt a frequency-multiplier-last architecture [21], [30]. The strength of this 300 GHz TX is that it supports QAM despite the fact that it operates above the transistor $f_{\rm max}$. Note that the data rates quoted in Table I do not always represent the highest value achievable by the respective TX. This is because some of the experimental data are from wireless transmission experiments and some are from direct ("wired") measurements. It is also possible that the measured performance data were limited by the availability or performance of the test equipment. All the measurement data presented in this paper are from wired measurements. The results of wireless measurements with the improved setting [40] mentioned at the end of Section IV are presented elsewhere [42].

VI. CONCLUSION

We developed a QAM-capable 300 GHz TX fabricated using a 40 nm CMOS process that operated beyond the transistor $f_{\rm max}$. The key enabling component was its linear subharmonic mixer called the cubic mixer, which allowed the mixer-last architecture required for QAM signal transmission to be implemented without undue layout complication. The active balun and the quad-rat-race further contributed to realizing a compact power splitter and combiner. A data rate of 17.5 Gb/s was achieved with 32 QAM over six channels. The gross aggregate data rate reached 105 Gb/s. At an optimal frequency of 282 GHz, the highest single-channel data rate of 30 Gb/s with 32 QAM was achieved.

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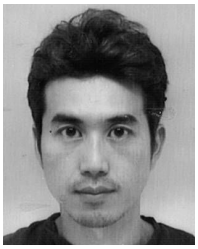

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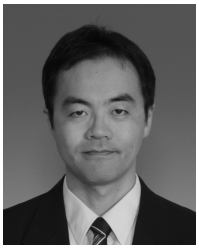

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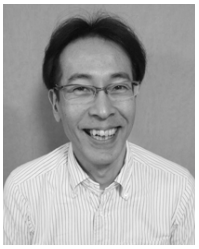

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