A 9-bit 1.8 GS/s 44 mW Pipelined ADC Using Linearized Open-Loop Amplifiers

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***Abstract*— This paper presents a 9-bit 1.8 GS/s pipelined analog-to-digital converter (ADC) using open-loop amplifiers. In this ADC, open-loop amplifiers are used as residue amplifiers to increase the sampling rate of the ADC with relatively low power consumption. A linearization technique is proposed to suppress the SNDR decrease caused by the nonlinearity of open-loop amplifiers. The attenuation in the capacitor digital-to-analog converter (CDAC) is utilized to calibrate the gain error of the pipelined stages. In addition, top-plate sampling is proposed to further enhance the power efficiency of the residue amplifiers. With these techniques, the ADC achieves a high sampling rate and high power efficiency. A prototype of the ADC is fabricated in 65 nm CMOS technology. An SNDR of 47 dB and a FoM of 134 fJ/conversion-step is achieved at a sampling rate of 1.8 GS/s with 900 MHz input, while consuming 44 mW from a 1.2 V supply.**

***Index Terms*— Analog-to-digital converter, double sampling, linearity enhancement, open-loop amplifier, pipelined ADC.**

I. Introduction

ADCS with a Gigahertz sampling rate and moderate resolution are widely used in software radios and 60 GHz wireless systems. To fulfill the performance requirements, pipelined ADC is a competitive candidate. However, realizing a Gigahertz sampling rate with relatively low power consumption is still very challenging for pipelined ADC, because the main difficulties lie in the residue amplifier.

Conventional pipelined ADCs use closed-loop amplifier to carry out residue amplification [1]–[3]. The closed-loop structure has two disadvantages. The first disadvantage is that the required high DC gain of the operational amplifier (opamp) becomes more costly due to the reduction of the intrinsic gain in advanced CMOS technology. The opamp used in [4] applies two level gain boosting to obtain a high DC gain. The gain of the main booster is also enhanced by a nested booster. However, the two-level gain boosting leads to more power consumption and lower bandwidth because more internal amplifiers are added. In [5], the high DC-gain is realized by increasing the stage number of the opamp. This method also costs more power and decreases bandwidth, because one more stage and pole are introduced. The second disadvantage is that the closed-loop structure has a stability issue, so that a sufficient phase margin is required. To obtain a sufficient phase margin, generally the second pole of the closed-loop amplifier should be three times higher than the first pole. Therefore, extra power is consumed to realize the required bandwidth and the power efficiency is lowered. Such as [6]–[8], the ADCs consume relatively high power to realize a Gigahertz sampling rate due to the low power efficiency of the closed-loop structure. In summary, it is difficult for the closed-loop structure to achieve a Gigahertz sampling rate with relatively low power.

To relax the requirement of the high DC gain of the amplifier, interpolation-based amplification has been reported [9]–[11]. Two signal paths are used for the interpolation, so that only the relative gain accuracy is required instead of the absolute value. Although this technique reduces the power consumed by realizing high-DC gain and sufficient phase margin, two signal paths as well as two CDACs and residue amplifiers are needed. Thus, the power consumption is proportional to twice of the bandwidth. In addition, to relax the linearity requirement of its open-loop amplifier, a 4-bit first pipelined stage is used to reduce the effective input range of the amplifier. However, the number of comparators and input load of the ADC [10] are increased.

In the open-loop structure, the output of the CDAC is connected directly to the input node of the open-loop amplifier. Therefore, this structure does not have the requirement of a high DC gain and a sufficient phase margin, and only needs one signal path. Thus, open-loop based amplification has higher power efficiency and bandwidth. However, due to the nonlinearity of open-loop amplifiers, the resolution of the ADC is limited. In [12] and [13], only 6-bit resolution is achieved. To enhance the resolution, techniques such as those in [14-18] use digital-domain calibration to suppress the nonlinearity caused by open-loop amplifiers. However, digital-domain calibration usually estimates the nonlinearity factor from output codes of the ADC by using statistical methods or complex algorithms. According to the estimation, factors in the transfer function are corrected step by step through the least mean squares (LMS) method, until the distortion becomes smaller than expected. Therefore, this kind of method needs a large number of samples and hundreds of thousand conversions [15], [16]. Usually off-chip memories and a processor are required, which are difficult to integrate [17], [18].

In this work, a high-speed and low-power open-loop pipelined ADC is developed. A linearization technique is proposed to suppress the nonlinearity of the open-loop amplifier

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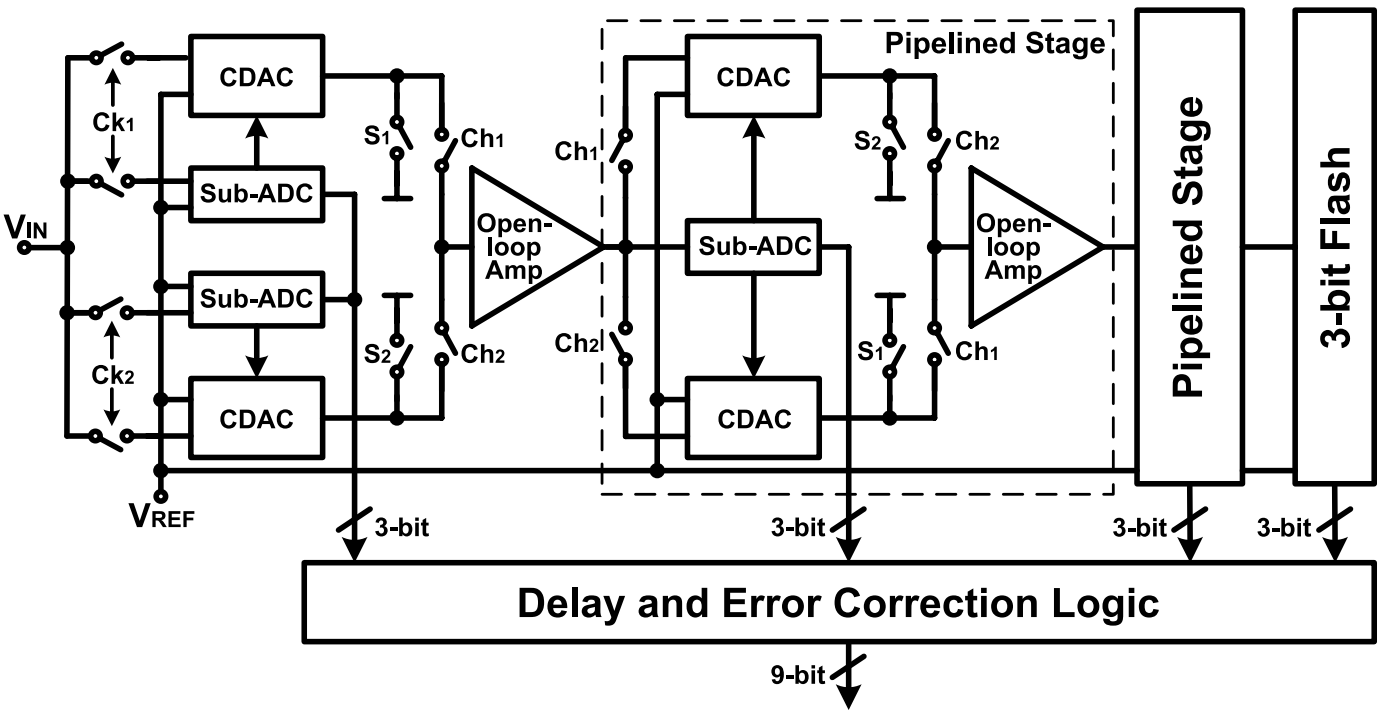

Fig. 1. Block diagram of the proposed ADC.

without any digital-domain calibrations. CDAC based gain calibration is proposed to obtain the accurate gain of the pipelined stages. Top-plate sampling is proposed to further enhance the power efficiency of the open-loop amplifier. By using these techniques, the issues of open-loop structure are suppressed, while maintaining the advantages. Thus, a 9-bit resolution and a sampling rate of 1.8 GS/s are achieved with a power consumption of 44 mW.

This paper is organized as follows. Section II introduces the architecture of the proposed ADC. Section III describes the proposed linearization technique for the open-loop amplifier, stage gain calibration and top-plate sampling timing diagram. Then, the measurement results are presented in Section IV. The paper is concluded in Section V.

II. ADC Architecture

A. Block Diagram of the Proposed ADC

Conventional pipelined ADCs use a high DC gain opamp in a closed-loop. Benefit from the high gain, the accurate stage gain is achieved by a negative feedback loop and the nonlinearity is also suppressed. As introduced above, to achieve high power efficiency and bandwidth, open-loop amplifiers are used in the proposed ADC. The block diagram is shown in Fig. 1. The ADC consists of four stages. In the first stage, the input analog signal is sampled by two channels of CDACs and sub-ADCs alternatively. When one channel of the CADC is sampling the input signal, another channel of the CDAC outputs the folded signal to the open-loop amplifier. The open-loop amplifier is shared between the two channels to enhance its efficiency. In the second and the third stage, sub-ADC is shared and connected directly to the output of the previous amplifier without sampling network, so that the load of the residue amplifier is reduced sufficiently. The flash ADC in the last stage is also connected directly to the output of the residue amplifier and converts at the same rate of the sampling clock. The three pipelined stages convert 3-bit output codes including 1-bit redundancy, and the last stage is a 3-bit Flash ADC. The output codes from each stage flow into the digital logic of delay and error correction, and then compose the 9-bit output. In this ADC, linearization technique for open-loop amplifier and CDAC based calibration for stage gain are proposed, and top-plate sampling for double sampling structure is employed. Each technique will be introduced one by one in Section III.

B. Linearity Requirement of the Open-Loop Structure

One of the most important factors in the open-loop based pipelined ADC is linearity. Because of the feature of pipelined ADC, the nonlinearity of open-loop amplifier in the first stage is dominant. Assuming, only the open-loop amplifier in the first stage is non-ideal. Since the distortion of the ADC output mainly comes from the error at the folding point in the first stage, it can be derived as follows. Assuming the transfer function of the open-loop amplifier is $V_{OUT} = \alpha V_{IN} + \beta V_{IN}^3$, where α and β are the first-order coefficient and the third-order coefficient of the open-loop amplifier, respectively. The input-referred error at the folding point of pipelined transfer function can be expressed as $Error = 2\beta(0.5F_s/2^{N_1})^3/\alpha$, where N_1 represents the resolution of the first pipelined stage, $0.5F_s/2^{N_1}$ is the input amplitude of the residue amplifier, and V_{FS} represents the full-scale reference range. Substituting $LSB = 2F_S/2^N$ (N is the ADC resolution) into it, (1) can be derived. Since $6.02ENOB + 1.76 = 10log_{10}(^{P_{Signal}/}_{\frac{LSB^2}{12} + P_{Error}})$ and the effective number of bits (ENOB) equals to N if there is no distortion, the ENOB can be described as $ENOB = N - 1.67log_{10}(1 + 12P_{Error}/LSB^2)$,

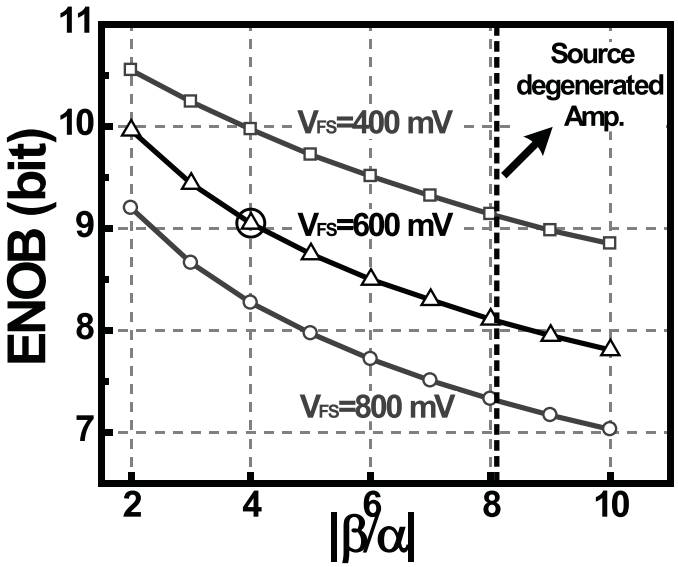

Fig. 2. Simulated result of ENOB vs. linearity and signal range.

where $P_{Error} = Error^2$. Thus, ENOB can be described as (2).

$$Error/_{LSB} = \frac{\beta}{8\alpha} \cdot 2^{N-3N_1} V_{FS}^2 \tag{1}$$

$$\begin{aligned} ENOB \approx & N - 1.67 log_{10} \left\{ 1 + 12 Error^2 / LSB^2 \right\} \\ = & N - 1.67 log_{10} \left\{ 1 + \frac{3}{16} (|\beta/\alpha| \cdot 2^{N-3N_1} V_{FS}^2)^2 \right\} \end{aligned} \tag{2}$$

Therefore, the performance of the pipelined ADC is strongly affected by the linearity of the residue amplifier, the resolution of the first pipelined stage, and the reference range.

Generally, the linearity of an amplifier's output signal decreases along with the increasing of the input signal range. Therefore, a smaller V_{FS} and a larger N_1 are preferred to suppress the distortion caused by the nonlinearity of the residue amplifier. However, a smaller V_{FS} leads to a lower signal-to-noise ratio, and a larger N_1 leads to higher stage gain, larger power consumption, and heavier load for front-end circuits. Thus, trade-off exits among these parameters.

By considering the linearity, stage gain, and power consumption, N_1 is designed as 3 in the proposed ADC. The simulated result of the relationship among ENOB, $|\beta/\alpha|$ and V_{FS} is shown in Fig. 2. In the simulation, a 3-bit pipelined stage using open-loop amplifier is followed by an ideal back-end ADC. Obviously, a smaller V_{FS} (such as 400 mV) relaxes the requirement of the amplifier's linearity. However, considering the trade-off among the requirement of noise, sampling capacitance and power consumption, larger signal-to-noise ratio is better in terms of power efficiency. On the other hand, a larger V_{FS} (such as 800 mV) leads to more stringent requirement of linearity. According to the PVT simulation result of the proposed amplifier's linearity (shown in the next section), a V_{FS} of 600 mV is the largest range which the proposed amplifier can tolerance. Under this condition which $V_{FS} = 600\,mV$ and $N_1 = 3$, the $|\beta/\alpha|$ of conventional source-degenerated amplifier is 8, which is only able to support an 8-bit resolution (shown in Fig. 2) and becomes worse if PVT variations are considered. The PVT simulation result shows the $|\beta/\alpha|$ of conventional source-degenerated amplifier will be higher than 14. To support a resolution of 9 bits, at least a $|\beta/\alpha|$ less than 4 is required even when there are some PVT variations. The proposed linearization technique, which is introduced in the following section, is able to suppress the nonlinearity of the open-loop amplifier to fulfill the requirement.

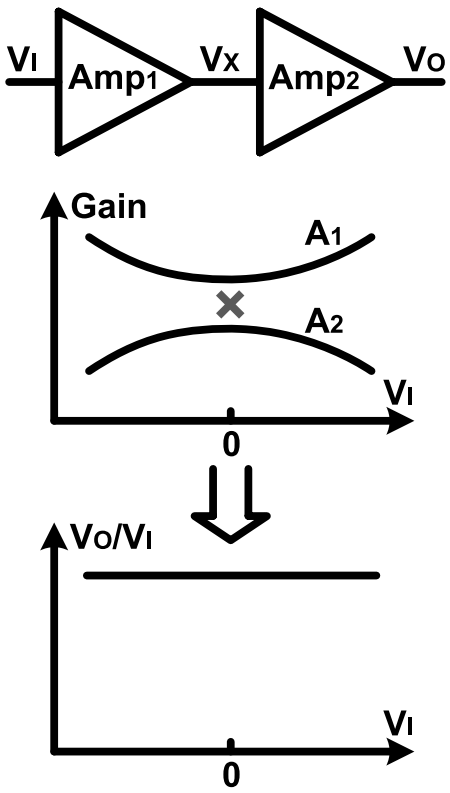

Fig. 3. Product of two gains with reversed nonlinearity.

III. Circuit Design

A. Linearized Open-Loop Amplifier

The idea is to make a product of two reversed nonlinearities, shown in Fig. 3. Conventionally, due to the variation of the drain-source voltage and g_m, the differential current of the input transistors does not follow the input amplitude linearly. This results in a decreasing of gain while input amplitude becomes larger, such as A_2 (the gain of Amp_2). Therefore, if a gain with reversed nonlinearity, such as A_1 (the gain of Amp_1), can be obtained, the product of these two gains can be much flatter. It is assumed that the transfer functions of amplifier Amp_1 and Amp_2 in Fig. 3 are $V_X = \alpha_1 V_I + \beta_1 V_I^3$ and $V_O = \alpha_2 V_X + \beta_2 V_X^3$, respectively. Here α_i and β_i represent the first-order and the third-order coefficients, respectively. The final output V_O can be described as:

$$V_O = \alpha_1 \alpha_2 V_I + (\alpha_1^3 \beta_2 + \alpha_2 \beta_1) V_I^3 \tag{3}$$

In (3), $\alpha_1^3 \beta_2 + \alpha_2 \beta_1$ is the third-order coefficient of this two-stage amplifier. It is obvious that α_1 and α_2 have the same sign. Thus, if β_1 and β_2 are opposite, the $\alpha_1^3 \beta_2 + \alpha_2 \beta_1$ could approach zero, which means high linearity.

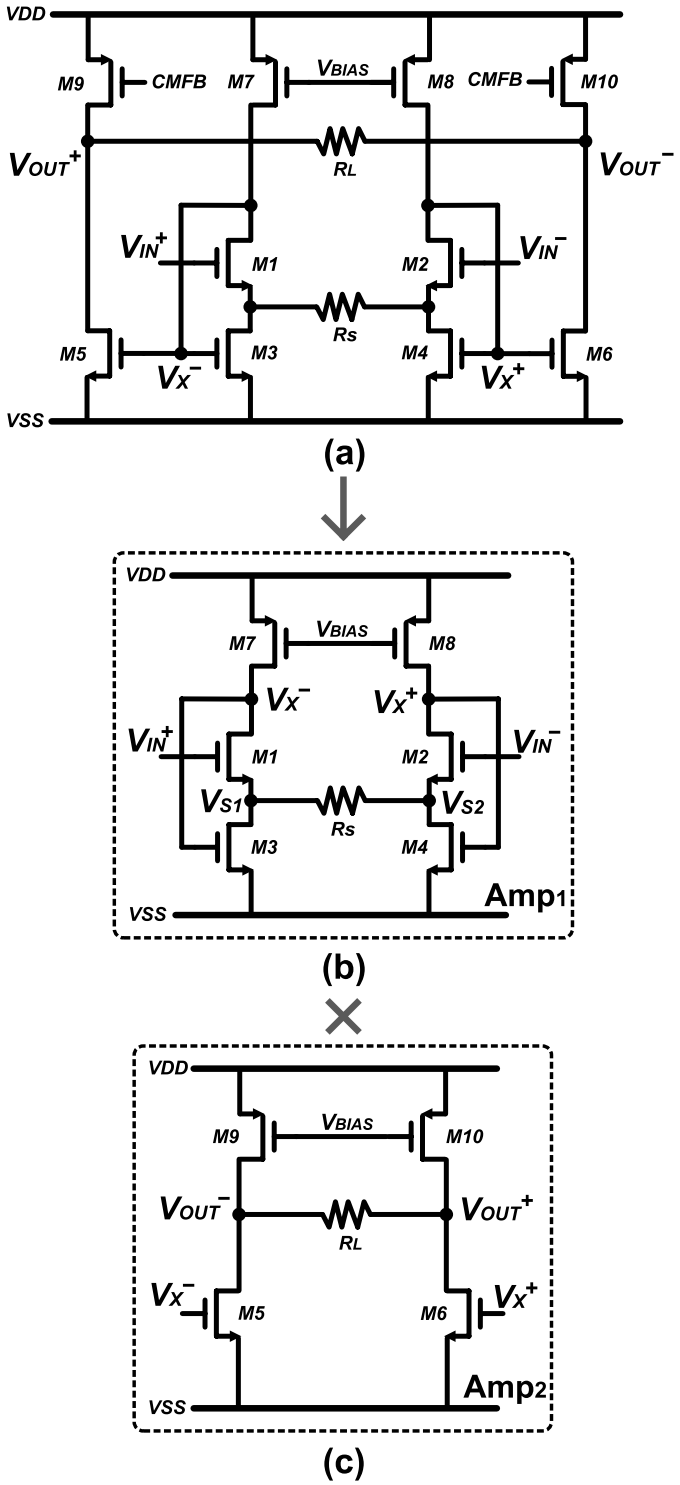

Fig. 4. Circuit implementation of the linearized open-loop amplifier.

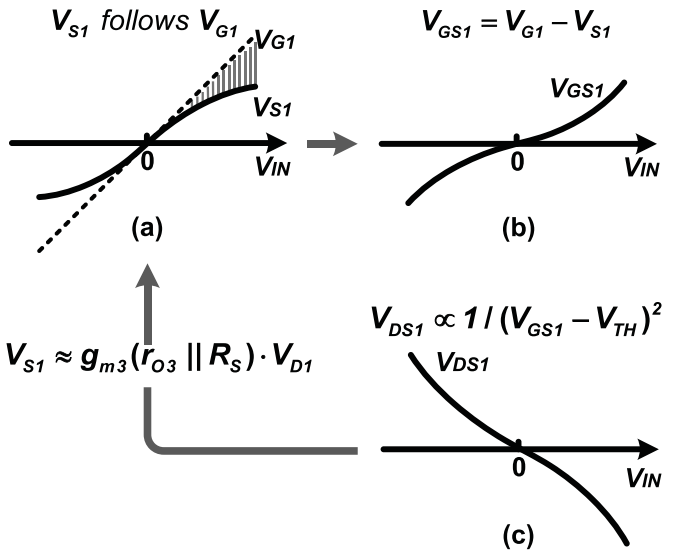

Fig. 5. Flow of the generation of A_1

The circuit implementation of the linearized open-loop amplifier is shown in Fig. 4(a). Although, the transconductor used in the Gm-C filter [19] has a similar topology, this kind of current mirror is difficult for realizing sufficient linearity and bandwidth for a 9-bit resolution and a Gigahertz sampling rate, due to the following two reasons. (1) The transconductor works under the condition that $g_{m1}r_{O1}g_{m3}R_S \gg 1$, so that V_{S1} follows V_{INP} linearly, and a linear current in the first-stage can be obtained, expressed as $I_{M3} \approx -(V_{IN}^{+} - V_{IN}^{-})/R_S$. (where g_{mi} is defined as the transconductance of M_i, r_{Oi} is defined as output resistance of M_i) Then, the linear current is copied to the output by the current mirror. Although the transconductor uses a large R_S to obtain a linear current in the first stage, due to the non-ideal current mirror and the nonlinear feature of M_5, the output voltage becomes nonlinear. (2) Because the gain of the amplifier is proportional to R_L/R_S, a large R_S leads to high output impedance. Therefore, the transconductor is not suitable for the high-speed application.

To realize an open-loop amplifier with high linearity and low output impedance, the amplifier in Fig. 4(a) is considered to consist of two voltage amplifiers, shown in Fig. 4(b) and (c). If the nonlinearities of amplifier Amp_1 and Amp_2 are reversed, their product can achieve high linearity, as discussed above.

Amplifier Amp_2 is a conventional common-source amplifier. Its gain A_2 is decreasing as the input amplitude becomes larger, which means β_2 is negative. Thus, to compensate the nonlinearity of A_2, β_1 should be positive with a proper value. Fig. 5 shows the generation of A_1 intuitively. Assuming M_7 and M_8 are ideal current sources, the gain between V_{S1} and V_{IN}^{+} can be described as (6), which is derived from (4) and (5).

$$g_{m1}\left(V_{IN}^{+} - V_{S1}\right) + \left(V_X^{-} - V_{S1}\right)/r_{O1} = 0 \tag{4}$$

$$V_{S1}/r_{O3} + g_{m3}V_X^{-} + \left(V_{S1} - V_{S2}\right)/R_S = 0 \tag{5}$$

$$V_{S1}/V_{IN}^{+} = \frac{1}{\frac{1/r_{O3}+2/R_S}{g_{m1}g_{m3}r_{O1}} + \frac{1}{g_{m1}r_{O1}}}, \tag{6}$$

where $V_{S1} = -V_{S2}$. As in the conventional amplifier, $g_{m1}r_{O1}$ decreases when input amplitude becomes larger. Therefore, V_{S1}/V_{IN}^{+} is decreasing, as shown in Fig. 5(a).

Because V_{IN}^{+} is also V_{G1}, drawn as a dashed line, the difference between the dashed line and V_{S1} is the gray area, V_{GS1}. The gray area indicates that, the gain between signal V_{GS1} and V_{IN}^{+} is increasing when input amplitude becomes larger, as shown in Fig. 5(b). Because the current in M_1 is almost constant, V_{DS1} is proportional

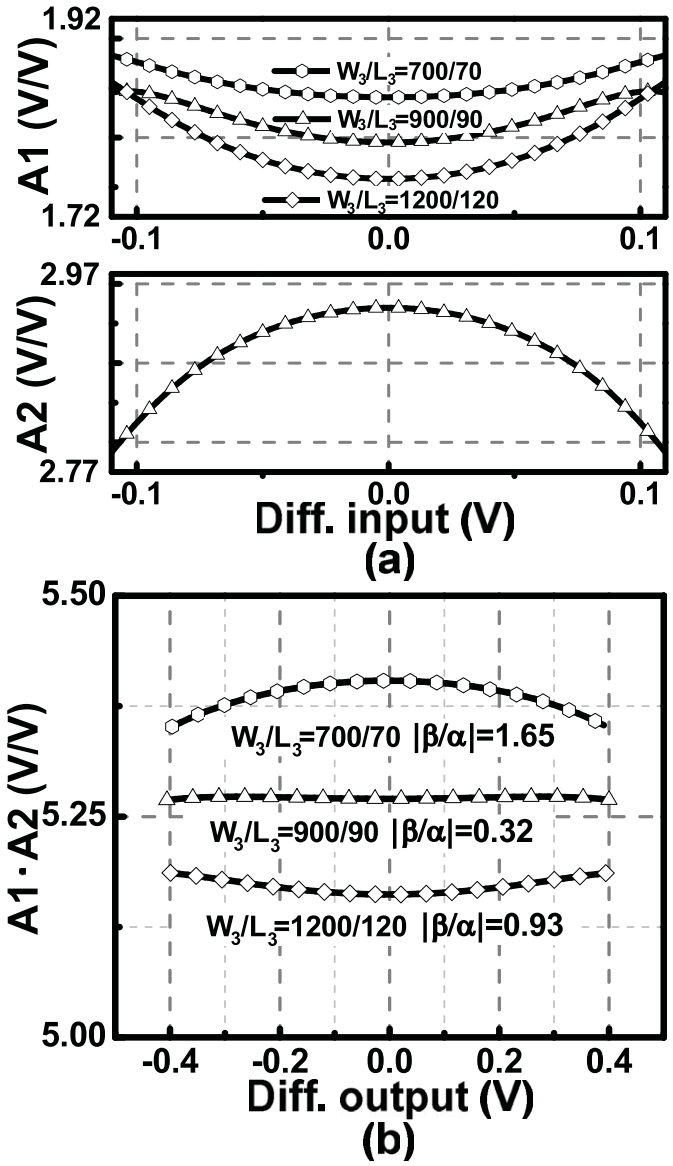

Fig. 6. Simulated result of the linearized open-loop amplifier. (In order to compare them when the gain is different, the same output range is used as a reference. α and β represent the first order coefficient and the third order coefficient, respectively.)

to $1/(V_{GS1,2} - V_{TH})^2$. Therefore, the area drawn in gray is amplified and the gain between signal V_{DS1} and V_{IN}^+ is increasing when input amplitude becomes larger, as shown in Fig. 5 (c). As a result, the gain of amplifier Amp_1 is also increasing when input amplitude becomes larger. Therefore, a positive β_1 is realized.

Until now, a positive β_1 and a negative β_2 are obtained, so the linearity of the amplifier is already enhanced. To further suppress the nonlinearity, the values of β_1 and β_2 need to be matched, described as follows.

The signal V_{D1} is feedback to V_{S1} through transistor M_3. The feedback factor is described by (7):

$$Loop\ gain \approx g_{m3}(r_{O3}||R_S) \tag{7}$$

As shown in Fig. 5, curves V_{S1}, V_{GS1}, and V_{DS1} are in the feedback loop, therefore the shapes of these curves are affected by the feedback loop gain. In (7), the value of g_{m3}, r_{O3}, and R_S can affect the nonlinearity by adjusting the local loop gain. In the design, g_{m3} is decided by the current and $V_{GS3} - V_{TH}$ in Amp_1, which are designed under the consideration of power efficiency and transistor's operation region. The value of R_S is decided by the amplifier's gain and R_L, where small resistances are preferred. Thus, the parameter r_{O3} is selected to adjust the loop gain in the design. Therefore, the value of β_1 can be adjusted to match with β_2.

TABLE I
SUMMURIZED VARIATION OF $|\beta/\alpha|$ UNDER DIFFERENT CORNERS

Corners	ss	sf	tt	fs	ff
Average	1.52	3.05	0.39	1.89	1.85
Standard deviation	0.20	0.12	0.08	0.13	0.38

In summary, the proposed amplifier utilizes two gains with reversed shapes to suppress the nonlinearity of each other. In addition, the local feedback loop gain is optimized to match the value of β_1 and β_2, so that the linearity is highly improved.

The simulated result of the linearized open-loop amplifier is shown in Fig. 6. The gains of amplifier Amp_1 with different r_{O3} values are shown in Fig. 6(a). The r_{O3} is adjusted by changing the channel length of M_3 while maintaining the ratio between width and length. As shown in Fig. 6(a), the nonlinearity of A_1 in all three cases is different, and all of them are reversed to A_2. The product of A_1 and A_2 is shown in Fig. 6(b). With a different A_1, the gain of the proposed two-stage amplifier shows different linearity. When L_3 is 70 nm, the gain is still decreasing when the input amplitude becomes larger ($|\beta/\alpha| = 1.65$). When L_3 is 90 nm, the optimized gain is almost flat ($|\beta/\alpha| = 0.32$). When L_3 is 120 nm, the gain starts to increase when the input amplitude is larger ($|\beta/\alpha| = 0.93$). α and β represent the first order coefficient and the third order coefficient, respectively. And they are obtained by polynomial fitting of the simulated output of the amplifier. Even under the non-optimized cases, the linearity of the proposed amplifier is still much higher than that of conventional open-loop amplifiers ($|\beta/\alpha| = 8$).

As discussed before, the proposed method does not require large R_S to obtain a linear current in Amp_1. And even realizing a linear current by employing a large R_S, the linearity of the whole amplifier is still not good. The following simulation compares the linearity of current in Amp_1 and the gain of the whole amplifier. The simulated results of the transconductance between $I_{M3} - I_{M4}$ and the input signal with different R_S values are shown in Fig. 7(a). The simulated voltage gain of the two-stage amplifier with different R_S and R_L is shown in Fig. 7(b), and proves that using large R_S to obtain a more linear current in the first stage can-not realize a high-linearity open-loop amplifier, as discussed before.

As discussed in Section II, $|\beta/\alpha|$ should be smaller than 4 to support 9-bit resolution even when PVT variations exit. Although the open-loop amplifier is more sensitive, the gain of the proposed amplifier is the product of two gains with

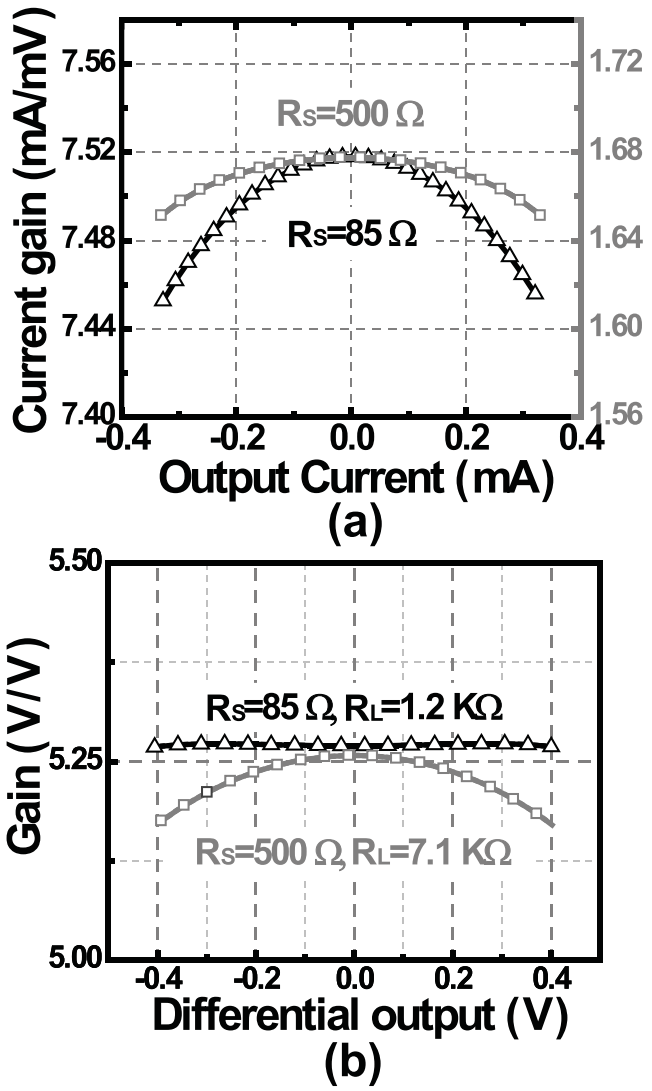

Fig. 7. Simulated results of (a) transconductance of Amp_1, and (b) voltage gain of the two-stage amplifier with different R_S and R_L.

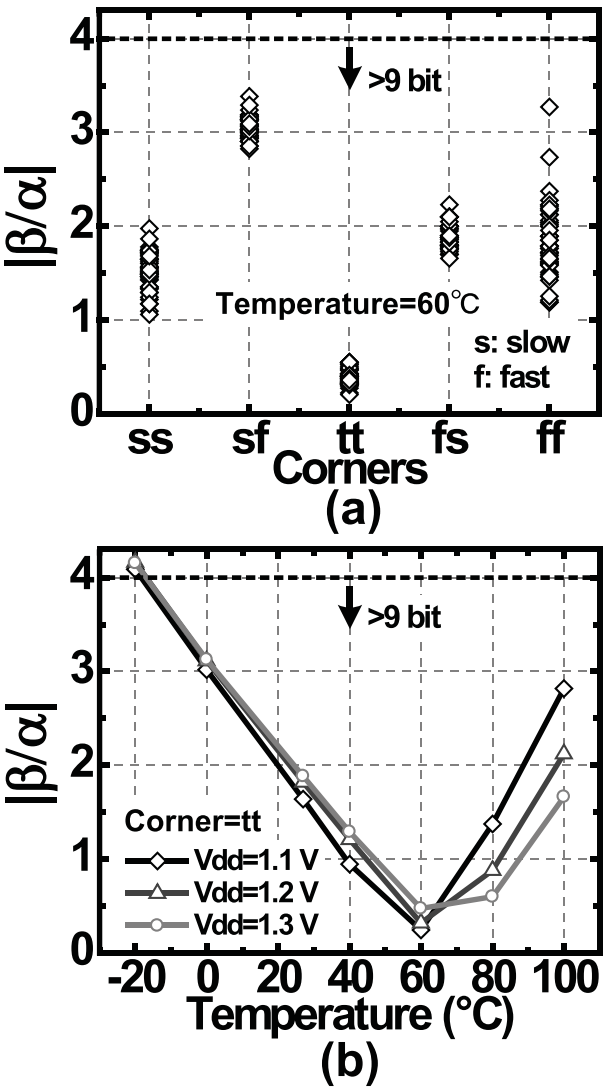

Fig. 8. (a) Simulated $|\beta/\alpha|$ of the proposed amplifier under different corners, and (b) with different supply voltages and temperature variations.

reversed nonlinearities. Therefore, even when there are some PVT variations, the linearity of the proposed amplifier is still higher than that of conventional open-loop amplifiers. The Monte Carlo simulation results of the linearity under different corners at the temperature of 60 C are shown in Fig. 8(a). A 50-iteration Monte Carlo simulation is run under the corners of ss, sf, tt, fs, and ff. The results indicate that the linearity of the proposed open-loop amplifier is high enough to support 9-bit resolution. Table I summarizes the average value and standard deviation of $|\beta/\alpha|$ under each corner. The averaged $|\beta/\alpha|$ under the corner of tt is the best, because the matching between Amp_1 and Amp_2 is optimized under the corner of tt, as discussed before. The nonlinearity of Amp_1 is decided by the local feedback loop gain $g_{m3}(r_{O3}||R_S)$. Thus, its value varies under different corners, since the value of V_{TH} affects both g_{m3} and r_{O3}. In consequence, the variation of the nonlinearity of Amp_1 causes the different $|\beta/\alpha|$ under each corner. Under all situations, the value of $|\beta/\alpha|$ is smaller than 4 which can support a resolution of higher than 9 bit. The simulated linearity with different supply voltages and temperature variations when under the corner of tt is shown in Fig. 8(b). When the supply voltage is 1.1 V, 1.2 V, and 1.3 V, the linearity of the proposed open-loop amplifier is high enough to support 9-bit resolution even when the temperature varies from 10 degrees to 100 degrees. As discussed above, the value of local feedback loop gain affects the nonlinearity. Therefore, different V_{TH} under different temperature causes the variation of nonlinearity. Since the optimization of the matching between Amp_1 and Amp_2 is carried under 60 C, the value of $|\beta/\alpha|$ increases when temperature is changed.

In terms of settling time, although the proposed open-loop amplifier is a two-stage amplifier with a local feedback loop, the frequency response is only slightly affected because the load capacitance of the first stage is very small. The simulated step response of the proposed amplifier is compared with a single-stage amplifier in Fig. 9(a) and the partially enlarged view of settling point is shown in Fig. 9(b). In the simulation, the two amplifiers have the same load capacitance of 200 fF and consume the same current of 7.6 mA. (The sampling capacitance in the second pipelined stage is 100 fF.

TABLE II
STEP RESPONSE COMPARISON

Corner @ 27 ℃	tt	ss	ff	fs	sf
Δt (ps)*	28	45	6	71	24
Temperature (℃) @ tt	-40	0	40	80	120
Δt (ps)	32	29	26	23	16

* Δt equals to the settling time of the proposed amplifier minus that of single stage amplifier

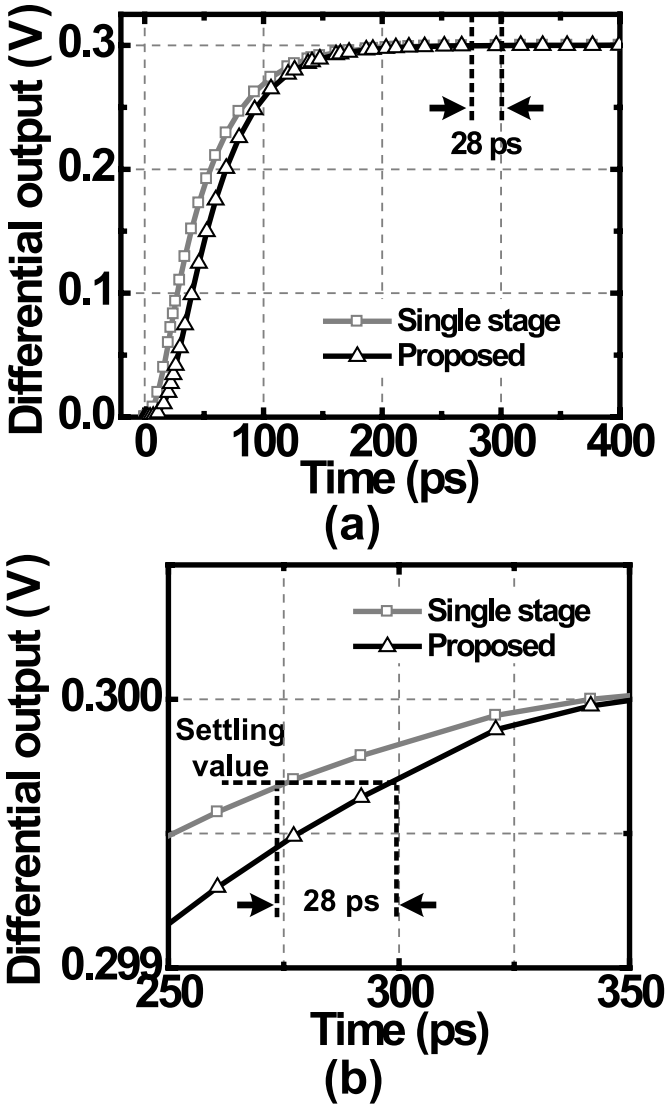

Fig. 9. (a) Comparison of step response between the proposed amplifier and a single-stage amplifier, (b) partially enlarged view of settling point.

Considering the parasitic and the input load of sub-ADC, 200 fF is used in the simulation) At room temperature and the corner of tt, the settling time of the proposed amplifier is about 28 ps longer than the single-stage open-loop amplifier,

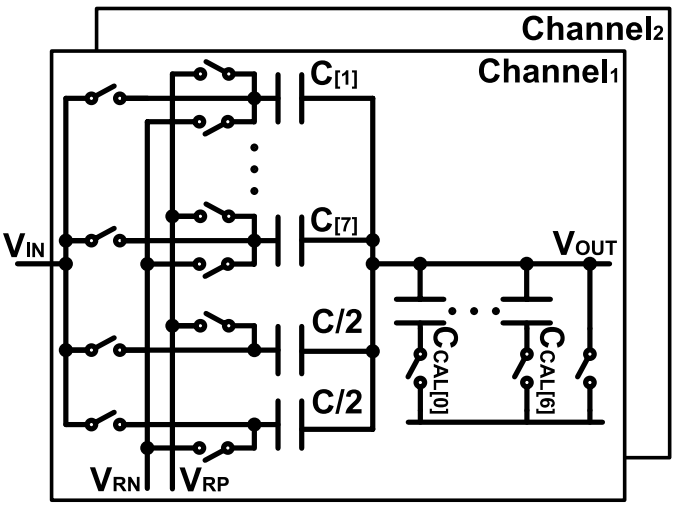

Fig. 10. The CDAC of the propsed ADC.

when settling error is 0.1%. In addition, the simulated results of settling time under different corners and temperature are compared in Table II. The drawback of settling time is much less than the benefit of high linearity.

B. CDAC and Gain Calibration

Pipelined ADC requires accurate gain of the pipelined stages. The stage gain error can be easily estimated at the folding point of the pipelined stage transfer curve. The error compensation is introduced in the following.

The proposed ADC uses the CDAC to do stage gain calibration. The detail of the CDAC is shown in Fig. 10. There are two channels of CDACs, and the output node of each channel connects to the input node of the residue amplifier alternatively. Each CDAC has seven capacitors with the same capacitance, and two with half of the capacitance. These capacitors compose the sampling network for the input signal. The total sampling capacitance in each channel of the CDAC and sub-ADC in the first stage is approximately 480 fF. After sampling the input, $C_{[1]}$ to $C_{[7]}$ are connected to either V_{RP} or V_{RN}, decided by the sub-ADC. The comparator used in sub-ADC has the same structure as that in [20]. The other two capacitors are connected to V_{RP} and V_{RN}, respectively. In this way a 3-bit (with 1-bit redundancy) pipelined transfer function can be obtained. The ADC references for CDAC as well as sub-ADC are generated by off-chip voltage source. And there are some large on-chip decoupling capacitors around the ADC core. The capacitance is about 150 pF for each. The power consumed by references is approximate 0.8 mW. At the output node of the CDAC, a 7-bit capacitor array is added. The top-plates of this array are connected together to the output node. The bottom-plates of this array are either floating or connected to ground, as decided by the control codes for the stage gain. Therefore, the stage gain can be described as (8):

$$Stage\ gain = \frac{8C}{8C + \sum C_{CAL[i]}} \cdot A_1 A_2 \tag{8}$$

The total sampling capacitance in the CDAC is 240 fF. The total calibration capacitance is 40 fF. The parasitic capacitance

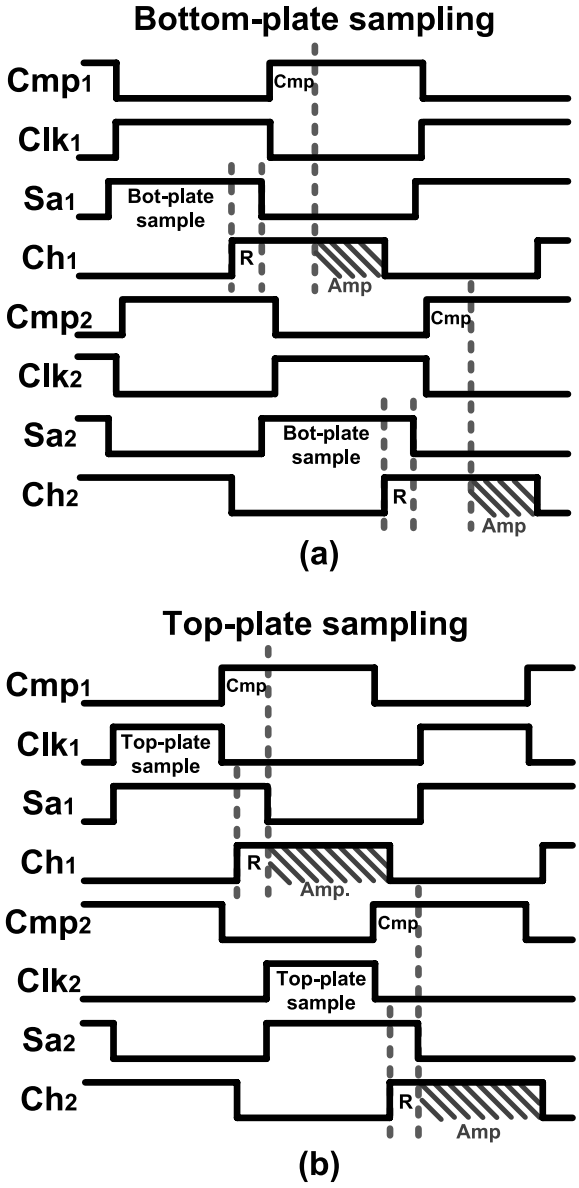

Fig. 11. (a) Timing diagram of bottom-plate sampling. (b) Timing diagram of top-plate sampling.

at the output of the CDAC is approximate 50 fF. The cover range of the stage gain calibration and the simulated gain of residue amplifier are summarized in Table III. The calibration is able to cover the gain variation of amplifier from 40 degree to 120 degree and the corners except ss. In addition, the V_{BIAS} in Amp_1 can tune the gain. The resolution of the capacitor array is decided by the requirement of the stage gain. For this ADC, the requirement of stage-gain error can be derived as follows. The maximum error caused by inaccurate stage gain is occurred at the folding point of pipelined transfer function. Therefore, $\Delta\text{gain}\frac{V_{FS}}{2^{N_1}}/gain < \frac{1}{8}LSB$, where $N_1 = 3$, $\text{LSB} = \frac{2V_{FS}}{2^9}$. Thus, $\frac{\Delta gain}{gain} > 0.39\%$. If considering the worst case, $1 - \frac{240}{240 + C_{CAL_{LSB}}} > 0.39\%$ should be satisfied. Therefore, The $C_{CAL[0]}$ should be less than 1 fF, which means the capacitor array should at least has 6 bit. In the design, a 7-bit array is employed for some margin.

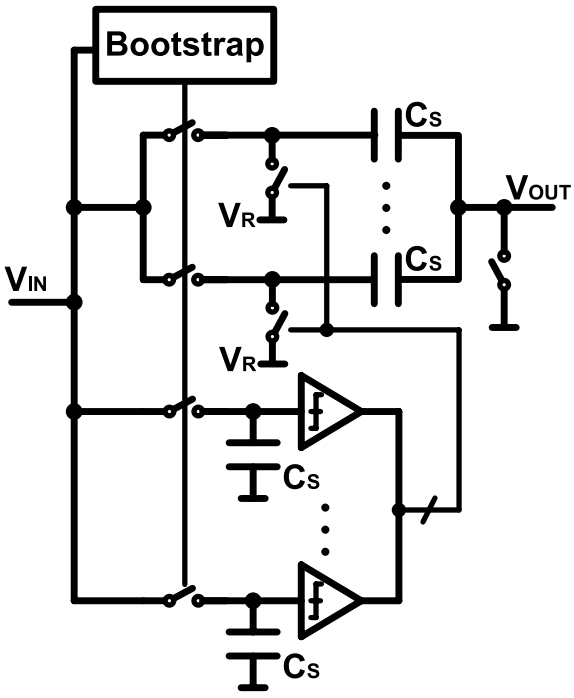

Fig. 12. The sampling network of CDAC and sub-ADC.

In this way, the stage gain of the pipelined ADC is controlled by the CDAC instead of the residue amplifier. Therefore, the linearity of the amplifier will not be affected.

C. Top-Plate Sampling

This ADC applies double sampling architecture, therefore a memory effect occurs between two channels. When the CDAC of channel1 is outputting the analog signal to the residue amplifier, the CDAC of channel2 is sampling the input signal. After channel1 finishes its amplifying phase, some charges remain at the input node of the residue amplifier. Then, when the CDAC of channel2 starts to connect to the input node, the remaining charges cause distortion. Therefore, a reset phase is needed between the two channels to get rid of the charges.

If a conventional bottom-plate sampling is used shown in Fig. 11(a), the sampling maintains until the reset phase is finished because the reset is carried out at the bottom-plate of sampling capacitors. Then, the comparator starts to compare. Therefore, the amplification must wait a reset time pluses a comparison time. As a result, the bottom-plate sampling causes some waste of time in case of double sampling.

To overcome this issue and further enhance the power efficiency, top-plate sampling is proposed in this ADC, as shown in Fig. 11(b). After the top plates of the sampling capacitors disconnecting to the input signal, the charges stored in the capacitors are conserved. Then the comparison and reset are started and use almost the same time window. Thus, the amplifier only needs to wait a comparison time before amplifying. At the same time, another channel is starting to sample when the reset phase is finished. In this way, the amplification time is increased, which is about 400 ps when the sampling rate is 1.8 GS/s.

TABLE III
GAIN VARIATION OF AMPLIFIER AND COVER RANGE OF CALIBRATION

Corner @ 60 ℃	ss	sf	tt	fs	ff	Cover range
Amplifier's gain	5.83	5.36	5.27	5.03	4.93	4.83-5.50
Temperature (℃) @ tt	-40	0	40	80	120	
Amplifier's gain	5.43	5.39	5.35	5.22	5.08	

TABLE IV
KEY PARAMETERS OF THE PROPOSED ADC

Amplifier (First stage)	Power Con. (mA)	$\lvert\beta/\alpha\rvert$	Gain (V/V)
	7.6	0.32	5.3
Capacitance (fF)	Sampling (1^{st} stage)	Sampling (other stages)	Total C_{CAL}
	480	100	40
Timing (ps)	Amplifier	Comparator	Reset
	400	150	100

To suppress the non-ideal effects caused by top-plate sampling, bootstrap switches are used in the sampling network of CDAC and sub-ADC. The topology of them is shown in Fig. 12, drawn in single ended. The sampling switches in CDAC and sub-ADC are driven by the same bootstrap driver. In addition, the LPE simulation result of the top-plate sampling network using bootstrap switches shows a resolution higher than 9 bit.

Table IV summarizes the key parameters of the proposed ADC. The linearized open-loop amplifier in the first stage has a $|\beta/\alpha|$ of 0.32 in the simulation, while the $|\beta/\alpha|$ of the source-degenerated amplifier is 8. The sampling capacitance in the first stage is about 480 fF, including the capacitors of the CDAC and the sub-ADC. In the second and third stages, the capacitance of the CDAC is approximately 100 fF. The capacitance for the CDAC gain calibration is approximately 40 fF. The input capacitances of amplifier and comparators, and other parasitic capacitors are not included in the values shown in Table IV. Also the times of the rising and falling edge are not contained.

IV. EXPERIMENTAL RESULTS

The prototype ADC has been fabricated in 65 nm CMOS technology with an active core area of 0.15 mm^2. Fig. 13 shows the chip die photograph. The ADC has been measured with package. All the measurement data reported below are

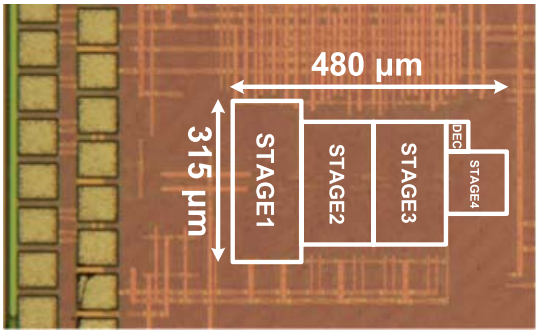

Fig. 13. ADC chip photograph.

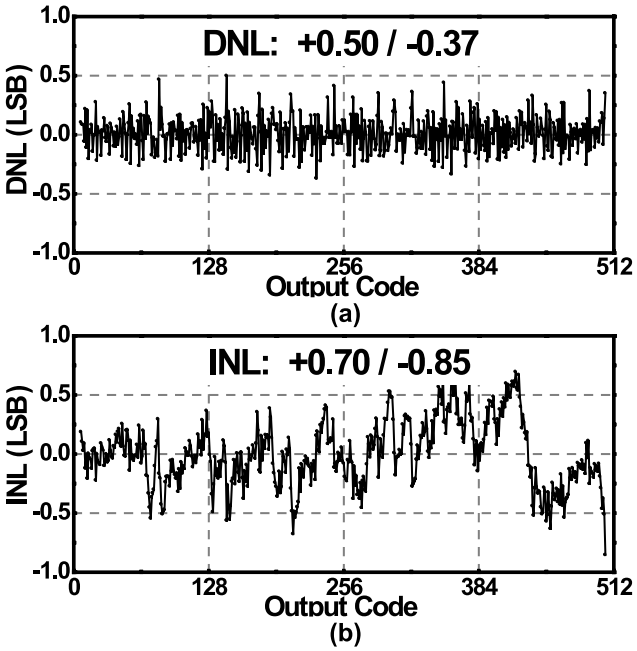

Fig. 14. Measured DNL and INL.

at a sampling rate of 1.8 GS/s, and the power supply is 1.2 V. Fig. 14(a) and (b) show the measured differential nonlinearity (DNL) and integral nonlinearity (INL), respectively. The maximum DNL is within +0.50 LSB and 0.37 LSB. The maximum INL is within +0.70 LSB and 0.85 LSB. Fig. 15(a) and (b) show the output spectrums when the analog input frequency is 10 MHz and 900 MHz, respectively (the output code is down sampled by a factor of 9). When the

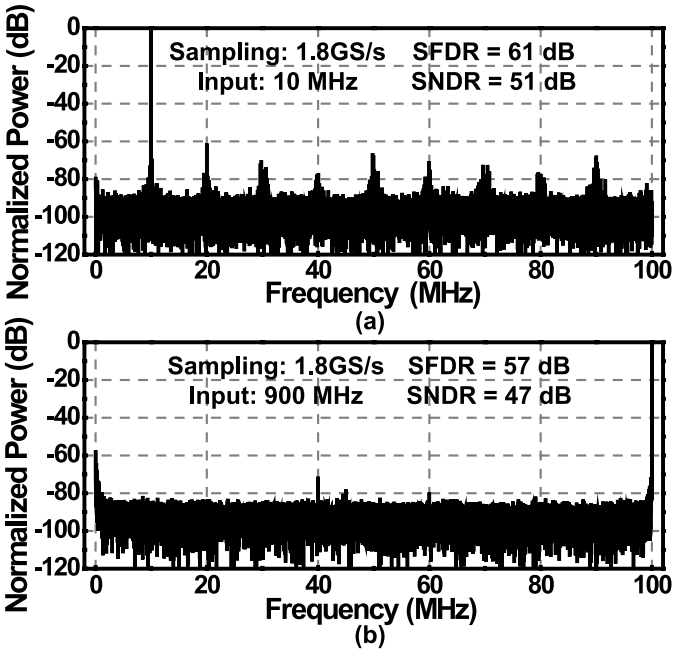

Fig. 15. ADC output spectrum at the sampling rate of 1.8 GS/s, (a) when input frequency is 10 MHz and (b) when input frequency is 900 MHz. (The output code is down sampled by a factor of 9).

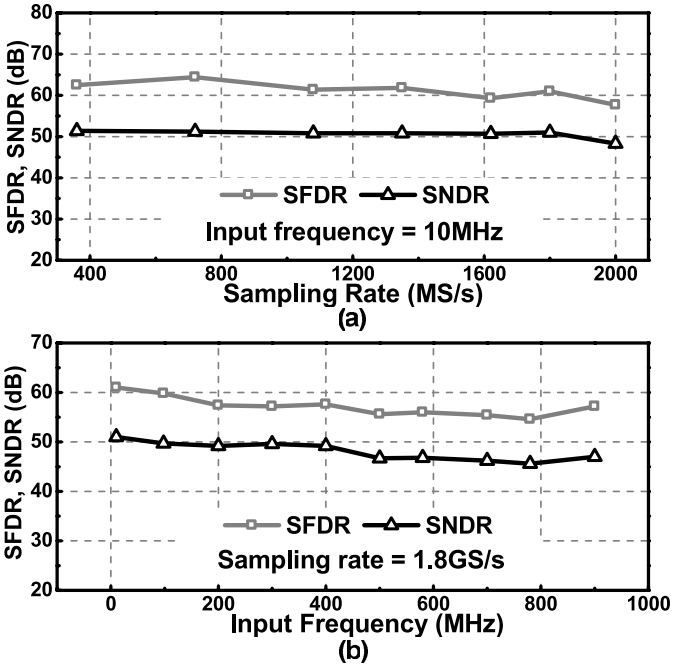

Fig. 16. Measured SFDR and SNDR, (a) when the sampling rate is swept and (b) when the input frequency is swept.

TABLE V
MEASURED PERFORMANCE OF FOUR CHIPS

	Chip 1	Chip 2	Chip 3	Chip 4
SFDR (dB)	60.6	61.0	62.0	59.0
SNDR (dB)	49.4	51.0	50.0	51.0

input frequency is 10 MHz, it gives an SFDR of 61.0 dB and an SNDR of 51.0 dB, results in an ENOB of 8.2 bits. The spurs at 90 MHz which equals to half of the sampling frequency minus the input frequency are caused by the gain mismatch between two channels. Although the residue amplifier is shared during double sampling, unbalanced layout of power supply and reference line between two channels lead to different settling time and gain in CDACs. Other spurs are mainly caused by gain error in pipelined stages. Simulation result shows similar spurs when there is some stage-gain error. When input frequency is 900 MHz, it gives an SFDR of 57.2 dB and an SNDR of 47.0 dB, results in an ENOB of 7.5 bits. Fig. 16(a) and (b) plot the SFDR and SNDR as functions of the input frequency and the sampling rate, respectively. When the input frequency maintains 10 MHz, the sampling rate is swept from 350 MS/s to

2GS/s. As the black line shown in Fig. 16(a), the SNDR maintains 51 dB when the sampling rate is up to 1.8 GS/s. When the sampling rate maintains 1.8 GS/s, the input frequency is swept from 10 MHz to 900 MHz. As the black line shown in Fig. 16(b), it gives a SNDR of 47 dB when the input is at the Nyquist frequency. To show the insensitivity of the amplifier's linearity against process variation, four chips in total are measured at the sampling rate of 1.8 GS/s when the input frequency is 10 MHz, as listed in Table V. The

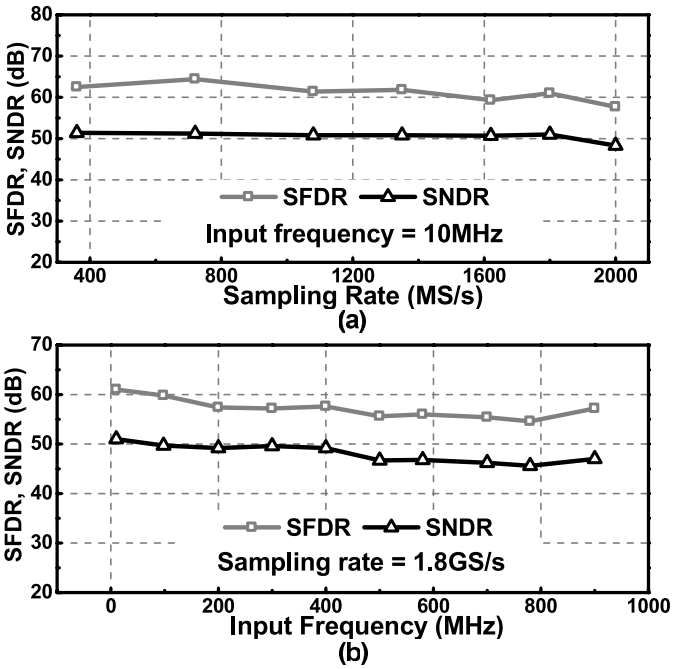

Fig. 17. Measured (a) SFDR and (b) SNDR under different supply voltages with temperature variations.

measurements are carried out under room temperature and 1.2 V power supply is used. The chips are from the same wafer. All measured chips show a similar performance, indicating that the linearity of the proposed open-loop amplifier is not sensitive to process variation. Furthermore, one chip is measured under different supply voltages with temperature variations, as shown in Fig. 17. (The temperature range of the measurement equipment is from 20 degrees to 95 degrees).

TABLE VI
ADC PERFORMANCE SUMMARY AND COMPARISON

	[21]	[22]	[23]	[24]	This Work
Architecture	Pipe, closed-loop	Pipe, open-loop	Pipe, closed-loop	Pipe, closed-loop	Pipe, open-loop
Technology	65 nm	65 nm	45 nm	45 nm	65 nm
f_s (GS/s)	0.8	1.0	1.3	2.0	1.8
Resolution (bit)	10	9	7	9	9
Power (mW)	19	7.1	22	45	44
SNDR (dB) Low Freq./ Nyquist	55 / 52	51 / 48	41 / 33	48 / 44	51 / 47
FoM (fJ/CS) @ Low Freq.	53	25	190	116	83
FoM (fJ/CS) @ Nyquist	71	34	460	167	134
Area (mm^2)	0.18	0.1	0.023	0.22	0.15
Nonlinearity calibration for amplifier	Off-chip	Off-chip	No	No	No

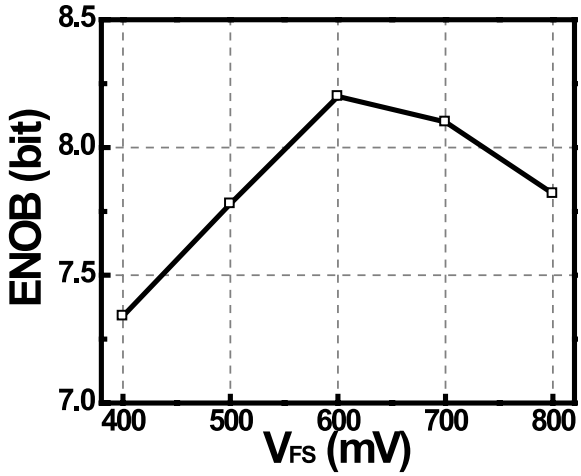

Fig. 18. Relationship between ENOB and V_{FS}.

Although the stage gain needs to be calibrated under different supply voltages and temperatures, the linearity of the proposed open-loop amplifier is not sensitive to the environment. The SNDR variation is mainly due to the speed changes of the circuits, instead of the amplifier's linearity. Fig. 18 shows the relationship between ENOB and V_{FS} at a sampling rate of 1.8 GS/s and an input frequency of 10 MHz. The result shows that the ENOB firstly is increasing to an optimal point along with the increase of V_{FS}. And then it starts to decrease. This is because the limitation of ENOB firstly lies in signal-to-noise ratio when V_{FS} is small. When V_{FS} increases to an optimal value, distortion starts to become the bottleneck and ENOB starts to decrease.

Table VI summarizes the performance of the prototype and other pipelined ADCs with similar sampling rates and resolutions. This work achieves a relatively high sampling rate and moderate resolution. Although, [21] and [22] report achieving quite low power consumption, their sampling rates are approximately half of that in this work and both of them use off-chip nonlinearity calibration for residue amplifier, which usually requires off-chip memories and a processor. For the ADCs without off-chip calibration, this work achieves the lowest FoM, both when the input frequency is low and at the Nyquist frequency.

V. CONCLUSION

In this paper, a 9-bit 1.8 GS/s 44 mW pipelined ADC using linearized open-loop amplifiers is introduced. A linearization technique is proposed to enhance the linearity of the open-loop residue amplifier. The open-loop amplifier is able to support 9-bit resolution after enhancement, where conventional works only achieve 6-bit resolution. With the high-linearity open-loop amplifier, Gigahertz sampling rate and moderate resolution are realized with a relatively low power consumption of 44 mW. CDAC gain calibration is proposed to obtain the accurate stage gain, so that the linearity of the open-loop amplifier will not be affected. Top-plate sampling timing for double sampling is also proposed to further enhance the power efficiency of the residue amplifier. With these techniques, this ADC achieves the lowest FoM of the pipelined ADCs who do not need off-chip nonlinearity calibration for the residue amplifiers. The proposed linearization technique relaxes the nonlinearity issue of the open-loop amplifier while maintaining its advantages, proved that it is an efficient technique under advanced CMOS technologies.

REFERENCES

[1] L. Sumanen, M. Waltari, and K. A. I. Halonen, "A 10-bit 200-MS/s CMOS parallel pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1048–1055, Jul. 2001.

[2] J. Arias *et al.*, "Low-power pipeline ADC for wireless LANs," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1338–1340, Aug. 2004.

[3] C.-J. Tseng, H.-W. Chen, W.-T. Shen, W.-C. Cheng, and H.-S. Chen, "A 10-b 320-MS/s stage-gain-error self-calibration pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1334–1343, Jun. 2012.
[4] Y. Chiu, P. R. Gray, and B. Nikolic, "A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2139–2151, Dec. 2004.
[5] Y.-J. Kim *et al.*, "A 9.43-ENOB 160MS/s 1.2V 65nm CMOS ADC based on multi-stage amplifiers," in *Proc. Custom Integr. Circuits Conf.*, Sep. 2009, pp. 271–274.
[6] J. Wu *et al.*, "A 240-mW 2.1 GS/s 52-dB SNDR pipeline ADC using MDAC equalization," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1818–1828, Aug. 2013.
[7] C.-J. Tseng, C.-F. Lai, and H.-S. Chen, "A 6-bit 1 GS/s pipeline ADC using incomplete settling with background sampling-point calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2805–2815, Oct. 2014.
[8] T. Yamase, H. Uchida, and H. Noguchi, "A 22-mW 7b 1.3 GS/s pipeline ADC with 1-bit/stage folding converter architecture," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2011, pp. 124–125.
[9] K. Kusumoto *et al.*, "A 10 b 20 MHz 30 mW pipelined interpolating CMOS ADC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, vol. 36. Feb. 1993, pp. 62–63.
[10] M. Miyahara, H. Lee, D. Paik, and A. Matsuzawa, "A 10b 320 MS/s 40 mW open-loop interpolated pipeline ADC," in *Dig. Symp. VLSI Circuits*, Jun. 2011, pp. 126–127.
[11] J. Lin, D. Paik, S. Lee, M. Miyahara, and A. Matsuzawa, "An ultra-low-voltage 160 MS/s 7 bit interpolated pipeline ADC using dynamic amplifiers," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1399–1411, Jun. 2015.
[12] D.-L. Shen and T.-C. Lee, "A 6-bit 800-MS/s pipelined A/D converter with open-loop amplifiers," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 258–268, Feb. 2007.
[13] F.-C. Hsieh and T.-C. Lee, "A 6-bit pipelined analog-to-digital converter with current-switching open-loop residue amplification," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2008, pp. 61–64.
[14] B. D. Sahoo and B. Razavi, "A 10-Bit 1-GHz 33-mW CMOS ADC," in *Dig. Symp. VLSI Circuits*, pp. 30–31, Jun. 2012.
[15] A. Verma and B. Razavi, "A 10-bit 500-MS/s 55-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3039–3050, Nov. 2009.
[16] J. A. McNeill, S. Goluguri, and A. Nair, "'Split-ADC,' digital background correction of open-loop residue amplifier nonlinearity errors in a 14b pipeline ADC," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2007, pp. 1237–1240.
[17] J. Yuan, N. H. Farhat, and J. Van der Spiegel, "Background calibration with piecewise linearized error model for CMOS pipeline A/D converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 1, pp. 311–321, Feb. 2008.
[18] B. Murmann and B. E. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.
[19] T.-Y. Lo, C.-S. Kao, and C.-C. Hung, "A Gm-C continuous-time analog filter for IEEE 802.11 a/b/g/n wireless LANs," in *Proc. IEEE Int. Symp. Signals, Circuits Syst.*, vol. 1. Jul. 2007, pp. 1–4.
[20] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2008, pp. 269–272.
[21] S.-H. W. Chiang, H. Sun, and B. Razavi, "A 10-bit 800-MHz 19-mW CMOS ADC," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2013, pp. C100–C101.
[22] S. Hashemi and B. Razavi, "A 7.1 mW 1 GS/s ADC with 48 dB SNDR at Nyquist rate," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1739–1750, Aug. 2014.
[23] T. Yamase, H. Uchida, and H. Noguchi, "A 22-mW 7b 1.3 GS/s pipeline ADC with 1-bit/stage folding converter architecture," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2011, pp. 124–125.
[24] J. Pernillo and M. P. Flynn, "A 9b 2GS/s 45mW 2X-interleaved ADC," in *Proc. IEEE ESSCIRC*, Sep. 2013, pp. 125–128.

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