A 3.6 GHz Low-Noise Fractional-N Digital PLL Using SAR-ADC-Based TDC

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***Abstract*— This paper presents a fractional-N digital phase-locked loop (PLL) that achieves low in-band phase noise. Phase detection is carried out by a proposed 10-bit, 0.8 ps resolution time-to-digital converter (TDC) using a charge pump and a successive-approximation-register analog-to-digital converter (SAR-ADC) with low power and small area. The latency of the TDC is addressed by the designed building blocks. The fractional spurs are reduced by dual-loop least-mean-square (LMS) calibration. A $\Delta\Sigma$-less and MOS varactor-less LC digitally-controlled oscillator (DCO) is proposed whose frequency resolution is enhanced to 7 kHz (or a unit variable capacitance of 2.6 aF) using a bridging capacitor technique. A prototype chip is fabricated using a 65 nm CMOS process, occupying an active area of 0.38 mm^2 and consuming a power of 9.7 mW at a reference frequency of 50 MHz. The measured in-band phase noise is 107.8 dBc/Hz to 110.0 dBc/Hz with a loop bandwidth of 1 to 5 MHz.**

***Index Terms*— digital phase-locked-loop (PLL), frequency synthesizer, time-to-digital converter (TDC), successive-approximation-register analog-to-digital converter (SAR-ADC), sub-picosecond resolution; digitally controlled oscillator (DCO), least-mean-square (LMS), CMOS.**

I. Introduction

THE last decade has witnessed the transition from analog phase-locked loops (PLLs) to digital PLLs, which are imperative building blocks in wireless/wireline transceivers and systems-on-chip (SoCs). Compared with their analog counterparts, digital PLLs have advantages such as a small and configurable loop filter, gear-shifted fast settling, and portability to other process technologies.

Fractional-N PLLs provide higher frequency resolution, which facilitates frequency planning with a single reference input clock. A conventional analog charge-pump fractional-N PLL is realized using a delta-sigma ($\Delta\Sigma$) modulator that dithers a divider to generate a fractionally divided frequency. By doing so, the $\Delta\Sigma$ modulator contributes the out-band phase noise of the PLL [1] and also modulates charge pump's mismatches, increasing in-band phase noise and incurring fractional spurs [2]. Although $\Delta\Sigma$-noise cancellation assisted by a digital-to-analog converter (DAC) has been proposed[2]–[9], the gain mismatch between the DAC and the charge pump undermines the cancellation. While a narrow loop bandwidth (BW) can be set to lower overall root-mean-square (RMS) noise, doing so leads to a higher power budget for a low-noise oscillator, slows down the loop settling, reduces noise suppression from the power supply to the oscillator, and results in a large area of the analog loop filter, thus increasing the die cost. A digital PLL, on the other hand, offers a more straightforward fractional-N operation [10]–[26]. The divider-based architecture cancels $\Delta\Sigma$-noise in digital domain, while the counter-based architecture enables phase-domain operation without using a $\Delta\Sigma$-modulator. Both avoid the mismatch issue between the DAC and the charge pump in analog PLLs. Thus, digital PLLs also enable wider loop BW to suppress the noise from the oscillator. In addition, the loop BW in a digital PLL can be set more flexibly by changing the coefficients in the digital loop filter. Furthermore, digital circuits of filtering and cancellation scale down with more advanced technologies, enabling even smaller area and lower power consumption in the future.

Despite these advantages, unlike analog phase detectors, digital phase detectors realized with time-to-digital converters (TDCs) suffer from quantization noise that contributes in-band phase noise. Hence, in previous studies, efforts have been made to enhance the resolution of TDCs with the proposals of Vernier [27], [28], noise shaping [29], and time amplification [30], for example. In these TDCs, since delay chains are generally still used as core quantizers, complex and delicate timing control is typically needed in order to enhance the resolution. This timing control can be vulnerable due to the inability to store time, leakage, and power supply variation. Moreover, achieving high dynamic range (DR) is challenging due to intrinsic jitter and nonlinearity, which is generally traded off with signal bandwidth, power consumption, and area occupation. While an alternative solution for high DR involves the use of a high-resolution short-range TDC with a digital-to-time converter (DTC) for phase shifting [25], [31], [32], a DTC may cause the timing increment in each reference cycle to be different from the nominated one, resulting in the deviation of the synthesized frequency. Consequently, more calibration is needed among the TDC, the DTC, and the $\Delta\Sigma$ modulator (or the reference phase generator).

In this paper, we present a 3.6 GHz low-noise fractional-N digital PLL [33] with a 0.8 ps resolution and 10-bit TDC featuring less complexity, low power, and small area [34] [35]. An equation manifesting the trade-off between quantization noise and thermal noise is derived, offering the insight into this type of TDCs for PLLs. To accommodate the TDC

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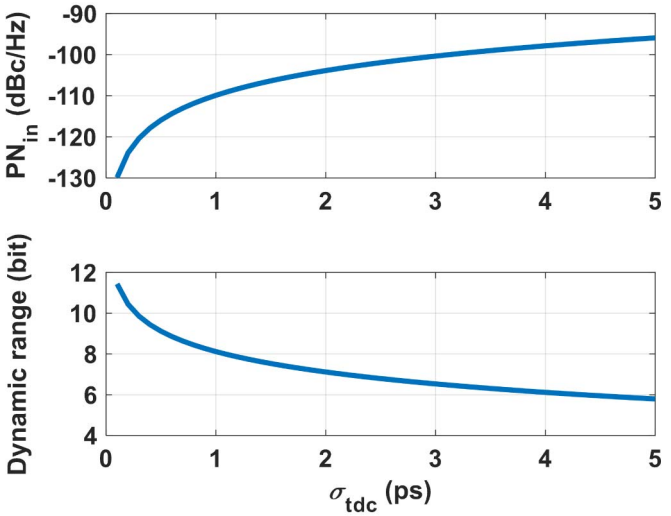

Fig. 1. Effective resolution and calculated in-band phase noise and dynamic range of the TDC. The reference and output frequencies are 50 MHz and 3.6 GHz, respectively.

to the PLL, building blocks addressing the latency and the gain mismatch are designed. The capacitor banks of the LC digitally-controlled-oscillator (DCO) is implemented with only MOM capacitors, where a bridging capacitor technique is proposed to enhance the frequency resolution [36]. Section II describes the principle and characteristics of the proposed TDC. Section III discusses architecture-level considerations on accommodating the TDC into the digital PLL. Section IV describes circuit design of building blocks. Section V shows and discusses the measurement results, and Section VI draws the conclusion.

II. Proposed TDC

The in-band phase noise contributed by a TDC is calculated with

$$PN_{in} = \frac{(2\pi\sigma_{tdc}f_v)^2}{f_{ref}}, \tag{1}$$

based on the calculation in a previous study [37], where f_{ref} and f_{v} are the reference and output frequencies, respectively, and σ_{tdc} is the effective resolution of the TDC, defined as

$$\sigma = \sqrt{\frac{t_{res}^2}{12} + \sigma_{tin}^2}, \tag{2}$$

where t_{res} is the nominal time resolution, and σ_{tin} is the lumped input-referred jitter due to intrinsic noise. The DR of a TDC in this context is defined as $\log_2(T_{\text{range}}/\sigma_{\text{tdc}})$, where T_{range} is the nominal conversion range. Fig. 1 shows the in-band phase noise and required DR versus σ_{tdc} for the case of a reference frequency of 50 MHz and an output frequency of 3.6 GHz, and T_{range} is equal to one period of the oscillator's output. It can be seen from the figure that, for an in-band phase noise of 110 dBc/Hz, an effective resolution of less than 1 ps and a DR of more than 8 bits are required.

Since a high-resolution core quantizer is crucial to the overall performance, instead of using a delay chain, we address time quantization in voltage domain where several advantages are provided, compared with a delay chain. First, a voltage-domain time quantizer generates less quantization noise.

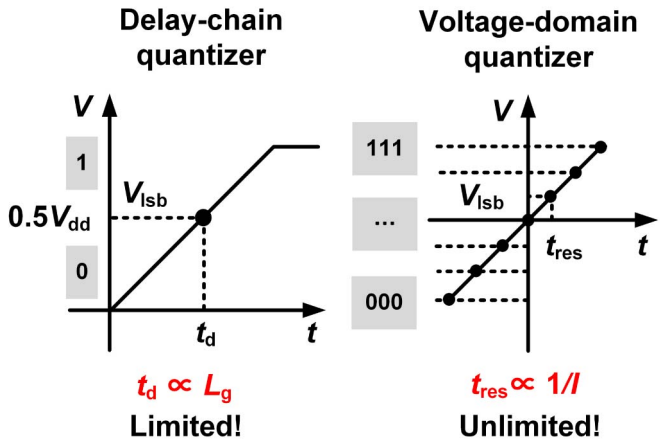

Fig. 2. Concept of a time quantizer realized by a delay cell and voltage-domain digitization.

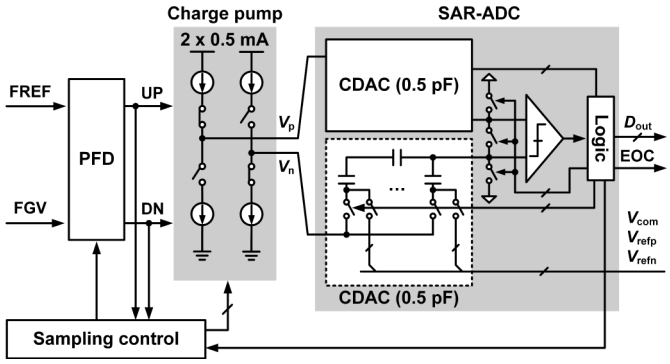

Fig. 3. Block diagram of the proposed TDC.

As shown in Fig. 2, the time resolution of a delay chain is the output rise time of one delay cell, t_{d}, which is proportional to the transistor's channel length, L_{g}. Since minimum L_{g} is limited by the process technology, the resolution in a delay chain is also limited. On the other hand, in a voltage-domain time quantizer, finer resolution is always possible by using more current due to $t_{\text{res}} = CV_{\text{lsb}}/I$. Here, t_{res} and V_{lsb} represent the time resolution and the minimum resolvable voltage of an analog-to-digital converter (ADC), respectively. Fig. 3 shows our proposed TDC [34], where EOC indicates the end of one conversion. The PFD and the charge pump translate time difference to voltage on the capacitive DAC (CDAC) of the SAR-ADC. Bottom-plate sampling is employed to reduce the charge injection in the switches of charge pump and SAR-ADC.

The second advantage of the proposed TDC over a delay chain is the less jitter generation. The jitter of an inverter is calculated with [38]

$$\sigma_{tall}^2 = \frac{4kT\gamma}{V_{dd} - V_t}\frac{t_d}{I_N} + \frac{kT}{V_{dd}/2}\frac{t_d}{I_N}, \tag{3}$$

where I_{N} is inverter's nominal charging current. Similarly, the input-referred jitter of the proposed TDC can be calculated as

$$\sigma_{tin\_cp}^2 = \frac{4kT\gamma}{V_{gs} - V_t}\frac{t_{res}}{I_{cp}} + \frac{kT}{V_{lsb}}\frac{t_{res}}{I_{cp}}, \tag{4}$$

where V_{gs} is the gate bias voltage of a current source, and I_{cp} is charge pump's current. For fair comparison, we assume $t_d = t_{res}$. Since I_{cp} is determined for sufficient dynamic range, it is significantly greater than I_N. Although V_{lsb} is far less than V_{dd}, the second terms of (3) and (4) are comparable but the first term in (4) is much smaller. Therefore, the proposed TDC contributes less jitter than a delay chain does.

Third, the proposed TDC has better power efficiency for the same level of jitter. To hold the same level of jitter, I_N should be set closed to I_{cp}. Note that I_N is the current of only one inverter. For n-bit range, the total power consumption can be 2^n times higher than I_{cp}. Additionally, the AD conversion involves only one CDAC, one dynamic comparator, and a small amount of logic circuits. For this reason, a SAR-ADC is believed to consume the lowest power and occupies the smallest area among other types of ADCs.

The detail analysis of σ_{tin} in (2) was done in a previous study [35]. The derived maximum (full-range) input-referred jitter is calculated as follows:

$$\sigma_{tin}^2 = \left[\frac{4kT\gamma}{C}\frac{g_m}{I}\frac{1}{V_{ref}}\left(1+\frac{4T_d}{T_{range}}\right)+\frac{4kT}{C}\frac{2}{V_{ref}^2}\right]\cdot T_{range}^2, \tag{5}$$

where g_m/I is a constant for transistor sizing, V_{ref} is the reference voltage of the ADC, T_d is the feedback delay in the PFD to avoid dead zone, T_{range} is the conversion range of the TDC, and n is the resolution of the ADC. To analyze the effect of quantization noise, t_{res} should be bounded by

$$t_{res} = \frac{T_{range}}{2^n}. \tag{6}$$

Substituting (5) and (6) to (2), (2) is rewritten as

$$\sigma = T_{range} \cdot \sqrt{\frac{1}{2^n}\frac{1}{12}+\frac{4kT\gamma}{C}\frac{g_m}{I}\frac{1}{V_{ref}}\left(1+\frac{4T_d}{T_{range}}\right)+\frac{4kT}{C}\frac{2}{V_{ref}^2}}. \tag{7}$$

Fig. 4 shows the plot of (7) in the case that $T_{range} = 3/f_v$ (due to implementation consideration), $g_m/I_d = 8$, $V_{ref} = 0.8$, and $T_d = 120$ ps. This figure quantitatively shows how to determine the specification of the charge pump and the SAR-ADC to satisfy with the PLL's required phase noise. It can be also seen from the figure that 1) a higher-resolution ADC reduces quantization noise, and 2) larger sampling capacitance suppresses thermal noise but requires proportionally larger current to maintain the same conversion range.

According to Fig. 4, with a charging current of 0.5 mA, a CDAC of 0.5 pF, and a 10-bit SAR-ADC, the proposed TDC was measured with a resolution of 0.8 ps and an LSB single-shot precision of less than 1. The latency of the SAR-ADC is approximately 12 ns, enabling a conversion rate of up to 83 MS/s, which is sufficient in the present study because the reference frequency is 50 MHz. At this frequency, with a 1 V power supply, the power consumption of the TDC is less than 3 mW. The active area of the TDC in the 65 nm CMOS technology is only 0.018 mm^2.

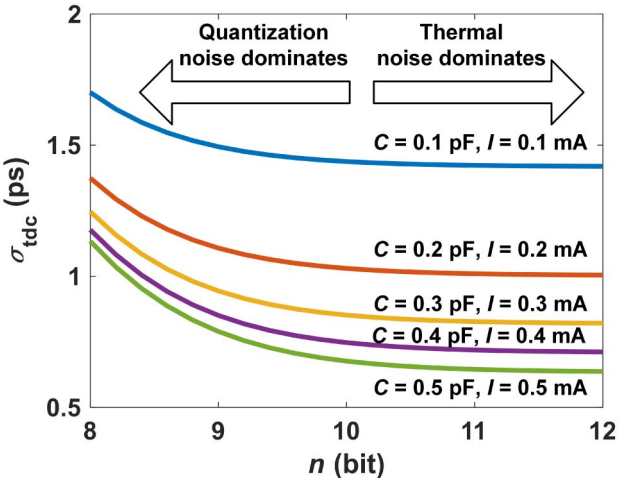

Fig. 4. Relationship among effective resolution (σ_{tdc}), ADC resolution (n), CDAC capacitance (C), and charge pump current (I).

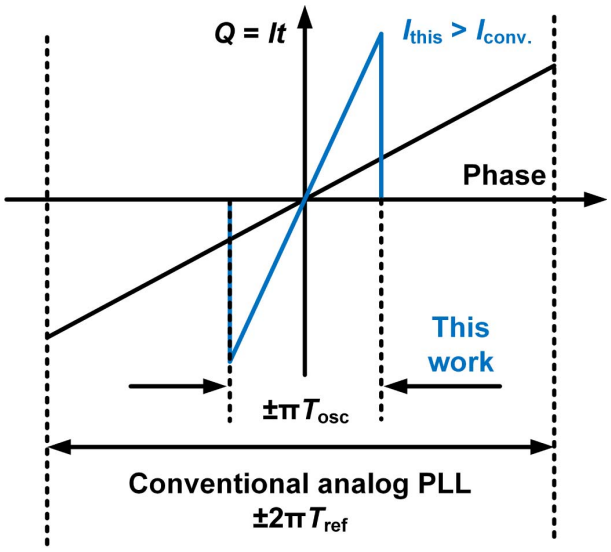

Fig. 5. Detection range requirements of the charge pump in this work and those in conventional analog PLLs.

Although a charge pump and capacitors are used in the proposed PLL, the proposed PLL differs from conventional analog PLLs in the following aspects. First, the CDAC does not serve as a loop filter and is only used for sampling and conversion, whereas the converted time difference is filtered by the following digital filter. A conventional analog PLL typically contains around a 100 pF capacitor, whereas the CDAC considered herein contains a 0.5 pF capacitor. Second, the required detection ranges of the charge pumps are different, as shown in Fig. 5. In an analog PLL, the charge pump must cover an input range of $\pm T_{ref}$, where T_{ref} is the period of the reference clock. Such a long detection range requires a small-current charge pump in order to avoid output saturation. However, a small charge pump current causes less suppression of its own noise contribution. On the other hand, the charge pump in the proposed PLL is only required to cover around one period of the oscillator's output. Consequently, a larger current can be used for higher TDC resolution and lower in-band phase noise.

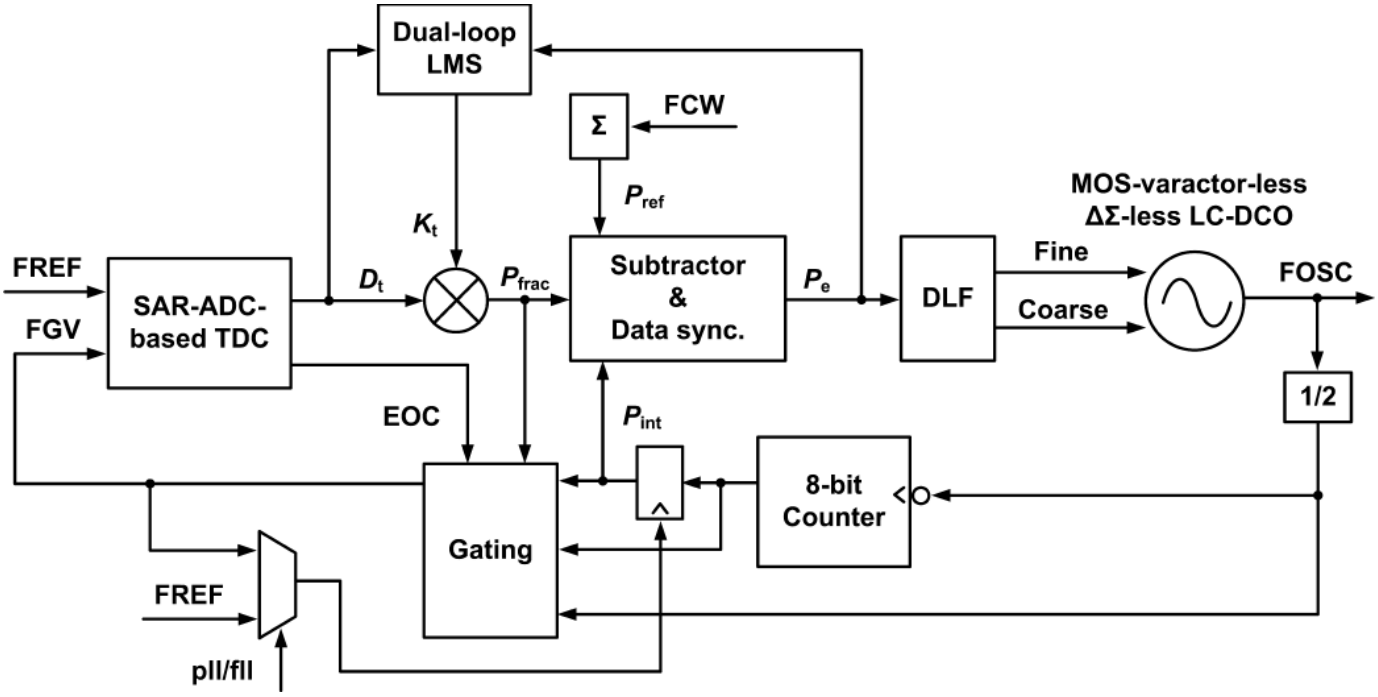

Fig. 6. Architecture of the proposed digital PLL.

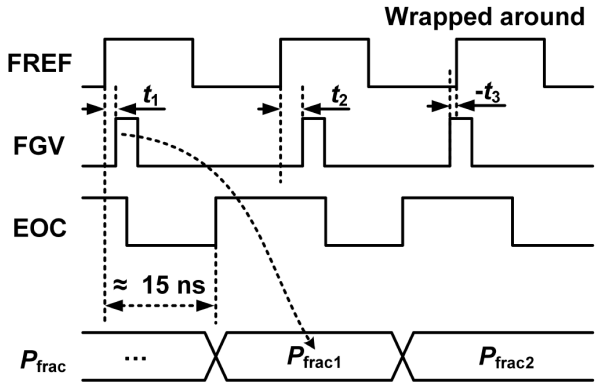

Fig. 7. Main timing diagram of the fractional phase quantization.

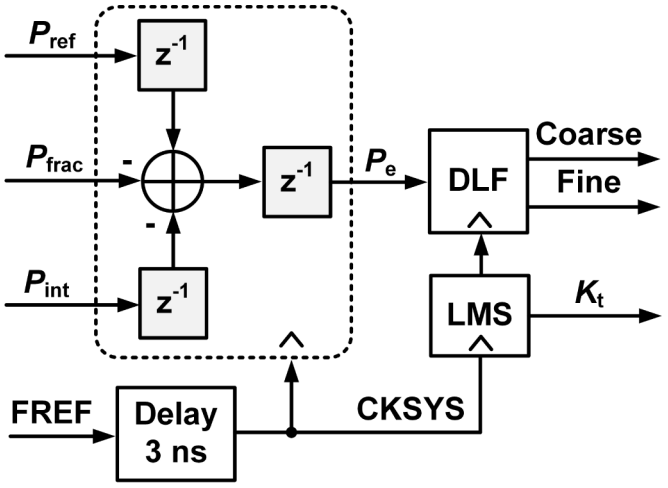

Fig. 8. Block diagram of clocking and data synchronization.

Note that PLLs using ADCs for phase detectors have been studied recently. In [21], [39], ADCs were placed in noise-shaping topologies, where the available loop BWs are limited. In two other studies [40], [41], ADCs were used in digital sub-sampling PLLs, in which the realization of fractional-N operation is challenging due to a limited linear detection range.

III. Architecture

Generally, there are two main types of architectures of TDC-based digital PLLs: the ones with dividers and the ones with counters. When loop are locked, the behaviors of the two are equivalent if a first-order $\Delta\Sigma$ modulator is used in the divider-based architecture. A problem in divider-based architecture for a digital PLL may occur during phase acquisition. Since the TDC's range generally cannot cover one period of the reference input, in fractional-N mode, the TDC can experience a failure of acquisition. In order to avoid this situation, a counter would still be needed for frequency locking in order to pull the phase of the divider's output closer to that of the reference input. Thus, a counter-based architecture is chosen, as shown in Fig. 6, where FREF, FOSC, and FGV are the reference input, the output of the PLL, and periodically gated pulses of the output of the DCO, respectively. When the counter's output is latched using the reference clock, the loop operates in the frequency-locked-loop (FLL) mode. The loop enters the PLL mode when the counter's output is latched by the gating block's output. A phase-domain operation is carried out by never resetting the counter or the accumulator of the frequency-control word (FCW). For practical reasons, the output of the DCO is divided by two for the counter.

The gating block assists fractional-N operation and addresses the issue of fractional phase latency. This latency is illustrated in Fig. 7, where the fractional phase, P_{frac}, is updated approximately 15 ns after its sampling time, due to the latencies of the SAR-ADC and the following multiplier. Thus, the TDC cannot directly receive the high-frequency output

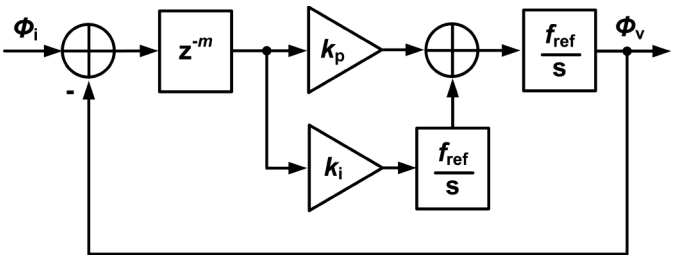

Fig. 9. Loop model with lumped m cycles of delay. K_{dco} is normalized in this model.

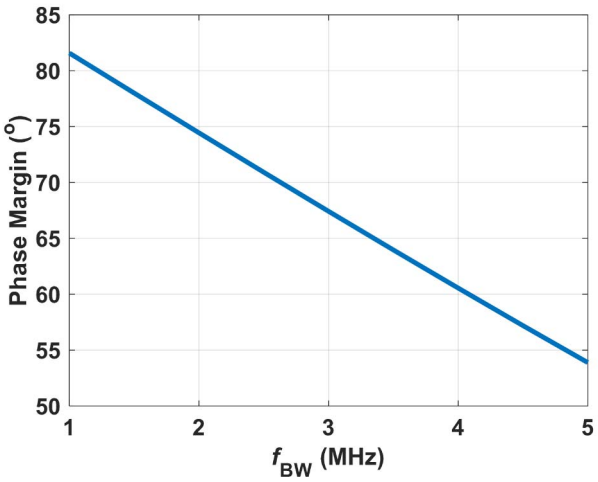

Fig. 10. Phase margin vs. loop BW in the case of 2 cycles of delay.

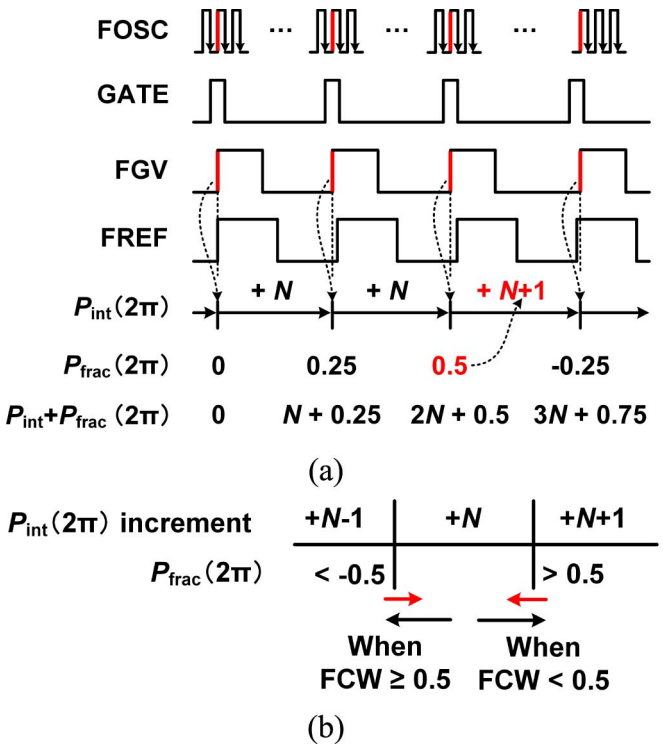

Fig. 11. (a) Timing diagram when the loop is locked when FCW = 0.25. (b) Fractional phase kept within approximately 0.5 periods of the DCO.

of the DCO, which also consumes an unreasonable amount of power. Moreover, the fractional relationship between the reference and output frequencies leads to endless increasing of the phase difference which exceeds TDC's conversion

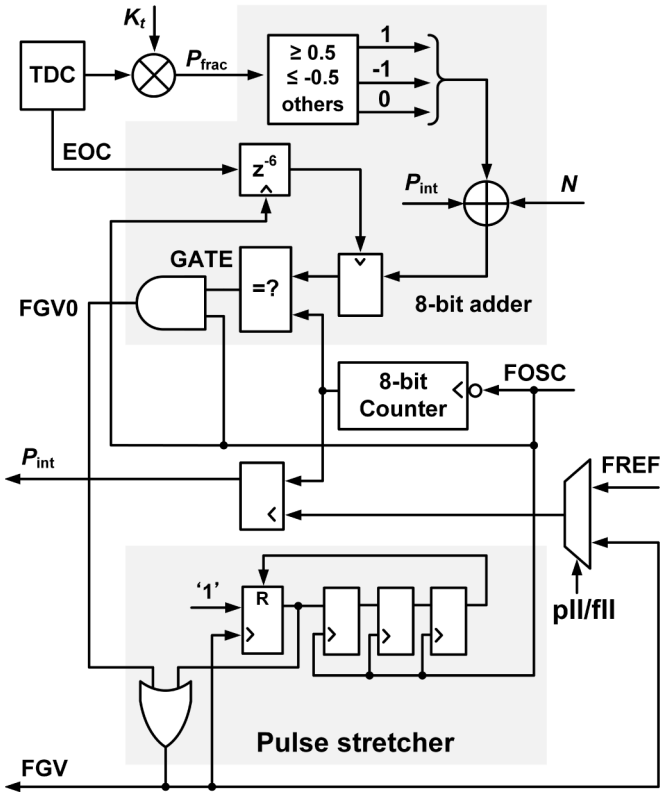

Fig. 12. Block diagram of the gating block (shaded area).

range. Thus, the input of the TDC should be kept within a reasonable range. Conventionally, a divider modulated by a $\Delta\Sigma$-modulator wraps around the input phase to the TDC. In a counter-based architecture, windowing circuits were proposed to constrain the input range of the TDCs [16] [42]. In this work, the gating block keeps the input to the TDC being within approximately 0.5 periods of the DCO. It functions as part of a synchronous divider, extracting one pulse of the output of the DCO in every reference cycle according to the quantized integer (P_{int}) and fractional phases. Also, the extracted pulse is stretched inside the gating block in order to avoid driving problems.

The gain stage after the TDC normalizes the quantized time to the period of the DCO. In a conventional counter-based digital PLL, the period of the DCO is measured by a delay-chain TDC. Since it is not practical to perform this operation using the proposed TDC, in this work, an LMS method is carried out, as shown in Fig. 6. The block generates two multiplexed gains addressing the issue of the gain mismatch between the positive and negative outputs of the charge pump in the TDC. The coarse and fine loop filters tune the corresponding banks of the DCO. The filters are both 9-bit, type-II filters with proportional and integral paths. The coarse filter is used for both FLL and coarse PLL modes and is configured as a type-II filter in order to minimize the phase offset after coarse tuning.

IV. Design of Other Building Blocks

A. Data Synchronization and Clocking

Although the TDC can complete digitization before the next rising edge of FREF, the resulting P_{frac} is asynchronous with

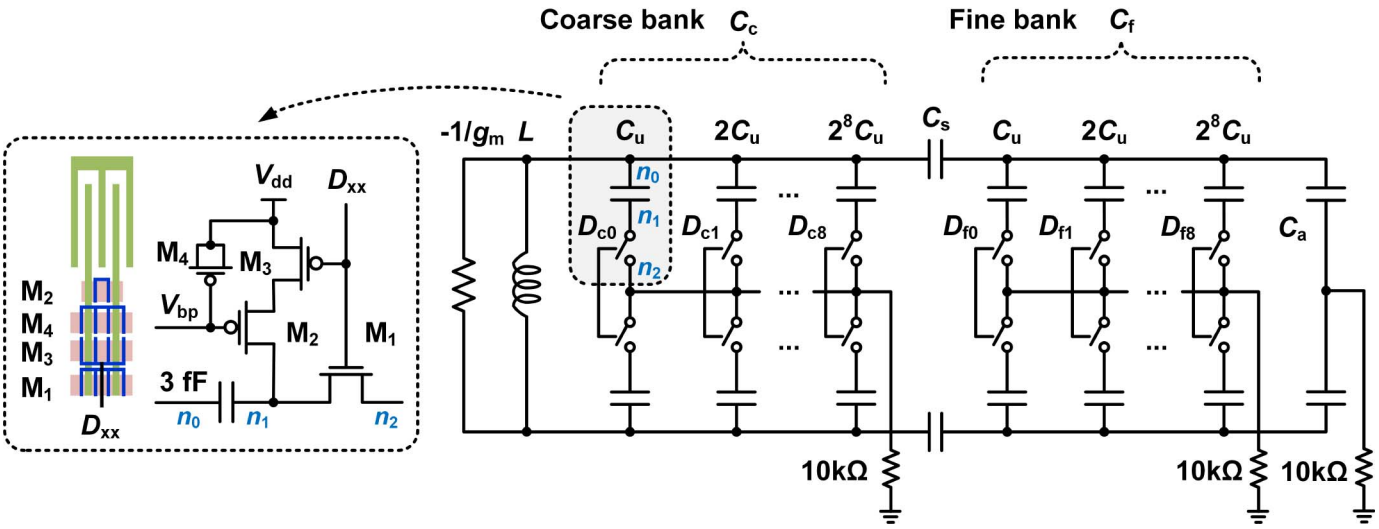

Fig. 13. Equivalent model of the proposed LC-DCO and the topology of the capacitor-switch unit.

respect to P_{int}, as shown in Fig. 7. The conversion latency causes P_{frac} to be read in the next cycle of FREF. Thus, P_{int} and the reference phase, P_{ref}, are delayed by one cycle for data synchronization, as shown in Fig. 8. The clock for digital processing blocks is generated by delaying FREF for approximately 3 ns in order to avoid triggering the digital block simultaneously when the TDC is sampling the input.

The stability with inserted cycle delay is analyzed as follows. The loop model with a lumped cycle delay is shown in Fig. 9, where k_{p} and k_{i} are the coefficients of the proportional and integral paths of the loop filter, respectively, and m is the number of cycle delay. Using bilinear transform, $z = (2f_{\text{ref}} + s)/(2f_{\text{ref}} - s)$, the open-loop transfer function is derived as

$$H_{ol}(s) = \left(\frac{2f_{ref} - S}{2f_{ref} + S}\right)^{m} \cdot \frac{k_p(k_i f_{ref}/k_p + s)}{s} \cdot \frac{f_{ref}}{s}. \quad (8)$$

The delay introduces zeroes and poles that can undermine phase marge. The phase margin is thus calculated with

$$PM = \tan^{-1}\left(\frac{2\pi f_{BW}}{f_{ref}} \cdot \frac{k_p}{k_i}\right) - 2m \cdot \tan^{-1}\left(\frac{\pi f_{BW}}{f_{ref}}\right), \quad (9)$$

where f_{bw} is the unity gain frequency of $H_{\text{ol}}(\text{s})$ or BW in this context. Fig. 10 plots the calculated phase margin when $f_{\text{ref}} = 50$ MHz, k_{p} and k_{i} are set so that the damping factor (which is defined assuming no delay in the loop) is 2, and $m = 2$. The implantation of this work contains 2 cycles of delay, one from Fig. 7 and the other one from the filter's output. It can be seen from the figure that the phase marge becomes less than 45 when f_{bw} is wider than 3 MHz.

B. Gating Block

The behavior of the gating block and the phase relationship (when the loop is locked) is shown in Fig. 11(a). The falling edges of the output of the DCO, i.e., FOSC, are counted. Once the count reaches a target value, a window pulse, GATE, is generated to gate out the following rising edge of FOSC, as FGV, whose pulse width is then stretched to avoid driving problems. In this illustration, the fractional part of FCW is 0.25, and the increment of P_{frac} is positive. Phase wrapping takes place when P_{frac} reaches 0.5, by adding N+1 to the target value. In the case when FCW is greater than 0.5, the increment of P_{frac} becomes negative because of the implementation of the reference generator. Thus, when P_{frac} reaches 0.5, the phase is wrapped around by adding $\text{N} - 1$ to the target value. The operation of the phase wrapping is illustrated in Fig. 11(b). Since the TDC accepts both positive and negative phases, the proposed operation requires no de-glitching [14]. The operation also requires no clock retime, avoiding the risk of metastability [10].

Fig. 12 shows a block diagram of the gating block (shaded region). The counter increments and wraps around, quantizing the integer phase. The instantaneous output is latched out by FREF in the FLL mode, or by FGV in the PLL mode. The target value is generated by adding P_{int} to N, $N+1$, or $N-1$, depending on P_{frac}, where N is the integer part of the FCW. The adder is designed to have the same bit width as that of the counter. Thus, the adder wraps around one-cycle earlier than the counter, correctly setting the target value. Due to the delay of combinational logics between D_{t} and the comparator, the output of the adder is resynchronized with FOSC, which samples and aligns the end-of-conversion signal, EOC, from the TDC, and the resulting aligned signal latches the output of the adder to the comparator.

C. MOS-Varactor-Less and $\Delta\Sigma$ -Less LC- DCO

An NMOS LC-DCO is designed, and its equivalent model is shown in Fig. 13. The 9-bit coarse bank is implemented using switched metal-oxide-metal (MOM) capacitors. With a 3 fF unit capacitor (C_{u}), the simulated unit variable capacitance ($\Delta\text{C}_{\text{coarse}}$) is approximately 1 fF. This translates to a frequency resolution of 1.2 MHz at an output frequency of 3.6 GHz. Conventionally, a fine bank is implemented using discrete MOS varactors. Although a discrete MOS varactor operates in only two regions, the capacitance in each varactor still varies with the override voltage [39], which may be sensitive to

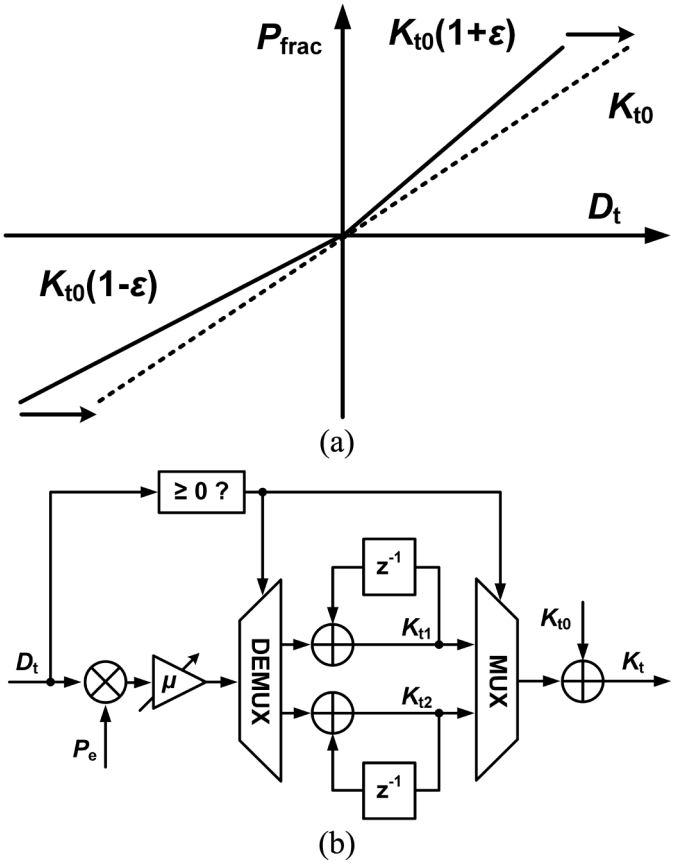

Fig. 14. (a) Gain mismatch between positive and negative inputs, and the purpose of gain calibration, and (b) dual-loop LMS-based TDC gain calibration resolving the issue in (a).

power supply noise. Moreover, since the capacitance is determined by the override voltage, when the output common-mode voltage of the DCO is lowered, e.g., in the case of a lower power supply, a MOS varactor can go to a high-capacitive-gain region, resulting in degradation of robustness. On the other hand, since switched MOM capacitors are less sensitive to power supply, they are also applied in the fine bank.

It is impractical to reduce the size of a 3 fF capacitor by hundreds of times for kHz-level frequency resolution. Although a conventional solution involves dithering using a $\Delta\Sigma$-modulator, the resulting out-band noise and possible folded noise due to element mismatch are a concern in the case of a wide loop bandwidth. Instead, in order to enhance the resolution, bridging capacitors are set between the coarse and fine banks, as shown in Fig. 13. Differentiating the total capacitance of the bridging capacitors and the fine bank, the unit variable capacitance in the fine bank is calculated as

$$\Delta C_{fine} = \left[\frac{C_s}{2C_f}\right] \cdot \Delta C_f, \tag{10}$$

assuming $C_a = C_f - C_s$, where C_a, C_f, and C_s are the lumped attenuating and parasitic capacitance, the total capacitance of the fine bank, and the bridging capacitance, respectively. In this work, the fine bank is a copy of the coarse bank, *i.e.*, $C_f = 512C_u$ and $\Delta C_f = \Delta C_{coarse}$. Therefore, with $C_s = 52C_u$, $\Delta C_{fine} \approx \Delta C_{coarse}/400 = 2.6$ aF can be realized. The average measured frequency resolution of the

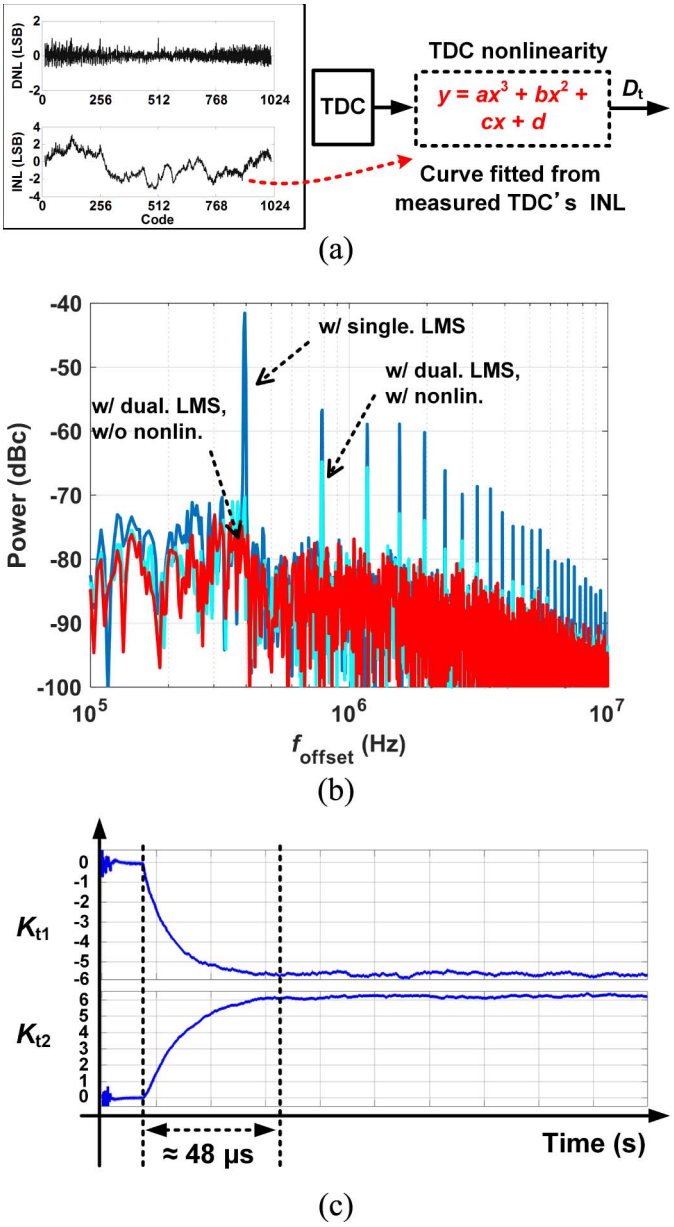

Fig. 15. (a) Modeling of TDC's nonlinearity using curve fitting from measured INL. (b) Behavioral simulation of in-band spur with single-loop LMS and dual-loop LMS calibration methods, and the effect of TDC's nonlinearity. (c) Settling time of normalizers in dual-loop LMS calibration.

DCO is 7 kHz, which theoretically translates to a phase noise of 131 dBc/Hz at 1 MHz offset and a reference spur of 81 dBc, according the equations in [37]. Note that the gains of the two banks need not be matched because, when the loop is locked, only the fine bank is switched. Fig. 13 also shows the topology of the single-ended capacitor-switch unit and its layout. A pull-up resistor is generally required in order to prevent the partial turn-off of switch M_1. At a carrier frequency of 3.6 GHz, a 3 fF unit capacitor requires a resistance of hundreds of kilo-ohms, which is area consuming if a poly resistor is implemented. Thus, a transistor in sub-threshold region, M_2, is used to provide high resistance. Switch M_3 cuts off the resistor path when M_1 is on, in order to prevent the dc current from flowing, and M_4 provides local decoupling. The higher bits of discrete

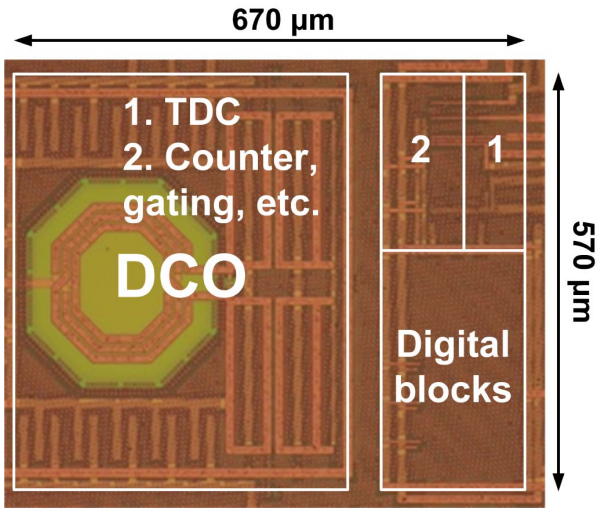

Fig. 16. Chip photo.

capacitors are made by duplicating the capacitor-switch units. The pitches of switches and capacitors are made uniform so that when combining units, gaps between neighboring units are eliminated. In this way, the area is significantly reduced. The area of two banks that differentially contain 5 pF capacitors is only 0.07 mm^2.

D. Dual-Loop LMS-Based TDC Gain Calibration

The phase of the output of the TDC is converted by multiplying D_t by K_t. An LMS-based calibration method is used to adaptively calibrate K_t so that the power of the phase error, P_e, is minimum in the sense of the RMS. In this way, fractional spurs are suppressed. In the proposed TDC, however, the gains (resolutions) are different for positive and negative inputs due to mismatches in the charge pump and CDAC, as shown in Fig. 14(a). Therefore, a dual-loop LMS calibration method is applied, as shown in Fig. 14(b), where two normalizers, K_{t1} and K_{t2}, are generated and multiplexed according to the sign of D_t, and μ is the attenuation factor tuning LMS loop's settling time. Compared with single-loop LMS calibration, only one more digital integrator is needed; thus, the resulting power and area consumptions are negligible.

To simulate the fractional spur, the nonlinearity of the TDC should also be considered. As shown in Fig. 15(a), we model TDC's nonlinearity using curve fitting from the measured integral nonlinearity (INL). Fig. 15(b) shows the spectrum of behaviorally simulation (with Simulink®) of single-loop and dual-loop LMS calibration methods, and the effect of TDC's nonlinearity. The gain variation, ε in Fig. 14(a) is set as 1%. Fig. 15(b) suggests that the dual-loop LMS effectively calibrate the gain mismatch, compared with the single-loop one. Unfortunately, the nonlinearity of the TDC contributes the fractional spur to be around 65 dBc. Improving the TDC's linearity or removing such spur is our next research target.

Fig. 15 (c) shows the behaviorally simulated settling time of two normalizers. The settling time in this simulation is approximately 48 μs when μ equals 0.0625.

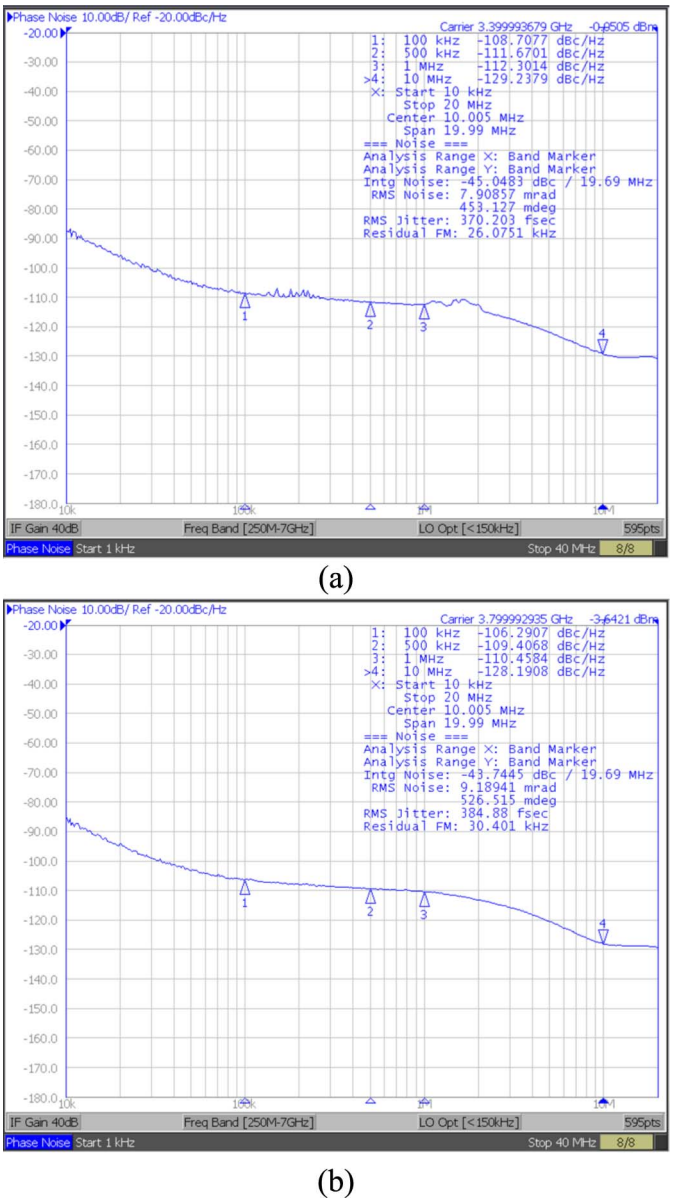

Fig. 17. Measured phase noise in integer-N mode at (a) 3.4 GHz (FCW = 34) and (b) 3.8 GHz (FCW = 38).

V. Experimental Results

The prototype chip was fabricated using a 65 nm CMOS process with an active area of 0.38 mm^2, as shown in Fig. 16. The chip is bonded in an 80-pin package, with a bond wire length of approximately 2 mm. For a 1.0 V power supply, a reference frequency of 50 MHz, and an output frequency of 3.625 GHz, the power consumption is 9.7 mW, where the digital power supply consumes 4.5 mW, including the digital block, the counter, the gating block, and the digital logics in the TDC.

The measured in-band phase noise is well consistent with the previously analyzed and measured TDC's performance. Fig. 17 shows the measured phase noise in integer-N mode at 3.4 GHz and 3.8 GHz, for which the in-band phase noise at 500 kHz is 111.7 dBc/Hz and 109.4 dBc/Hz, respectively.

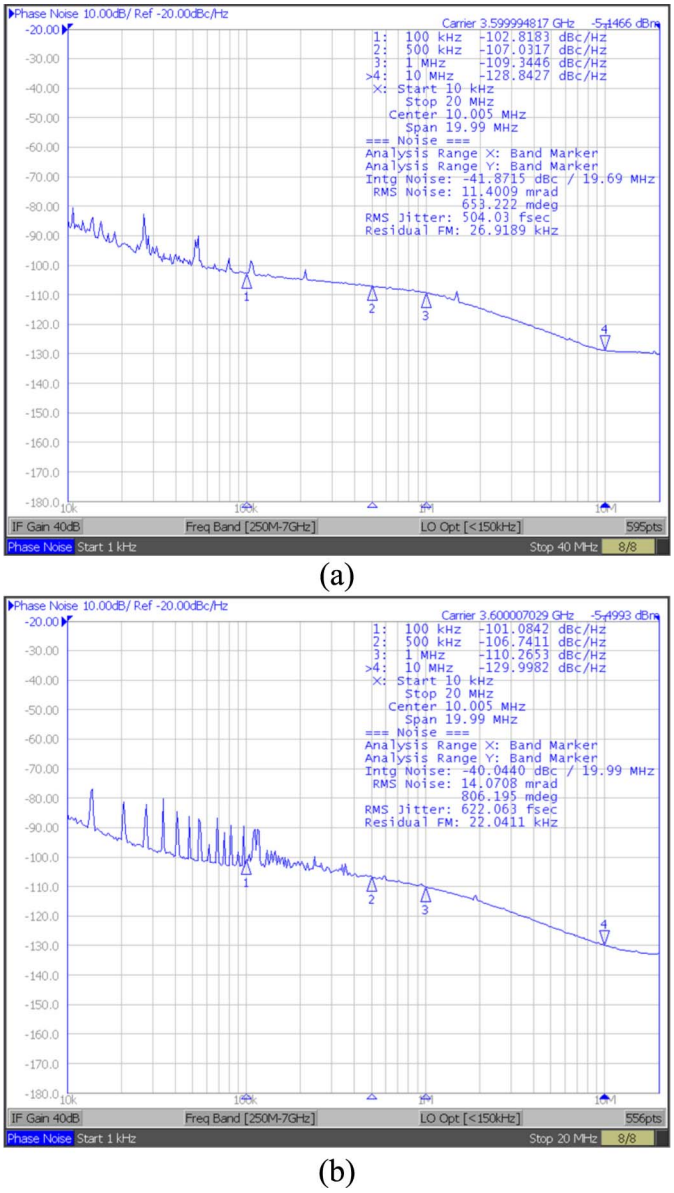

Fig. 18. Measured phase noise in fractional-N mode for (a) FCW $= 36 + 1/2^{16}$ and (b) FCW $= 36 + 9/2^{16}$.

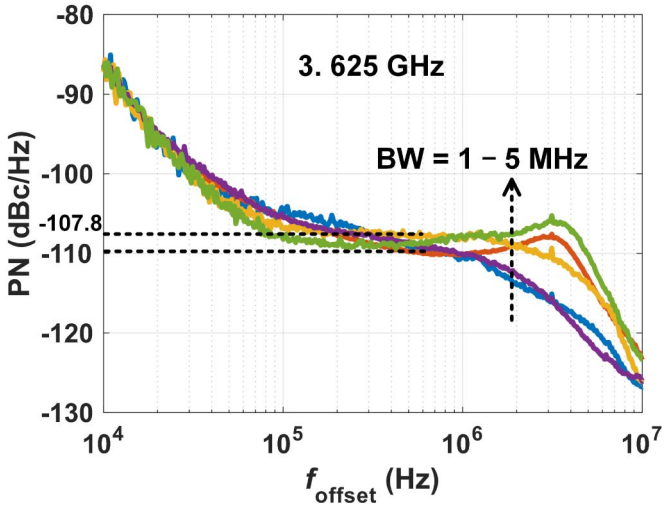

Fig. 19. Measured phase noise at 3.625 GHz (FCW $= 36 + 0.25$) with a loop BW ranging from 1 to 5 MHz.

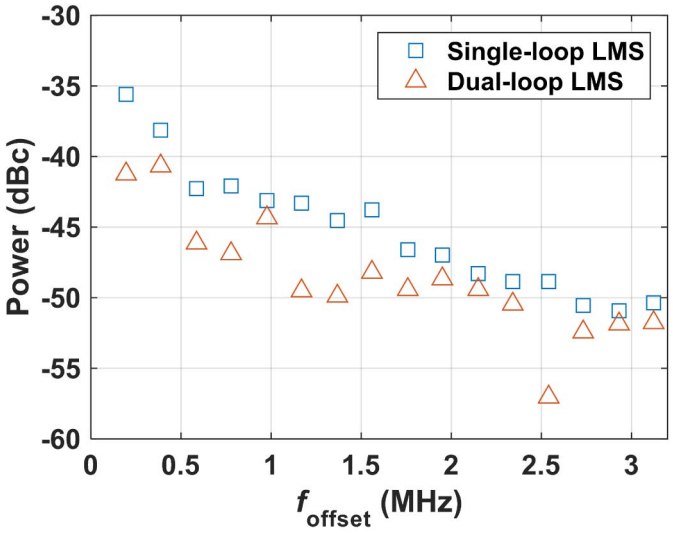

Fig. 20. Measured fractional spurs with dual-loop LMS and single-loop LMS calibration.

Fig. 18 shows the measured phase noise in fractional-N mode with the FCW set as $(36 + 1/2^{16})$ and $(36 + 9/2^{16})$, for which the in-band phase noise at 500 kHz is 109.3 dBc/Hz and 110.3 dBc/Hz, respectively. In-band fractional spurs corresponding to FCW are also observed. Fig. 19 shows the measured phase noise at 3.625 GHz (FCW $=$ 36.125), where the loop bandwidth was set from 1 to 5 MHz. Since the purpose is to verify the estimated TDC's noise contribution, we still tried higher loop BW to suppress more DCO's noise, aware of the influence to the stability. The in-band phase noise ranges from 107.8 dBc/Hz to 110.0 dBc/Hz. The resulting integrated jitter (10 kHz to 10 MHz) ranges from 390 fs to 560 fs.

The reference spur is measured to be 39.6 dBc, and the out-band phase noise does not fall, but rather rises after a 10 MHz offset. The poor noise and spur issues are due primarily to the improper on-chip grounding, the single-ended structure of the output buffer, and the parasitic inductance in the bond wire. The on-chip ground of the output buffer is connected to the ground of the digital block. Thus, the large transient current at 50 MHz modulates the output phase. In order to verify this, we have simulated the output spectrum of the output buffer at 3.6 GHz with a parasitic inductance of 2 nH at 50 MHz, current pulse of 40 mA, and a pulse width of 200 ps. The resulting spur at the offset of 50 MHz is 44.3 dBc, and the noise floor is around 136 dBc/Hz. This result is consistent with the measured reference spur and the noise floor shown in Fig. 17 and Fig. 18. Since in the actual circuit, the frequency of such current vibration cannot be purely 50 MHz due to the great amount of logic transitions and the bond wire effect, the noise spectrum closed to 50 MHz is also degraded. This problem could be resolved by carefully separating the on-chip grounds and by using a differential output buffer.

Fig. 1 shows the fractional spurs measured with dual-loop LMS and single-loop LMS calibrations. For each, the

TABLE I
PERFORMANCE COMPARISON

	This work		Venerus JSSC`15 [39]	Yao JSSC`13 [21]	Hsu JSSC`08 [13]	Lee JSSC`09 [14]	Siriburanon ISSCC`15 [40]	Chen ISSCC`15 [41]
CMOS (nm)	**65**		65	180	130	65	65	65
Technique	**TDC CHP + SAR-ADC**		ΔΣ FDC w/ ADC[5]	TDC GRO+ADC[5]	TDC GRO	TDC TA	Sub-sampling Pre-amp + ADC[5]	Sub-sampling SAR-ADC
Out. Freq. (GHz)	**3.625 (3.3 – 3.8)**		3.5 (2.8 – 3.5)	3.2 (2.8 – 3.2)	3.67 (N/A)	1.6824 (N/A)	2.2 (2.15 - 2.35)	2.68 (2.6 - 3.9)
Ref. Freq. (MHz)	**50**		26	52	50	25	100	40
Loop BW (MHz)	**5**	**1**	0.04	0.95	0.5	0.7	4	0.7
In. PN (dBc/Hz)	**-110.0**	**-107.3**	-70	-108.4	-108	-116	-112	-110.6
IPN_{norm} (dBc/Hz)[1]	**-110.1**	**-107.4**	-72.6	-107.2	-108.2	-112.4	-104.7	-109.0
Frac. Spur (dBc)	**-41**		43	-55	-42	-48	N/A[3]	N/A[4]
RMS Jitter (fs)	**560** **(10k – 10 MHz)**	**390**	N/A	230 (1k – 40 MHz)	204 (1k – 40 MHz)	495 (1k – 10 MHz)	380 (10k – 40 MHz)	226 (1k – 100 MHz)
FoM (dB)[6]	**-235.1**	**-238.3**	N/A	-240.4	-237.1	-225.3[2]	-242	-241.8
Power (mW)	**9.7**		21	17	46.7	121[2]	4.2	11.5
Area (mm^2)	**0.38**		0.56	0.62	0.95	2.25[2]	0.15	0.23

Note: [1.] Normalized using $IPN_{norm} = PN_{in} + 10\log_{10}((3.6\text{GHz})^2/50\text{MHz}) - 10\log_{10}(f_{out}^2/f_{ref})$.

[2.] Including the amplitude and frequency modulation.

[3.] It is an integer-N digital PLL.

[4.] In-band fractional spurs are not shown.

[5.] It is a flash ADC.

[6.] FoM = 10log[(Jitter/1s)^2(Power/1mW)].

in-band spurs are measured to be 41 dBc and 36 dBc, respectively, at the offset of 195 kHz. Although the improvement was observed when using dual-loop LMS calibrations, the results were worse compared to those of the simulation. With largely experimental tweaking and circuit re-checking, we found several possible reasons for the existence of poor fractional spurs. First, we found some loss of precision due the order of multiplication in the LMS block. According to RTL-level simulation, K_{t1} and K_{t2} less accurately settle to the expected values, leading to fractional spurs. Second, as shown in Fig. 15(b), the nonlinearity of the TDC causes fractional spurs. This effect is also verified observing the change of spur power when tweaking the common-mode and reference voltages, and the bias current. Second, the aforementioned grounding causes periodic vibration detected by the PFD, as reported in a previous study [7]. We found that the spur power changes after changing even 10 mV of the supply voltage. Since supply voltage affects the logic threshold, the triggering time of the PFD may be moved to another point in a ripple with determinist characteristics.

The performance is compared in Table I with PLLs using ADCs and the ones with GRO- and TA- TDCs. Since in-band phase noise depends not only on the output but also on the reference frequencies, the noises normalized to the case of (3.6 GHz)^2/50 MHz are also compared. In this comparison, the proposed PLL achieves competitive in-band phase noise, lowest power, and smaller area.

VI. CONCLUSION

This paper presents a fractional-N digital PLL with low in-band phase noise using the proposed high-resolution TDC. The achieved in-band phase noise measured at various frequencies was consistent with the measured effective resolution of the TDC. A high-resolution, ΔΣ-less and MOS-varactor-less LC-DCO is proposed with bridging capacitors to lower the quantization noise. The building blocks accommodating the TDC are designed as well. With the proposed TDC and DCO, the digital PLL has achieved 110 dBc/Hz in-band phase noise at 3.625 GHz output, with 9.7 mW power consumption, and 0.38 mm^2 area. In conclusion, a high-performance digital PLL with a practically designed TDC and DCO was demonstrated in this work.

REFERENCES

[1] T. A. D. Riley, M. A. Copeland, and T. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, May 1993.

[2] T.-H. Lin, C.-L. Ti, and Y.-H. Liu, "Dynamic current-matching charge pump and gated-offset linearization technique for delta-sigma fractional-N PLLs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 877–885, May 2009.

[3] H.-M. Chien *et al.*, "A 4 GHz fractional-N synthesizer for IEEE 802.11a," in *Proc. IEEE VLSIC*, Jun. 2004, pp. 46–49.

[4] S. Pamarti, L. Jansson, and I. Galton, "A wideband 2.4-GHz delta-sigma fractional-NPLL with 1-Mb/s in-loop modulation," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 49–62, Jan. 2004.

[5] E. Temporiti, G. Albasini, I. Bietti, R. Castello, and M. Colombov, "A 700-kHz bandwidth $\Sigma\Delta$ fractional synthesizer with spurs compensation and linearization techniques for WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1446–1454, Sep. 2004.

[6] M. Gupta and B.-S. Song, "A 1.8-GHz spur-cancelled fractional-N frequency synthesizer with LMS-based DAC gain calibration," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2842–2850, Dec. 2006.

[7] K. J. Wang, A. Swaminathan, and I. Galton, "Spurious tone suppression techniques applied to a wide-bandwidth 2.4 GHz fractional-N PLL," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2787–2797, Dec. 2007.

[8] A. Swaminathan, K. J. Wang, and I. Galton, "A wide-bandwidth 2.4 GHz ISM band fractional-N PLL with adaptive phase noise cancellation," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2639–2650, Dec. 2007.

[9] H. Hedayati, W. Khalil, and B. Bakkaloglu, "A 1 MHz bandwidth, 6 GHz 0.18 μm CMOS type-I $\Delta\Sigma$ fractional-N synthesizer for WiMAX applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3244–3252, Dec. 2009.

[10] R. B. Staszewski *et al.*, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

[11] R. B. Staszewski *et al.*, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2480, Dec. 2005.

[12] E. Temporiti, C. Weltin-Wu, D. Baldi, R. Tonietto, and F. Svelto, "A 3 GHz fractional all-digital PLL with a 1.8 MHz bandwidth implementing spur reduction techniques," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 824–834, Mar. 2009.

[13] C.-M. Hsu, M. Z. Straayer, and M. H. Perrott, "A low-noise wide-BW 3.6-GHz digital $\Delta\Sigma$ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2776–2786, Dec. 2008.

[14] M. Lee, M. E. Heidari, and A. A. Abidi, "A low-noise wideband digital phase-locked loop based on a coarse–fine time-to-digital converter with subpicosecond resolution," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2808–2816, Oct. 2009.

[15] L. Xu, S. Lindfors, K. Stadius, and J. Ryynanen, "A 2.4-GHz low-power all-digital phase-locked loop," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1513–1521, Aug. 2010.

[16] T. Tokairin, M. Okada, M. Kitsunezuka, T. Maeda, and M. Fukaishi, "A 2.1-to-2.8-GHz low-phase-noise all-digital frequency synthesizer with a time-windowed time-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2582–2590, Dec. 2010.

[17] M. S.-W. Chen, D. Su, and S. Mehta, "A calibration-free 800 MHz fractional-N digital PLL with embedded TDC," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2819–2827, Dec. 2010.

[18] E. Temporiti, C. Weltin-Wu, D. Baldi, M. Cusmai, and F. Svelto, "A 3.5 GHz wideband ADPLL with fractional spur suppression through TDC dithering and feedforward compensation," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2723–2736, Dec. 2010.

[19] M. Zanuso, S. Levantino, C. Samori, and A. L. Lacaita, "A wideband 3.6 GHz digital $\Delta\Sigma$ fractional-N PLL with phase interpolation divider and digital spur cancellation," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 627–638, Mar. 2011.

[20] K. Takinami, R. Strandberg, P. C. P. Liang, G. Le Grand De Mercey, T. Wong, and M. Hassibi, "A distributed oscillator based all-digital PLL with a 32-phase embedded phase-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2650–2660, Nov. 2011.

[21] C.-W. Yao and A. N. Willson, "A 2.8–3.2-GHz fractional-N digital PLL with ADC-assisted TDC and inductively coupled fine-tuning DCO," *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 698–710, Mar. 2013.

[22] H. S. Kim *et al.*, "A digital fractional-N PLL with a PVT and mismatch insensitive TDC utilizing equivalent time sampling technique," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1721–1729, Jul. 2013.

[23] A. Samarah and A. Chan Carusone, "A digital phase-locked loop with calibrated coarse and stochastic fine TDC," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1829–1841, Aug. 2013.

[24] S. Ryu, H. Yeo, Y. Lee, S. Son, and J. Kim, "A 9.2 GHz digital phase-locked loop with peaking-free transfer function," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1773–1784, Aug. 2014.

[25] A. Elkholy, T. Anand, W. S. Choi, A. Elshazly, and P. K. Hanumolu, "A 3.7 mW low-noise wide-bandwidth 4.5 GHz digital fractional-N PLL using time amplifier-based TDC," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 867–881, Apr. 2015.

[26] L. Vercesi, L. Fanori, F. De Bernardinis, A. Liscidini, and R. Castello, "A dither-less all digital PLL for cellular transmitters," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1908–1920, Aug. 2012.

[27] L. Vercesi, A. Liscidini, and R. Castello, "Two-dimensions Vernier time-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1504–1512, Aug. 2010.

[28] J. Yu, F. F. Dai, and R. C. Jaeger, "A 12-bit Vernier ring time-to-digital converter in 0.13 μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 830–842, Apr. 2010.

[29] M. Z. Straayer and M. H. Perrott, "A multi-path gated ring oscillator TDC with first-order noise shaping," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1089–1098, Apr. 2009.

[30] M. Lee and A. A. Abidi, "A 9 b, 1.25 ps resolution coarse–fine time-to-digital converter in 90 nm CMOS that amplifies a time residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769–777, Apr. 2008.

[31] N. Pavlovic and J. Bergervoet, "A 5.3 GHz digital-to-time-converter-based fractional-N all-digital PLL," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 54–56.

[32] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9-to-4.0GHz fractional-N digital PLL with bang-bang phase detector and 560fsrms integrated jitter at 4.5mW power," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 88–90.

[33] Z. Xu, M. Miyahara, and A. Matsuzawa, "A 3.6 GHz fractional-N digital PLL using SAR-ADC-based TDC with -110 dBc/Hz in-band phase noise," in *Proc. IEEE A-SSCC*, Nov. 2015, pp. 1–4.

[34] Z. Xu, S. Lee, M. Miyahara, and A. Matsuzawa, "A 0.84 ps-LSB 2.47 mW time-to-digital converter using charge pump and SAR-ADC," in *Proc. IEEE CICC*, Sep. 2013, pp. 1–4.

[35] Z. Xu, S. Lee, M. Miyahara, and A. Matsuzawa, "Sub-picosecond resolution and high-precision TDC for ADPLLs using charge pump and SAR-ADC," *IEICE Trans. Fundam.*, vols. E98-A, no. 2, pp. 476–484, 2015.

[36] Z. Xu, M. Sugawara, K. Mori, M. Miyahara, and A. Matsuzawa, "A varactor-less and dither-less LC-digitally controlled oscillator with 9-bit fine bank, 0.26 mm2 area, and 6.7 kHz frequency resolution," in *Proc. Int. Conf. SSDM*, 2014, pp. 986–987.

[37] R. B. Staszewski and P. T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*. New York, NY, USA: Wiley, 2006.

[38] A. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.

[39] C. Venerus and I. Galton, "A TDC-free mostly-digital FDC-PLL frequency synthesizer with a 2.8–3.5 GHz DCO," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 450–463, Feb. 2015.

[40] T. Siriburanon *et al.*, "A 2.2GHz–242dB-FOM 4.2 mW ADC-PLL using digital sub-sampling architecture," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[41] Z.-Z. Chen *et al.*, "14.9 sub-sampling all-digital fractional-N frequency synthesizer with –111dBc/Hz in-band phase noise and an FOM of –242dB," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[42] V. K. Chillara *et al.*, "An 860 μW 2.1-to-2.7 GHz all-digital PLL-based frequency modulator with a DTC-assisted snapshot TDC for WPAN (Bluetooth smart and ZigBee) applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 172–173.

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