A Sub-0.5 Electron Read Noise VGA Image Sensor in a Standard CMOS Process

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***Abstract*— A sub-0.5 e^-_{rms} temporal read noise VGA (640H×480V) CMOS image sensor has been integrated in a standard 0.18 μm 4PM CMOS process. The low noise performance is achieved exclusively through circuit optimization without any process refinements. The presented imager relies on a 4T pixel of 6.5 μm pitch with a properly sized and biased thin oxide PMOS source follower. A full characterization of the proposed image sensor, at room temperature, is presented. With a pixel bias of 1.5 μA the sensor chip features an input-referred noise histogram from 0.25 e^-_{rms} to a few e^-_{rms} peaking at 0.48 e^-_{rms}. The imager features a full well capacity of 6400 e^- and its frame rate can go up to 80 fps. It also features a fixed pattern noise as low as 0.77%, a lag of 0.1% and a dark current of 5.6 e^-/s. It is also shown that the implementation of the in-pixel n-well does not impact the quantum efficiency of the pinned photo-diode.**

***Index Terms*— CMOS, CIS, image sensor, low noise, sub-electron, low light, $1/f$ noise, thermal noise, thin oxide, thick oxide.**

I. Introduction

THE market demand for electronic image sensors, and particularly CMOS compatible, is in continuous growth. Over the last decade, mobile handset and digital cameras occupied the biggest part of the market and fuelled the development of CMOS image sensors for low cost and performance applications. For decades charge-coupled devices (CCDs) have been the technology of choice in terms of noise and dynamic range performance. Compared to CMOS active pixel sensors (APS), CCDs are expensive, present higher power consumption, lower speed and preclude on-chip integration. Regarding the sensitivity, the considerable gap between CCDs and CMOS image sensors based on conventional PN junction photodiodes was mainly due to the reset kTC noise. The development of pinned photodiodes (PPDs) also known as buried photodiodes in CMOS technology reduced dramatically that gap. Indeed, CMOS image sensors (CIS) with PPDs present a lower dark current and a lower noise achieved thanks to the double sampling readout scheme. Today, markets like medical, security, industrial vision, defence, scientific imaging or space are expected to grow and increase the demand for more sensitive CIS operating in low light conditions.

During the last few years, many works focused on the reduction of the temporal readout noise (TRN) in CMOS image sensors based on pinned photodiodes in order to enhance their performance under low light conditions. To this purpose, the noise of the whole readout chain has to be minimized, starting with the thermal noise using conventional circuit techniques, e.g. bandwidth control, in-pixel or column-level amplification and correlated multiple sampling (CMS) [1] [2] [3]. After thermal noise reduction, the $1/f$ noise originating from the pixels becomes the dominant noise source. At the circuit level, the correlated double sampling (CDS) and CMS reduce dramatically that $1/f$ noise, but not enough to reach sub-electron noise performance [4] [3]. Pixel-level optimization is required in order to further reduce the $1/f$ noise. In [1], 0.86 e^-_{rms} input-referred TRN has been achieved by implementing a PMOS in-pixel open-loop amplifier. It showed that sub-electron performance can be reached, using only circuit techniques, at the cost of a lower dynamic range and higher photo-response non-uniformity (PRNU) [1]. Other works focused on process level techniques. In [2], 0.7 e^-_{rms} input-referred TRN is reached by implementing a buried channel source follower (SF) together with CMS. More recently, 0.74 e^-_{rms} TRN (in the SF readout mode) has been demonstrated by combining a buried channel SF with the reduction of the sense node capacitance obtained through process optimization [5]. Deep sub-electron noise performance has been recently reported by implementing process level techniques reducing the sense node (SN) capacitance [6] [7] but at the cost of a low full well of 200 e^- in [6] and the use of a 25 V off-chip reset clock voltage in [7].

The purpose of this work is to exploit the only few degrees of freedom left to the designer, in a standard process, to further reduce the input-referred TRN to sub-0.5-electron level. We have presented, in a recently reported work [8], a detailed noise analysis showing that the selection of a thin-oxide SF with a lower gate size and proper biasing comes with a lower $1/f$ and thermal noise. We showed that an average TRN as low as 0.4 e^-_{rms} is reached but on a small number of isolated pixels.

This paper presents the first implementation, in a standard process, of pixels with thin oxide PMOS SFs in a full VGA (640H×480 V) APS. The proposed imager features an input-referred noise histogram ranging from 0.25 e^-_{rms} to a few e^-_{rms} and peaking at 0.48 e^-_{rms}. In the mean time, it features a pixel pitch of 6.5 μm, a dynamic range of 82.5 dB corresponding to a full well capacity of 6400 e^- and a frame rate up to 80 fps.

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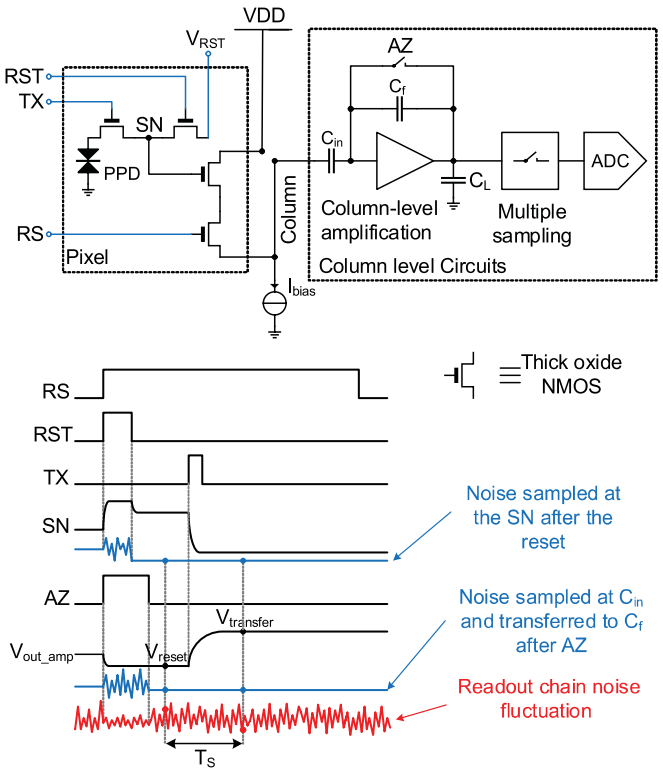


Fig. 1. Schematic and timing diagram of a conventional CIS readout chain based on a 4T pixel.

This imager crosses the bridge between highly sensitive low-light CIS and conventional imagers. It demonstrates the efficiency of the proposed design level noise reduction technique that can be easily combined with the process optimizations mentioned above for even more noise reduction.

This paper is organized as follows. Section II reviews the low noise CIS readout chain architecture and noise sources. In Section III, the noise reduction mechanism is recalled. Section IV presents the overall architecture of the imager as well as the most important blocks. Section V details the test and characterization of the proposed imager, presents the experimental setup, the measurement method and results. Section VI discusses the measurement results.

II. Read Noise in Low Light CMOS Image Sensors

Conventional low-noise CIS readout chains are based on active pixels, column-level amplifiers that control the bandwidth and introduce a gain minimizing the noise contribution of the next stages and CMS or CDS stages. The latter can also be performed after analog-to-digital conversion. Fig. 1 shows a schematic of a conventional low-light CIS readout chain together with the pixel timing diagram. Conventional pixels encompass a PPD, a transfer gate (TG), a reset switch, a row selection switch and an SF transistor. The PPD accumulates the photo-generated electrons in its buried potential well. The transfer gate controls the potential barrier between the PPD and the floating diffusion. The SF gate is connected to the floating diffusion (FD) in order to sense its voltage level. During the readout, the reset gate is switched-on in order to empty the FD from electrons. The column-level amplifier auto-zero (AZ) is performed in order to reset the feadback capacitance, cancel the offset and reduce its low frequency noise [9]. The floating diffusion voltage reset level is sampled at the output of the column-level amplifier. The transfer gate is then switched-on in order to transfer the accumulated photo-electrons to the floating diffusion. The voltage level after this operation is again sampled at the output of the column-level amplifier and differentiated with the reset level voltage. In some low noise CIS the SF transistor is replaced by a gain stage like a common-source [1] or transimpedance amplifiers (CTIAs). It has been shown in a previous work [10] that a readout chain based on in-pixel gain does not necessarily introduce a lower noise compared to a readout chain with an in-pixel source follower scheme and column-level amplification.

The CIS readout chain noise mechanisms are depicted in the timing diagram of Fig. 1. It shows two types of noise. The first is the sampled noise constant in time during one readout of the pixel and randomly changing at the next readout and from pixel to pixel. It includes the noise sampled at the sense node after its reset (mainly kTC noise) and the noise sampled at the integration capacitor and transferred to the output after the colum-level amplifier AZ [11]. This sampled noise originates from the thermal and low frequency noise of the SF stage and the column-level amplifier before opening the AZ switch. The second type of noise is the random fluctuation of the signal during the readout originating from the SF stage and the column-level amplifier after opening the AZ switch. All these noise sources are uncorrelated and add to each other at the output of the readout chain.

The double sampling and differentiation (CDS or CMS) performed at the output of the CIS readout chain has two main advantages regarding its noise performance. The first one consists in the cancellation of the sampled noise. The second one consists in the reduction of the $1/f$ noise of the SF stage and column-level amplifier. After the double sampling, the dominant noise source is the random fluctuation originating from the thermal, $1/f$ and random telegraph signal (RTS) noise of the readout chain transistors. RTS noise is a severe problem that especially appears in small sized transistors like the in-pixel SF. But for current CIS processes, it only appears in a minority of pixels.

III. Noise Reduction Mechanism

The noise reduction starts by implementing enough column-level gain in order to minimize the noise contribution of the next stages and limit the noise analysis and optimization to the in-pixel SF stage, the current source of the SF and the column-level amplifier.

The thermal noise originating from the SF stage and column-level amplifier is reduced using a proper design of the SF current source and bandwidth control obtained with high column-level amplification [8]. Simulation results from [12] show that thermal noise originating from the SF stage, the column-level amplifier and the current source can be reduced to about $0.2\,e^-_{rms}$ if the bandwidth is limited to 265kHz. Thermal noise can be reduced using CMS at the end of the

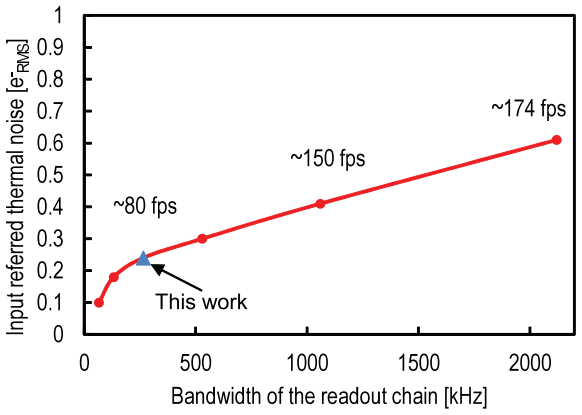


Fig. 2. Simulated input-referred thermal noise as a function of the readout chain bandwidth set by the column level amplifier with the estimated framerates achievable for the presented VGA imager.

readout chain [3] [13] [14] but at the cost of a larger readout time. It has been shown in [8] that the input-referred thermal noise can also be reduced by increasing the conversion gain of the pixel. In this work we chose to perform a simple CDS for a faster readout. The bandwidth of the readout chain is roughly inversely proportional to the product of the column level gain and the load capacitance of the column level amplifier [8]. It has been set to 265 kHz with a gain of 64 in order to make the thermal noise lower than the $1/f$ noise (below $0.3\,e^-_{rms}$). Fig. 2 shows the simulated input-referred thermal noise of the conventional readout chain of Fig. 1 as a function of the readout chain bandwidth which is tuned using different combinations of the column-level gain and the load capacitance. It also indicates the estimated framerates achievable for each bandwidth. For large readout chain bandwidths, the framerate becomes limited by the time required by the ADC to convert and shift the data to the output which is about $10\,\mu$s. At about 80 fps, the low frequency noise of the readout chain becomes the dominant noise source.

The $1/f$ noise is dramatically reduced by the AZ and CDS or CMS. However, it remains the dominant noise in the readout chain [12] [3]. The critical transistors of the column-level circuitry can be designed to have gate sizes large enough to make their contribution to the total $1/f$ noise of the readout chain negligible compared to the in-pixel SF's. Thus, in a conventional low noise CIS readout chain, with column amplification, bandwidth control and careful design, the $1/f$ noise originating from the in-pixel SF remains the dominant noise source.

The gate-referred power spectral density (PSD) of the $1/f$ noise generated by the in-pixel SF is inversely proportional to its gate size and the squared oxide capacitance per unit-area. But the conversion gain of the pixel is linearly dependent on the product of the in-pixel SF gate size and oxide capacitance per unit area. Consequently, it is important to start from a detailed analytical calculation of the input-referred $1/f$ noise. Based on [8] and using the EKV formalism [15], the input-referred $1/f$ noise charge variance can be expressed as

$$\overline{Q^2_{n,1/f}} = \alpha_{CMS}\frac{K\left(C_P + 2C_e \cdot W + \frac{2}{3}C_{ox} \cdot W \cdot L\right)^2}{C^2_{ox} \cdot W \cdot L} \quad (1)$$

with

$$K = K_G \cdot k \cdot T \cdot q^2 \cdot \lambda \cdot N_t. \quad (2)$$

In (2), k is the Boltzman constant, T is the absolute temperature, q is the electron charge, λ is the tunneling attenuation distance ($\simeq 0.1$ nm) [16], N_t is the oxide trap density, and K_G is a bias-dependent parameter close to unity when the transistor is operating in the weak and moderate inversion [15].

In (1), W and L are the SF gate width and length, respectively, C_{ox} is the SF gate oxide capacitance per unit area, C_P is the total capacitance at the SN made of the SN junction capacitance, the transfer gate and reset transistor overlap capacitances and the metal wires parasitic capacitance. C_e is the extrinsic capacitance per unit width of the SF transistor that includes the fringing-field and overlap capacitances and which can be considered as bias-independent in this first order analysis. α_{CMS} is a unitless circuit design dependent parameter reflecting here the impact of the correlated sampling [3] [14]. For a simple CDS, assuming enough time for the signal settling between the samples, α_{CMS} ranges between 4 and 5 [12].

Based on (1), the $1/f$ noise originating from the in-pixel SF can be reduced through process level optimizations, column-level design and pixel-level design.

The process level optimizations include the reduction of K and C_P. For instance, the parameter K has been reduced, in [2], by using a buried channel SF. In [2] [6], the parameter C_P has been minimised by applying process refinements reducing the overlap and junction capacitances connected to the SN. In this work, we use a standard CIS technology and cannot drastically change these parameters. Nevertheless, they can be addressed by making a good device choice among the standard transistors and careful layout, with respect to the standard design rules, in order to keep the term C_P as low as possible.

At the column-level circuit design, the $1/f$ noise reduction consists in the correlated multiple or double sampling with a careful design of the column-level circuitry. It is reflected by the term α_{CMS} in (1). In this work, a simple CDS is performed.

The design optimization at the pixel level is the focus of this work. The idea is to exploit all the few degrees of freedom left to the designer in order to achieve a $1/f$ noise as low as possible. Equation (1) suggests that the $1/f$ noise can also be reduced by increasing C_{ox}, reducing W and using an optimal L. From a designer perspective, this corresponds to using a thin oxide SF transistor instead of the traditionally used thick oxide SF. This choice allows to take advantage of the lower minimum gate width and higher C_{ox}. Thick oxide transistors are used in order to support the high voltages (around 3 V) used in pixels based on PPDs. Thin oxide transistors are used for digital design. For this 180 nm CIS process, thick oxide transistors feature an oxide thickness of 7 nm compared to 3 nm for the standard digital thin oxide transistors. Thick oxide transistors feature a lower leakage current and are more suited to be used as switches than thin oxide transistors. Thus, in this work, we propose a pixel design where only the SF transistor features a thin oxide. This choice is not obvious since practical issues related to the use of a thin oxide SF need to be solved. Indeed, for the process used in this work, the thin

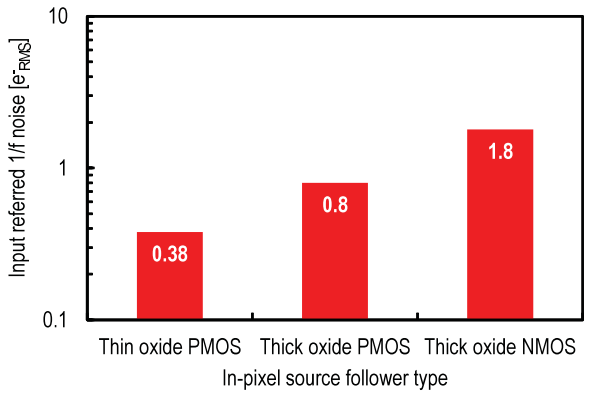


Fig. 3. Simulated input-referred $1/f$ noise for three readout chains sharing the same column-level circuitry and using different in-pixel SF transistor types.

oxide transistor supports low voltages (1.8 V) but must operate in a high voltage (3.3 V) environment without a dramatic impact on the dynamic range of the pixel. These points will be discussed in the next Section together with the design of the newly proposed pixel. Fig. 3 presents the simulated input-referred $1/f$ noise of readout chains sharing the same column-level amplifier and CDS circuits and based, respectively, on in-pixel thick oxide NMOS, thick oxide PMOS and a the newly proposed thin oxide PMOS. The difference between the input-referred noise of the thick oxide transistors is due to the lower K factor of the PMOS. The thin oxide PMOS combines a lower K factor with a higher C_{ox} and smaller gate size. Hence, its implementation as a SF results in the best $1/f$ noise performance as expected theoretically.

IV. Chip Architecture and Circuit Design

A. Imager Architecture

Fig. 4 shows the overall architecture of the imager. It is a rolling shutter CMOS image sensor with 640(H)×480(V) array of the newly proposed 4T pixels with standard PPDs. A row control mixed signal block generates for each line of pixels the reset (RST), transfer (TX) and selection (RS) signals (Fig. 9). The row control block also allows the control of the integration time. Each column of the pixels array is connected to a closed loop gain amplifier introducing gain and limiting the bandwidth. A mixed signal analog multiplexing block made of shift registers, voltage level shifters and analog switches is implemented at the output of the column-level amplifiers. It allows to choose between an analog or digital output. In the digital readout mode, each column-level output is simply connected to the input of a 10 bits single-slope ADC (SS-ADC). All the columns are read in parallel. In this configuration, the imager operates at 80 fps. In the analog readout mode, the shift registers and analog switches connect the columns to the analog output. In this case, the columns are read one after the other. The analog readout mode is important for proper characterization of the pixels. In this mode the frame rate is 640 times slower but the column and pixel readout time remain the same.

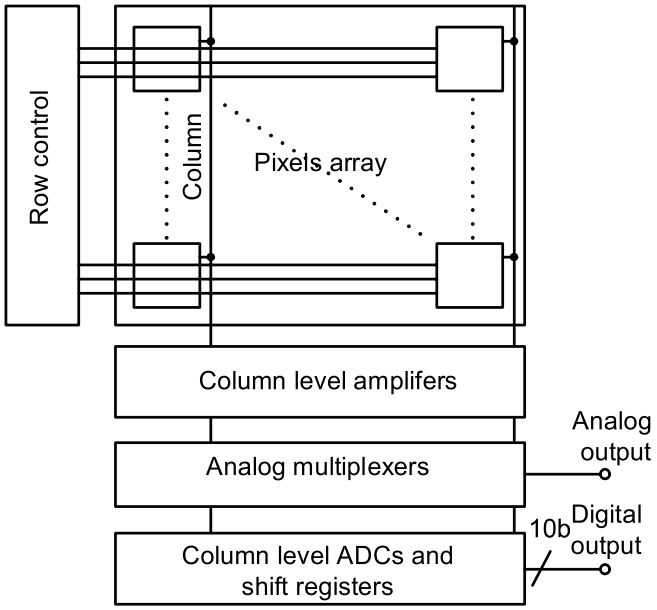
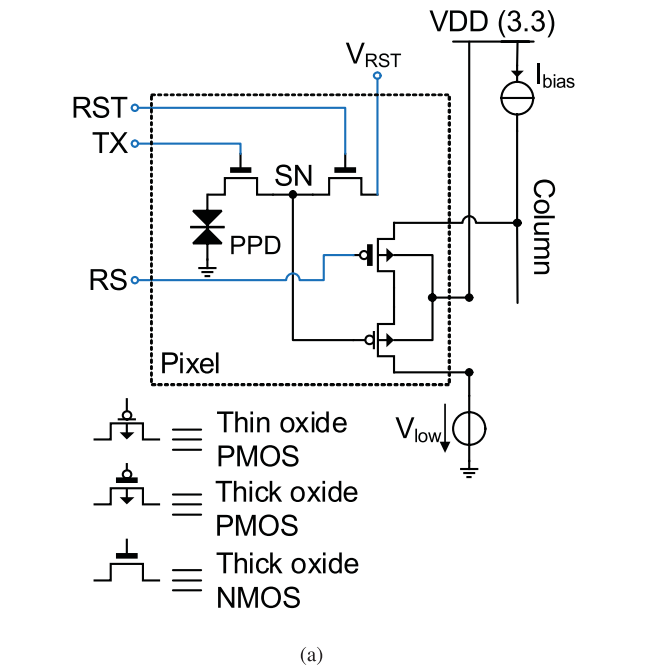


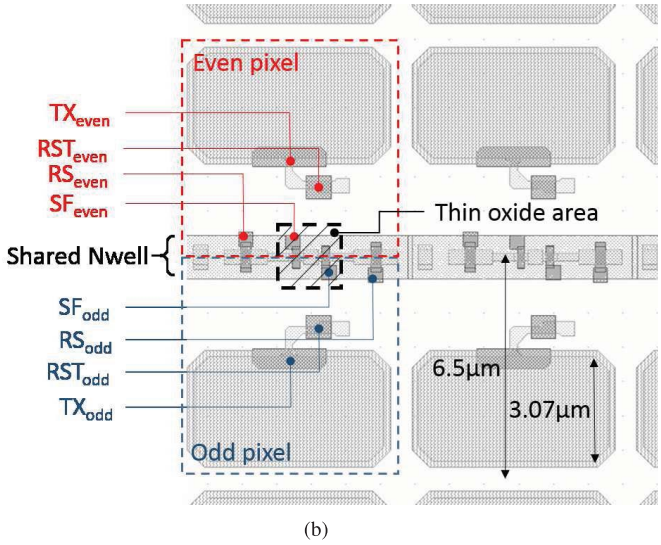
Fig. 4. Overall architecture of the proposed image sensor.

B. Pixel Design and Layout

As discussed in the previous section, the $1/f$ noise originating from the SF transistor can be reduced using a SF with a thinner oxide and lower gate width. From a designer perspective, this can be achieved by using a thin oxide (1.8 V) transistor instead of a thick oxide (3.3 V) in the 180 nm CMOS process used for this work. The sense node needs to be reset at a voltage higher than 2 V for a good dynamic range and also to make sure that the sense node attracts efficiently the charges from the PPD when the potential barrier under the transfer gate is removed. Yet, the voltage difference between the gate and the bulk of the thin oxide SF must remain smaller than 1.8 V. Hence, the bulk voltage of the thin oxide SF must be shifted. To this purpose a PMOS thin oxide transistor is chosen. Indeed, the bulk voltage of a PMOS transistor can be controlled through the n-well connection. An NMOS transistor with a separated p-well could also be used, but at the cost of a larger area. Also, a PMOS thin oxide SF usually shows a lower $1/f$ noise parameter K than NMOS in the target technology nodes. Consequently, the K parameter in (1) is expected to be lower for the PMOS thin oxide SF. A thick oxide PMOS row select (RS) transistor is chosen in order to put it in the same n-well as the SF and optimize the layout footprint of the in-pixel readout transistors. Fig. 5(a) shows the schematic of the proposed pixel. The bulk voltage of the thin oxide PMOS SF is set to V_{DD} at 3.3 V to insure that the voltage difference between its bulk and the gate (sense node) is positive and below 1.8 V. The drain voltage of the SF is connected to (V_{low}) which is set to 1.5 V in order to shift the ground of the SF stage and make sure that the voltage differences between all the thin oxide SF terminals remain below 1.8 V. The SF gate is sized to minimize its input-referred TRN according to 1, which is plotted in Fig. 6 versus the gate width W and length L. It clearly shows that W should be chosen as minimum ($W = 0.22\,\mu$m) whereas L should



(a)



(b)

Fig. 5. Timing diagram of the proposed readout chain.

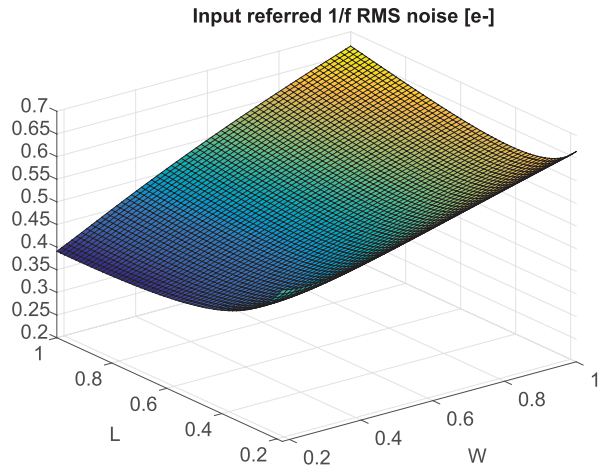


Fig. 6. Schematic of the proposed pixel (a) and a layout view of the neighboring pixels (b).

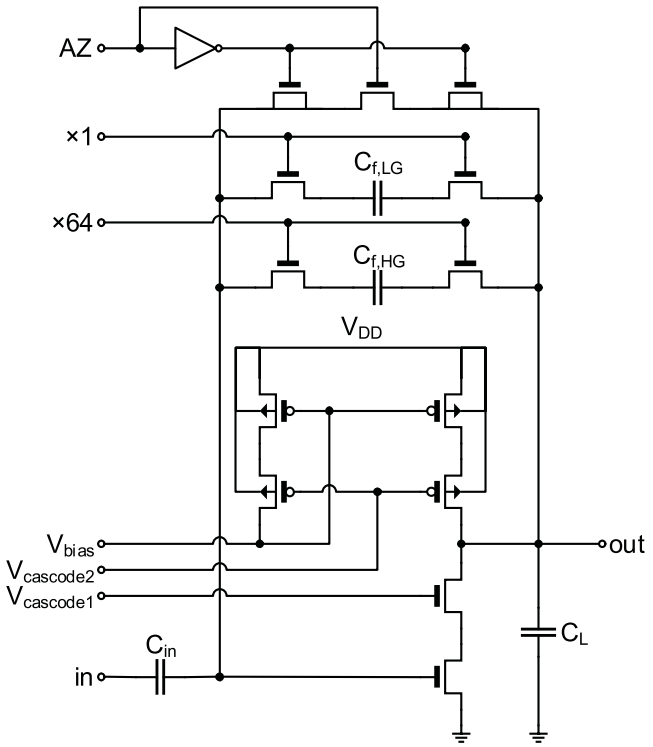


Fig. 7. The calculated input-referred $1/f$ noise, based on (1), as a function of the in-pixel source follower width W and length L for a thin oxide transistor in a 180nm technology where $C_e = 0.95\,\text{fF}/\mu\text{m}$, $C_{ox} = 9.5\,\text{fF}/\mu\text{m}^2$, $C_P = 0.75\,\text{fF}$ and the minimum gate width is $0.22\,\mu\text{m}$.

be chosen at a higher value ($L = 0.5\,\mu$m). But based on the noise analysis detailed in [8], the variance of the input-referred thermal noise contribution of the pixel increases with L^3 while the one originating from the column-level amplifier increases with L^2. Hence the slight additional reduction of the $1/f$ noise obtained by increasing L would be at the cost of a much larger thermal noise. The transfer (TX) gate and reset (RST) transistor are thick oxide NMOS.

Introducing an n-well in the pixel of a CIS can be harmful for the fill factor. Indeed, a minimum distance is imposed between the n-well and the neighboring NMOS and PPD. Also, a minimum distance between thin oxide and thick oxide transistors has to be fulfilled. In order to address these issues, an optimized layout still filling all the standard design rules is proposed. The optimization relays on putting the maximum number of transistors in the same n-well and keeping this latter away from the PPDs. Fig. 5(b) shows the proposed layout of neighboring pixels. The repeated pattern of the pixels array consists of two symmetrical pixels sharing a common n-well with the two SFs and RSs. Inside the N well, a common thin oxide area contains the two SFs. This compact layout results in a fill factor of 40% with a pixel pitch of 6.5 μm.

C. Column-Level Amplifier

Fig. 7 shows the schematic of the column-level adjustable gain amplifier. The closed-loop gain is set by the ratio of the

integrating and feedback capacitors. The feedback capacitors can be switched in order to change the gain between two levels: 1, for high dynamic range in normal light conditions and 64 for low noise at low light conditions. The open-loop gain is provided by an OTA. For the OTA design and layout, the priority is given to the noise constraint. The dynamic range is not critical since the voltage swing at the output of the pixel is not higher than 1.5 V. A single-ended structure is used because it involves half the number of noisy transistors compared to a differential one. Differential amplifiers are certainly better at rejecting any common mode noise (e.g. noise coming from the substrate and power supply) but at the cost of more noise and more power. Indeed, in the case of an operational transconductance amplifier (OTA) such as the one used in this amplifier, the differential structure requires to duplicate the circuit branch resulting in twice the power consumption and twice the thermal noise excess factor for achieving the same transconductance. In order to achieve low noise and to stay within our power budget, we have chosen a single ended implementation. The noise originating from the power and bias sources is reduced on-bord by using power filters. Regarding the area, it is manly set by the input and feedback capacitors especially for high gains. Hence, a differential topology would occupy about the same area but, as explained above, with the penalty of double power and noise. The situation would be even worse for a fully differential amplifier (differential input differential output) since it would generate twice as much noise, power and area compared to the single ended implemented in this work. The high closed-loop gain of 64 requires a large open-loop gain hard to achieve with a simple single ended amplifier. It is known that cascode structures provide much higher gain with a negligible noise contribution of the cascode transistors. Hence, a fully cascoded single-ended amplifier is used. In order to make the $1/f$ noise contribution of the column-level amplifier negligible compared to the one originating from the pixel, the transistors of the OTA have gate areas more than 10 times larger than the SF. The charge injection of the AZ switch can reduce considerably the output voltage swing of the amplifier in the high column-level gain mode. In order to reduce that charge injection, dummy devices with a proper sizing are used in order to compensate the charge injected by the main NMOS switch.

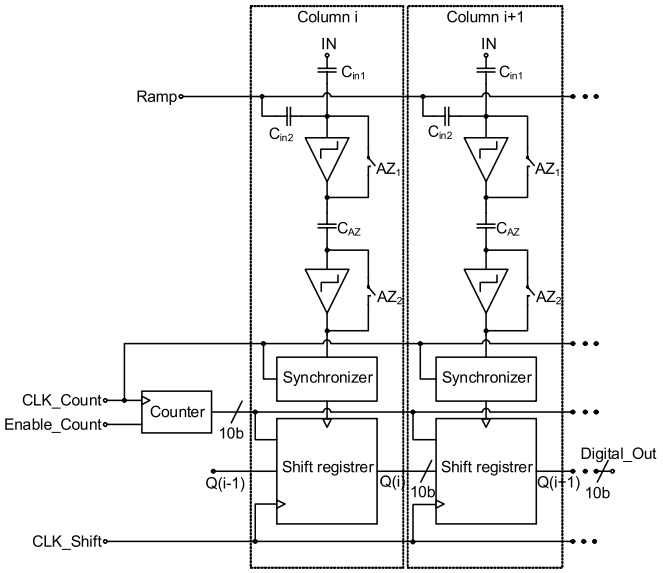


Fig. 8. Schematic of the column-level amplifier.

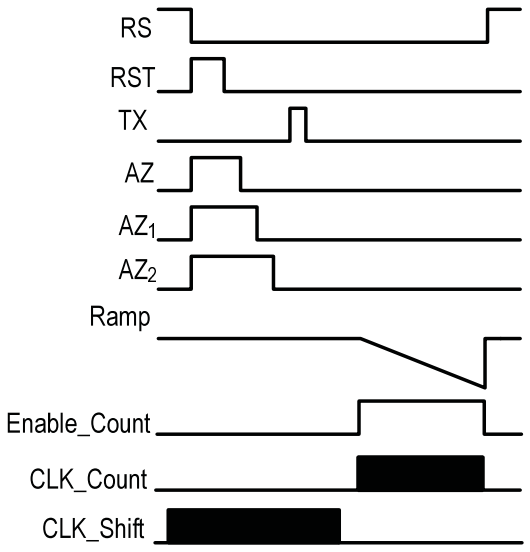


Fig. 9. Block diagram of the SS-ADC of two neighboring columns.

D. Column-Level SSADC

Fig. 8 shows the schematic of two neighboring column-level SS-ADCs. A double stage comparator is used to reduce the offset [17]. Fig. 9 shows the timing diagram of the whole readout chain. After the reset of the SN, the auto-zeros of the consecutive column-level amplifier and comparators are opened sequentially in order to minimize the impact of charge injection [9]. Then the charges are transferred to the SN and the voltage at the input of the comparator is equal to the difference between the transfer and reset levels. The ramp is then activated together with the counter. Shift registers are used in order to memorise the 10 bit code once the output of the comparators is high. The CDS time is defined by the time between the opening of the AZs and the moment when the output of the comparator is high. During the readout of the next line, the 10 bit codes of all the column-level registers are shifted horizontally to the digital output.

E. Physical Implementation

The chip has been fabricated in a CIS standard 1P4M process (digital: 1.8 V transistors:, analog: 3.3 V transistors, pinned photodiode, color filters and microlenses). The microlenses layer was not used in this work. The chip area is 5mm×5mm. The analog parts of the chip are powered with a 3.3 V source and digital parts with a 1.8 V. Fig. 10 shows a chip micrograph locating the main design blocks. The VGA pixels array meant for a front side illumination occupies an area of 4.16mm×3.12mm. Standard PPDs were used in the pixels array and the area between the even and odd

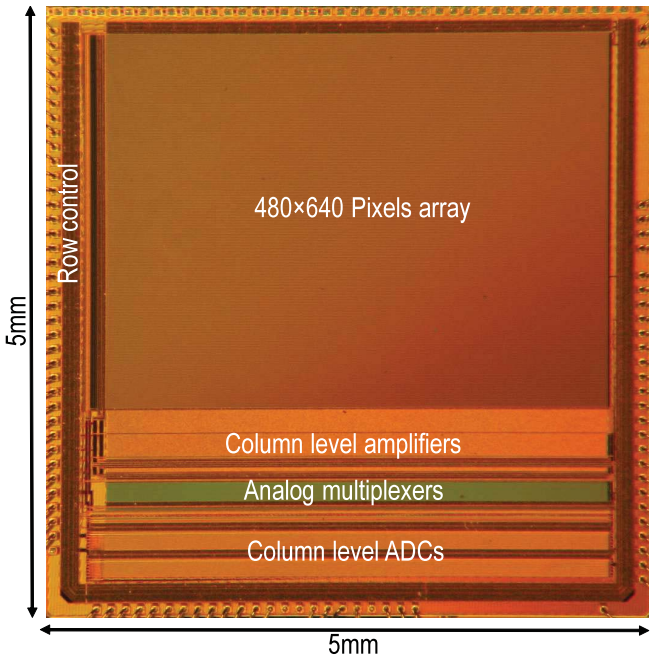


Fig. 10. Chip micrograph showing the main design blocks of the imager.

pixels [Fig. 5(b)] occupied by the in-pixel transistors is covered by a metal layer.

V. Test and Characterization

A. Experimental Setup

In order to test the presented chip, the latter was packaged in a PGA 144. A PCB board has been designed to generate the different bias voltages and power supply ranging from 0 to 3.3 V, control the shape of the (TX) signal and generate the ramp of the SS-ADC. The chip is mounted on the board through a socket over which an optical objective is assembled. the board is powered with an external 5 V source and encompass power supply filters for low noise requirements. The board is connected to a PXI rack with two FPGAs that, on the one hand generate the digital control signals, and on the other receive the digital and analog outputs of the board coming out of the chip. The analog input of the FPGA has an integrated 14 bit ADC with an LSB of about 200 μV. It was used to characterise the pixels using the analog output mode. The FPGAs are programmed with a computer using LABVIEW©. For measurements requiring the variation of the input light, a simple led powered with a low noise tunable voltage source was used. The LED were fixed at the end of a dark tube put on top of the imager.

B. Conversion Gain Measurement

In order to measure the conversion gain of the readout chain, the photon transfer curve (PTC) measurement technique is used [18]. Fig. 12(a) shows the variance versus the signal PTC of the sensor measured from 5000 pixels. It is obtained using the analog output of the sensor and the column-level gain set to 64. The sensor is exposed uniformly to different levels of light provided by the LED and controlled with the voltage source.

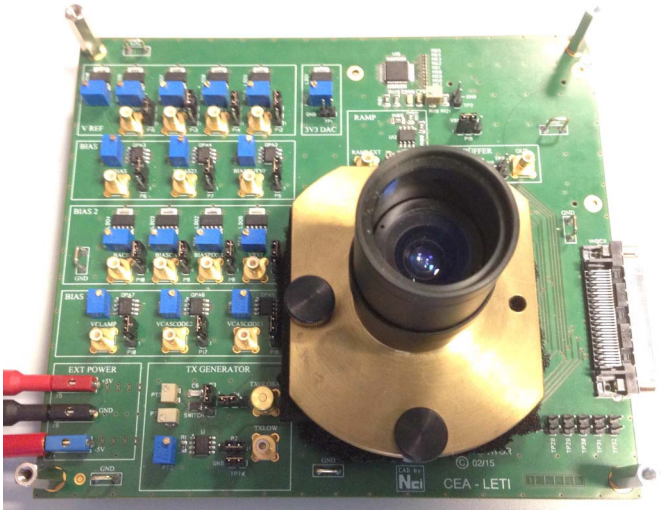
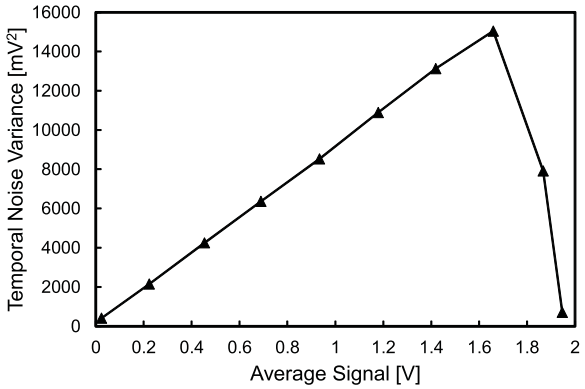
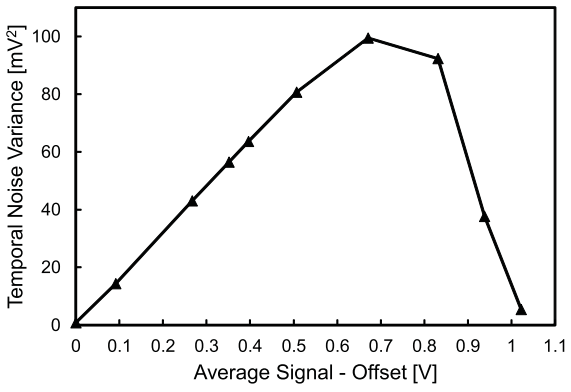


Fig. 11. The designed PCB board and the assembled optical objective used to test the presented image sensor.



(a)



(b)

Fig. 12. Variance versus signal photon transfer curve (PTC) of the image sensor with (a) ×64 column-level gain and (b) ×1 column-level gain.

The variance and mean value are extracted from 100 images for each light level. The PTC curve collapses around 2 V due to the column-level readout chain saturation. The measured conversion gain is 160 μV/e$^-$. It is measured by estimating the slope factor in the linear part of the PTC and dividing it by the measured gain of the readout chain. Fig. 12(b) shows

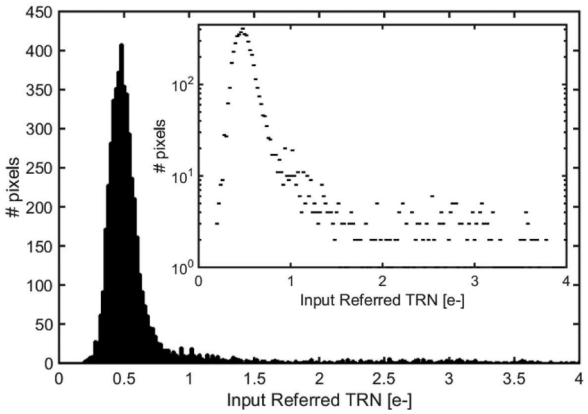


Fig. 13. Input-referred temporal read noise histogram of the image sensor with the vertical axis in linear and log scale (inset).

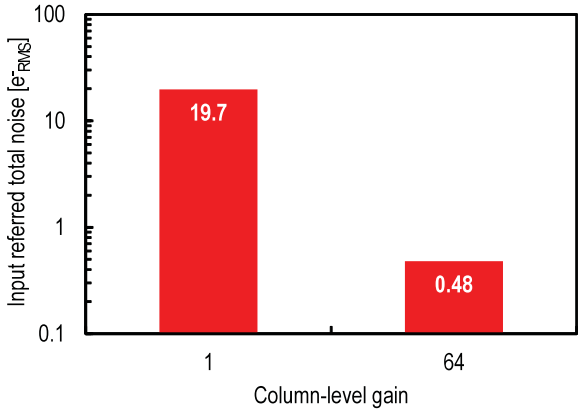


Fig. 14. Measured input-referred noise in the log scale for the two column level gains.

the PTC obtained by performing the same measurement with the column-level gain is set to 1. In this case, the PTC collapses around 1.02 V. This time, the saturation originates from the pixel. This curve allows the measurement of the pixel full well capacity. Using the measured conversion gain of $160\,\mu\mathrm{V/e^-}$ the pixel full well capacity is about $6400\,\mathrm{e^-}$. Typical values of full well capacities for pixels based on photodiodes with similar area are of the order of $10000\,\mathrm{e^-}$, but for conversion gains of about $50\,\mu V/\mathrm{e^-}$. The pixel presented in this work features a higher conversion gain of about $160\,\mu\mathrm{V/e^-}$. The voltage swing of the in-pixel source follower stage is about 1 V, which corresponds to about $6250\,\mathrm{e^-}$ for this particular conversion gain. Therefore, a FWC higher than $6400\,\mathrm{e^-}$ would be unnecessary since it would saturate the source follower stage. This limit can be overcome to extend the dynamic range by reducing the conversion gain when the imager operates in high illumination level [5] [19]. This work does not focus on extending the dynamic range for high signal level but rather by pushing down the noise floor. Now all the noise reduction techniques presented in this work remain compatible with all the techniques used to reach high full well capacities with pixels based on pinned photodiodes [5] [19].

C. Temporal Read Noise

In order to measure the input-referred noise of the presented imager, the output voltage noise is first measured. Then it is referred to the input using the readout chain conversion gain. This operation was applied to 5000 pixels after performing 100 readouts with a CDS of $5\,\mu\mathrm{s}$ and a line (pixel) readout time of $25\,\mu\mathrm{s}$. The in-pixel SF current bias is set to $1.5\,\mu\mathrm{A}$ and the TX is off. The column-level amplifier gain is set to 64, limiting the bandwidth to about 300 kHz in order to reduce the thermal noise and the noise originating from the next stages. Fig. 13 shows the resulting histogram of the input-referred TRN. The golden pixels of the array feature a read noise as low as $0.25\,\mathrm{e^-_{rms}}$. The maximum of the histogram corresponds to $0.48\,\mathrm{e^-_{rms}}$. The inset of Fig. 13 shows the histogram in a log scale highlighting a minority of pixels featuring an RTS noise of a few $\mathrm{e^-_{rms}}$. Note that the noise estimation shown in Fig. 6 takes only into account the $1/f$ noise. The input-referred noise of $0.48\,\mathrm{e^-_{rms}}$ measured at the peak of the noise histogram represents the total noise of the readout chain including the $1/f$ and thermal noise. Additionally, the estimation of the input-referred $1/f$ noise is based on the simulated values of the capacitances connected to the sense node. These values depend on the layout and the process, hence it was expected to obtain values slightly different from the calculation and simulation. Fig. 14 shows the input-referred noise for the two column level gains. It shows a large noise increase in the $\times 1$ gain configuration as the bandwidth becomes much larger (more thermal noise) and all the noise sources after the column-level amplifier are no longer negligible. Thanks to the high column level gain of $\times 64$, the noise originating from the output buffers and analog to digital conversion is completely negligible. For the $1/f$ noise, the contribution of the column level amplifier is negligible compared to that of the in pixel source follower. For thermal noise, the column level amplifier contribution is $0.16\,\mathrm{e^-_{rms}}$ which represents 56% of the total thermal noise and 14% of the total measured noise.

D. Photo-Response Non-Uniformity

This measurement is important in order to verify that the input-referred noise reduction does not come at the cost of higher PRNU. The PRNU represents the spatial variation of the gain. It is given as an RMS percentage. For the presented imager, the PRNU was also measured using the PTC. The optical objective of the imager is removed. The chip is exposed directly to the LED put far enough to have a uniform illuminance for all the pixels array. 5000 pixels exposed to the same level of light with the same exposure time are read 100 times. The average output signal is calculated for each of the 5000 pixels. Then the standard deviation of the spatial variation of the pixels output voltage is plotted in Fig. 15 as a function of the average over time and space of the pixels output signal for different lighting conditions. The curve is linear as expected and the resulting PRNU corresponds to a value of 0.77%.

E. Dark Current

To measure the dark current, the imager is covered protecting it from any light. The chip is set to low column-level

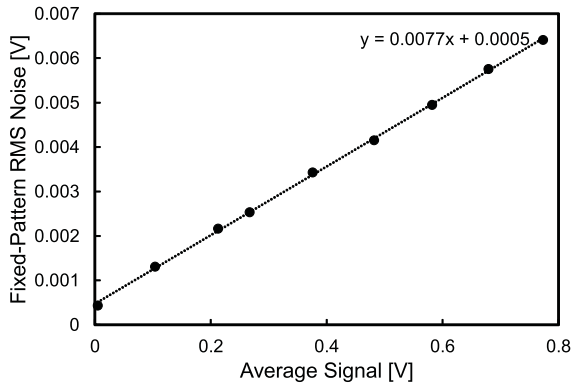


Fig. 15. PTC alike characterization of the fixed-pattern noise or PRNU. The measured value is 0.77%.

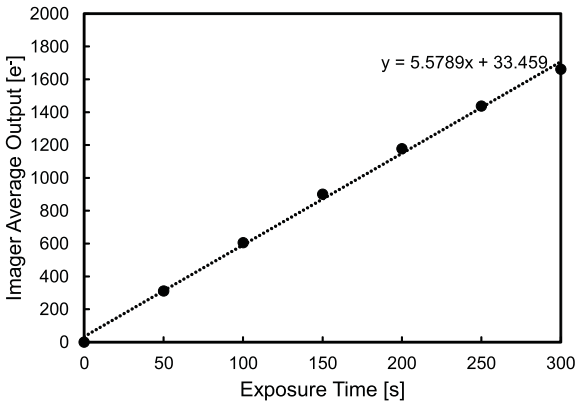


Fig. 16. Measurement of the dark current as the slope of the output versus exposure time curve.

gain mode ($\times 1$). The average output signal of the sensor is measured, at room temperature, for different exposure times. Fig. 16 shows the curve obtained by plotting the measured average output signals of the chip versus the exposure time. For integration times below 300 s, the number of accumulated charges in dark increases linearly with the integration time. The slope factor of the curve indicates a dark current of $5.6\,e^-/s$. Usually, integration times above a few tens of ms are not needed. Based on these measurements, the integrated charge originating from the dark current is not supposed to be more than a few $0.05\,e^-$ which can still be neglected compared to the read noise.

F. Imager Lag

In order to measure the lag, the imager is exposed to a LED with a constant illumination. the imager exposure time is set to 50ms and each pixel is read 2 times. Each line readout takes $20\,\mu s$. The signal from the second readout of the pixel comes from the electrons left in the PPD after the charge transfer in the first readout. The lag is obtained by dividing the signal from second readout over the one from the first readout. The lag was measured with different input light levels. When the PPD accumulates about 2500 photo-electrons the average measured lag was 0.1%. For an average number of accumulated electrons around 5000 the obtained lag increases to about 1%.

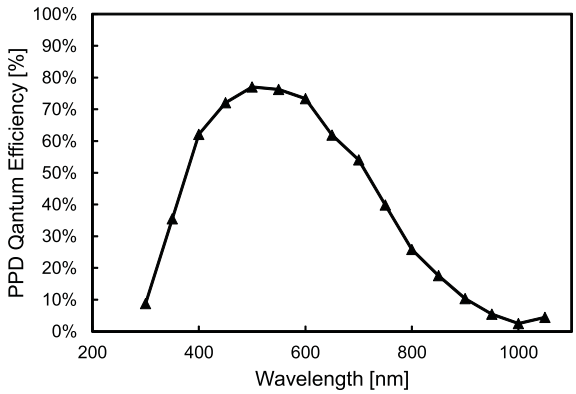


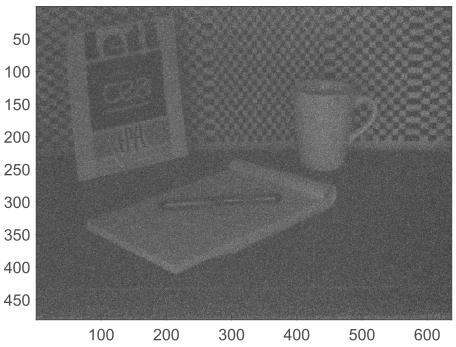
Fig. 17. Quantum efficiency of the PPD (active area) obtained by dividing the QE of the sensor by the fill factor of 40%.

G. Quantum Efficiency

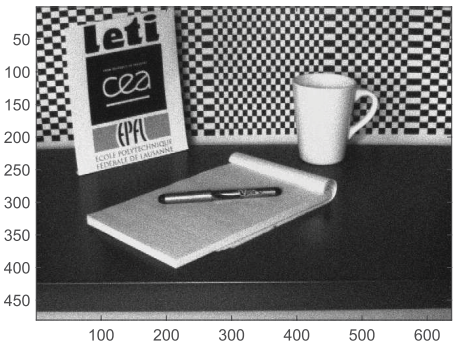
It is important to verify that the n-well containing the PMOS transistors of the pixel does not act as a photodiode competing with the PPD. To this purpose, a measurement of the quantum efficiency (QE) is required. Fig. 17 shows the measured QE of the active area of the imager chip. It is obtained by dividing the effective QE by the pixel fill-factor of 40%. The resulting QE is as good as state-of-the-art PPDs designed exclusively using NMOS pixels. This means that the in-pixel n-well does not compete with the PPD. Furthermore, the micro-lens layer have not been used in this imager. This layer focuses the light at the active area of the pixels and increases the effective QE.

H. Imaging Demonstration

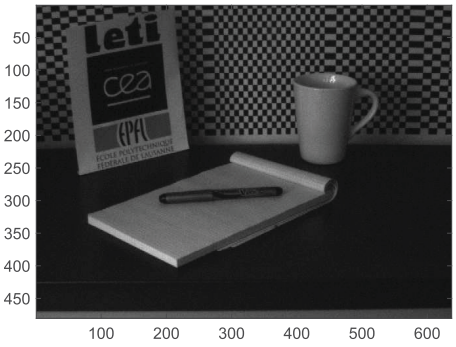
Based on the measured performance, the presented imager is supposed to operate in both low light and normal light conditions. In order to validate this idea, images were taken using the presented image sensor in a dark room with a controlled level of light. The imager was set with an exposure time of 12ms and a frame rate of 84 fps. Fig. 18(a) and (b) show images taken with the chip under different low light levels using the $\times 64$ column gain mode at light levels of 0.005 lux and 0.066 lux corresponding to an average of 3 and 41 photo-generated electrons per pixel, respectively. In Fig. 18(a), the SNR of the input light (limited by the photon shot noise) is below 5 dB. The dominant noise sources are the photon shot noise and the temporal read noise. One can see that even with such a low input light, the objects in the scene can still be distinguished. In Fig. 18(b), the SNR of the input light is about 16 dB. Due to the high column gain, one can see that the image is not far from saturation due to voltage swing of the column-level amplifier. In these conditions, the photon shot noise and fixed pattern noise are supposed to be the dominant noise sources. Fig. 18(c) shows an image obtained at a light level of 0.5 lux corresponding to an average of 320 photo-generated electrons per pixel and the column-level gain set to 1. Here the input SNR is about 25 dB.



(a)



(b)



(c)

Fig. 18. Images of the same scene taken with the presented chip for different amounts of input light. (a) shows the obtained image at 0.005 lux with a column-level gain set to 64 and an average of 3 photogenerated electrons per pixel. (b) at 0.066 lux with the column-level gain set to 64 and an average of 41 photo-generated electrons per pixel. (c) at 0.5 lux with the column-level gain set to 1 and an average of 320 photo-generated electrons.

VI. Discussion and Comparison to State-of-the-Art

The measurement results of the proposed imager, presented in the previous Section, are summarized and compared to recent state-of-the-art works in Table I. Table I shows that the proposed noise reduction technique is efficient. The noise is reduced, as expected, to a record low level of $0.48\,e^-_{rms}$ which is about 1.5 times lower than state-of-the-art [2] and [5] in a full imager with the conventional SF based readout scheme. This record low noise does not come at the cost of a slow readout, a low fill factor or a low SNR. Indeed the line readout time of $25\,\mu s$ is actually 64 and 5.7 times faster than [2] and [5], respectively. A dynamic range of 82.5 dB in the dual gain mode is achieved without using any dynamic range enhancement techniques like lateral overflow capacitance (LOFIC) [5].

The improvements achieved in this work were obtained only by making design choices and careful layout based on a detailed noise analysis [8]. The thin oxide transistor used as an SF is a standard "digital" transistor not optimized for analog applications, thus there is still some room left for process optimization at the SF transistor level. Moreover, (1) suggests that the input-referred noise can also be mitigated by reducing the contribution of all the parasitic, overlaps and junction capacitances to the sense node (C_P). But this approach requires process refinements. Indeed, in [5], the overlap capacitances were reduced by using reset, transfer and gates without low doped drains. In a recently reported work, a mean noise of $0.29\,e^-_{rms}$ was measured on a small array of pixels (12×12), by using a low doped PN junction isolated from the transfer gate as well as a tapered SF [6]. This result came at the cost of a low full well capacity and a relatively higher lag. In [7], $0.27\,e^-_{rms}$ at -10 has been reported by implementing a special implant isolating the FD from the TG (reducing the overlap capacitance) and by replacing the reset transistor by an implant connected to a reset clock. But this was achieved at the cost of a high off-chip reset voltage of 25 V and a low full well capacity of $1500\,e^-$. No characterization has been reported in order to verify the impact of these process modifications on the global performance of the pixels. Note that these process level techniques are compatible with the circuit techniques presented in this work. A combination between the reduction of C_P and using thin oxide SF with optimized gate size is expected to come with even more noise reduction.

VII. Conclusion

This work demonstrates that deep sub-electron noise, in a full VGA APS, can be achieved using a standard CIS process by a proper circuit noise optimization exploiting all the degrees of freedom left to the designer for minimizing the total input-referred noise. The proposed techniques include the following steps: a) introduce enough column level gain to, on one hand, reduce the pixel and column-level amplifier thermal noise and on the other the noise contribution of the next stages, b) design the column-level amplifier with a minimum number of devices large enough to make the residual noise after auto-zero small enough compared to the SF noise, c) replace the conventional thick oxide NMOS SF with a minimum width and optimum length thin oxide PMOS, d) draw a compact layout with common n-well and minimum sense node parasitic capacitance. All these measures result in the best pixels of the full VGA array featuring an input-referred TRN as low as $0.25\,e^-_{rms}$, the majority of pixels peaking at $0.48\,e^-_{rms}$ and a minority of pixels showing an RTS noise of a few electrons. The input-referred TRN is measured without CMS and at

TABLE I
SUMMARY OF THE IMAGER PERFORMANCE WITH COMPARISON TO STATE OF THE ART

Reference	This work	[2]	[5]	[6]	[7]
Circuit level noise reduction techniques	Standard thin oxide PMOS SF and column-level gain	Column-level gain and CMS	Column-level gain	Column-level gain and off-chip CMS	Column-level gain and CMS
Process modifications for noise reduction	Standard process	Buried channel SF	Buried channel SF and process refinements to reduce the SN capacitance	Special potential profile for a FD distant from the TG and tapered reset transistor	Special implants for distant FD from the TG and replacement of the reset transistor by an implant connected to a 25V reset clock voltage
Process	180 nm CIS	180 nm CIS	180 nm CIS	BSI[a] CIS	110 nm CIS
Active array size	640(H)×480(V)	128(H)×198(V)	180(H)×480(V)	12(H)×12(V)	25(H)×512(V)
Pixel size [μm^2]	6.5×6.5	10×10	5.5×5.5	1.4×1.4	11.2×5.6
Fill factor [%]	40	33	48.8	N.R	N.R
Conversion gain [$\mu V/e^-$]	160	45	240	413.4	220
Full well capacity [e^-]	6400	N.R	76000[b]	210	1500
Column-level gain	×1 ×64	×1 ×4 ×16	Dual gain	×8 ×16 ×24	×128
Pixel readout time [μs]	25	1600	143	N.R	N.R
Read noise (peak) [e^-_{rms}]	0.48 @ room T°	0.7 @ room T°	0.74 [c] @ room T°	0.29 @ room T°	0.27 @ -10°
Dark current [e^-/s]	5.6 @ room T°	N.R	N.R	0.1 @ room T°	N.R
PRNU [%]	0.77	N.R	N.R	N.R	N.R
Imager lag [%]	0.1	N.R	N.R	1	N.R

[a]Back Side Illumination
[b]Using a lateral overflow capacitance
[c]The noise reported when the pixel is operated in the source follower configuration.

a short pixel (line) readout time, for a sub-electron read noise CIS, of 25 μs.

This work also provides a full characterization of the VGA imager showing that neither of the dynamic range, the imager lag and the PRNU are compromised with the proposed noise reduction technique. The characterization also shows that the QE of the PPD is not affected by the neighboring PMOS n-wells.

Note that the proposed approach can be combined with any known additional noise reduction techniques at system (e.g. CMS), device (e.g buried channel) and process level (e.g. C_P reduction) to further reduce the TRN.

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Prof. Enz has been a member of several technical program committees, including the IEEE International Solid-State Circuits Conference (ISSCC) and the European Solid-State Circuits Conference (ESSCIRC). He served as a vice-chair for the 2000 International Symposium on Low Power Electronics and Design (ISLPED), exhibit chair for the 2000 International Symposium on Circuits and Systems (ISCAS), and Chair of the technical program committee for the 2006 European Solid-State Circuits Conference (ESSCIRC). He has been elected as a member of the IEEE Solid-State Circuits Society (SSCS) Administrative Commmittee (AdCom) from 2012 to 2014. He is also Chair of the IEEE SSCS Chapter of Switzerland.