A Wideband 20 to 28 GHz Signal Generator MMIC With 30.8 dBm Output Power Based on a Power Amplifier Cell With 31% PAE in SiGe

Benedikt Welp, *Student Member, IEEE*, Karam Noujeim, *Member, IEEE*, and Nils Pohl, *Senior Member, IEEE*

***Abstract*— High-frequency systems such as mm-wave radar transmitters and LO/RF driver chains in vector network analyzers (VNAs) often require the generation of signals with high output power. While these systems benefit considerably from the reduction in size and cost provided by SiGe integration, their output power must be further increased in order to meet the performance of other technologies (e.g., GaAs). To this end, a SiGe signal generator MMIC was developed that achieves 28.7 dBm peak output power with 21.9% PAE and over 27.4 dBm of output power over the whole frequency range from 19.7 GHz to 28.2 GHz. The output power is scalable with DC current up to a maximum of 30.8 dBm. The signal generator is based on a VCO, power amplifier cells (PA cells) and lumped-element Wilkinson power combiners/dividers. The VCO's phase noise is less than −96 dBc/Hz at 1 MHz offset over the entire frequency range. The developed single PA cell achieves a maximum saturated output power P_{sat} of 24.7 dBm with peak PAE of 31%. This article describes the design and performance of all components. The signal generator MMIC has been integrated in an evaluation board together with a PLL, power supply, and serial interface.**

***Index Terms*— High power, *K*-band, MMIC, power amplifier, SiGe, signal generation, VCO.**

I. Introduction

A CHALLENGING requirement in modern high-frequency SiGe technologies is the generation of sufficient output power for use in a variety of applications such as communications, radar, and instrumentation. This requirement is a necessity for SiGe to further extend its benefits of large-scale integration and low cost (i.e., when compared with GaAs, InP, or GaN) to these applications. For instance, high-frequency measurement instruments such as VNAs would be prime beneficiaries of high-output-power SiGe since a highly stable signal source with high output power could be used to drive nonlinear transmission lines (NLTLs) that generate VNA stimulus frequencies in the mm-wave range up to 200 GHz or more [1]. In this work, the goal was to realize a high-power, wideband signal generator chip in SiGe with high PAE in order to reduce the size and cost of frequency-multiplication chains and related components.

Manuscript received February 11, 2016; revised April 15, 2016; accepted May 10, 2016. Date of publication June 10, 2016; date of current version September 1, 2016. This paper was approved by Guest Editor Jean-Baptiste Begueret.

B. Welp and N. Pohl are with Fraunhofer FHR, 53343 Wachtberg, Germany (e-mail: benedikt.welp@fhr.fraunhofer.de; nils.pohl@rub.de).

K. Noujeim is with Anritsu, Morgan Hill, CA 95037-2809 USA (e-mail: karam.noujeim@anritsu.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2016.2570940

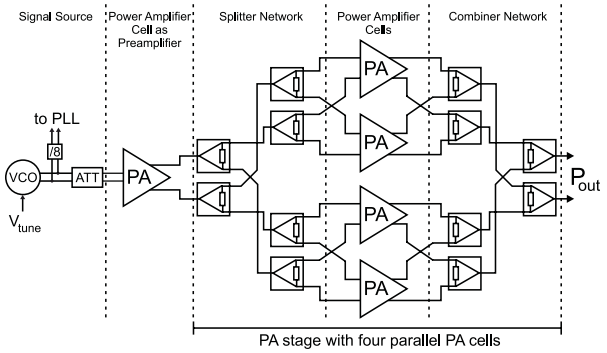


Fig. 1. Block diagram of signal generator MMIC.

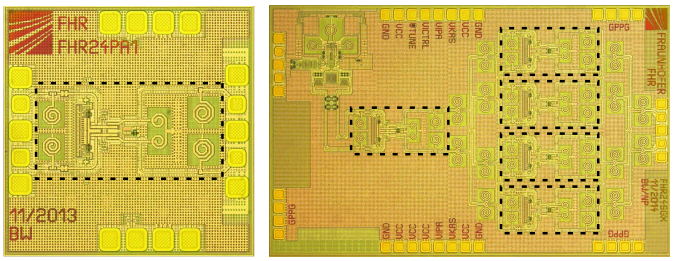


Fig. 2. Photographs of (a) PA cell MMIC (1×1 mm^2). (b) Signal generator MMIC (3×2 mm^2). The dashed areas mark the active PA area of 0.252 mm^2.

The developed signal generator consists of a 24 GHz VCO with a static divide-by-8 section [2] for PLL stabilization, five identical PA cells with one used as a preamplifier to saturate the other four that work in parallel, and Wilkinson power combiners/dividers for the splitter and combiner networks. The 24 GHz VCO in this work is a modified version of the VCO presented in [3] and [4] and is shown in Fig. 1 along with the preamplifier and the PA stage (four parallel PA cells). The system is set up to be completely differential, and all component interconnections consist of transmission lines with 50 Ω characteristic impedance. Fig. 2(a) and (b) shows chip photographs of the PA cell itself and of the complete signal generator MMIC, respectively.

Both MMICs were developed in Infineon's current SiGe production technology (B7HF200) which is based on a 0.35 μm node with an effective emitter width of 0.18 μm, an f_T of 170 GHz, and an f_{max} of 250 GHz. This technology also provides four metal layers which enables the use of low-loss microstrip transmission lines that are shielded against

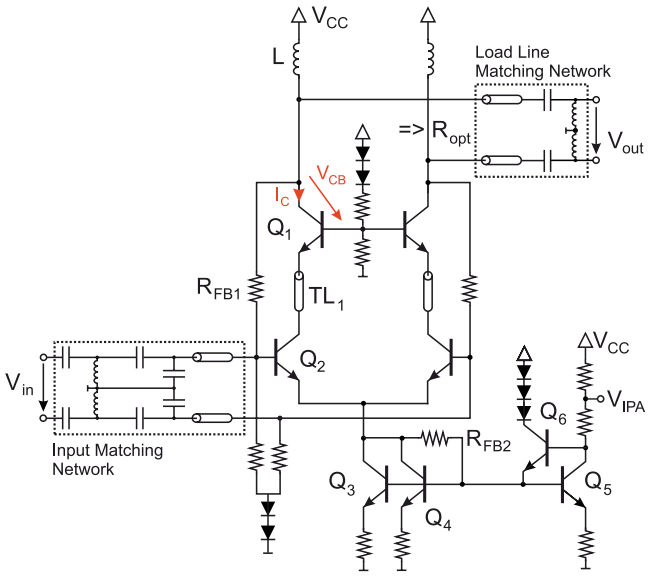


Fig. 3. Schematic of the PA cell architecture.

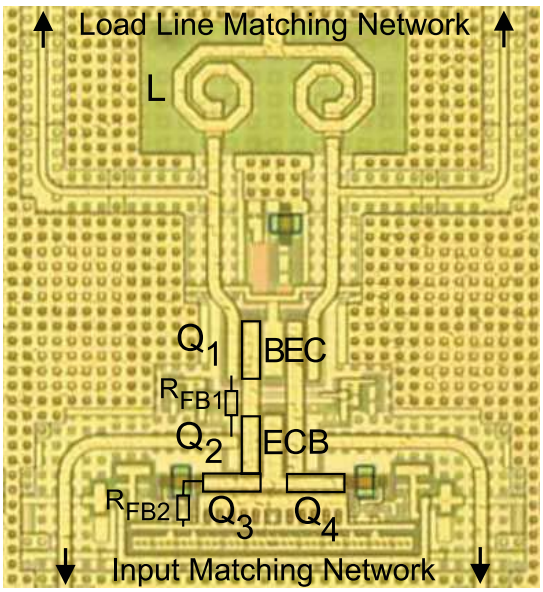


Fig. 4. Layout of the PA cell architecture.

the silicon substrate. This is an advantage especially in high-power circuit design, in particular when compared to many III-V technologies in which unshielded coplanar transmission lines need to be used which interfere with the substrate and introduce more loss because of only one metal layer available.

II. Power Amplifier Cell

A. Architecture

The PA cell's fully differential architecture is shown in Fig. 3. It consists of a common emitter stage Q_2 with a current source Q_3–Q_6, followed by a cascode stage Q_1 which is connected to an inductive load L. Transistors Q_1 and Q_2 consist of five parallel CBEBEBC blocks with 0.35 μm emitter width and 10 μm emitter length. These dimensions were chosen so as to find a good compromise between transistor area and length. The maximum number of base fingers was used to keep the parasitic base resistance and inductance as low as possible. This is very important at the cascode stage which is discussed in Section II-C. The input matching network is designed for wideband operation between 20 and 28 GHz. The output matching network topology selected to achieve the load line transformation is based on a minimum number of components in order to reduce the insertion loss at the PA cell's output. In addition, large valued feedback resistors at the current source (R_{FB2}), and from the output to the input of the amplifier (R_{FB1}) were used to achieve both differential and common-mode stability. This low-loss stacked architecture and its accompanying output matching network are in sharp contrast with multistage transformer coupling or folded architectures but require a high supply voltage of 5 V in this case.

There are multiple effects that limit output power in SiGe bipolar technologies and make it challenging to design efficient PAs with high output power. The avalanche breakdown limit occurs at relatively low voltages in modern SiGe technologies compared with III-V. This is due to the extremely thin base region ($<$ 30 nm) that is needed to obtain high transit frequencies, resulting in a collector-emitter breakdown voltage BV_{CES} of typically 6.5 V, with the base shorted to ground. This voltage decreases even more with a higher load impedance at the transistor base. For transistors with an open base, the breakdown voltage BV_{CEO} is typically 1.7 V. The avalanche-breakdown is most critical at the cascode stage where a high output voltage swing is generated.

It is for this reason that a differential architecture was chosen since it leads to a low-impedance virtual-ground connection at the transistor base of the cascode stage for differential high-frequency signals. Hence, BV_{CES} can be expected for those signals. For the PA layout shown in Fig. 4 in particular, the base interconnection at the cascode stage is most critical because it demands a very low parasitic inductance and resistance in order to handle the high output current, and to ensure stability. The cascode-stage's bases are in close proximity. All high-frequency interconnections in the PA cell consist of 50 Ω or 70 Ω transmission lines and have been part of the simulations.

Another important performance factor is the high-current limit. It degrades the transistor's current amplification factor β and consequently reduces the cut-off frequency [5], [6]. The high-current limit restricts the maximum possible current amplitude $\hat{I}_{\mathrm{out,max}}$, while the avalanche-breakdown limit restricts the maximum possible differential voltage amplitude $\hat{V}_{\mathrm{out,max}}$. In order to achieve maximum output power, it is necessary to reach maximum voltage and current amplitude at the same time. Thus, the inner current sources of the cascode stage transistors must work on an ohmic load. Hence, the inductive load L from Fig. 3 is in resonance with the parasitic collector-base capacitance C_{CB} of the cascode transistors. Finally, the differential 100 Ω load has to be transformed by the output load line matching network to match the optimum load impedance given by

$$R_{\mathrm{opt}} = \frac{\hat{V}_{\mathrm{out,max}}}{\hat{I}_{\mathrm{out,max}}}. \tag{1}$$

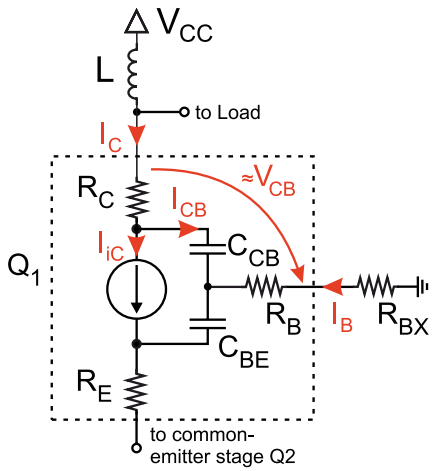


Fig. 5. Simplified standard Gummel–Poon transistor model of one half of the cascode stage Q_1.

In this case, $\hat{V}_{\mathrm{out,max}}$ of 4 V was chosen as a safety margin (theoretical limit 5.7 V of V_{CB} for 0.8 V of V_{BE}) and $\hat{I}_{\mathrm{out,max}}$ is 72 mA. These values were chosen to achieve an output power of at least 21 dBm and result in an optimum load resistance R_{opt} of 55 Ω which was also found to be the best value in the load pull simulations. Therefore, the maximum current through the inner current source is $2\hat{I}_{\mathrm{out,max}}$. It is important to choose a transistor size which is able to handle a collector current density j_C that corresponds to $2\hat{I}_{\mathrm{out,max}}$ and that does not cause high-current limit effects because of excessively high current density. The transistor current density for an optimal f_{T} is 5 mA/μm^2 in the chosen technology. For small signal applications this value can be used for DC current which biases the transistor while for large signal applications such as in this work 3 mA/μm^2 has been chosen as DC bias current density so that the transistor is still able to handle $2\hat{I}_{\mathrm{out,max}}$ (i.e., twice the DC current).

Measurements of different PA versions showed that bypass capacitors at the cascode base had neither measurable influence on the DC biasing potential nor on the output power or PAE. This is because the largest amount of differential output current flows through the collector-base capacitance and thus no rectification of any signals takes place.

B. Dynamic Load Line

The principle of load line matching for this architecture leads to a dynamic load line that shows a resistive load impedance as illustrated in Fig. 6. The dynamic load line can be derived from Fig. 5 for an optimal output power. On the other hand, the current source of the inner transistor Q_1 needs to work on an ohmic load. Therefore, the relationship between I_{iC} and V_{CB} must be linear, and V_{CB} is equal to half of the differential output voltage V_{out}.

To achieve high output power and good PAE, it is important to choose a transistor layout with multiple fingers in order to reduce R_B, R_{BX}, R_C, and R_{E}. The internal series base resistance R_B of the transistors Q_1 is approximately 0.8 Ω in this design which is small versus the impedance of the

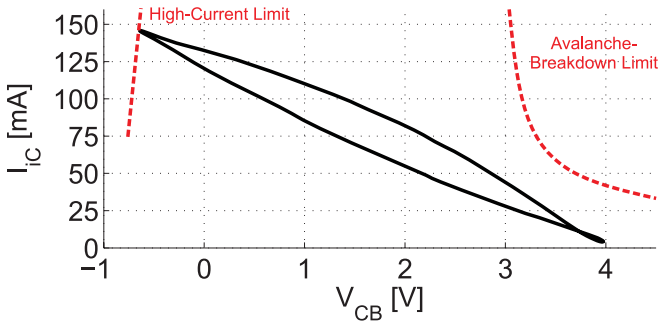


Fig. 6. Simulation of the dynamic load line of the inner transistor current source of the cascode stage at 24 GHz for 169 mA DC current.

collector–base capacitance C_{CB} of about 40 Ω. R_C and R_{E} are even smaller than R_B, and the external parasitic base resistance R_{BX} can also be minimized by appropriate layout. Hence, the current $i_{\mathrm{iC}}(t)$ of the transistors' current source can be calculated using

$$R_{BX,B,C} \approx 0\ \Omega. \tag{2}$$

By neglecting these small resistances, it follows that

$$i_{\mathrm{iC}}(t) = i_{\mathrm{C}}(t) - i_{\mathrm{CB}}(t) \tag{3}$$

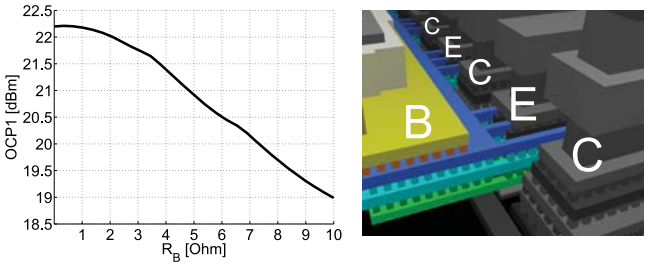
where

$$i_{\mathrm{CB}}(t) = C_{\mathrm{CB}} \frac{\partial v_{\mathrm{CB}}(t)}{\partial t}. \tag{4}$$

The collector–base capacitance C_{CB} was approximated with the area capacitance value of the transistor from the datasheet together with the parasitic capacitance between collector and base from parasitic extraction. Plotting (3) versus V_{CB} results in the dynamic load line of the PA cell for a load-line-matched single-ended output at 24 GHz which is shown in Fig. 6.

The dynamic load line depends on the phase relationship between output current and output voltage swing. In Fig. 6, the inner collector current I_{iC} (which is generated by the transistor's current source) is plotted against the collector–base voltage V_{CB} given the critical nature of these values vis-à-vis the inner transistors [5]–[7]. The nearly linear behavior shows that the transistor's load is mainly ohmic. With a more imaginary load, this curve would get more circular which would increase the likelihood that the dynamic load line will run into the critical high-current limit or avalanche-breakdown limit regions which are marked with the dashed lines that are approximated. Both limits are reversible effects, and therefore the transistors are not destroyed if the dynamic load line runs into those regions but they are degraded and thus the output power decreases.

The transistor model does not contain self-heating and high-current effects but the avalanche-breakdown behavior is modelled by Miller's avalanche multiplication coefficient and is thus part of the simulation. This extended transistor model is extremely important in simulating the cascode stage transistors Q_1 which are biased with a very high collector–base voltage V_{CB} of over 2 V. Due to the influence of impact ionization the high DC voltage of V_{CB} causes a negative base current I_{B} which can change the bias voltage of the



(a) (b)

Fig. 7. (a) Simulated sweep of the base resistance of the cascode stage transistors Q_1 from Fig. 5 and (b) principle of cascode base (colored/left) connection to virtual ground with multiple metal layers.

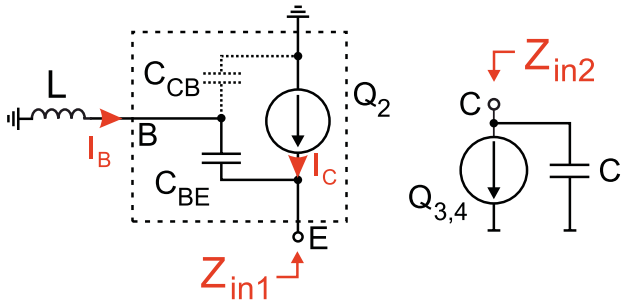


Fig. 8. Input impedance of (a) one half of the differential common-emitter stage Z_{in1} and (b) of the current source Z_{in2}.

cascode stage's base negatively [6]. Besides a low impedance base connection, higher transistor temperature increases the voltage values for the avalanche breakdown even more while f_T decreases [8]. This load-line simulation is a realistic approximation since the real transistor model is much more complex, and thus it is extremely difficult to calculate $i_{iC}(t)$ exactly.

C. Influence of the External Cascode Base Resistance R_{BX} on Compression Behavior

One reason for the importance of a low impedance base connection to virtual ground at the base of the cascode stage is to reach the highest breakdown voltage BV_{CES} (6.5 V) that the transistor is able to handle. Another reason is implied in Fig. 5. The current source of the inner transistor delivers power to the amplifiers load and compensates for the energy lost in the lossy resonant circuit made of L and C_{CB}.

The influence of the swept external base resistance R_{BX} of Q_1 is shown in Fig. 7(a). A 5 Ω base resistance causes a decrease in the 1 dB output compression point OCP1 of 1.2 dB. This resistance determines the quality factor of the collector-base capacitance C_{CB}. Worth mentioning here is also the fact that the quality factor of the load inductance L is equally important. Wide line widths were chosen in the load inductor design to handle the high DC current and to improve its quality factor.

These two aspects (the quality factor of the resonant circuit (L, C_{CB}), and the need for a low impedance virtual ground connection at the base of the cascode stage for maximum BV_{CE}), show the major importance of a low impedance base connection to ground and the advantages of the differential architecture. Both aspects can be optimized by reducing R_{BX} and all other parasitic series transistor resistances R_B, R_C, and R_E. Most single-ended power amplifier architectures with a cascode stage output circuit achieve the base ground connection with big bypass capacitors which always have a series resistance or impedance that is bigger than the metal conductor connection between the bases of a differential cascode stage. This reduces the output compression point and PAE of the power amplifier in many single-ended designs. In order to reduce the parasitic R_{BX}, the transistor base was connected with multiple metal layers which is shown in the outline of Fig. 7(b).

D. Stability

Stability investigations are mandatory in the design of power amplifiers. This is especially so in differential architectures as there is a risk of differential oscillation and also common-mode oscillation, e.g., at the current-source can occur. This can be seen in Fig. 3 in which the circuit can separated into two parts at the common emitter node of Q_2 and with that, the input impedances of both nodes can be calculated.

Fig. 8 shows the separated and simplified schematic of the PA cell used to estimate Z_{in1} and Z_{in2} for stability considerations. The input matching network has an inductive behavior to compensate the capacitive input impedance of Q_2. Thus, the matching network is substituted by L. C_{CB} and the load impedance of Q_2 are neglected for this investigation, and the current source of the power amplifier which consists of the current mirror Q_3–Q_6 is approximated as an ideal current source having a parallel capacitance C which is large for this power amplifier architecture due to the large transistors needed for the high DC current. Also, the series resistors of the transistors R_{BX}, R_B, R_C and R_E are again neglected (they are small for multi-fingered transistor layouts) to simplify the calculation and to get a worst-case scenario. With

$$\beta = -j\frac{\omega_T}{\omega} \tag{5}$$

for high frequencies, it follows that the input impedances are

$$Z_{in1} = -\frac{\frac{\omega_T}{\omega}}{1+\left(\frac{\omega_T}{\omega}\right)^2}\left(\omega L - \frac{1}{\omega C_{BE}}\right) + j\frac{1}{1+\left(\frac{\omega_T}{\omega}\right)^2}\left(\omega L - \frac{1}{\omega C_{BE}}\right) \tag{6}$$

and

$$Z_{in2} = -j\frac{1}{\omega C}. \tag{7}$$

These formulas show that by connecting the nodes of Z_{in1} and Z_{in2} together, the oscillation conditions for a negative resistance oscillator can be fulfilled for particular values of ω, C, L and C_{BE}. The conditions for oscillation are given as follows:

$$\mathrm{Re}(Z_{in1}) < -\mathrm{Re}(Z_{in2}) \tag{8}$$

$$\mathrm{Im}(Z_{in1}) = -\mathrm{Im}(Z_{in2}). \tag{9}$$

There are many approaches to minimize the risk for common-mode oscillation and not to fulfill the oscillation

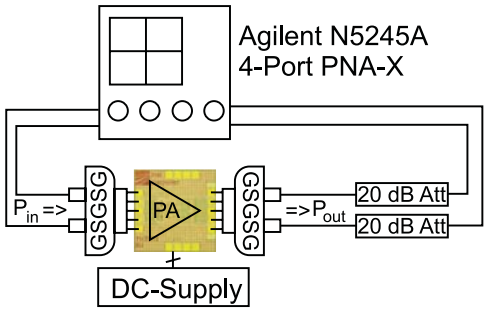


Fig. 9. True differential stimulus measurement setup for the PA cell MMIC.

conditions of this PA architecture. An inductor can be placed in series with Z_{in2} to compensate for C. However, an inductor requires a lot of space and the power amplifier in this design was required to be compact. The solution in this design can be seen in Fig. 3. $R_{\text{FB2}}(200\ \Omega)$ was placed between the collector and the base of $Q_{3,4}$ to degrade the quality factor of C_{CB} for those transistors. If R_{FB2} is too small, $Q_{3,4}$ get self biased and the PA cell cannot be completely turned off by switching V_{IPA} to 0 V. Nonetheless, this design approach performed well in the stability simulation ($K_{\text{f}} > 1, B_{1\text{f}} > 0$) and in reality.

The differential stability for this architecture is most critical at the cascode stage. The reasons for possible oscillation at the cascode stage are the same as those for instability at the current source, and were discussed above. If the cascode base interconnection is inductive, and the common-emitter stage Q_2 loads the cascode's emitter capacitively, there is also a risk for oscillation which is used in the design of the 24 GHz VCO [3]. Therefore, it is important to keep the cascode base interconnection in the layout as short and wide as possible to reduce parasitic resistance and inductance.

There is also a transmission line TL_1 between Q_2 and Q_1 to compensate for the capacitance of Q_2, and additional feedback resistors R_{FB1} which help ensure differential stability. It is important to note that R_{FB1} is about 1 kΩ and does not affect bandwidth, gain, output power, or PAE. In the simulation, parasitic inductances at the cascode base and capacitances at the cascode emitter have been added, and R_{FB1} was integrated to ensure stability even under these harsh conditions. Emitter or base degeneration with series resistance is not an option for ensuring stability neither at the cascode stage Q_1 (because this decreases the output compression point OCP1 and the output power P_{sat} as discussed in Section II-C), nor at the emitter input stage Q_2 (because Q_2 isolates the input from oscillations at the cascode stage and it would also decrease the PA's gain).

E. Measurement Results of the Single PA Cell

The measurement setup in Fig. 9 was used to measure the PA cell. The setup consists of an Agilent N5245A 4-Port PNA-X capable of generating a true differential stimulus to drive the PA cell differentially. The additional 20 dB attenuators serve the purpose to drive the VNA's receivers below their 0.1 dB compression point for accurate measurements.

The comparison between simulated and measured true-differential S-parameters is shown in Fig. 10. The deviation

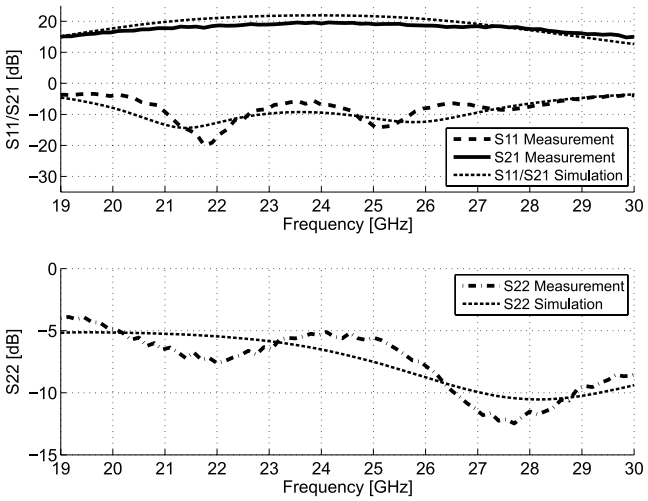


Fig. 10. Simulated and measured differential S-parameter of the PA cell.

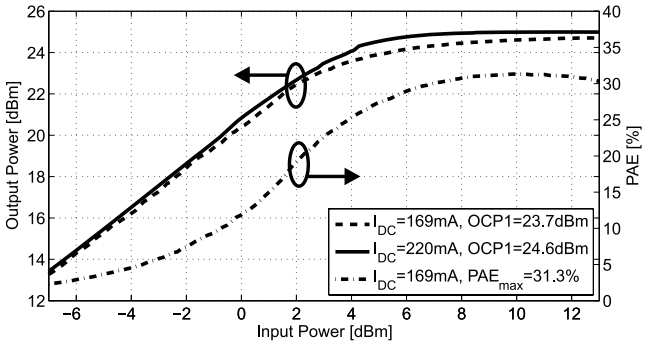


Fig. 11. Measured compression behavior of the PA cell at 24 GHz with 24.7 dBm P_{sat} and 31.3% PAE.

between measurement and simulation is caused by additional transmission lines and pads which have not been de-embedded from the measurement results. The isolation is better than 25 dB over the whole frequency range, and the output load line match also follows the simulated curve.

The PA cell shows a simulated OIP3 and IIP3 at 24 GHz of 23.8 dBm and -0.1 dBm, respectively. However, in our application as a signal generator with a VCO, there are no two-tone input signals. The differential design causes the suppression of the even harmonics of the PA cell output with at least 40 dB, and the third harmonic is at least 25 dB below the carrier. The measured third harmonic of the signal generator is more than 60 dB below the carrier because of the low-pass Wilkinson combiners.

Fig. 11 shows the measurement results of the PA cell's OCP1 of 23.7 dBm, P_{sat} of 24.7 dBm, and PAE of 31% at 24 GHz for a DC current I_{DC} of 169 mA (incl. bias current). This shows that the architecture and the used load-line matching is really able to exploit the theoretical limit of the maximum voltage amplitude $\hat{V}_{\text{out,max}}$ of 5.7 V in a stable operating point. By increasing the PA's DC current up to 220 mA at the V_{IPA} pin (see Fig. 3) the OCP1 rises up to 24.6 dBm with a maximum saturated output power of 25 dBm. This shows that the OCP1 can be increased by nearly 1 dB

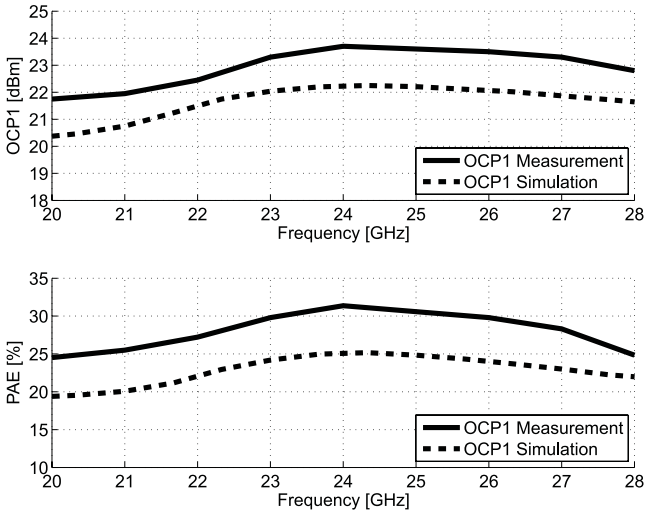


Fig. 12. Comparison between measured and simulated OCP1 (top) and PAE over frequency (below) of the PA cell.

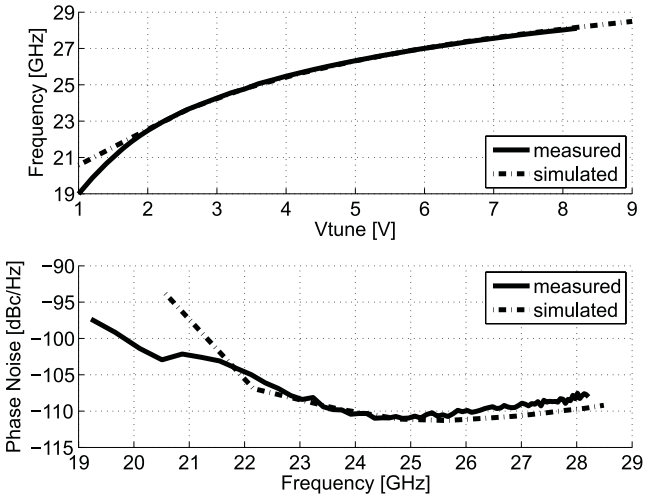


Fig. 13. Measured and simulated tuning characteristic (top) and phase noise behavior at 1 MHz offset (bottom) of the signal generator MMIC.

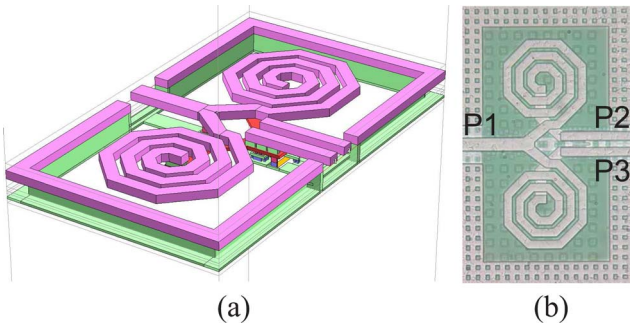


Fig. 14. (a) EM model of the Wilkinson divider and (b) chip layout (0.15×0.26 mm^2).

with DC current while P_{sat} raises only by about 0.3 dB because of the physical high-current and avalanche breakdown limits.

Comparison between the measured and simulated results of the OCP1 and PAE over frequency are shown in Fig. 12. Over the whole frequency range, the measured OCP1 values are about 1 dB higher than the simulated ones. The reason for this mismatch between simulation and measurement is most likely due to the conservative modelling of the transistors (minimum values for BV_{CEO} and BV_{CES} of 1.4 V and 5.8 V, respectively). On the other hand, the fabricated transistors in the measured PA cell offer in all likelihood the typical values for BV_{CEO} and BV_{CES} of 1.7 V and 6.5 V, respectively. This results in a more conservative simulation than real measurements.

In addition the transistors' self-heating is not included in the models but an important aspect in transistor compression behavior. The breakdown voltages BV_{CEO} and BV_{CES} rise at higher temperatures [8] which also explains why the measured PA cell delivers more output power than is predicted by the simulations. This shows the importance of extended transistor models, especially in large-signal and high-power applications.

III. Signal Generator

A. System Design

The signal generator contains a 24-GHz VCO with a static divide-by-8 section for PLL stabilization, one PA cell as a preamplifier in order to drive the PA stage into saturation, and lumped-element Wilkinson power dividers/combiners. The PA stage consists of four parallel PA cells. The block diagram is shown in Fig. 1.

B. 24 GHz VCO

Fig. 13 shows the measured and simulated tuning characteristic of the 24 GHz VCO in the top graph and the measured and simulated phase noise behavior of the complete signal generator in the bottom graph. The VCO itself is able to generate signals from 19.7 GHz up to 28.2 GHz which results in a relative bandwidth of 35.5%.

The measured phase noise is better than -96 dBc/Hz at 1 MHz offset over the whole frequency range, and reaches a minimum phase noise of about -111 dBc/Hz at 1 MHz offset from 24.5 GHz. The measurements match the simulations very well, except for the deviation at low tuning voltages. This is because the model of the differential varactor in the VCO core dynamically leaves the accurately modelled reverse biased region due to the fact that the DC voltage across the diodes in this area is about 0 V.

C. Wilkinson Divider/Combiner

In this design, a lumped-element Wilkinson power dividers were chosen to combine the output power of the four PA cells. It was derived from an ideal Wilkinson divider with quarter-wave transformers and simulated with an EM analyzer [9], [10]. The advantage of the lumped-element Wilkinson combiner is that it requires less space at 24 GHz than one with quarter-wave transmission lines. In Figs. 14(a)–14(b), an image of the EM model and of the final chip layout can be seen.

Port 1 in Fig. 14(b) combines the signals from Ports 2 and 3. The return loss of all ports is below -10 dB from 10 GHz to 33 GHz and is shown in Fig. 15.

The Wilkinson divider was specifically optimized for low insertion loss which is stringently required in this system.

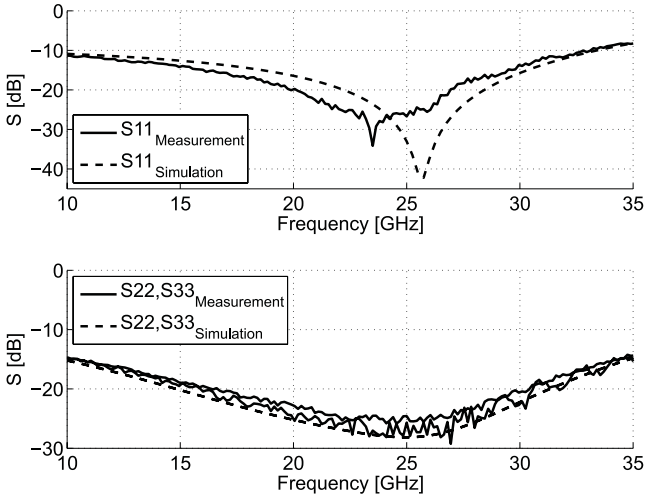


Fig. 15. Measured and simulated S_{11}(top) and S_{22}, S_{33} (bottom) of the Wilkinson divider.

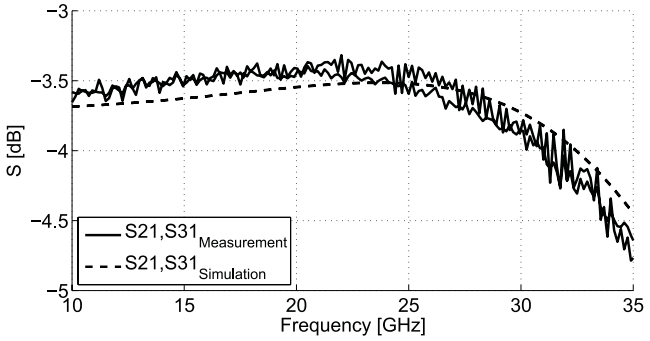


Fig. 16. Measured and simulated S_{21} and S_{31} of the Wilkinson divider.

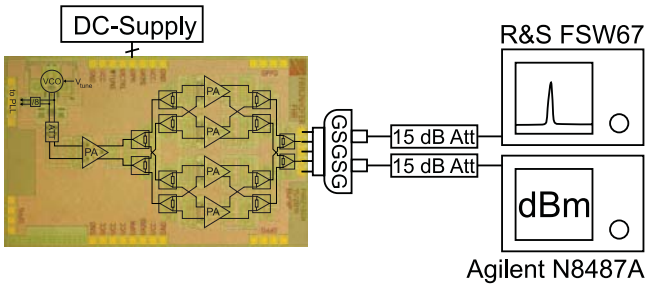


Fig. 17. Measurement setup for the signal generator MMIC.

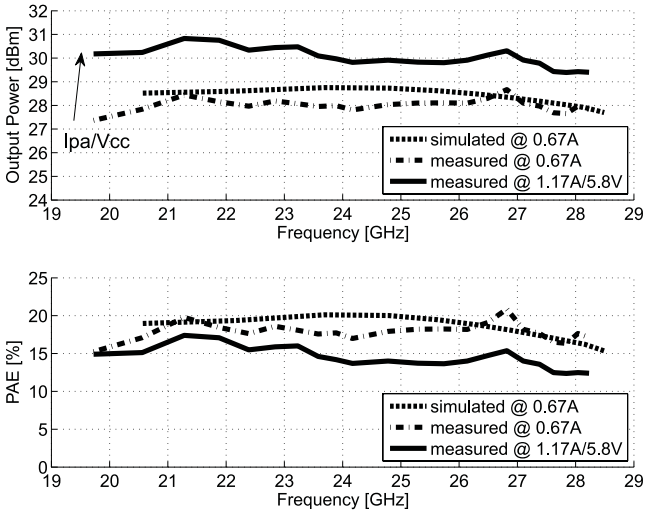


Fig. 18. Measured signal generator output power with variation of DC current (higher current results in higher PA cell OCP1 and higher P_{sat}) and PAE over frequency.

It was achieved by increasing the line width of the inductors and choosing a correct LC ratio, including parasitics of the non-ideal inductors. The insertion loss is plotted in Fig. 16. In the frequency range from 20 GHz to 29 GHz, it reaches a minimum insertion loss of 0.4 dB. The combiner's bandwidth and the correlation between simulation and measurement are very good. The slightly lower center frequency shown in Fig. 15, and the lower cut-off frequency in the S21/S31 measurements are due to the additional transmission lines and pad capacitances in the measurement setup which have not been de-embedded by calibration.

D. Measurement Results of the Power Amplifier Stage

The measurement setup for the signal generator MMIC is illustrated in Fig. 17. The MMIC's output is contacted by a differential probe where one channel of the differential output is guided to an R&S FSW67 spectrum analyzer in order to measure the signal generator's phase noise and tuning characteristic. The other channel of the differential probe is used to transmit the signal to an Agilent N8487A power meter to measure the output power.

In Fig. 18, a simulated peak output power of about 28.7 dBm can be seen in addition to the corresponding curve of the measured PA stage with 0.67 A of DC current at +5 V bias. The achieved PAE of the PA stage (Fig. 1) is 21.9% (Fig. 18). The PAE of the complete system including the preamplifier and the VCO is 17%. The deviation of the measurement from the simulation is caused by neglected losses of the transmission line interconnections between the PA cells and the Wilkinson combiners/dividers (about 700 μm which have not been part of the simulation).

By increasing the PA stage's DC current up to 1.17 A, the signal generator achieves over 29.4 dBm of output power which is very flat in the complete frequency range from 19.7 GHz to 28.2 GHz and 30.8 dBm peak output power at the expense of a drop in PAE to 17.6%.

The presented design is very robust to temperature variations as can be seen in Fig. 19. The signal generator MMIC's output power decreases by about 1.2 dB for a chuck temperature $\vartheta_{\mathrm{Chuck}}$ of 120°C. There are two effects that compensate each other and cause the stability of this design. The transit frequency f_{T} (and therefore β) decreases for higher temperature which is especially a problem in designs that operate near f_{T} at very high frequencies. In this design at 24 GHz this effect is much smaller. Countering this is the transistor breakdown voltage BV_{CE} which increases at higher temperature, enabling the transistors to produce higher output voltages in saturation, and thus higher output power. This shows the good thermal stability of the architecture and as a result, techniques like emitter/base ballasting are not needed.

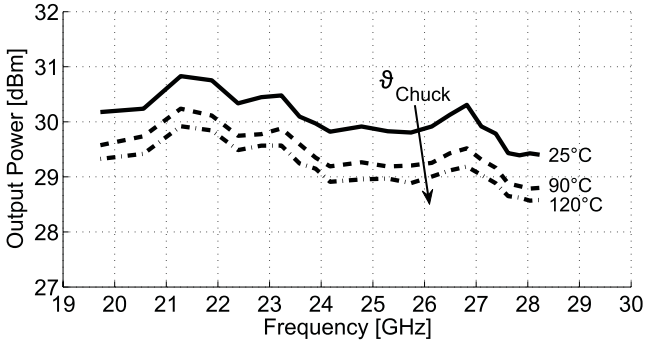


Fig. 19. Signal generator MMIC output power for different chuck temperatures ϑ_{Chuck}.

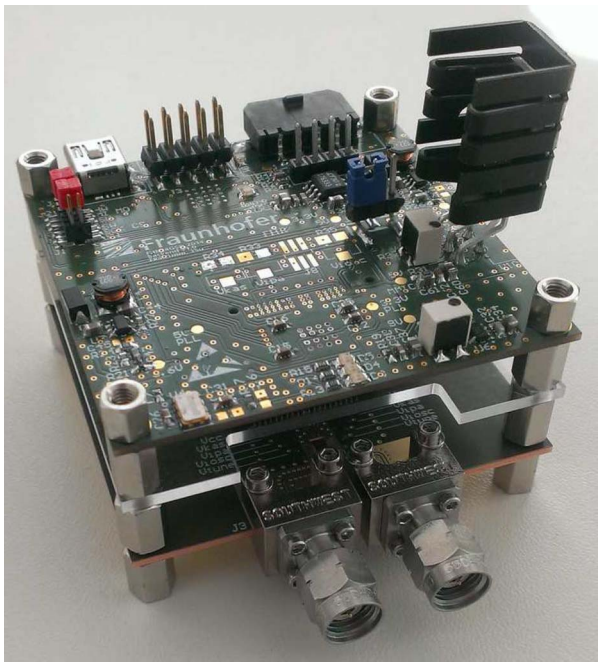


Fig. 20. Evaluation board for the signal generator MMIC together with PLL, power supply and serial interface.

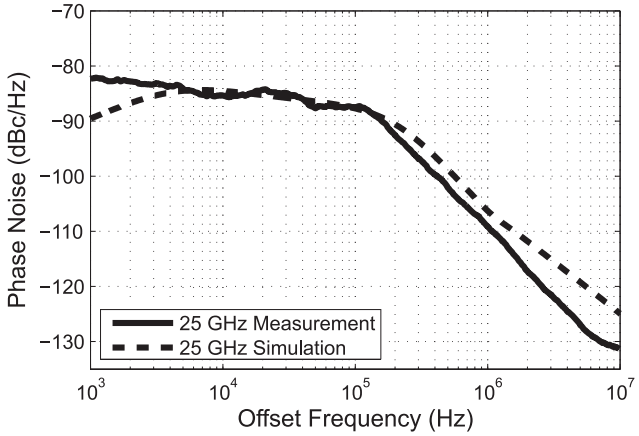


Fig. 21. PLL phase noise performance at 25 GHz from [3].

E. Signal Generator Evaluation Board With PLL

Fig. 20 shows the evaluation board for the signal generator MMIC. It consists of a lower board on Rogers 5880 substrate with 1 mm copper backside metallization and a cavity in which the MMIC is placed to get optimal thermal coupling for cooling. The upper board is a standard FR4 substrate which contains the power supply, the PLL circuitry, and a microcontroller to operate the PLL and the serial interface.

Because of bondwires, transmission lines, and connectors on the evaluation board, the output power is about 3 dB lower than the measured on-chip values. The PLL performance is plotted in Fig. 21. At 25 GHz it is better than −80 dBc/Hz at 1 kHz offset. More about the PLL design can be found in [3].

IV. Conclusion

We have presented the development and measurement of a 19.7 to 28.2 GHz PA cell and its application together with a 24 GHz VCO as part of a signal generator MMIC. Both systems were realized in Infineon's current 0.35 μm SiGe production technology (B7HF200). The standalone PA cell and the signal generator consume 845 mW and 4.35 W respectively from a single 5 V supply voltage V_{CC}, unless otherwise mentioned, with all biasing on chip. All presented measurements were done on-chip except for the results of the evaluation board with PLL stabilization. The on-chip measurements have been verified at a chuck temperature of 25 °C and 120 °C with a decrease of output power of 1.2 dB for the higher temperature.

The PA cell itself is able to reach a maximum saturated output power P_{sat} of 25 dBm, while the signal generator is able to reach over 29.4 dBm of output power with good phase noise performance. The peak output power is 30.8 dBm. All together, five samples of both MMICs, the PA cell, and the signal generator have been measured. All samples showed the similar results in performance within 0.4 dB of variation.

In Table I, the developed PA cell and the PA stage are compared with recently published SiGe, CMOS and HEMT PAs. The mid-frequency and the maximum values of P_{sat}, PAE, and Gain are listed. Considering only the SiGe designs, the combination of high output power and power-added efficiency are very good, and the achieved 31% PAE of the single PA cell together with 24.7 dBm P_{sat} clearly exceeds the state of the art to the best of the authors' knowledge. In addition, the PA stage with its maximum PAE of 21.9% and 28.7 dBm of output power attests to the excellent performance of the design. The high efficiency and output power are the result of a carefully designed stacked differential architecture and a PA output network which compensates parasitic effects of the cascode stage while providing low insertion loss. In particular, the load-line matched differential architecture enables the output transistors to work at their inherent physical limits in order to deliver maximum output power to the load. Furthermore, the designed lumped-element Wilkinson combiner with its low insertion loss of about 0.6 dB plays a major role in generating high output power with good PAE.

Fig. 22 illustrates the results of the different SiGe PA realizations of Table I. The PA cell and the PA stage from this work show an excellent combination of P_{sat} and PAE in comparison with other state-of-the-art PA designs.

The PA stage scales linearly with variations in DC current and supply voltage. Even more output power would be possible

TABLE I
COMPARISON OF SiGe PAs (THE VALUES WRITTEN IN ITALICS FOR CURRENT AND POWER ARE CALCULATED BY OUTPUT POWER AND PAE VALUES)

Ref	Freq. [GHz]	P_{sat} [dBm]	PAE [%]	Gain [dB]	Chip Area [mm^2]	Supply	Technology
This work (PA cell)	24	24.7	31	18.5	0.86	5 V @ 169 mA	0.35 μm SiGe
This work (PA stage)	24	28.7 29.8 30.8	21.9 19.8 17.6	$\approx$16.1	5.37	5 V @ 0.67 A 5 V @ 0.96 A 5.8 V @ 1.17 A	0.35 μm SiGe
[11]	22	23	19.7	19	6	1.8 V @ *561 mA*	0.18 μm SiGe
[12]	24	20	14	12	1.02	5.1 V @ *140 mA*	0.18 μm SiGe
[13]	24	19.4	22.3	37.6	1.1	2.4 V @ *163 mA*	0.18 μm BiCMOS
[14]	27	31	13	20.7	2.83	6.9 V @ *1.4 A*	0.25 μm BiCMOS
[15]	22	20.6	29	37.6	2	2 V @ *197 mA*	0.18 μm BiCMOS
[16]	14	39.5	30	12	11.12	*29.7 W*	AlGaAs/InGaAs/GaAs PHEMT
[17]	23	37	48	16.8	6.8	*10.4 W*	GaN on SiC HEMT
[18]	19	23.8	25.1	22	0.96	2.4 V @ *398 mA*	65 nm SOI CMOS
[19]	15	22.5	24.2	15	0.99	6.6 V @ *111 mA*	45 nm SOI CMOS

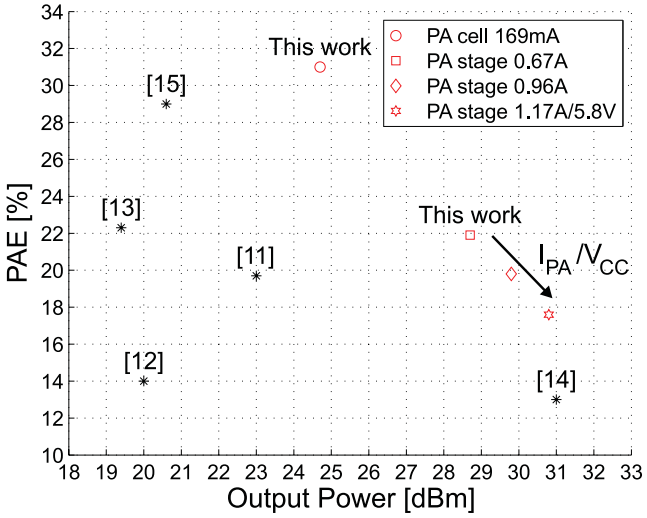


Fig. 22. Comparison with similar SiGe PAs in output power and PAE.

by increasing transistor size and current and scaling the other components, or by extending the parallelization of the developed PA cells which consume only 0.252 mm^2 of active chip area. Scaling transistor size is the better choice in order to reduce the number of stages in the divider, and in particular in the combiner networks so as to keep their total insertion loss as low as possible, provided that the impedance levels inside of the PA architecture do not get too low.

Table I also shows designs in CMOS and HEMT technologies. While CMOS PAs reach similar performance like most SiGe designs, HEMT PAs are able to generate much more output power with very good PAE up to 48% with the Doherty architecture in [17]. The advantages of III–V technologies are clearly excellent efficiency, high output power and low noise. In contrast, disadvantages when compared to SiGe include high cost, poor reproducibility and therefore low yield, making the building of complex systems on one chip cost prohibitive. Furthermore, it is difficult to integrate CMOS circuitry on III–V MMICs, and the thermal conductivity of GaAs and InP is about three times lower than that of silicon. This shows what makes SiGe competitive to III–V technologies. It is cheap, can be produced with very high yield, and offers good reproducibility. This enables the development of complex single chip systems which can also be integrated with CMOS, and where all biasing can easily be implemented on chip with very good repeatability and highly desirable thermal characteristics.

ACKNOWLEDGMENT

The authors would like to thank Infineon Technologies AG and its staff members for fabricating the chips and for helpful discussions.

REFERENCES

[1] K. Noujeim, J. Martens, and T. Roberts, "A frequency-scalable NLTL-based signal-source extension," in *Proc. 41st Eur. Microw. Conf.*, Manchester, U.K., Oct. 2011, pp. 476–479.
[2] H. Knapp *et al.*, "Static frequency dividers up to 133 GHz in SiGe:C bipolar technology," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Austin, TX, USA, Oct. 2010, pp. 20–32.
[3] C. Bredendiek *et al.*, "A 24 GHz wideband monostatic FMCW radar system based on a single-channel SiGe bipolar transceiver chip," *Int. J. Microw. Wireless Technol.*, pp. 1–9, Mar. 2013.
[4] N. Pohl, T. Klein, K. Aufinger, and H.-M. Rein, "A low-power wideband transmitter front-end chip for 80 GHz FMCW radar systems with integrated 23 GHz downconverter VCO," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 1974–1980, Sep. 2012.
[5] M. Rickelt and H.-M. Rein, "A novel transistor model for simulating avalanche-breakdown effects in Si bipolar circuits," *IEEE J. Solid-State Circuits*, vol. 37, no. 9, pp. 1184–1197, Sep. 2002.
[6] M. Rickelt, H.-M. Rein, and E. Rose, "Influence of impact-ionization-induced instabilities on the maximum usable output voltage of Si-bipolar transistors," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 774–783, Apr. 2001.
[7] H. Li, H.-M. Rein, T. Suttorp, and J. Böck, "Fully integrated SiGe VCOs with powerful output buffer for 77-GHz automotive radar systems and applications around 100 GHz," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1650–1658, Oct. 2004.

[8] A. Omprakash *et al.*, "On the potential of using SiGe HBTs on SOI to support emerging applications up to 300°C," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technol. Meeting*, Boston, MA, USA, Oct. 2015, pp. 27–30.
[9] N. Pohl, T. Jaeschke, and K. Aufinger, "An ultra-wideband 80 GHz FMCW radar system using a SiGe bipolar transceiver chip stabilized by a fractional-N PLL synthesizer," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 3, pp. 757–765, Mar. 2012.
[10] P. Davidge and A. Freundorfer, "Converting from distributed to lumped elements," in *Proc. Int. Symp. Signals, Circuits Syst.*, Lasi, RO, Jul. 2013.
[11] T. S. D. Cheung and J. Long, "A 21–26-GHz SiGe bipolar power amplifier MMIC," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2583–2597, Dec. 2005.
[12] J. P. Comeau, J. M. Andrews, and J. D. Cressler, "A monolithic 24 GHz, 20 dBm, 14% PAE SiGe HBT power amplifier," in *Proc. 36th Eur. Microwave Conf.*, Manchester, UK, Sep. 2006, pp. 419–422.
[13] K. Kim and C. Nguyen, "A 16.5–28 GHz 0.18μm BiCMOS power amplifier with flat 19.4±1.2 dBm output power," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 2, pp. 108–110, Dec. 2013.
[14] J. Essing, D. Leenaerts, and R. Mahmoudi, "A 27 GHz, 31 dBm power amplifier in a 0.25 μm SiGe:C BiCMOS technology," in *Proc. Bipolar/BiCMOS Circuits Technol. Meeting*, Boston, MA, USA, Oct. 2014, pp. 143–146.
[15] K. Kim and C. Nguyen, "Design of a K-band power amplifier for high gain, output power and efficiency on 0.18 μm SiGe BiCMOS process," in *Proc. Asia–Pacific Microw. Conf.*, Sendai, JP, Nov. 2014, pp. 594–596.
[16] C. Lin *et al.*, "A fully matched Ku-band 9W PHEMT MMIC high power amplifier," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, San Antonio, TX, USA, Nov. 2006, pp. 165–168.
[17] C. Campbell, K. Tran, M.-Y. Kao, and S. Nayak, "A K-band 5W Doherty amplifier MMIC utilizing 0.15 μm GaN on SiC HEMT technology," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, La Jolla, CA, USA, Oct. 2012, pp. 1–4.
[18] Y. Kawano *et al.*, "A fully-integrated K-band CMOS power amplifier with PSAT of 23.8 dBm and PAE of 25.1%," in *Proc. IEEE Radio Frequency Integr. Circuits Symp.*, Baltimore, MD, USA, Jun. 2011, pp. 1–4.
[19] I. Sarkas, A. Balteanu, E. Dacquay, A. Tomkins, and S. Voinigescu, "A 45 nm SOI CMOS class-D mm-wave PA with > 10 Vpp differential swing," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2012, pp. 88–90.

Benedikt Welp (S'13) received the B.Sc. and M.Sc. degree in electrical engineering and information technology from the Ruhr-University Bochum, Bochum, Germany, in 2010 and 2012, respectively.

Since 2013, he has been with the Department of Millimeter Wave Radar and High Frequency Sensors, Fraunhofer Institute for High Frequency Physics and Radar Techniques, Wachtberg, Germany. His research activities are in the fields of concepts for ultra-wideband signal generation for MIMO radar systems and efficient high frequency signal synthesis with high output power.

Mr. Welp is a member of VDE.

Karam M. Noujeim (S'85–M'98) received the M.Eng.-I degree from McGill University, Montréal, QC, Canada, in 1990, and the M.A.Sc. and Ph.D. degrees from the University of Toronto, Toronto, ON, Canada in 1994 and 1998, respectively.

From January 1990 to September 1992, he was a Member of the Scientific Staff with Bell-Northern Research (Nortel), Ottawa, ON, Canada, where he was involved with the development of computer-aided design (CAD) tools for assessing the susceptibility of printed-circuit boards to electromagnetic interference. From August 1998 to June 1999, he was a Senior Member of the Technical Staff with Stellex Microwave Systems (a divestiture of the Watkins-Johnson Company), Palo Alto, CA, USA, where he was involved in the development of millimeter-wave components for LMDS. In June 1999, he joined the Microwave Measurements Division, Anritsu Company, Morgan Hill, CA, USA, as a Senior Microwave Design Engineer and is currently Technology Fellow and Director. From June to December 2001, he was a Visiting Academic Researcher with the Picosecond Electronics Laboratory, University of California at Santa Barbara, where he was involved with the design, fabrication, and testing of GaAs circuits based on nonlinear transmission lines. From August 2003 to December 2004, he designed and led the prototyping of high-sensitivity micromachined thermal power sensors at the Stanford Nanofabrication Facility (SNF), Stanford, CA, USA. He holds several patents. His current areas of interest include nonlinear-transmission-line structures for use in microwave and millimeter-wave harmonic generation, sampling, reflectometry, imaging, and beam-scanning antennas; miniature frequency extenders for spectrum and vector network analyzers; high-sensitivity sensors for millimeter-wave power measurements and automotive-radar testing; and high-speed signal integrity.

Dr. Noujeim is a member of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES Editorial Review Board.

Nils Pohl (S'07–M'11–SM'14) received the Dipl.-Ing. and Dr.Ing. degrees in electrical engineering from Ruhr-University Bochum, Bochum, Germany, in 2005 and 2010, respectively.

He was a Research Assistant with the Institute of Integrated Systems, Ruhr University Bochum, Bochum, Germany, from 2006 to 2011, where he was involved in integrated circuits for millimeter-wave (mm-wave) radar applications. In 2011, he became an Assistant Professor of Integrated Systems at Ruhr University Bochum. Since 2013, he has been the Head of the Department of Millimeter Wave Radar and High Frequency Sensors at the Fraunhofer Institute for High Frequency Physics and Radar Techniques, Wachtberg, Germany, and additionally in 2015 became a Professor of integrated RF circuits at the Ruhr University Bochum. His main fields of research are concerned with ultra-wideband millimeter-wave radar, design and optimization of mm-wave integrated SiGe circuits and system concepts with frequencies up to 240 GHz and above, as well as frequency synthesis and antennas. He is the author or coauthor of more than 100 scientific papers and has issued several patents.

Prof. Pohl is a member of VDE, ITG, and URSI. He was a co-recipient of the 2009 EEEfCom Innovation Award, the 2012 EuMIC Prize and the 2015 Best Demo Award of the IEEE Radio Wireless Week. In 2013 he received the Karl-Arnold Award of the North Rhine-Westphalian Academy of Sciences, Humanities and the Arts.