A Dynamic Vision Sensor With 1% Temporal Contrast Sensitivity and In-Pixel Asynchronous Delta Modulator for Event Encoding

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***Abstract*—A dynamic vision sensor (DVS) encodes temporal contrast (TC) of light intensity into address-events that are asynchronously transmitted for subsequent processing. This paper describes a DVS with improved TC sensitivity and event encoding. To enhance the TC sensitivity, each pixel employs a common-gate photoreceptor for low output noise and a capacitively-coupled programmable gain amplifier for continuous-time signal amplification without sacrificing the intra-scene dynamic range. A proposed in-pixel asynchronous delta modulator (ADM) better preserves signal integrity in event encoding compared with self-timed reset (STR) used in previous DVSs. A 60×30 prototype sensor array with a 31.2 μm pixel pitch was fabricated in a 1P6M 0.18 μm CMOS technology. It consumes 720 μW at a 100k event/s output rate. Measurements show that a 1% TC sensitivity with a 35% relative standard deviation is achieved and that the in-pixel ADM is up to 3.5 times less susceptible to signal loss than STR in terms of event number. These improvements can facilitate the application of DVSs in areas like optical neuroimaging which is demonstrated in a simulated experiment.**

***Index Terms*—Address event representation (AER), asynchronous delta modulator (ADM), capacitively coupled programmable gain amplifier (CC-PGA), communication delay, dynamic vision sensor (DVS), event encoding, noise, optical neuroimaging, photoreceptor, refractory period, self-timed reset (STR), temporal contrast sensitivity.**

I. Introduction

EVENT-DRIVEN sensors [1]–[9] transform real-world analog signals into asynchronous electrical event sequences. These sensors are used as inputs for either algorithmic [10]–[13] or hardware post-processing [14]–[16] in event-driven neuromorphic systems which are gaining increasing interest in academia and industry for emulating the speed and power efficiency of biological nervous systems in processing sensory information. One such sensor is the dynamic vision sensor (DVS) that encodes temporal contrast (TC) of light intensity into streams of events [1], [6]–[9] which are then transmitted via asynchronous digital circuits, using the so-called address event representation (AER) [17]. Its most significant feature is the pixel-autonomous delivery of sparse output events with sub-millisecond latency, making it suitable for low-power real-time applications in contrast to power-hungry data-redundant conventional APS imagers [18]. For example, a robotic goalie system using a 128×128 DVS showed a mean latency of only 2.2 ms from ball movement onset to generated motor command thanks to the low 20 k event/s (40 kB/s, 16-bit encoding for each event) average event rate [12], whereas a comparable system using an APS imager with the same resolution running at 400 fps would have a raw data rate of 6.6 MB/s (8-bit ADC).

TC sensitivity is an important performance specification of DVSs. It is defined as the detection threshold across which a TC signal can elicit an event. Improving the TC sensitivity is crucial for applications such as fine texture recognition and optical neuroimaging (voltage-sensitive dye imaging (VSDI), fluorometric calcium imaging, etc.). For example, in VSDI, the transient fluorescence signal change is typically below 1% within tens of milliseconds [19], while in calcium imaging the signal is about 10% for a single action potential [20]. Several reported values of minimum TC sensitivity lie around 10% [1], [6], [7], [9]. Setting TC sensitivity smaller than the minimum value results in excessive output noise events, therefore making it difficult to detect any useful visual input of DVSs. A recent design improved the minimum TC sensitivity to 1.5% by incorporating a subthreshold transimpedance preamplifier [8]. Despite the measured 2.1%-2.5% rms equivalent input contrast noise, the minimum 1.5% TC sensitivity in [8] was obtained by averaging the output events over the entire pixel array [21]. Hence a low noise design of the pixel front-end is essential to obtain a reasonable signal-to-noise ratio (SNR) at the sensor output enabling even smaller TC sensitivities.

The in-pixel event encoding mechanism in DVSs has only been the self-timed reset (STR) since their advent [1], [4], [6]–[9]. In STR, the signal change in log intensity since last event is amplified, and a new event is generated when the amplified signal exceeds a comparator threshold. This event generation mechanism was modeled as a time-encoding machine [22] without considering the nonidealities in practical DVSs, such as delays in comparison and arbitration queueing, and switch-holding during the refractory period, which in

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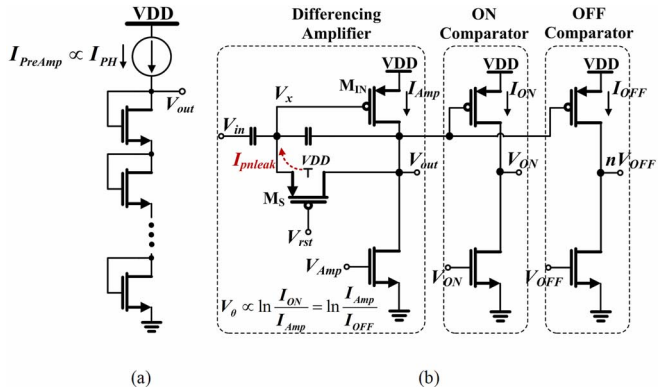

Fig. 1. (a) Preamplifier used in [8] for high TC sensitivity. (b) Typical transistor implementation of STR [1].

principle lead to signal loss. An asynchronous delta modulator (ADM) that uses δ subtraction feedback instead of reset [23] can be used to address the signal loss problem. Unlike the STR, the subtraction in ADM occurs without disturbing the incoming signal. Therefore, an ADM usually results in higher signal-to-distortion ratio (SDR) than STR, especially at high input frequencies and large amplitude-to-quantization-threshold ratios [24]. ADM has recently attracted academic attention in the form of level-crossing ADCs in clockless systems [25]–[27]. DVSs can also benefit from the ADM encoding, particularly when the goal is to reconstruct the temporal signal waveform like real-time video reconstruction [28], [29].

Previous DVS pixels with enhanced TC sensitivity and/or using STR have additional circuit problems, listed here.

1) *Preamplifier headroom*: The preamplifier for high pixel gain in [8] uses a series of diode-connected transistor load as simplified in Fig. 1(a). Ideally, the DC output should be centered at VDD/2 for maximum output swing. However, this circuit topology not only consumes a large voltage headroom but also makes a VDD/2 output DC impossible for all pixels in an array because its bias current I_{PreAmp} is dependent on the local photocurrent I_{PH} in each individual pixel, which can span over several decades. Consequently the intrascene dynamic range (DR) is limited to 60 dB even with a 3.3 V power supply.
2) *Background junction leakage events*: All existing DVSs have undesired background event activity, which is caused by transistor junction leakage in the reset switch. As depicted in Fig. 1(b), the STR implementation uses a common-source differencing amplifier which, after each event address transmission, is reset by shorting the gate and drain of pFET $\mathrm{M_{IN}}$ via the switch $\mathrm{M_S}$. The bulk-source junction leakage of $\mathrm{M_S}$ charges V_x towards VDD when $\mathrm{M_S}$ is off, giving rise to ON background events that are not correlated to visual input. Although these events can be filtered out by simple algorithms [30], they increase the load of post-processing and hence system level power consumption.
3) *Asymmetrical threshold-dependent comparator speed*: The current-mode ON and OFF comparators in many DVS designs are biased with largely different currents I_{ON} and I_{OFF} to create reasonably spaced event thresholds V_θ. For example, $V_\theta = 50$ mV (usually the minimum achievable V_θ constrained by transistor mismatch) leads to $I_{ON}/I_{OFF} = 22$. The resulting low bias current of the OFF comparator causes significant feedback delay that severely limits the encoding SDR.

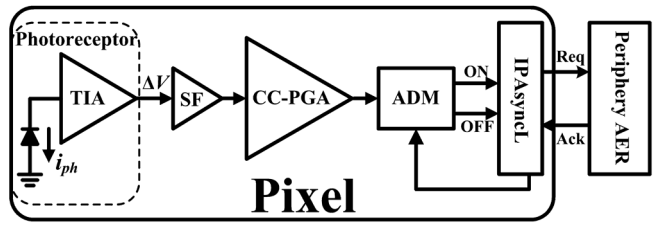

Fig. 2. Building blocks in the proposed pixel including a photoreceptor, a SF, a CC-PGA, an ADM, and IPAsyncL.

This work focuses on the analysis and design of a new low-noise high-gain DVS pixel front-end for improved TC sensitivity, and on the implementation of an in-pixel ADM for event encoding that better preserves signal integrity. The proposed design also addresses the three circuit problems outlined above by the following solutions respectively: 1) Employing an amplifier whose DC output is set to VDD/2 regardless of the local I_{PH}; 2) using a pseudo-resistor for continuous-time feedback; and 3) using two voltage-mode comparators with identical biases. A MATLAB simulation comparison between STR and ADM encoding was presented in a previous conference publication [24].

The remainder of this paper is organized as follows. The pixel design is detailed in Section II. The consideration of the pixel layout and system design is described in Section III. The experimental results are given in Section IV, and the concluding remarks are given in Section V.

II. Pixel Design

The block diagram of a complete pixel is illustrated in Fig. 2. The photoreceptor that is composed of a photodiode and a transimpedance amplifier (TIA) logarithmically converts a small-signal photocurrent i_{ph} into a voltage output ΔV, which is then buffered by a source follower (SF) before it is amplified by a capacitively coupled programmable gain amplifier (CC-PGA). The amplified analog signal is encoded into events by the ADM and the events are transmitted off-chip by in-pixel asynchronous logic (IPAsyncL) and the peripheral AER circuitry. The bias currents of the TIA, SF and CC-PGA are adjustable to control the front-end bandwidth [31]. The gain of the CC-PGA is programmable with 2 bits, and the threshold voltages of the ADM can be adjusted for different TC sensitivity settings. A simplified illustration of the pixel communication with the periphery AER is shown in Fig. 2; in the complete sensor array, the 2-dimensional AER communicates X and Y addresses in a burst-mode word-serial fashion [17].

A. Photoreceptor and SF Buffer

Two types of photoreceptors have been used in DVSs as shown in Fig. 3: One is named as SF photoreceptor (SFPR) because the feedback nFET $\mathrm{M_{3s}}$ and the photodiode form a source follower [1], and the other is named as common-gate photoreceptor (CGPR) because of the common-gate feedback

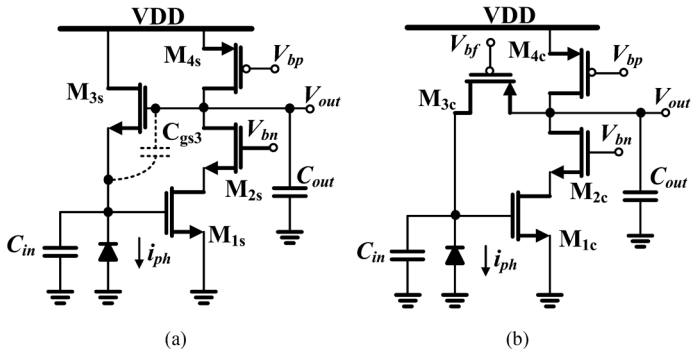

Fig. 3. Circuit diagrams of (a) the SFPR and (b) the CGPR.

TABLE I
COMPARISON OF THE OUTPUT VOLTAGES OF SFPR AND CGPR WITH DIFFERENT i_{ph} CHANGE

	normalized DC gain $V_{out}/(i_{ph}/I_{PH})$	ΔV_{out} (mV) at 10% i_{ph} change	ΔV_{out} (μV) at 1% i_{ph} change
SFPR	U_T/κ	3.05	305
CGPR	U_T	2.59	259
Notes	U_T: thermal voltage, 25.9 mV; i_{ph}: small signal photocurrent; I_{PH}: DC background photocurrent; κ: subthreshold slope factor, 0.8.		

TABLE II
SIZES OF THE TRANSISTORS IN FIG. 3

Device	W(μm)/L(μm)
M_{1s}/M_{1c}	0.24/2.00
M_{2s}/M_{2c}	0.24/0.18
M_{3s}/M_{3c}	0.60/0.20
M_{4s}/M_{4c}	0.24/1.00

pFET M_{3c} [7]. Considering the low noise requirement for enhanced TC sensitivity, the CGPR was chosen because pFETs are often observed to have a lower $1/f$ noise compared to nFETs [32], [33]. As shown by the theoretically-calculated results listed in Table I, for 1% TC detection by a single pixel, the rms integrated output noise should be less than 305 and 259 μV for SFPR and CGPR, respectively.

With the transistor sizes given in Table II and using Cadence Spectre, the simulated output noise for both SFPR $V_{n,outs}$ and CGPR $V_{n,outc}$ within 100 Hz bandwidth are plotted in Fig. 4(a), along with numerically calculated noise using simple noise models [33]. M_{1s}/M_{1c} is a 3.3 V transistor in simulation; otherwise, $V_{\rm out}$ would be too low for M_{2s} in SFPR to stay in saturation at low I_{PH}. A 1.8 V M_{1c} is used in fabrication for CGPR. For small $I_{PH} < 100$ fA, $V_{n,outs}$ and $V_{n,\rm outc}$ are approximately the same because the photocurrent shot noise dominates. As I_{PH} increases, shot noise contribution decreases, and transistor $1/f$ noise becomes prominent. $V_{n,outs}$ saturates to 350 μV at $I_{PH} \approx 50$ pA, still above its 1% TC level. In contrast, $V_{n,outc}$ continues to decrease until $I_{PH} \approx 50$ pA, and saturates at about 50 μV, 7 times lower compared to SFPR. Fig. 4(b) shows the simulated $V_{n,outc}$ as a function of both I_{PH} and pixel front-end bandwidth using a 1.8 V M_{1c}. Larger bandwidth results in increased $V_{n,outc}$ under the same

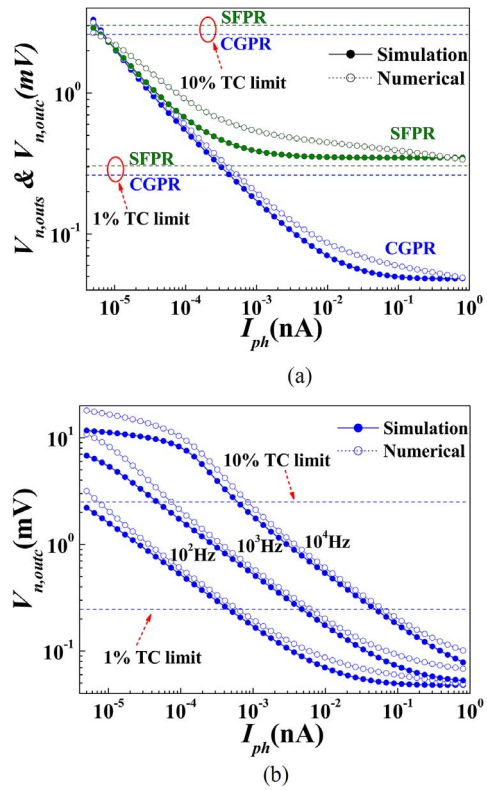

Fig. 4. Spectre-simulated and theoretically calculated (a) output noise of both SFPR and CGPR band-limited within 100 Hz and (b) output noise of CGPR with different pixel front-end bandwidths.

illumination. The plateau of the 10^4-Hz curve is due to the fact that the CGPR bandwidth under low illumination is already less than 10^4 Hz, and thus the integrated noise remains relatively constant. The pixel front-end bandwidth can be controlled by the CC-PGA as will be described in Section II-B.

The CGPR cannot have a large capacitive load in light of the stability requirement for a wide range of I_{PH}. The maximum quality factor $Q_{\rm max}$ can be derived as

$$Q_{\rm max} \approx \frac{\sqrt{\frac{AC_{out}}{C_{in}}}}{2} \tag{1}$$

where A is the open-loop gain of the feedforward amplifier (M_{1c}, M_{2c} and M_{4c}), and $C_{\rm in}$ and C_{out} are the input and output capacitances, respectively, as shown in Fig. 3. If the CGPR is directly connected to the CC-PGA which gives a 380 fF C_{out}, it can easily become unstable due to a large $Q_{\rm max}$. Hence, a SF buffer (Fig. 2) is used so that C_{out} can be kept small for an acceptable $Q_{\rm max}$ that ensures stability. pFETs are used in the unity-gain SF buffer considering the low noise requirement. The additive noise is below 10 μV within 100 Hz bandwidth.

B. Capacitively Coupled Programmable Gain Amplifier

The CC-PGA is shown in Fig. 5. The 2 bits G_1G_0 are used for four-level programmable closed-loop gain control via combinational logic, from 18 dB (00) to 36 dB (11) with a 6 dB step. Note that, when the capacitors $C_{fbi}(i = 0-2)$ are not connected in the feedback loop, their right plates are connected to V_{ref}.

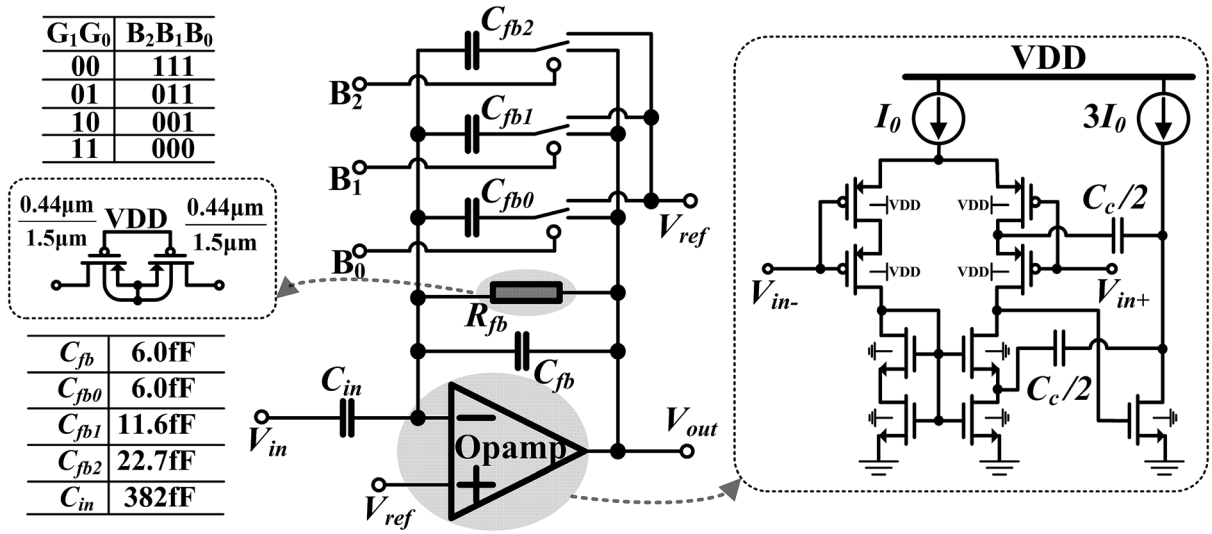

Fig. 5. Circuit diagram of the CC-PGA, including illustration of the pseudo-resistor and the Opamp [37].

Adapted from [34], this configuration prevents frequency response distortion at low frequencies due to finite off-state resistance of open switches, which are avoided in the feedback loop. V_{ref} is set to VDD$/2 =$ 0.9 V for maximum output swing. The feedback pseudo-resistor R$_{fb}$ comprises two off-pFETs in series providing a large resistance [35] so that the high pass corner is low enough not to filter out low frequency visual signals. A two-stage Opamp with pseudo-cascode compensation [36] is adopted for wide output range, low noise, and sufficient phase margin over a wide biasing range. An area-efficient split-transistor subthreshold DC-gain enhancement technique exploiting small-size effects of MOSFETs without body biasing is employed in the Opamp for high open-loop gain and extending the lower-end biasing range [37]. The nFETs in the first stage of the Opamp occupy most of the area to minimize their $1/f$ noise contribution.

The noise of the CC-PGA has a direct tradeoff with its closed-loop gain A_c. Considering only thermal noise, the input referred noise can be approximated by [38]

$$V_{n,ir} \approx \sqrt{\frac{8kT}{3C_cA_c}} \tag{2}$$

where C_c is the total compensation capacitance. With $C_c =$ 32.8 fF, $V_{n,ir} =$ 73 and 202 μV when $A_c =$ 36 and 18 dB, respectively. If a 50 μV noise is contributed by the CGPR, a 6 dB SNR can still be obtained for a single pixel at $A_c =$ 36 dB with a 1% TC signal. Limiting the bandwidth by either lowering the bias current of the CC-PGA or using larger C_c could further improve SNR, but they are limited by voltage headroom and pixel area, respectively.

Instantaneous DR is limited by the output range of the CC-PGA. Let us assume that the range is within 0.2–1.6 V without severe transient output distortion or clipping. At $A_c =$ 18 dB, the input range of the CC-PGA is about 170 mV which allows 57 dB instantaneous i_{ph} change. At $A_c =$ 36 dB, the input range is about 22 mV, which allows only 7.4 dB instantaneous i_{ph} change. In terms of signal integrity, higher gain is at the cost of smaller allowable DR of a dynamic visual scene. However, in the long run, the CC-PGA output will eventually adapt to its DC level of 0.9 V through R_{fb}, and is independent of I_{PH}, therefore the intrascene DR is only limited by the CGPR, in contrast to [8] where the intrascene DR is limited by the transimpedance preamplifier to only 60 dB.

C. Asynchronous Delta Modulator

Area constraint is the main challenge for the design of an in-pixel ADM. Previous implementations of ADMs as level-crossing ADCs often require a large area of resistive or capacitive feedback DACs [25], [26]. The 1-bit capacitive DAC used in [27] can potentially reduce the area, but because of the passive capacitive division, the input signal is attenuated after the DAC. With 36 dB gain from the CC-PGA, the 1% TC is amplified to about 16 mV which is still too small for comparison considering the output DC variation of the ADM amplifier and the input offset of the comparators respectively. The closed-loop gain of the CC-PGA cannot increase much due to limited area available for its input capacitor; therefore additional gain from the ADM is necessary.

The idea of realizing the δ subtraction feedback in ADM was first suggested in [39], but instead of using a full DAC for feedback, a novel asynchronous δ-subtraction switched-capacitor circuit is proposed here for a more area-efficient implementation. As shown in Fig. 6(a), the closed-loop gain of the ADM is determined by $C_{in}/C_{fb} =$ 24 dB, and the Opamp is optimized for slew rate instead of noise. The amplified 1% TC after ADM is about 260 mV, and is detectable by comparators as long as $V_{refh} <$ 1.16 V and $V_{refl} >$ 0.64 V with $V_{ref} =$ 0.9 V. The control signals $\boldsymbol{\varphi}_x(x = \mathrm{s,l,h})$ of switches $\boldsymbol{S}_i(i = 0, 1, 2)$ are generated by the IPAsyncL as described in Section II-D. The switching sequence for ON events is described as follows.

1) When V_{out} exceeds V_{refh}, $\boldsymbol{\varphi_h}$ becomes high, and $\boldsymbol{S_2}$ is connected. The top plate of C_{rst} is charged to V_{refh}. The row request nR_{req} (active low) is communicated to the periphery AER.
2) After a four-phase AER handshake to transmit the row and column addresses of this pixel, the column acknowledge

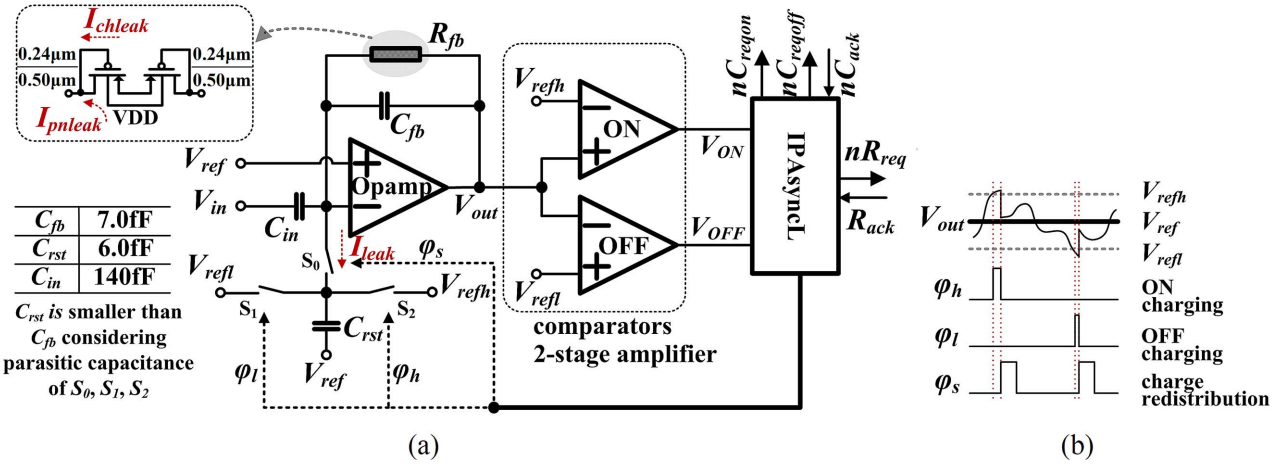

Fig. 6. (a) Circuit diagram of the ADM with illustration of the pseudo-resistor. (b) Timing diagram of the analog output V_{out} and switch control signals φ_h, φ_l, and φ_s.

nC_{ack} (active low) is activated leading to $\boldsymbol{\varphi_h}$ switching low and $\boldsymbol{\varphi_s}$ switching high, and therefore disconnecting $\boldsymbol{S_2}$ and connecting $\boldsymbol{S_0}$. V_{out} is reset towards V_{ref}.

3) After a certain reset time controlled by the IPAsyncL, $\boldsymbol{\varphi_s}$ switches low and $\boldsymbol{S_0}$ is disconnected. The ADM is ready for the next communication cycle.

For OFF events, the sequence is similar except the top plate of C_{rst} is charged to V_{refl} first by connecting $\boldsymbol{S_1}$ via a high $\boldsymbol{\varphi_l}$. The switching sequence is illustrated in Fig. 6(b) for both cases. Following charge conservation, δ that is either $(V_{refh} - V_{ref})C_{rst}/C_{fb}$ or $(V_{refl} - V_{ref})C_{rst}/C_{fb}$ is subtracted from V_{out} for each ON or OFF event [24]. Unlike STR, the voltage subtraction neither discards signals beyond V_{refh}/V_{refl} nor blocks the input V_{in} during the refractory period, and hence better preserves the encoding integrity.

The pseudo-resistor R_{fb} in ADM also needs to have a very large resistance for a sufficiently low high-pass corner frequency, given the small C_{fb}. However, the pseudo-resistor used in the CC-PGA is not suitable because the feedback loop can fail when the pseudo-resistor's PN junction leakage is too small to supply the leakage current of the switch $\boldsymbol{S_0}$. The proposed pseudo-resistor is shown in Fig. 6(a). With two pFETs in diode configuration and the bulk connected to VDD, it supplies both PN junction leakage and channel leakage currents. The connection of the bulk to VDD instead of the source not only prevents forward PN conduction, but also increases the effective resistance. The simulated highpass corner frequency is $<$ 0.25 Hz with $C_{fb} \approx$ 7 fF. The continuous-time feedback via R_{fb} avoids background ON events generated by leakage charging as in prior DVS pixels.

D. In-Pixel Asynchronous Logic

The IPAsyncL communicates with the peripheral AER and generates the switch control signals φ_h, φ_l, and φ_s for ADM. The circuit diagram is shown in Fig. 7(a), and the timing of the main signals is depicted in Fig. 7(b). φ_h or φ_l becomes high in response to active high *ONo* or *OFFo* after some delay controlled by Delay1, and returns back to low once nC_{ack} is active low. φ_s is high if both R_{ack} (row acknowledge, active high) and

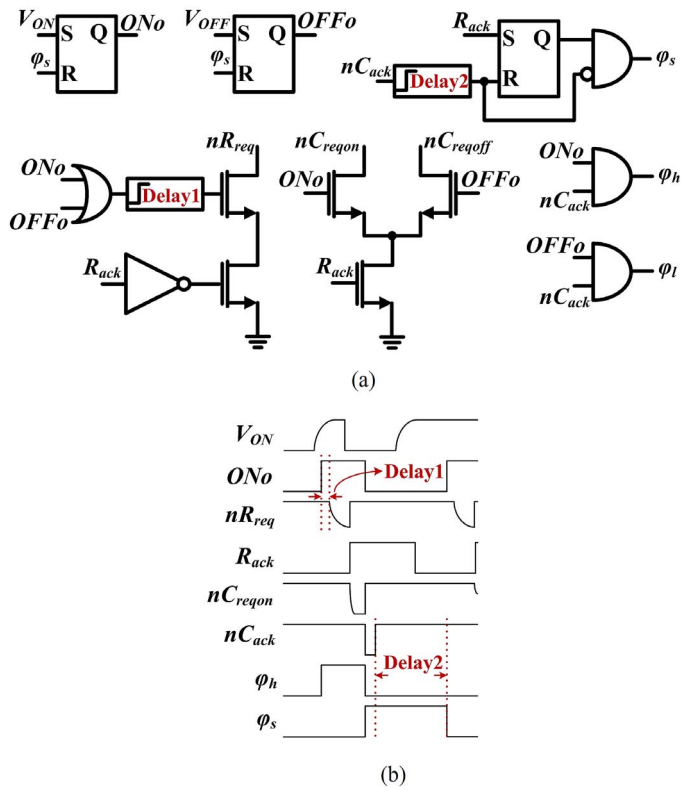

Fig. 7. (a) Circuit diagram of the IPAsyncL. (b) Timing diagram of the relevant signals for an ON event.

nC_{ack} are valid, and becomes low in response to high nC_{ack} after a delay controlled by Delay2. The two rising-edge delay elements Delay1 and Delay2 provide adjustable delay time so that the pulse widths of φ_h, φ_l, and φ_s are sufficient for capacitive charging and charge redistribution of resetting operations in ADM.

III. Pixel Layout and System Design

A 60×30 pixel array prototype named ADMDVS was fabricated in a 0.18 μm RF/MM 1P6M CMOS process. Fig. 8(a) illustrates the system architecture. The addresses of

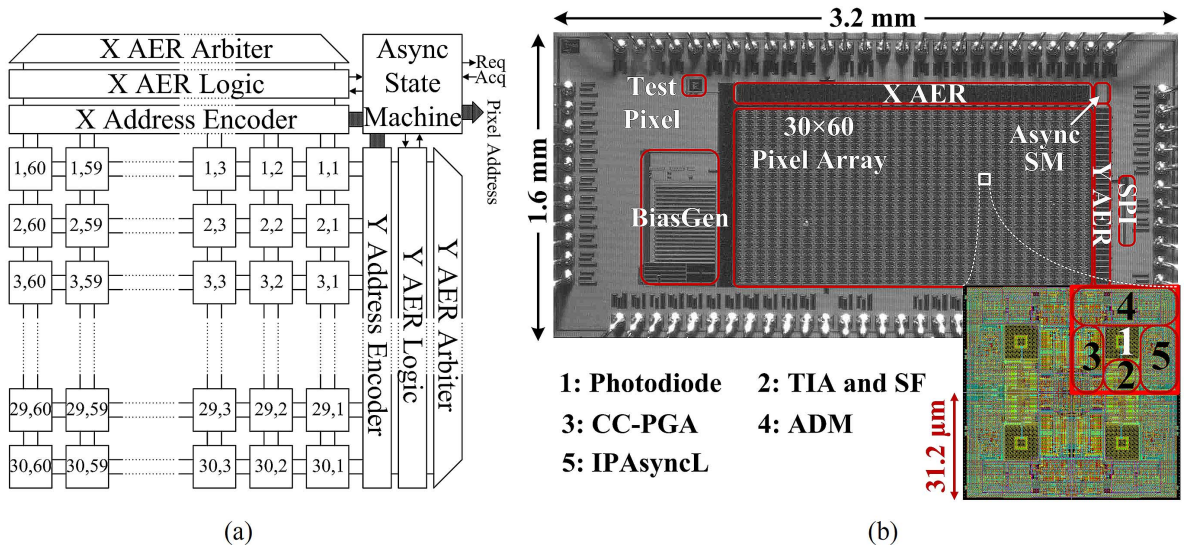

Fig. 8. (a) System-level architecture; (b) ADMDVS chip microphotograph and layout of 2×2 pixels.

active pixels are encoded by the X/Y address encoder and sent off-chip via the 2-D word-serial burst mode AER and the asynchronous state-machine [9], [17]. Fig. 8(b) shows the chip microphotograph and the 2×2 pixel layout arranged in a common centroid. The entire chip including the pads occupies an area of 3.2× 1.6 mm^2. The pixel pitch is 31.2 μm, and the fill factor is 10.3%. The photodiode is formed from a standard n-well/p-substrate structure, and is shielded by a ring of grounded metal wires from Metal1 to Metal6. All analog biases and signals are electrically shielded from digital lines by power or ground metals to minimize transient coupling. The pixel biases are supplied by a digitally programmable bias generator [31] and are used to control the bandwidths of the photoreceptor and the CC-PGA, and the pulse widths of φ_s, φ_h and φ_l. A serial-to-parallel interface (SPI) is used to configure the digital bits for pixel gain control, chip power down and debug. The USB interface, firmware logic, and host side codes in jAER[1] are based on existing designs.

IV. Characterization Results

The following sections discuss the measurement results of noise, TC sensitivity, and event encoding comparison from the fabricated prototype ADMDVS under room temperature. An application demonstration using the ADMDVS for simulated optical neuroimaging is also presented.

A. Noise

Noise performance is important because it determines the minimum TC sensitivity of a DVS. To estimate the average equivalent noise $V_{rms,n}$ at the output of a CGPR, the average noise event rate R_n of the sensor array under DC illumination was measured with the setup shown in Fig. 9. The chip was covered with an infrared blocking filter (IRBF) so that the value measured by the Tektronix J17 photometer approximately reflected the actual illuminance on the pixel array. The tunable light source was a QT-DE12R7s floodlight lamp with 500-W

[1][Online]. Available: http://jaerproject.org

Fig. 9. Experiment setup for measuring the noise of the ADMDVS array.

maximum power. A white Gaussian noise input is assumed for the ADMs in all pixels. Using (7) in the Appendix, $V_{rms,n}$ can be calculated as

$$V_{rms,n} = \frac{R_n \cdot V_\theta}{M \cdot N \cdot 2\sqrt{\frac{2\pi}{3}} \cdot f_{BW} \cdot A_{FE}} \tag{3}$$

where $M \cdot N = 1.8 \times 10^3$ is the total pixel number, $V_\theta (= V_{\text{refh}} - V_{\text{ref}} = V_{\text{ref}} - V_{\text{refl}})$ is the ADM threshold, f_{BW} is the CC-PGA bandwidth, and A_{FE} is the front-end gain including the gain of CC-PGA and ADM. Fig. 10 shows the plot of the measured R_n and calculated $V_{rms,n}$ versus background illuminance $E_{v,BG}$ with the TC threshold set to about 2.4% under two different nominal biases of the CC-PGA (50 pA and 1 nA). At 1 nA bias, the maximum R_n of about 220k event/s occupies a considerable portion of the array's total bandwidth of 10M event/s. Limiting f_{BW} by setting the bias to 50 pA lowers the R_n, and also lowers $V_{rms,n}$, because the noise contributed by CGPRs is further filtered. The $V_{rms,n}$ curves resemble the simulated CGPR output noise in Fig. 3(b). To keep $V_{rms,n}$ less than

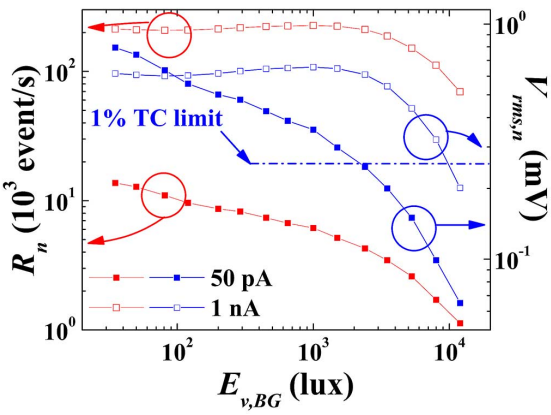

Fig. 10. Measured average noise event rate R_n of the ADMDVS array and calculated average equivalent noise voltage $V_{rms,n}$ at the output of one CGPR with two different bias settings of the CC-PGA, 50 pA and 1 nA.

TABLE III
STIMULUS CONTRAST C_{sti} USED FOR MEASURING THE TC SENSITIVITY OF THE ADMDVS AT DIFFERENT GAIN CODES G_1G_0 OF THE CC-PGA

G_1G_0	C_{sti}
00	1.17
01	0.628
10	0.340
11	0.174

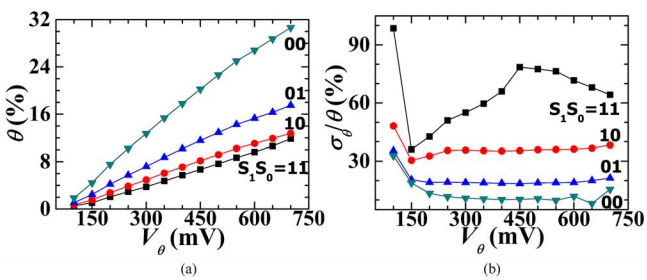

Fig. 11. (a) Measured average TC sensitivity θ of the ADMDVS and (b) measured relative standard deviation of the TC sensitivity σ_θ/θ at different threshold voltages V_θ of the ADM and different gain codes G_1G_0 of the CC-PGA.

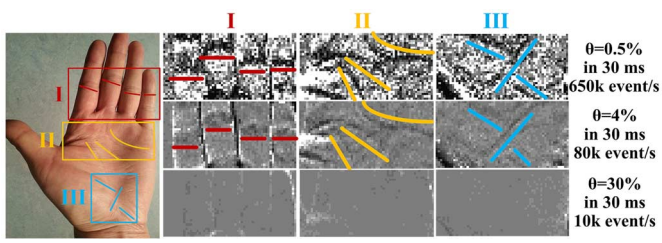

Fig. 12. Effect of different TC sensitivity settings on detecting fine palm lines. The vertically moving hand is divided into three different regions marked as I, II, and III. The ADMDVS is used to detect the lines of each region separately.

the 1% TC limit, $E_{v,BG} > 2.5$ k lux is needed at 50 pA bias, and $E_{v,BG} > 10$ k lux at 1 nA bias. Therefore, to achieve a $< 1\%$ TC sensitivity in a single pixel, low pixel bandwidth and sufficiently high illumination are the two essential factors.

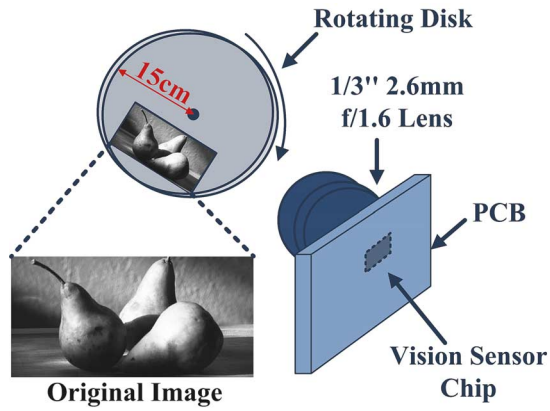

Fig. 13. Testing setup and the original image for the event encoding comparison experiment.

B. Sensitivity

A SST-90 white LED modulated by a sinusoidal signal $V_{sin}(t)$ is used to provide the input stimulus for the chip through an integrating sphere [40]. The peak-to-peak voltage of $V_{sin}(t)$ and DC bias current of the LED determines the stimulus contrast C_{sti}. The different C_{sti} values used for sensitivity testing (listed in Table III) at different CC-PGA gain codes G_1G_0 are used to keep relatively constant output event rate. C_{sti} is calculated as [8]

$$C_{sti} = \ln \frac{I_{\max}}{I_{\min}} \tag{4}$$

where $I_{\max}$ and $I_{\min}$ are the measured maximum and minimum illuminance from the LED. Using the signal event rate R_{sin} of the array in response to the stimulus $V_{sin}(t)$, the average detectable TC threshold, i.e., the TC sensitivity θ can be calculated as

$$\theta = \frac{2M \cdot N \cdot f_{sin} \cdot C_{sti}}{R_{sin}} \tag{5}$$

where f_{sin} is the frequency of $V_{sin}(t)$. To evaluate the standard deviation of the sensitivity σ_θ among all pixels, the signal event rate of each pixel $R_{sin,pixel}$ is used to calculate the sensitivity for each pixel θ_{pixel}, and σ_θ is obtained by applying a Gaussian fit to all θ_{pixel}.

As pointed out in Section IV-A, the noise event rate R_n is quite considerable when the ADM threshold is set small even with a high illuminance, so the actual measured event rate R_{sin+n} under stimulus is due to both the sinusoidal signal stimulus and the noise. Therefore, directly using R_{sin+n} to calculate θ results in overestimated sensitivity. However, with measured R_{sin+n} and R_n, the R_{sin} can be calculated using the following equation (see Appendix) assuming the noise is white and Gaussian:

$$R_{sin+n} = \sqrt{\frac{2}{\pi}} R_n e^{-b^2/4} \times \left[(1.25 + 0.63b^2) I_0\left(\frac{b^2}{4}\right) + 0.63b^2 I_1\left(\frac{b^2}{4}\right) \right] \tag{6}$$

where $b = \sqrt{\pi/2} R_{sin}/R_n$, and $I_v(x)$ (in (6), $v = 0$ or 1, $x = b^2/4$) is the modified Bessel function of the first kind.

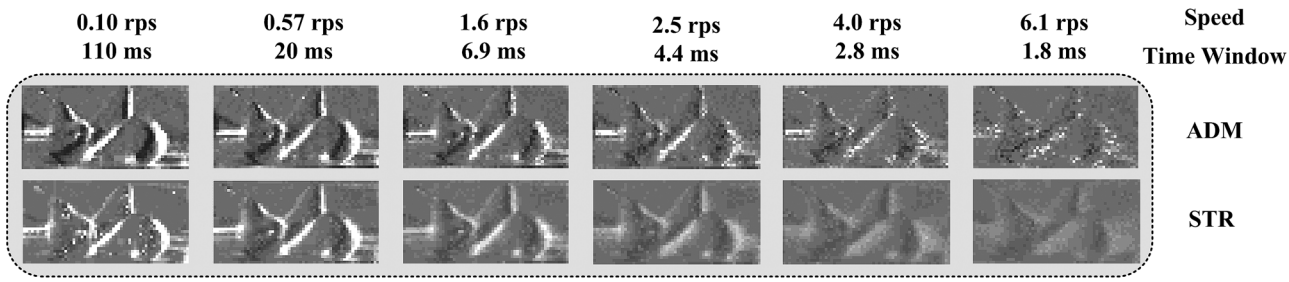

Fig. 14. Comparison of the event-accumulated histogram images acquired by the chip with ADM (ADMDVS) and the chip with STR (DAVIS) [9] at different rotational speeds within time windows which are inversely proportional to the rotational speeds.

The TC sensitivity θ versus V_θ at different gain codes G_1G_0 of the CC-PGA and the corresponding relative standard deviation σ_θ/θ versus V_θ are plotted in Fig. 11. Fig. 11(a) shows that θ increases by less than a factor of two at the same V_θ when G_1G_0 decreases one step, especially from 11 to 10 where θ increases by only $\times 1.25$ on average. This nonideal gain step is because the underestimated parasitic capacitance in the fabricated chips is comparable with C_{fb} in Fig. 5. θ increases relatively linearly with V_θ for all G_1G_0. The minimum measured θ is about 0.54% at $G_1G_0 = 11$ and $V_\theta = 100$ mV; below this V_θ, R_n is too large to detect any visual signal. The obvious penalty of small θ at high gain and low V_θ is the large θ variation as can be seen in Fig. 11(b). For a reasonable $\sigma_\theta/\theta \approx 35\%$, θ is about 1%. At high gains, the feedback capacitance in CC-PGA is small, which causes significant capacitance mismatch and in turn large σ_θ/θ. The mismatch decreases as the capacitance increases, i.e., the gain decreases. At low V_θ, the variation of the ADM amplifier's DC output and the input offset of the two comparators contribute substantially to σ_θ/θ, which is mitigated as V_θ increases because the DC variation and offset become a smaller portion of V_θ.

The effect of different TC sensitivity settings is demonstrated by detecting the fine palm lines of a moving hand under office lighting ($\sim$ 500 lux) as shown in Fig. 12. The hand moves at a speed of about 15 cm/s and it is about 6 cm away from the lens. The experiment was repeated for three different sensitivity settings. The palm lines in different parts of the hand are marked in the original hand image, and also in the accumulated-event histogram images (over a time window of 30 ms for $\theta = 0.5\%$, 4% and 30%) wherever they are visually detectable. It is clear that a small θ setting helps detection of low contrast objects, even though with a larger fixed-pattern noise. On the other hand, a large θ setting can be used to detect the contour of high contrast objects with minimal noise.

C. Event Encoding Comparison

To verify the improved event encoding of the proposed in-pixel ADM over STR, the ADMDVS chip is compared with a DAVIS chip with STR that is previously developed in our group [9], using a moving visual pattern as the input stimulus and a simple histogram reconstruction as output. For a fair comparison between the two chips, we paid attention to the following three factors in the designed experiment.

1) To ensure that the front-end bandwidth is not limited by the photoreceptor, the 500 W floodlight lamp is used to provide additional lighting so that the illuminance at the position of the rotating image is about 4k lux.
2) The front-end bandwidth is set to about 300 Hz by the source follower in STR pixel and the CC-PGA in ADM pixel, respectively, so that the signals fed into the two encoders have approximately the same bandwidth.
3) The cutoff frequency of the amplifiers for event encoding is set to about 500 Hz and the sensitivity to about 15%.

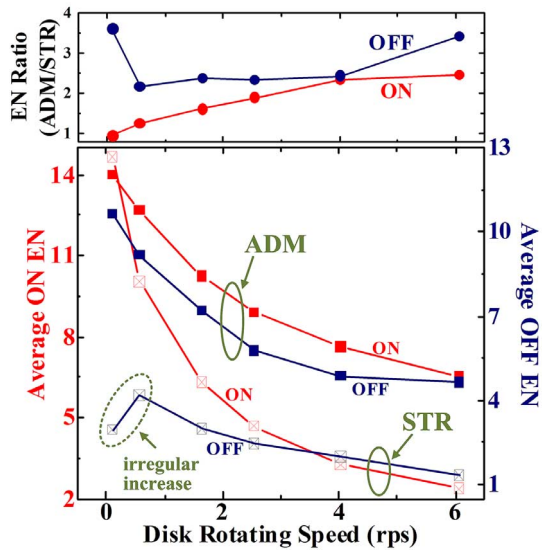

Fig. 15. Comparison of the average number of ON/OFF events (EN = event number) over the 108 brightest/darkest pixels and the EN ratio of ADMDVS over DAVIS.

As illustrated in Fig. 13, the sensors are mounted with a 1/3 in 2.6 mm f/1.6 lens, and a pear image is attached to a disk driven by a motor with an adjustable rotational speed. Because the DAVIS has a 240×180 resolution, a 60×30 region was selected to match with the ADMDVS. The accumulated-event histogram images in Fig. 14 are acquired by the two sensors at different rotational speeds from 0.10 to 6.1 rps within time windows inversely proportional to the rotational speeds. The dark edges in the ADM images are more clearly defined and the bright edges become obscure more slowly as rotational speed increases compared to those in the STR images.

To quantify the encoding improvement, the following method is proposed for comparing the number of produced events from the two sensors. Fig. 15 shows the comparison of the average number of ON/OFF events (EN = event number) from the

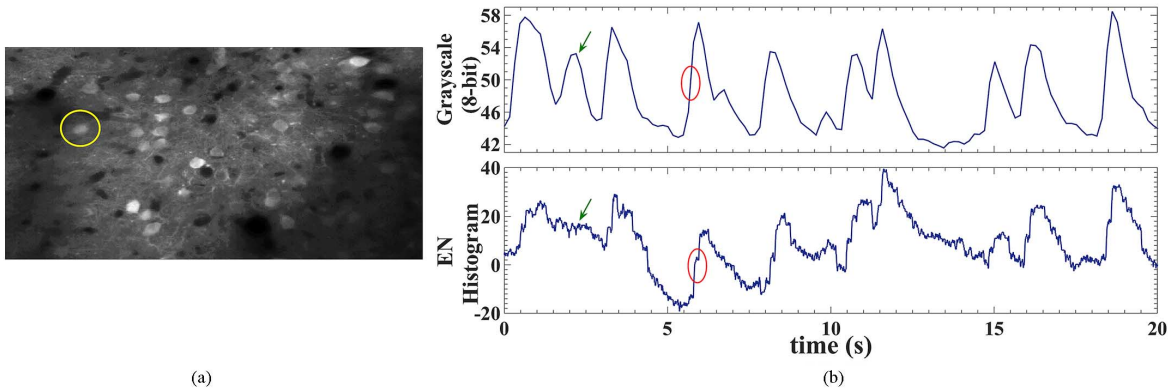

Fig. 16. (a) One frame of the optical neuroimaging video with the target neuron circled in yellow. (b) The temporal waveform averaged over a 5×5 pixel window within the target neuron of the video in (a) (upper plot). The linear signal reconstruction using the output ON and OFF events from one ADMDVS pixel whose visual field covers the region around the target neuron (lower plot).

108 most active pixels of the images in Fig. 14. The number of pixels chosen for EN averaging depends on the percentage of active pixels in the array. Ideally the average ON/OFF EN should stay constant with stimulus speed given infinite pixel bandwidth and instantaneous feedback. However because of the limited 300 Hz analog front-end bandwidth used in this experiment, the average EN in both STR and ADM decreases. Although the average ON EN in STR is approximately the same as that in ADM at 0.1 rps, implying the nearly identical sensitivity setting, it decreases faster with increasing rotational speeds as indicated by the increasing ON EN ratio up to 3 because of signal loss in STR during reset and refractory period. This ON EN ratio increase supports the SDR improvement of ADM against STR in model simulation [24]. The much lower average OFF EN in STR even at low rotational speeds is due to severe signal loss caused by large feedback delay with the threshold-determined low bias of the OFF comparator, and the maximum EN ratio is up to > 3.5. The irregular increase of average OFF EN in STR from 0.1 to 0.57 rps is due to the junction leakage of the reset switch M_S in Fig. 1(b) which tends to cause ON background events. This is eliminated in ADM because of the continuous-time DC feedback.

D. Simulated Optical Neuroimaging Experiment

The prototype ADMDVS is applied to a simulated optical neuroimaging experiment. A fluorescence imaging video recorded from a region in mouse cortex is displayed on a screen and the ADMDVS mounted with the same lens as in Section IV-C is placed in front of the screen. The average illuminance on the chip is about 6.9 lux calculated from the measured screen luminance. The TC sensitivity of the ADMDVS is set to 2.7%. Fig. 16(a) shows one frame of the optical neuroimaging recording. The target neuron circled in yellow is used to demonstrate the effectiveness of temporal signal reconstruction from the ADMDVS output events. The upper waveform in Fig. 16(b) is the grayscale value over time averaged from 5×5 pixels within the target neuron in the video. The lower waveform in Fig. 16(b) is the simple linear reconstruction from the ON and OFF events recorded by one ADMDVS pixel that has the visual field around the target neuron. The corresponding peaks in the two waveforms are evident. The missing peak pointed by the green arrow is likely due to the fact that the ADMDVS pixel may not have the exact visual field of the 5×5 pixels. On the other hand, the rising edge circled in red in the upper waveform has a contrast of 61% calculated according to the measured grayscale-luminance relationship, and the one in the lower waveform is composed of 26 ON events corresponding to a contrast of 69%, well close to 61%. The long-term DC level fluctuation of the peaks in the reconstructed waveform is caused by the unbalanced ON and OFF thresholds of the fabricated ADM circuit.

V. Conclusion and Discussion

The performance of the ADMDVS prototype vision sensor is given in Table IV and is compared with previous DVSs. Although the circuit area of this proposed pixel is approximately three times larger compared with [9], it achieves comparable power consumption per pixel, and a 1% TC sensitivity with a 35% relative standard deviation without sacrificing the intra-scene DR by using an in-pixel CC-PGA. The record TC sensitivity is 0.3% [41], but it was only demonstrated in a single pixel with a very limited pixel bandwidth. The prototype vision sensor also employs an in-pixel ADM for event encoding which has been in MATLAB simulation [24] and here experimentally verified to have a better encoding quality compared to STR. These improvements together with the intrinsic low-latency sparse-output features of DVSs pave the way for applications like wireless *in vivo* optical neuroimaging on free-moving animals, where the energy spent on RF data transmission can be reduced.

For VSDI with signal temporal contrast often less than 1% [19], further improved SNR at a high sensitivity setting is still necessary. One obvious means is to increase the photodiode size. Optimized photodiodes in a dedicated image sensor process with higher quantum efficiency and micro-lenses can be used to obtain higher photocurrent so that shot noise is reduced. Transistors with large L and W help lower the contribution of $1/f$ noise. According to (2), large compensation capacitance and large closed-loop gain can be used to reduce the CC-PGA noise at the cost of pixel area and power consumption.

Although an ADM improves the encoding integrity compared to STR, for real-time high-fidelity signal reconstruction

TABLE IV
ADMDVS PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS DVSS

	This work	2014 [9]	2013 [8]	2011 [7]	2011 [6]	2008 [1]
Technology	0.18 μm MM/RF 1P6M	0.18 μm IS 1P6M	0.35 μm IS 2P4M	0.35 μm MM/RF 2P4M	0.18 μm MM/RF 1P6M	0.35 μm MM/RF 2P4M
Resolution	60×30	240×180	128×128	128×128	304×240	128×128
Chip Area (mm^2)	3.2×1.6	5×5	4.9×4.9	5.6×5.5	9.9×8.2	6.3×6
Pixel Area (μm^2)	31.2×31.2	18.5×18.5[a]	31×30	35×35	30×30[b]	40×40
Fill Factor (%)	10.3	22	10.5	8.7	10[c]	8.1
Supply Voltage (V)	1.8	1.8/3.3	3.3	3.3	1.8/3.3	3.3
Power (mW)	0.72[d]	14[e]	4[d]	145[d]	175[e]	24[f]
Power/Pixel (μW)	0.40	0.32	0.24	8.8	2.4	1.5
Min. TC Sensitivity (%)	**1**	11	1.5	10	13	17
DR (dB)	130[g]	130	120	100	N.A.[h]	120
Intra-Scene DR (dB)	**130**	130	60	56	N.A.	120
Event Encoding	**ADM**	STR	STR	STR	STR	STR

a. Including 4T APS; b. Including PWM imaging circuits; c. Only DVS photodiode; d. At 10^5 event/s; e. High activity, including the imaging functionality; f. Non-optimized power-consuming biasgen; g. From about 0.03 lux to >100k lux; h. Only DR of PWM imaging given.

[28], [29], the problems of sensitivity variation among pixels and unbalanced ON and OFF thresholds remain. They could be addressed at the circuit level by using larger transistors and capacitors with increased pixel size. A novel encoding mechanism might give an area-efficient solution. For example, a threshold-variation-insensitive decoding algorithm was developed for the asynchronous sigma-delta modulation (ASDM) [42], although the ASDM generates idle output without any input signal change and thus results in a much more limited pixel bandwidth.

APPENDIX

Let us assume a white Gaussian noise input $x_n(t)$ that has zero mean, rms value $V_{rms,n}$, and bandwidth $f_{BW,n}$, then the output event rate R_n of an ADM can be derived as [23]

$$R_n = 2\sqrt{\frac{2\pi}{3}}\frac{f_{BW,n}\cdot V_{rms,n}}{\delta} \tag{7}$$

where δ is the ADM threshold. For a sinusoidal input $x_{sin}(t)$, the output event rate R_{sin} is

$$R_{sin} = 4\sqrt{2}\frac{f_{sin}\cdot V_{rms,sin}}{\delta} \tag{8}$$

where f_{sin} is the signal frequency, and $V_{rms,sin}$ is the rms amplitude.

Let $x_{sin+n}(t) = x_{sin}(t) + x_n(t)$ represent the sum of a sinusoidal signal and a white Gaussian noise. Based on the joint probability density function $p(x_{sin+n}, x'_{sin+n}, t)$ of the signal amplitude x_{sin+n} and its slope x'_{sin+n} at time t [43], and combining (7) and (8), the output event rate R_{sin+n} of an ADM with an input of $x_{sin+n}(t)$ can be derived as

$$R_{sin+n} = \sqrt{\frac{2}{\pi}}R_n\int_0^{\pi}[\varphi(b\sin\theta) + b\sin\theta\int_0^{b\sin\theta}\varphi(x)dx]d\theta \tag{9}$$

where $\varphi(x) = 1/\sqrt{2\pi}e^{-x^2/2}$, and $b = \sqrt{\pi/2}R_{sin}/R_n$.

With measured R_{sin+n} and R_n, by numerically solving (9) (which contains tabulated functions in the integral), R_{sin} can be obtained. Equation (3) can be easily derived from (7), and (6) is the numerically integrated version of (9) for faster computation.

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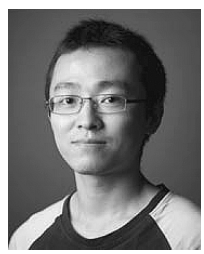

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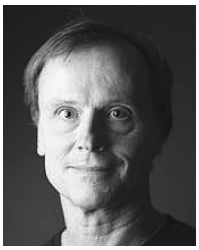

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