A mm-Sized Implantable Medical Device (IMD) With Ultrasonic Power Transfer and a Hybrid Bi-Directional Data Link

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***Abstract*—A first proof-of-concept mm-sized implantable device using ultrasonic power transfer and a hybrid bi-directional data communication link is presented. Ultrasonic power transfer enables miniaturization of the implant and operation deep inside the body, while still achieving safe and high power levels (100 μW to a few mWs) required for most implant applications. The current implant prototype measures 4 mm $\times$ 7.8 mm and is comprised of a piezoelectric receiver, an IC designed in 65 nm CMOS process and an off-chip antenna. The IC can support a maximum DC load of 100μW for an incident acoustic intensity that is $\sim$5% of the FDA diagnostic limit. This demonstrates the feasibility of providing further higher available DC power, potentially opening up new implant applications. The proposed hybrid bi-directional data link consists of ultrasonic downlink and RF uplink. Falling edge of the ultrasound input is detected as downlink data. The implant transmits an ultra-wideband (UWB) pulse sequence as uplink data, demonstrating capability of implementing an energy-efficient M-ary PPM transmitter in the future.**

***Index Terms*—AC-DC converter, active rectifier, antennas, bi-directional data communication, CMOS, IMD, implantable biomedical devices, mm-sized implants, piezoelectric receivers, radio transmitters, ultrasonic power transfer.**

I. Introduction

WIRELESSLY POWERED, highly miniaturized implantable medical devices (IMDs) can play a crucial role in eliminating the invasiveness and discomfort caused by batteries and wires in most traditional implants [1], [2]. Miniaturization of implants to mm and sub-mm dimensions can also open up the possibility of having a network of sensor nodes in body for applications such as multisite neural recording and stimulation [3], [4]. However, there exists the engineering problem of efficiently delivering hundreds of μW to a few mWs, to depths near $\sim$10 cm in body, for miniaturized implants in demanding applications such as: deep brain stimulation (DBS) [5], [6], optogenetics and peripheral nerve stimulation [7]. Besides powering of the implant, many applications would benefit from a bi-directional communication link for control functions and data uplink, and all of this functionality needs to be implemented into a small package for practicality. This paper demonstrates a new wireless power transfer and bi-directional data communication technology for a proof-of-concept miniature deep-tissue implant.

Conventional wireless powering techniques such as inductive coupling and RF power transfer are inefficient for large range-to-implant-size ratio [8]–[11]. Also, inductive powering is more sensitive to mutual orientation of coils as compared to far-field techniques [9], [11]. The inefficiency of RF power transfer in the body is due to mismatch between the wavelength ($\sim$ cm) and aperture of mm and sub-mm sized antennas, and the absorption of RF waves in tissue. The available power from such electrically small antennas is low due to a low radiation efficiency, small radiation resistance, large antenna quality factor (Q) [12], and losses in typical matching networks from limited Qs of on-chip inductors and capacitors [13]. Another major drawback of the large RF wavelength is that energy cannot be focused to a mm or sub-mm spot size [14], resulting in excessive heating, safety concerns, and low overall link efficiency. Other techniques such as ambient energy scavenging offer inadequate power densities [15] for applications such as DBS.

We use ultrasound for power transfer [16] since it has significantly smaller wavelength, comparable to miniature implant dimensions, due to orders-of-magnitude slower sound wave velocity. Smaller wavelength enables efficient focusing of energy at the implant as well as significantly improved coupling and transduction efficiency. The feasibility of beam-forming ultrasonic energy to mm-sized focal spots at large depths in body, in a controlled and programmable way, and without exceeding safety limits in surrounding tissue, has already been demonstrated [17]–[19]. Moreover, it is feasible to design miniature ultrasonic receivers with impedance profiles that allow for more efficient power transfer as compared to electrically small antennas, as discussed later in this paper. In addition, the FDA allows an intensity of 7.2 mW/mm^2 for diagnostic ultrasound applications [20], which is about two orders of magnitude higher than the safe RF exposure limit in body (10–100 μW/mm^2 [21], [22]). Fig. 1 shows a conceptual diagram of the regimes of applicability of different wireless powering techniques, with ultrasound being favorable for transferring high power levels to miniature, deeply implanted medical devices.

In addition to ultrasonic power transfer, we present the first demonstration of a hybrid bi-directional data communication

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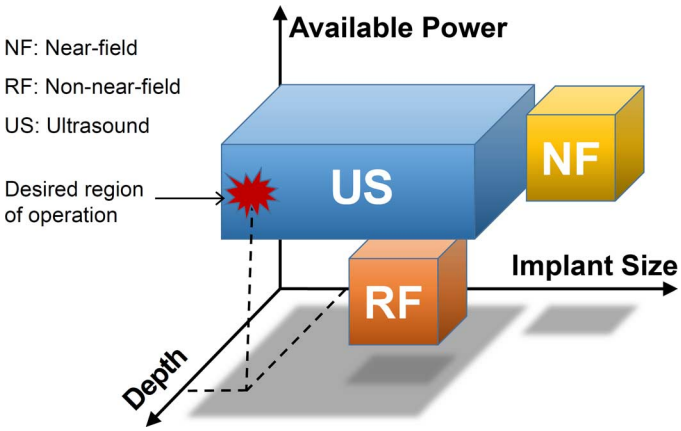


Fig. 1. Conceptual diagram showing the regimes of applicability of different wireless powering techniques and our desired region of operation.

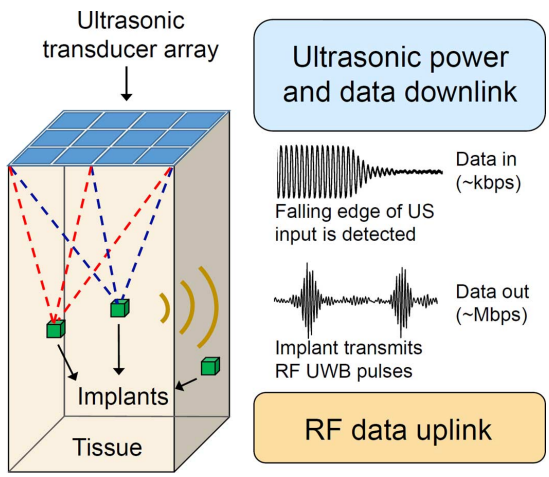


Fig. 2. Conceptual end application diagram showing external ultrasonic transducer array, a network of implants in body and the bi-directional data communication protocol in our current demonstration.

link for implants. Our proposed conceptual end application diagram is shown in Fig. 2, where a network of implants is powered by an external ultrasonic transducer array. We propose to use ultrasound for downlink and ultra-wideband (UWB) RF for uplink data transfer [16], [23]. While the ultrasonic downlink can be useful for transmitting low data rate ($\sim$ kbps) control, command, or clock signals to the implant, an energy-efficient RF uplink can be designed that enables high data-rates ($\sim$ Mbps) for recovering *in vivo* imaging data [24] and high-resolution, multi-site neural recordings. In lower data-rate applications, a purely ultrasonic data link could be implemented. While our current implant fully demonstrates ultrasonic power recovery and the capability of bi-directional data transfer, future designs could incorporate biosensors, electrodes for recording and/or stimulation, as well as clock recovery and data modulation circuits for implementing a more practical data link.

II. Overview of the Implant System

Our implant system consists of a piezoelectric energy receiver, an integrated circuit (IC) chip, and a loop antenna, as shown in Fig. 3. Ultrasonic energy is harvested in the form of AC power by the piezoelectric receiver, which is then converted to DC energy via power recovery circuits on the IC, and stored in an on-chip capacitor (C_{STOR}). The stored energy could be used for powering different functions such as stimulation, biosensing, and neural recording. The IC also includes a data recovery and transmitter circuit for downlink and uplink communication with the implant.

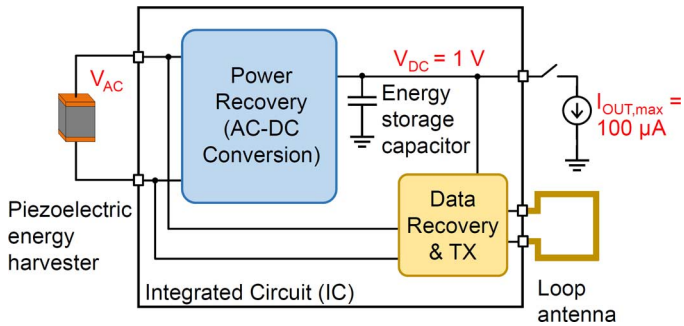


Fig. 3. System block diagram of the implant.

A. Design of the Piezoelectric Receiver

The piezoelectric receiver is designed to simultaneously achieve small dimensions, high available power, and favorable impedance for efficient energy harvesting. The impedance and available power for a piezoelectric receiver are dependent on several design variables, such as material, dimensions, and acoustic loadings from the package. Our design strategy for the piezoelectric device involves using the 1D Krimholtz, Leedom and Matthaei (KLM) model [25] for first-order insight and performing 3D finite element simulations using the COMSOL Multiphysics tool. For this demonstration, we choose lead zirconate titanate (PZT) as the piezoelectric material due to its high electromechanical coupling factor, though a more rigorous study could be performed in the future to optimize for power conversion efficiency, small dimensions, and biocompatibility. A piezoelectric device has a fundamental open-circuit and a short-circuit resonance frequency at which the device impedance can be purely real. From the KLM model, these frequencies are mainly controlled by the thickness of the device, which, to first order, is equal to its half-wavelength at the open-circuit resonance frequency for low-impedance acoustic loadings [25], [26]. Operating frequency of 1 MHz is chosen based on the trade-off between the thickness of the device and losses in tissue. In order to achieve short-circuit resonance for PZT at 1 MHz, the device thickness was chosen to be 1.4 mm. Further, the lateral dimension was chosen to be 1 mm in order to achieve minimal coupling to parasitic vibration modes of the device [27]. This sub-wavelength dimension also helps in achieving a large acceptance angle, thereby reducing the impact of implant rotations on power recovery [28]. Measurements of our piezoelectric devices are performed in a tank filled with mineral oil since it has similar acoustic impedance to soft tissue. Fig. 4(a) and (b) shows the measured and simulated impedance profiles (using COMSOL) of two different sized piezoelectric receivers in oil. The measurements and simulations show good agreement, demonstrating our simulations' utility in design. The measurement shows slightly lower Q because we have not modeled all of the packaging in the simulations. The simulated

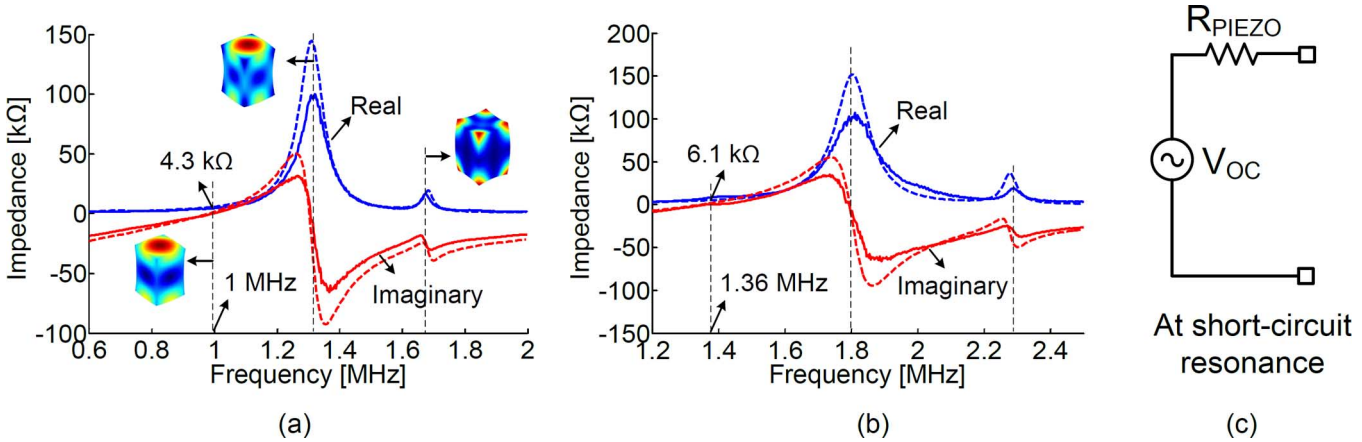


Fig. 4. Simulated (dashed line) and measured (solid line) impedance of (a) 1 mm × 1 mm × 1.4 mm, and (b) 0.7 mm × 0.7 mm × 1.0 mm piezoelectric devices, also showing the displacement profiles of the 1.4 mm^3 piezoelectric device at the resonance frequencies, (c) Equivalent circuit model of the piezoelectric device at short-circuit resonance frequency.

TABLE I
MEASURED ACOUSTIC-TO-ELECTRICAL CONVERSION EFFICIENCY (η) CALIBRATED USING A HYDROPHONE, AND CALCULATED AVAILABLE ELECTRICAL POWER (P_{AV}) FOR AN INCIDENT ACOUSTIC INTENSITY (I_0) OF 0.72 mW/mm^2 (10% OF THE FDA LIMIT).

Piezoelectric receiver dimensions	Measured η	Calculated P_{AV} for I_0 = 0.72 mW/mm^2 ($P_{AV} = \eta \times I_0 \times Area$)
1 mm × 1 mm × 1.4 mm (1.4 mm^3)	> 50 %	360 μW
0.7 mm × 0.7 mm × 1 mm (0.5 mm^3)	> 50 %	176 μW

displacement profile of the 1.4 mm^3 device is also pictured. The equivalent circuit model of the piezoelectric device at its short-circuit resonance frequency is shown in Fig. 4(c). The short-circuit impedance can be varied between 2–6 kΩ through design of the package loadings. Our 1.4 mm^3 and 0.5 mm^3 piezoelectric devices also achieve a high measured acoustic-to-electrical conversion efficiency (>50%) as shown in Table I. From the data, both devices achieve an electrical available power >100 μW at just 0.72 mW/mm^2 acoustic intensity (10% of the FDA diagnostic limit), allowing us to reach the mW range by further increasing the acoustic intensity.

B. Bi-Directional Data Link

Since downlink data rates required in typical implant applications are ∼kbps, an ultrasonic downlink operating at a carrier frequency of ∼MHz is feasible. Our proof-of-concept downlink protocol, as shown in Fig. 2, uses the falling edge of the ultrasound signal as an input "trigger" for the implant. In this protocol, the maximum achievable downlink trigger rate is determined by the minimum required ON and OFF times of the ultrasound input. The minimum OFF time is limited by the rate of discharge of the ultrasound envelope as well as the speed of the envelope detector circuit. The discharge rate of the ultrasound envelope largely depends on the impedance profile of the piezoelectric receiver, and other complex factors such as the dispersion of its acoustic-to-electrical conversion efficiency and the non-linear input impedance of the IC. The minimum ON time is determined by the time required to fully recharge C_{STOR}. Based on typical values of ON and OFF times from our design and measurements, downlink trigger rates >10 kbps can be achieved. For applications demanding a larger downlink data rate, a different protocol such as amplitude-shift keying with a small modulation depth can be implemented in the future.

In spite of the drawbacks of RF for wireless power transfer, it is still feasible to implement an RF data uplink, because signal level required at the external data receiver can be as low as −70 to −80 dBm, as opposed to −20 to 0 dBm for power. This is possible because the link is highly asymmetric, allowing the external receiver to be large, consume more power, and thus, have higher sensitivity as compared to the implant. Assuming a bandwidth of 1 GHz, a signal-to-noise ratio (SNR) of 10 dB, and a noise figure of 3 dB, the sensitivity of the external receiver can be calculated to be −71 dBm. Our uplink protocol consists of transmitting two UWB pulses from the implant, upon the recovery of the input trigger, as illustrated in Fig. 2. This demonstrates sufficient energy at the implant showing capability of implementing m-PPM modulation in the future, where the first pulse can serve as a calibration or synchronization pulse, and the second pulse can be positioned to lie in one of 'm' slots. This protocol enables heavy duty-cycling of the transmitter, resulting in extremely low average power consumption and an improved energy efficiency, as demonstrated in upcoming sections.

In this demonstration, we choose an RF frequency of 4 GHz, based on considerations of the implant antenna size and depth in tissue, as discussed further in Section V. The nominal pulse width is chosen to be 2 ns and the nominal inter-pulse delay is fixed at 10 ns. A further smaller pulse width could enable lower energy consumption per pulse and higher uplink data rates, but would require a wideband antenna and a higher RF carrier frequency which has larger losses in tissue. Accounting for losses in the link (discussed in Section V), the peak power delivered to the implant antenna is targeted to be between −10 and 0 dBm in order to meet the −71 dBm sensitivity of the external receiver. Thus, our current system demonstrates the capability of uplink

and downlink communication. However, in future work, additional blocks for clock recovery, data processing and modulation should be implemented for achieving a complete wireless data link.

III. Power Recovery Architecture

A power recovery and management circuit is required, along with a regulated output DC rail, for reliably powering data transmitters, sensors or stimulation circuits required in most implant applications. In this proof-of-concept design, we target a regulated DC output voltage of 1 V and a maximum DC output current ($I_{\rm out}$) of 100 μA, i.e., a maximum DC load power ($P_{\rm out,dc}$) of 100 μW. The target peak AC input voltage ($V_{\rm in}$) range for the power recovery circuit is 0.6–1.1 V, based on the threshold voltage of typical rectifiers and the breakdown voltage limit of transistors.

A. Chip-Piezoelectric Receiver Interface

The fundamental component of the input resistance ($R_{\rm in}$) of a typical AC-DC power recovery circuit is approximately given by

$$R_{\rm in} = \frac{V_{\rm in}^2}{2P_{\rm in,avg}} = \frac{V_{\rm in}^2 \times \eta_{\rm AC\text{-}DC}}{2P_{\rm out,dc}} \quad (1)$$

where $P_{\rm in,avg}$ is the average input power of the IC and $\eta_{\rm AC\text{-}DC}$ is the efficiency of the AC-DC converter. For $V_{\rm in}$ between 0.6–1.1 V, $P_{\rm out,dc}$ between 10–100 μW, and $\eta_{\rm AC\text{-}DC}$ between 30–70%, $R_{\rm in}$ is between 0.5–42.4 kΩ. The input impedance also is comprised of a shunt capacitance, which includes the parasitic capacitance of MOS transistors or diodes connected at the AC inputs. However, it can be ignored at the frequency of interest (1 MHz) and for the typical values of $R_{\rm in}$ in this design. Thus, the resistances of the AC-DC converter and the piezoelectric receiver can be designed to lie in a similar range ($\sim$ kΩ), allowing us to forego a dedicated input matching network, while still achieving good power transfer efficiencies.

B. Power Recovery Circuit Architecture

A typical Dickson multiplier used for power recovery in this design would require very large values of coupling capacitors due to low input frequency (1 MHz) and large $I_{\rm out}$ (100 μA) requirement [29]–[31]. The output DC voltage ($V_{\rm dc}$) of a single-stage Dickson multiplier is approximately given by $V_{\rm dc} = V_{\rm in} - I_{\rm out}/(C_C f)$, where C_C is the coupling capacitance and f is the input frequency. For simplicity, the above equation assumes zero voltage drop across the diodes in the multiplier circuit and ignores the effect of diode parasitic capacitance. Based on the above equation, if $V_{\rm in} = 1$ V, $I_{\rm out} = 100$ μA and $f = 1$ MHz, then for achieving $V_{\rm dc} = 0.9$ V, for instance, the required value of C_C is 1 nF. Moreover, the load capacitance at $V_{\rm dc}$ node is typically chosen to be an order of magnitude larger than C_C [30], resulting in a very large on-chip area.

Thus, in order to reduce the size of coupling capacitors, we decouple the constraints of low f and large $I_{\rm out}$ by designing a power recovery circuit with a hybrid two-path architecture as shown in Fig. 5. In this architecture, the main power path is designed to support the large $I_{\rm out}$ (100 μA) and operate at a high switching frequency (30 MHz) for reducing the size of coupling capacitors. In this path, the AC input voltage is first rectified to a DC voltage ($V_{\rm DC1}$) using a full-wave active rectifier. A high-frequency voltage doubler is then used to double this voltage to $V_{\rm DC2}$. Subsequently, a low dropout regulator (LDO), powered from $V_{\rm DC2}$, generates a constant DC rail ($V_{\rm LDO}$). In parallel to the main path, we implement an auxiliary power path consisting of a push-pull voltage doubler that generates an auxiliary DC rail ($V_{\rm DC,AUX}$) for powering low power consuming blocks, such as a constant-gm bias circuit and a ring oscillator that drives the high-frequency doubler. Due to low output power of this path, the size of coupling capacitors required in the push-pull doubler need not be large. This architecture thus enables the generation of reference and clock signals at low available powers during startup, while still supporting a large load power, without compromising efficiency or using impractical values of coupling capacitors.

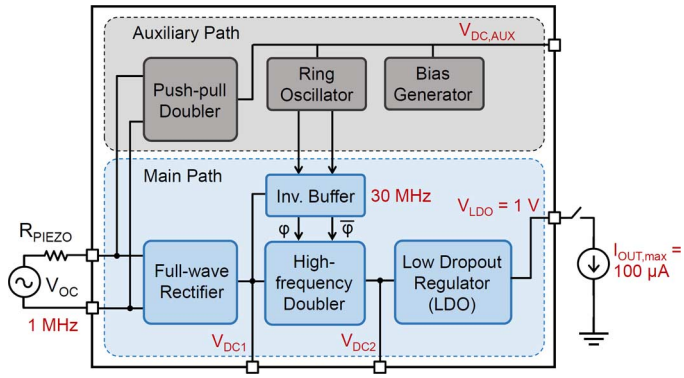


Fig. 5. Hybrid two-path architecture of the power recovery circuit.

For high available input power, power conversion efficiency (PCE) for this architecture increases with $P_{\rm out,dc}$ up to the maximum sustainable $P_{\rm out,dc}$. For very low $P_{\rm out,dc}$, PCE is limited by the quiescent power dissipation in the LDO and other circuit blocks. For low available input power, $V_{\rm in}$ is low, resulting in lower rectification efficiency. Techniques for improving the efficiency of the rectifier at low $V_{\rm in}$ [32], [33], and implementation of an efficient and reconfigurable charge-pump [34] for minimizing the voltage drop across the LDO pass transistor, can further improve the PCE across a wide range of input powers and load currents.

IV. Circuit Implementation

A. Power Recovery Circuits

Fig. 6(a) shows a schematic of the full-wave active rectifier consisting of a gate cross-coupled NMOS pair and active PMOS diodes operating as switches [35]. This topology enables low dropout voltage across the transistors, resulting in a high PCE. The active PMOS diode uses a high-speed comparator with a common-gate input stage. Current sources of the comparator are biased from the constant-gm bias circuit powered from the $V_{\rm DC,AUX}$ rail. Reliable startup of the active rectifier is, thus, guaranteed since $V_{\rm DC,AUX}$ rail is generated using a passive voltage doubler. Post-layout simulation of this rectifier results in a $V_{\rm DC1}$ of 0.72 V for peak $V_{\rm in}$ of 0.8 V and a load power

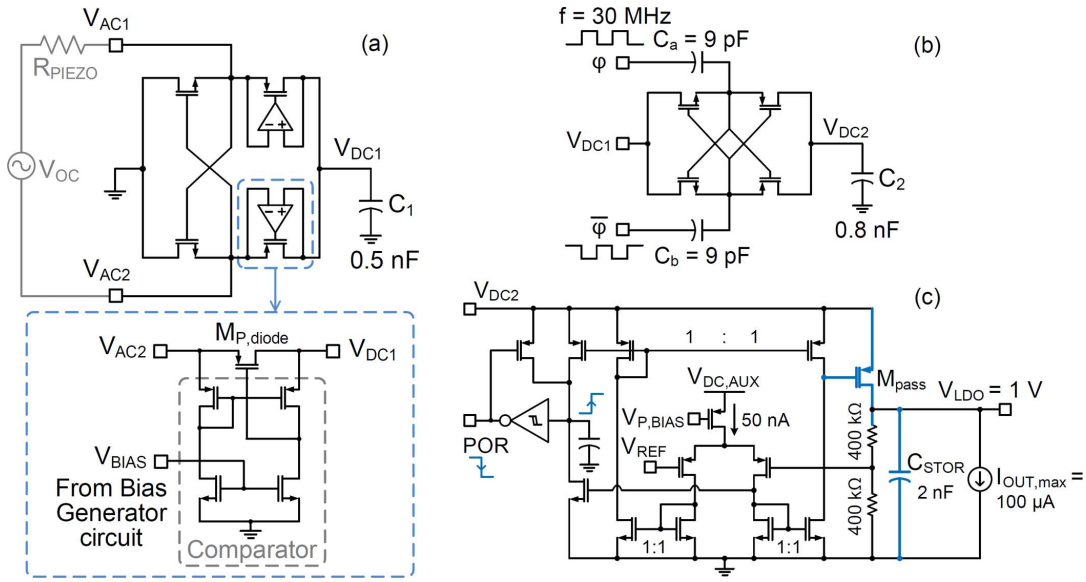


Fig. 6. Power recovery circuits in the main power path: (a) active full-wave rectifier and the comparator used in the active PMOS diode; (b) high-frequency voltage doubler; (c) LDO circuit and generation of the POR signal.

of 100 μW, confirming a voltage conversion ratio of 0.9 and a PCE of 89.4%. In this simulation, the dropout voltage across the NMOS transistors is 5.6 mV and that across the active PMOS diodes is 72 mV.

The high-frequency switched-capacitor voltage doubler, shown in Fig. 6(b), is implemented using cross-coupled MOS transistors with two coupling capacitors (C_a and C_b) driven by anti-phase clock signals φ and $\bar{\varphi}$. The values of these coupling capacitors (9 pF) and the switching frequency (30 MHz) are chosen based on the trade-off between switching losses, losses due to finite output resistance of the converter and charge redistribution losses [36]. For V_{DC1} of 1.0 V and a load power of 100 μW, post-layout simulations of this doubler yield a voltage conversion ratio of 1.78 and a PCE of 88%. The 30 MHz clock signal is generated using a 5-stage current-starved ring oscillator powered from $V_{\mathrm{DC,AUX}}$. The output of the ring oscillator is further level-shifted to V_{DC1} supply and fed at φ and $\bar{\varphi}$ through an inverter buffer.

The value of on-chip load capacitance of the rectifier (C_1) is chosen to be 0.5 nF, that of the doubler (C_2) is 0.8 nF, and the storage at the output of the LDO (C_{STOR}) is 2 nF, based on the trade-off between startup time and the discharge rate of these rails during OFF time of the ultrasound input, as well as for minimizing voltage ripple. In layout, these capacitors are implemented as a combination of MOS and metal–oxide–metal (MOM) capacitors, achieving a capacitance density of 3.8 nF/mm^2. On-chip capacitors are chosen in this design, since off-chip capacitors pose more integration challenges, in addition to consuming a large implant volume.

The schematic of the LDO is shown in Fig. 6(c) along with the scheme for generating a power-on-reset (POR) signal. The LDO, using a PMOS pass transistor and a current-mirror OTA as error amplifier, is designed for a maximum load of 100 μA and consumes a nominal quiescent current of 3.2 μA in simulation. The startup time of the LDO from post-layout simulations is 100 μs, which is also confirmed from measurements, as discussed in Section VII. The LDO startup time is important because it would influence the throughput of a system consisting of a network of implants accessed by the external unit through time-domain multiple access (TDMA).

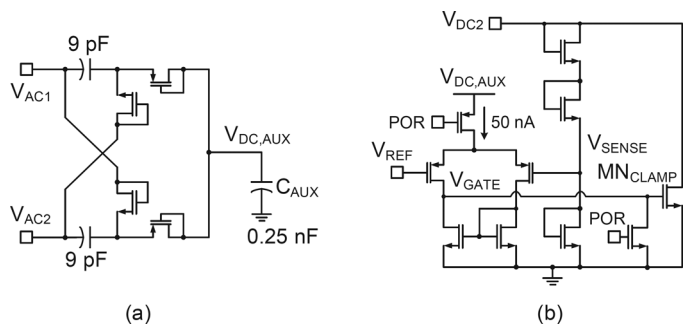


Fig. 7. (a) Push-pull voltage doubler circuit used in the auxiliary power path, (b) Over-voltage protection circuit for V_{DC2} rail.

In the auxiliary power path, the passive push-pull voltage doubler, shown in Fig. 7(a), is implemented using diode-connected transistors. Although the diode-connected transistors result in a forward voltage drop, the PCE of this block does not impact the overall PCE due to a small load current for this stage. In order to prevent breakdown due to over-voltage at the inputs, diode-based and active voltage limiting clamps are added between the two AC inputs of the IC and at the DC rails: $V_{\mathrm{DC,AUX}}$, V_{DC1} and V_{DC2}. The active clamp on V_{DC2} rail is shown in Fig. 7(b). It uses a negative feedback loop to sense a voltage excursion beyond ~1.6 V and, in response, draw more current through $\mathrm{MN_{CLAMP}}$ transistor, thereby, limiting V_{DC2} voltage.

B. Data Communication Circuits

Our novel technique of envelope detection for the data recovery circuit consists of reusing the comparator in the active PMOS diode of the rectifier, as shown in Fig. 8. When the envelope of the AC inputs, V_{AC1} and V_{AC2}, falls roughly below the sum of an NMOS and a PMOS threshold voltage, transistor

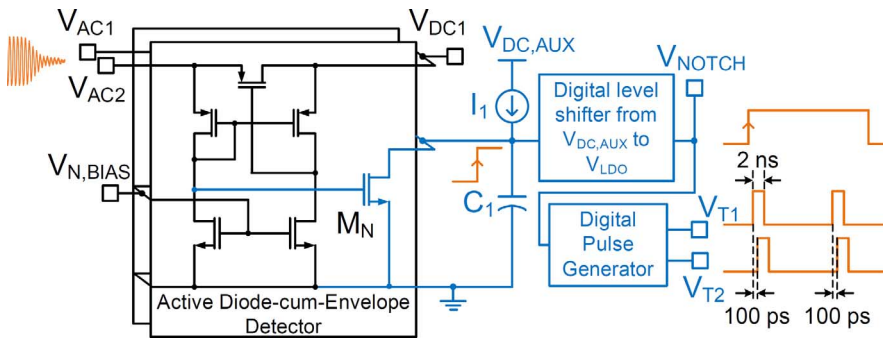


Fig. 8. Data recovery circuit showing envelope detection of ultrasound input and generation of trigger pulses, V_{T1} and V_{T2}.

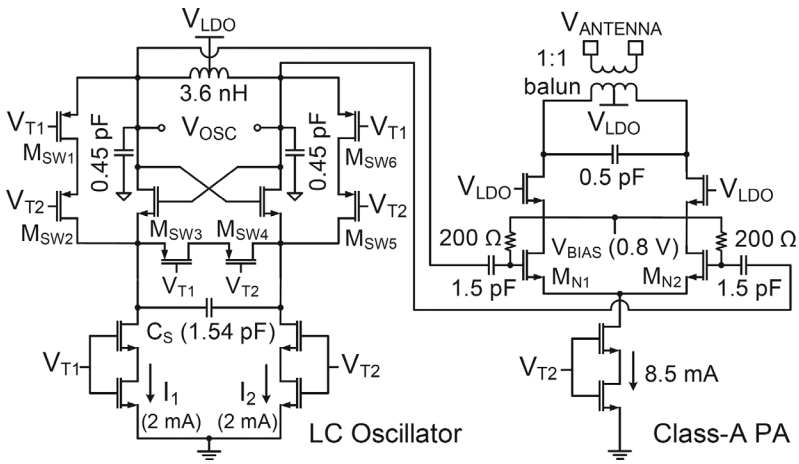


Fig. 9. RF data transmitter circuit showing the oscillator and the PA schematics.

M_N turns off, allowing current I_1 to charge capacitor C_1 to $V_{DC,AUX}$. As illustrated in Fig. 8, this triggers a digital pulse generator to generate two trigger voltages V_{T1} and V_{T2} with a nominal pulse-width of 2 ns and a fixed inter-pulse delay of 10 ns in post-layout simulations. These trigger voltages serve as "enable" signals for the RF transmitter. V_{T2} is simply a delayed version of V_{T1}, with a delay of 100 ps, and is required for the fast startup of the oscillator. The generation of these pulses during startup is avoided by gating the data recovery circuit with the POR signal.

Our RF UWB transmitter, shown in Fig. 9, consists of a 4 GHz LC oscillator with a cross-coupled NMOS pair, followed by a power amplifier (PA), both gated by V_{T1} and V_{T2} pulses. A major goal in the design of this transmitter is to minimize its total ON-time by ensuring fast startup and turn-off of elements that consume a high peak power. The number of cycles required for the startup of a conventional LC oscillator is proportional to the tank Q. However, a pulse width of 2 ns and a carrier frequency of 4 GHz necessitates startup of the oscillator within 3–4 cycles. We therefore use a modified tail current source [37] which provides an asymmetric drive to the oscillator, establishing a large initial condition for oscillations and resulting in a startup time <1 ns. Capacitance C_S in the modified tail current source is sized (1.54 pF) such that it provides a large voltage difference during startup, while minimally degenerating the transconductance of the cross-coupled NMOS transistors in steady-state. In post-layout simulations, the nominal ON-state oscillator current is 4 mA, resulting in a per-pulse energy dissipation of <9 pJ (0.9% of the total energy stored on C_{STOR}). Switches M_{SW1}–M_{SW6} ensure that the oscillator is fully turned OFF when the pulses are not being transmitted.

The PA uses a cascoded class-A topology and was co-designed with the antenna to generate a peak output power between -10 and 0 dBm. Fast startup of the PA is ensured by designing a strong driver for V_{T2} node. The input transistors of the PA are biased at a DC voltage of 0.8 V derived from the resistor divider of the LDO. The high-pass filter at the input of the PA ensures good AC coupling to the oscillator output at 4 GHz. An on-chip 1:1 balun/transformer, with its primary center tap connected to V_{LDO}, is designed to interface the PA to the off-chip antenna. The balun provides ESD protection [38], while also enabling direct measurement of the PA output using a single-ended probe. The nominal PA tail current in post-layout simulations is 8.5 mA, resulting in a per pulse energy consumption of <18 pJ (1.8% of the total energy stored on C_{STOR}). The OFF-state leakage power of the PA is limited to <50 nW.

HFSS models of the inductor and balun are shown in Fig. 10(a) and (b), respectively. The spiral inductor, designed with five turns, a trace width of 3 μm, and a spacing between traces of 4 μm, achieves an inductance of 3.6 nH, Q of 11, and a self-resonance frequency of 12.5 GHz. The 1:1 balun has four turns on each side, a trace width of 3 μm and a spacing of 2 μm between the primary and secondary turns. At 4 GHz, the balun achieves a coupling factor of 0.88, primary and secondary side

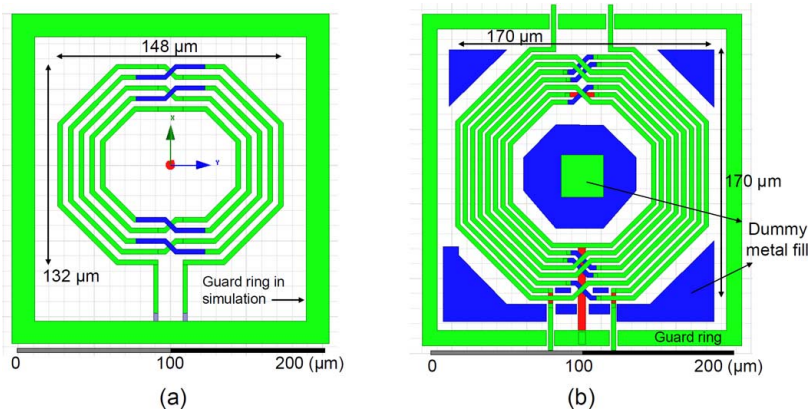


Fig. 10. HFSS simulation setups for the (a) inductor used in the LC oscillator and (b) balun at the output of the PA.

inductances of ∼3 nH with quality factors of ∼10. Epoxy and tissue surrounding the IC were found to have a minimal impact on the inductor and the balun in HFSS simulations.

V. Antenna Design

We have designed small loop antennas of 1.5 mm to 3 mm for data uplink for our proof-of-concept system. ANSYS HFSS software was used to simulate a full RF transmission link with the internal implanted antenna, in 3 cm of body tissue, and an external loop antenna. The simulation setup is shown in Fig. 11(a). We use a homogeneous muscle medium because we are not designing for a specific application, muscle is abundant around the body in thick layers and is a likely place for implants, and muscle has relatively high loss which will give a conservative link. When designing a miniature implanted antenna, there is a trade-off in frequency between the electrical length of the antenna and the losses in the tissue. Lower frequency operation results in high-Q impedance [39] and gives poor matching to the PA; however, high-frequency operation results in increased body losses [40]. For our design, we investigated antenna sizes between 1.5 mm to 3.0 mm since they are on the order of IC and piezoelectric receiver dimensions and keep the overall area of the implant small. The frequency range 3.5–4.5 GHz (1 GHz BW for 2 ns pulse) was found to be favorable, for the investigated antenna sizes, since the input impedance to the 2.5 mm antenna was largely real and optimal for the power and voltage levels in our design. Fig. 11(b) shows the impedance of a 2 mm, 2.5 mm, and 3 mm loop from 3.5 to 4.5 GHz on a Smith Chart. Based on this impedance, we designed a class-A PA to have a favorable load-pull profile for the 2.5 mm antenna, as also shown in Fig. 11(b).

After designing the implanted antenna, we parametrically designed an external loop receiving antenna such that we achieved high power link gain (G_p) in the 3.5-4.5 GHz band. The external receiver antenna in our system is a square loop of side length equal to 10.5 mm. In future systems, the design of this antenna should be optimized, primarily with the objectives of achieving maximum effective aperture or gain and circular polarization, within the size constraints set by the specific application. Fig. 11(c) shows G_p over 2–5 GHz, simulated with a load impedance of 50 Ω. We assumed a transmit power between −10 and 0 dBm and computed a −71 dBm sensitivity, in a previous section, meaning we needed at least −61 to −71 dB of link gain. As can be seen from the data, all three antenna designs have a link gain much greater than the required value over the entire band. G_p is relatively similar for the three antennas because they all have similar radiation patterns and G_p is normalized to input power to the antenna. Although, the overall received power is greatest for the 2.5 mm antenna, because of the impedance presented to the PA, the other antennas can also be used without significant degradation of received power. Since the implant could undergo small rotations in the body, we also performed simulations with the 2.5 mm antenna at 4 GHz to assess the angular dependence of G_p. We rotated the antenna about the x- and y-axis up to 90 degrees (angles labeled in Fig. 11(a) as θ_X and θ_Y), and found that G_p was insensitive to angle. Maximum G_p was obtained for the orientation shown in Fig. 11(a), and minimum G_p was just ∼ 1.5 dB below maximum G_p at larger values of θ_X with the loop faces normal to each other. We also performed measurements at a few discrete angles and observed that the link was relatively insensitive to angular rotations and misalignment, which is in agreement with simulations.

VI. Measurement Setup

In order to demonstrate the feasibility of wireless power and data transfer in body, we perform *ex vivo* measurements of the implant in chicken meat. Chicken meat is chosen because its acoustic and electromagnetic properties closely resemble those of human tissue [40], [41]. Our measurement setup is shown in Fig. 12. We note that while mineral oil is used for acoustic coupling and has a minimal impact on the RF link, in a real scenario, an acoustic matching layer will be used between the wearable ultrasonic transmitter and skin.

The external ultrasonic transmitter (Olympus A303S-SU) is driven at 1 MHz using a signal generator. For varying input power levels, the AC inputs and the DC outputs of the IC are measured for characterizing the performance of the power recovery circuit. An external load resistor is connected to V_{LDO} for characterizing the DC output power capability of the IC. An external RF receiver chain, consisting of an antenna, a low-noise amplifier, and an oscilloscope, is used to characterize the performance of downlink data recovery and uplink RF transmitter circuits. Additionally, we performed a blind test of our fully pack-

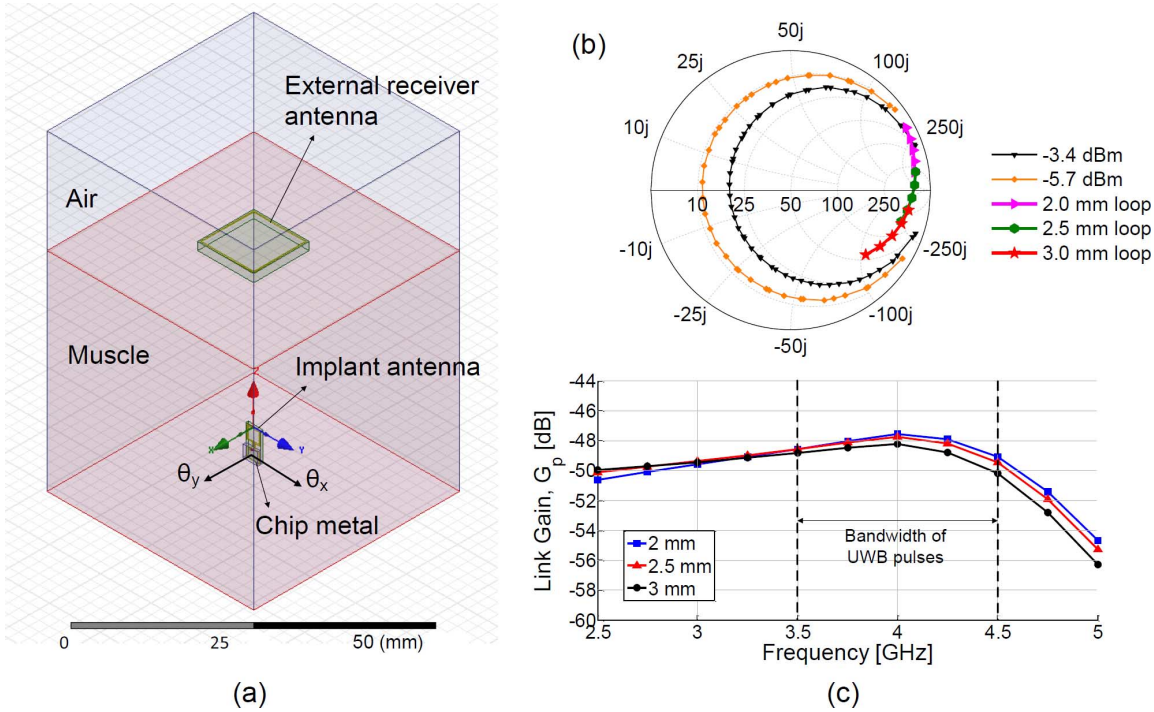


Fig. 11. (a) HFSS simulation setup for the antenna showing tissue modeled as muscle (muscle has high losses and gives conservative link gain results), antenna feed, bondwires, and IC modeled as a metal sheet. (b) Simulated load-pull curves of the PA superimposed with the simulated impedance for different antenna dimensions. (c) Simulated link gain, G_P, showing a flat gain profile between 3.5–4.5 GHz for all antenna sizes.

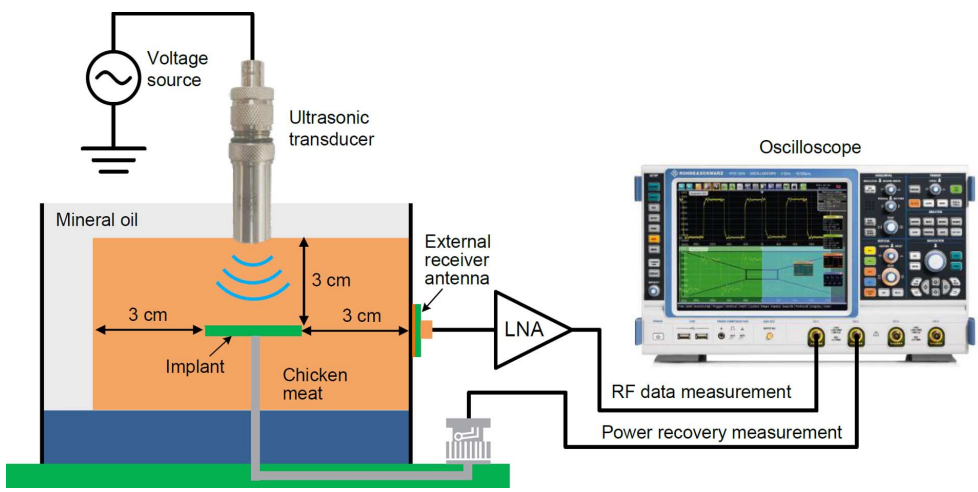


Fig. 12. Measurement setup for characterizing the implant.

aged implant, embedded in 3 cm of chicken meat on all sides, without accessing any of its terminals using PCB or wires.

A wideband needle hydrophone was used to characterize the vertical and horizontal beam profiles of our external ultrasonic transmitter, shown in Fig. 13(a) and (b). This measurement shows that the maximum RMS intensity is achieved at 3 cm depth, and therefore, our implant measurements are performed at this depth. Fig. 13(a) also shows the available power for our 1.4 mm^3 piezoelectric device, measured through oil and 2.7 cm of chicken meat for an acoustic intensity of 1 mW/mm^2 for this transmitter at 3 cm depth. Fig. 13(b) shows a horizontal beam diameter of $\sim$ 3 mm for our transducer, resulting in a beam spot size ($\sim$ 7 mm^2) which is $\sim$ 7$\times$ larger than the cross-sectional area of our piezoelectric device (1 mm^2). In the future, ultrasonic array beamforming can be used for further optimizing the beam spot size in order to maximize link efficiency at greater implant depths (up to 10 cm) [42], [43]. However, at larger implant depths, the efficiency of the RF data link may degrade, requiring a careful choice of the RF carrier frequency based on the trade-off between tissue losses and implant antenna size.

VII. Measurement Results and Discussion

Measurement results are presented for our implant system designed using the 1 mm $\times$ 1 mm $\times$ 1.4 mm piezoelectric receiver,

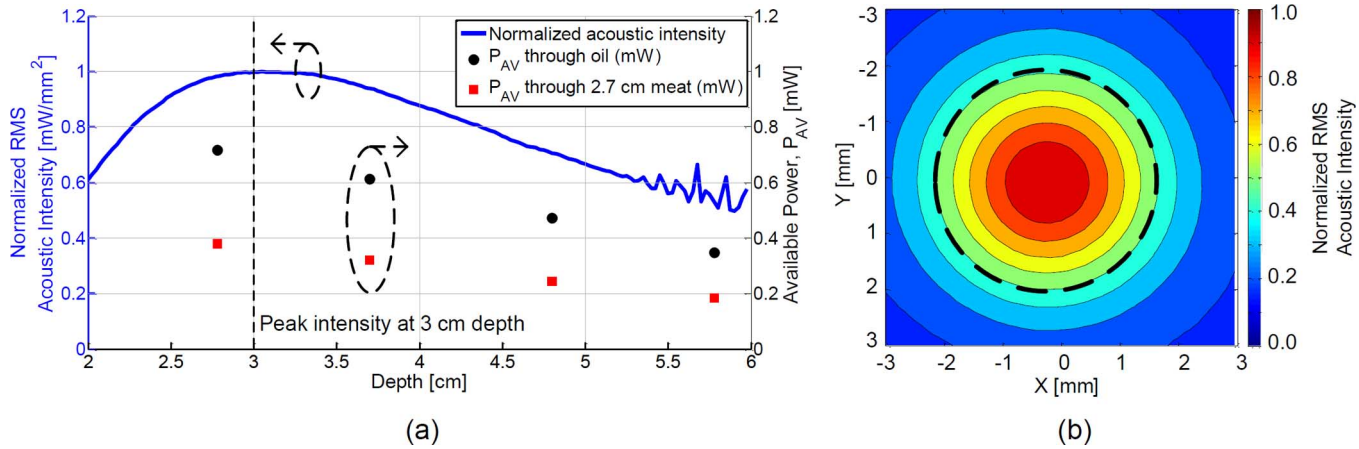


Fig. 13. Characterization of the external ultrasonic transducer. (a) Normalized RMS acoustic intensity vs vertical depth, measured in oil medium using a needle hydrophone with an aperture of 1.5 mm diameter. The plot also shows available power for our 1.4 mm^3 piezoelectric device through oil and 2.7 cm of chicken meat for an acoustic intensity of 1 mW/mm^2 at 3 cm depth. The device cross-section is 1 mm^2. (b) Beam profile of the transducer in the horizontal plane at 3 cm depth, showing a focal spot size of 3 mm (dashed circle).

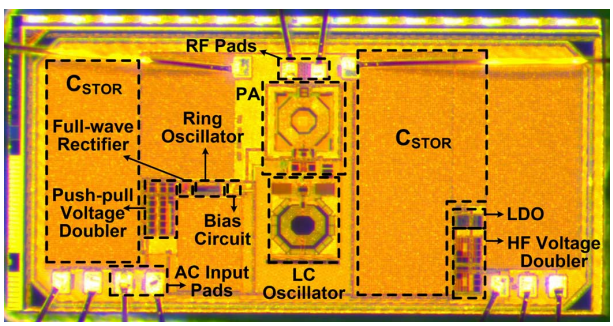


Fig. 14. Die photo of the IC (1 mm × 2 mm) with key circuit blocks annotated.

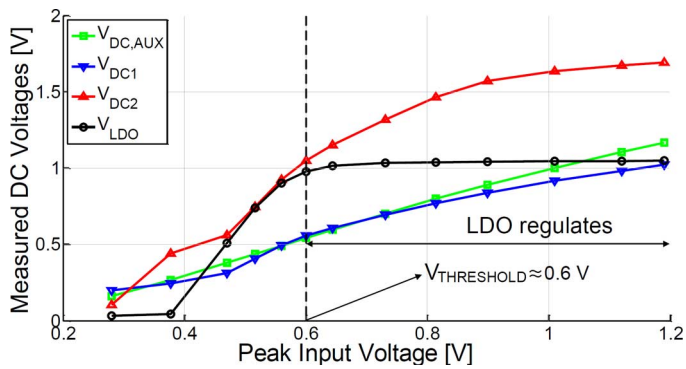
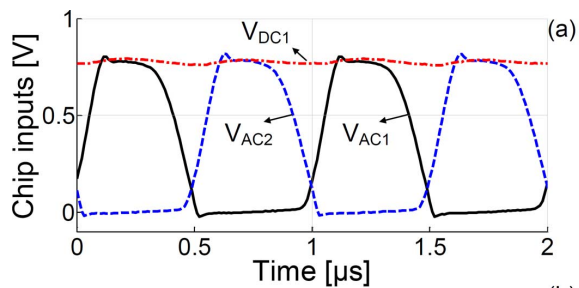


Fig. 15. Measured DC voltages of the IC as a function of the peak input AC voltage.

1 mm × 2 mm IC and square loop antenna sizes of 2.5 mm and 3 mm, packaged together on an FR4 PCB. The die photo of the IC, designed using TSMC 65 nm general purpose (GP) process technology, is shown in Fig. 14. For characterization tests, components were assembled on a PCB along with connectors for access to all terminals. Measurement results presented in Figs. 15–18 and 20(a) are with this PCB placed inside the oil tank, with the external transducer providing the ultrasound input. Measurement results for bench characterization of the IC are presented in Figs. 19(a) and 20(b).

Fig. 15 shows successful recovery of DC voltages, with no external load on V_{LDO}, for peak AC input voltages of the IC ranging from 0.6 to 1.2 V, as expected from design. Fig. 16(a) shows measured waveforms of the two AC input voltages of the chip (i.e., at the terminals of the piezoelectric receiver) and the output of the full-wave rectifier for an incident acoustic intensity of 0.13 mW/mm^2 (1.8% of the FDA limit) at the implant and no external load on V_{LDO}. The voltage conversion efficiency of the rectifier is 97.5%. Measured V_{DC2} (1.49 V) is lower than twice the value of V_{DC1} (0.78 V) because the active voltage limiter at V_{DC2} is partially ON. The output of the LDO is 1.04 V which is close to the simulated value of 1.0 V. This small difference could be attributed to the susceptibility of the LDO reference voltage to process variations in the constant-gm bias circuit. The value of $V_{\mathrm{DC,AUX}}$ in this



(b)

$V_{\mathrm{IN,PEAK}}$	$V_{\mathrm{DC,AUX}}$	V_{DC1}	V_{DC2}	V_{LDO}
0.8 V	0.69 V	0.78 V	1.49 V	1.04 V

Fig. 16. (a) Measured waveforms at the two AC inputs of the IC and the rectifier output voltage (V_{DC1}). (b) Measured values of peak AC input to the IC and the recovered DC voltages for an incident acoustic intensity of 0.13 mW/mm^2 (1.8% of FDA limit).

measurement is 0.69 V, and is lower than its value in Fig. 15 for $V_{IN} = 0.8$ V due to process variations, which further motivates the need for generating a regulated DC rail using an LDO in such applications.

Fig. 17 shows the measured startup waveforms of the DC rails for a peak AC input voltage of 0.8 V. It can be seen that V_{LDO}

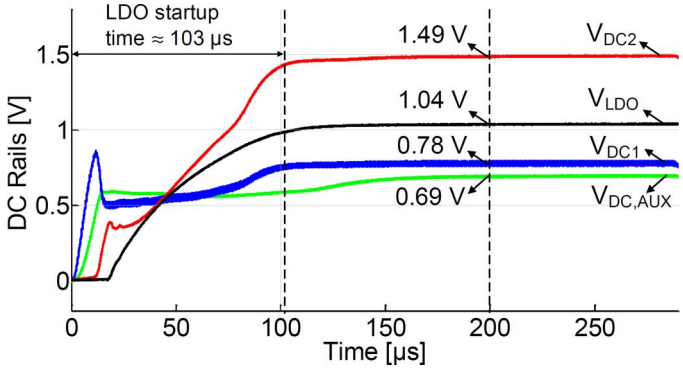


Fig. 17. Measured startup waveforms of the DC rails for a peak AC input voltage of 0.8 V.

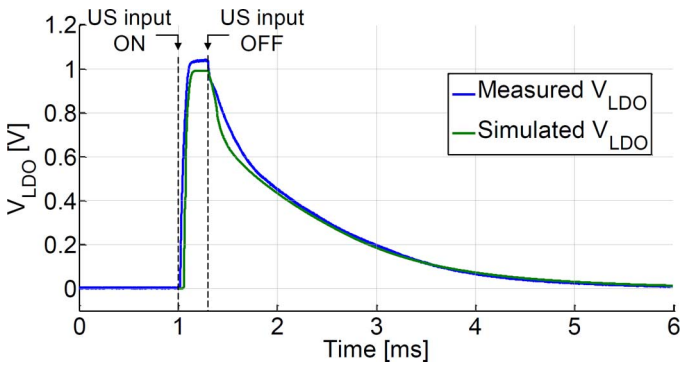


Fig. 18. Measured charging and discharging waveforms for the LDO output voltage (V_{LDO}) showing good correlation with simulation.

settles to 95% of its steady-state value in 103 μs, which is close to the simulation value of 100 μs. In Fig. 18, the startup and discharge profiles of V_{LDO} rail are compared with simulations. For this measurement and simulation, the ultrasound input is turned ON for 300 μs and is subsequently turned OFF for 5 ms. It can be noted that the measured discharge rate of V_{LDO} matches simulation, signifying that the leakage within C_{STOR}, as well as the leakage current of circuits powered from V_{LDO}, are modeled with good accuracy in simulation.

Data recovery and transmission of UWB pulses from the implant was demonstrated by modulating the amplitude of the ultrasound input at the external transmitter and detecting the resulting RF pulses via the external RF receiver chain. Fig. 20(a) shows the falling edge of the ultrasound input and the UWB pulses measured for the implant loop antenna size of 3 mm.

Fig. 19(a) shows the bench characterization result for the LDO output voltage and the AC-DC conversion efficiency of the IC for varying external load resistance (R_L) connected to V_{LDO}. The LDO regulates up to a maximum DC load power of 100 μW, as expected. At this full load, the IC achieves a maximum AC-DC conversion efficiency of 54%. As discussed previously, future designs can be optimized for maximizing this efficiency. The measurement with a 100 μW external load connected to the LDO was also performed in the oil tank and required an incident acoustic intensity of 0.36 mW/mm^2 (5% of the FDA limit). Fig. 19(b) shows a breakdown of the simulated power consumption of the IC, which is 85 μW for 100 μW load, highlighting that the largest power consumption (34.1%) is across the pass transistor of the LDO, and that the data communication circuits, which are OFF during ON time of the ultrasound input, consume the lowest (0.2%) percentage of total power. Fig. 20(b) shows the UWB pulses measured by probing the output of the PA with a $\sqrt{2}$:1 balun and connecting a 50 Ω oscilloscope on the secondary side, showing a peak PA output power of -4 dBm after accounting for external losses.

Finally, we have integrated all components (2.5 mm antenna) of our implant into a package size of 4 mm $\times$ 7.8 mm as shown in Fig. 21(a). The piezoelectric device is placed inside a through-hole of the PCB, chip-on-board assembly is used for the IC and the loop antenna is fabricated using a copper trace on the FR4 PCB. The two terminals of the piezoelectric device are interfaced to the two input terminals of the IC by using a copper foil and conductive epoxy for the bottom terminal and a bondwire for the top terminal. Further, the piezoelectric device and the IC are encapsulated in Sylgard 184 for protecting the bondwires and because Sylgard has minimal impact on their properties. The weight of our fully packaged implant is 0.07 ± 0.01 g. The fully wireless blind test performed for this implant, without any access to its terminals, demonstrates successful power transfer and bi-directional data communication capability. UWB pulses from this measurement, shown in Fig. 21(b), were received with an SNR of $\sim$13 dB through precisely 3 cm of chicken meat and another 3–4 mm of glass, as shown in the measurement setup of Fig. 12.

The dimensions of the implant can be further scaled down depending on the application requirements. UWB pulses have been successfully measured with smaller loop antennas down to 1.5 mm. Also, as discussed before, we have designed a 0.5 mm^3 piezoelectric receiver with high available power and $\sim$ kΩ range resonant impedance. Smaller piezoelectric receivers will typically require a higher ultrasound frequency, which can result in smaller areas for on-chip capacitors. However, high frequency operation will result in higher tissue losses as well as degradation of the PCE of the IC due to lower available power and input voltage levels. This will require further investigation of external transmitter design and low-voltage circuit techniques for optimizing the link and IC efficiencies. Moreover, reducing the size of the IC by implementing a part of the storage capacitor off-chip, and performing a full 3D integration of the package can allow further miniaturization of the implant.

VIII. Conclusion

A first proof-of-concept demonstration of a mm-sized implantable device, using ultrasound for power transfer, and a hybrid bi-directional data communication link, was presented in this paper. Ultrasonic power transfer is ideal for providing high power levels (100 μW to a few mWs) to mm and sub-mm sized implants operating deep inside the body (up to $\sim$10 cm). A hybrid data link consisting of ultrasonic downlink and RF uplink was proposed in this design. The RF uplink protocol consists of transmitting UWB pulses, demonstrating the feasibility of implementing an energy-efficient PPM transmitter in the future. Our current implant prototype supports a maximum measured DC load power of 100 μW,

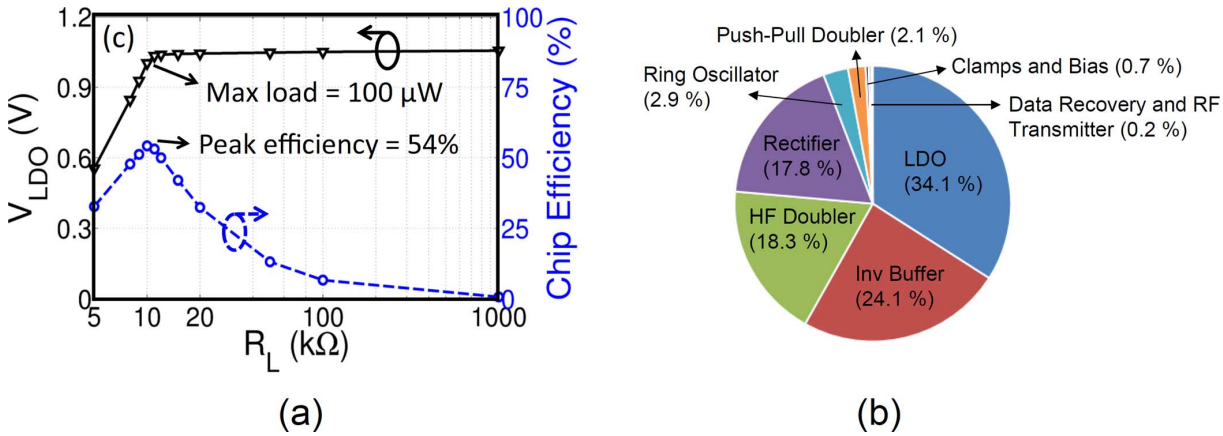


Fig. 19. (a) Measured LDO output voltage and the AC-DC conversion efficiency of the IC as a function of the external load resistor connected to V_{LDO}. (b) Simulated breakdown of power consumption of the IC, which is 85 μW for full load of 100 μW.

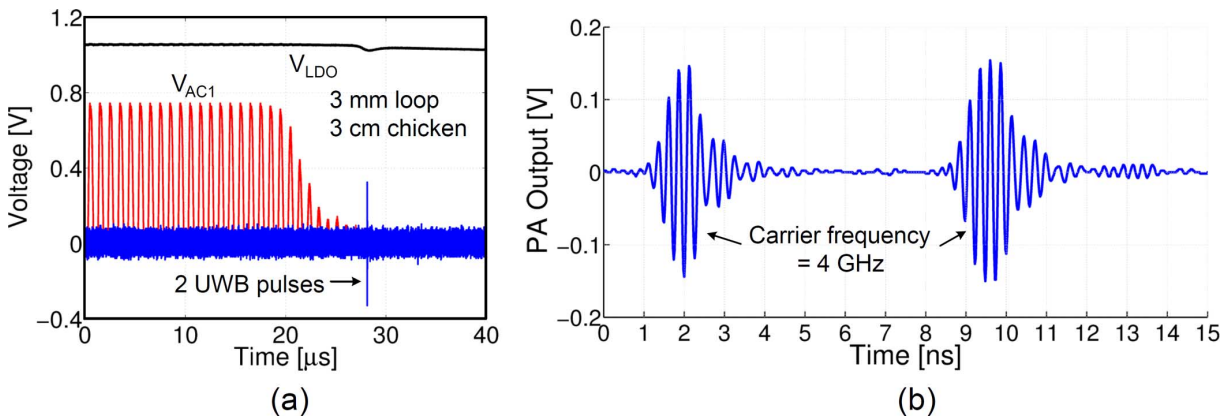


Fig. 20. (a) Wireless data recovery and transmission measurement through 3 cm of chicken meat for the implant with 3 mm loop antenna. (b) UWB pulses measured at output of the PA.

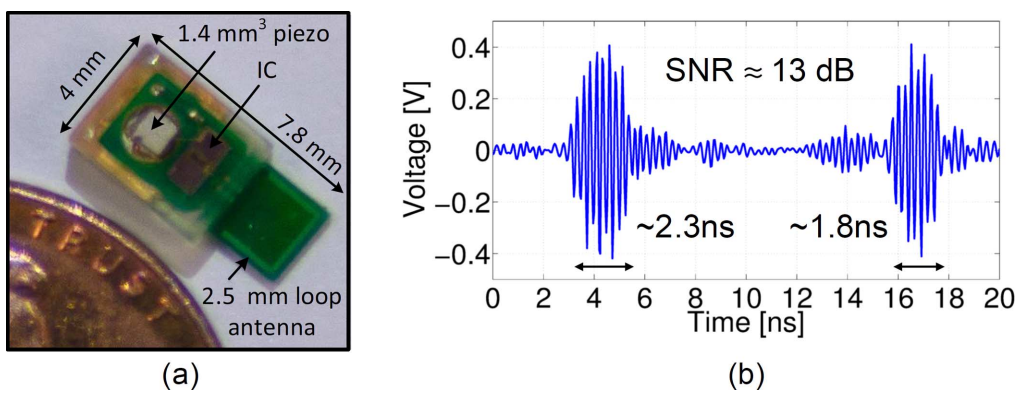


Fig. 21. (a) Fully packaged implant. (b) Results of the end-to-end blind test of the fully packaged implant showing successful recovery of UWB pulses at the external receiver.

while operating at an incident acoustic intensity of $\sim$5% of the FDA diagnostic ultrasound limit. Our current fully packaged implant has dimensions of 4 mm $\times$7.8 mm. Successful end-to-end tests were performed for the fully packaged implant, completely embedded in chicken meat (which emulates human tissue). Potential for further miniaturization of the implant is confirmed by our measurements with smaller piezoelectric receivers and antennas, and the possibility of 3D integration of components.

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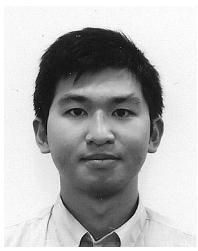
In 2008, he was a software engineering intern at GE Healthcare. He also worked as an electrical engineer in three cooperative education semesters at NASA Johnson Space Center from 2009 to 2011. From 2010 to 2012, he performed research as an undergraduate student at the University of Wisconsin-Madison, investigating the atmospheric effects on terahertz (THz) wave propagation. His research interests are broad and include implantable devices, biosensing, energy harvesting, low-power electronics, and analog and RF circuit design.

Mr. Weber was a recipient of the Stanford Graduate Fellowship (SGF) and the National Science Foundation Graduate Research Fellowship (NSF-GRP).



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Prof. Arbabian is the recipient/co-recipient of the 2015 NSF CAREER award, 2014 DARPA Young Faculty Award (YFA), 2013 IEEE International Conference on Ultra-Wideband (ICUWB) best paper award, 2013 Hellman Faculty Scholarship, 2010 IEEE Jack Kilby Award for Outstanding Student Paper at the International Solid-State Circuits Conference, two-time second place Best Student Paper Awards at 2008 and 2011 RFIC symposiums, the 2009 CITRIS (Center for Information Technology Research in the Interest of Society at UC Berkeley) Big Ideas Challenge Award and the UC Berkeley Bears Breaking Boundaries award, and the 2010–2011 as well as 2014–2015 Qualcomm Innovation fellowships. He currently serves on the TPC for the European Solid-State Circuits Conference and the Radio Frequency Integrated Circuits (RFIC) Symposium.