A 0.13 μm CMOS System-on-Chip for a 512 × 424 Time-of-Flight Image Sensor With Multi-Frequency Photo-Demodulation up to 130 MHz and 2 GS/s ADC

Cyrus S. Bamji, Patrick O'Connor, Tamer Elkhatib, *Associate Member, IEEE*, Swati Mehta, *Member, IEEE*, Barry Thompson, *Member, IEEE*, Lawrence A. Prather, *Member, IEEE*, Dane Snow, *Member, IEEE*, Onur Can Akkaya, Andy Daniel, Andrew D. Payne, *Member, IEEE*, Travis Perry, Mike Fenton, *Member, IEEE*, and Vei-Han Chan

***Abstract*—We introduce a 512 × 424 time-of-flight (TOF) depth image sensor designed in a TSMC 0.13 μm LP 1P5M CMOS process, suitable for use in Microsoft Kinect for XBOX ONE. The 10 μm × 10 μm pixel incorporates a TOF detector that operates using the quantum efficiency modulation (QEM) technique at high modulation frequencies of up to 130 MHz, achieves a modulation contrast of 67% at 50 MHz and a responsivity of 0.14 A/W at 860 nm. The TOF sensor includes a 2 GS/s 10 bit signal path, which is used for the high ADC bandwidth requirements of the system that requires many ADC conversions per frame. The chip also comprises a clock generation circuit featuring a programmable phase and frequency clock generator with 312.5-ps phase step resolution derived from a 1.6 GHz oscillator. An integrated shutter engine and a programmable digital micro-sequencer allows an extremely flexible multi-gain/multi-shutter and multi-frequency/multi-phase operation. All chip data is transferred using two 4-lane MIPI D-PHY interfaces with a total of 8 Gb/s input/output bandwidth. The reported experimental results demonstrate a wide depth range of operation (0.8–4.2 m), small accuracy error (<1%), very low depth uncertainty (<0.5% of actual distance), and very high dynamic range (>64 dB).**

***Index Terms*—Natural user interface (NUI), time-of-flight (TOF), quantum efficiency modulation (QEM), range imaging, 3D imaging.**

I. Introduction

TRADITIONAL monochrome and RGB imaging systems produce two-dimensional (2-D) images, which are appropriate for display purposes. However, when a computer vision system attempts to recognize, interpret, and track objects in a 2-D image, the task becomes error-prone because object size, distance, and shape are not always readily determinable. For such computer scene analysis, it is beneficial to provide the image-processing algorithm with depth information from which these parameters can be robustly determined. Three-dimensional (3-D) cameras, which include optical time-of-flight (TOF) cameras described herein, provide such depth information.

Generally, 3-D acquisition techniques can be classified into two broad categories: geometrical methods [1], [2], which include stereo and structured light, and electrical methods, which include ultrasound or optical TOF described herein. The operating principle of optical TOF is based on measuring the total time required for a light signal to reach an object, be reflected by the object, and subsequently be detected by a TOF pixel array. Optical TOF methods can be classified in two subcategories: 1) based on stopwatch technique [3], [4] and 2) accumulated charges principle [5], [8].

Stopwatch TOF methods are commonly implemented using single-photon avalanche diodes (SPADs) [9]. In this method, the round-trip time of a single light pulse is measured by generating a trigger signal to stop the time measurement in the circuit upon detection of the reflected signal [4]. The reported range of operation varies from a few meters to several kilometers using low optical signal power [3]. For good depth resolution, the imagers are required to emit and detect picosecond laser pulses [10]. Moreover, on-chip time-to-digital or time-to-amplitude converters required for this approach can use a significant pixel area, which can limit pixel array sizes. Pixel arrays of size 32×32 [3] and 4×64 [11] have been demonstrated with pixel sizes of $58 \times 58\ \mu m^2$ and $130 \times 300\ \mu m^2$, respectively.

In the most common embodiment of accumulation-based TOF imagers, such as the one described in this work, the phase difference between the amplitude modulated emitted light wave and the detected wave reflected off the object is measured from which the distance is calculated. Photo-generated charges are integrated over a long period of time, and the distance is computed from the integrated signal. These methods classify the photons arriving at a pixel into two or more groups based on their arrival time. This process is achieved using either an external shutter or on-chip CMOS/CCD structures. In this approach, the depth resolution increases with the light source modulation frequency. A depth resolution of 5 cm was demonstrated in [5] at 7.5 m and 20 MHz, and a precision of 2.7 cm was shown in [7] over a range of 0.2–6 m at 50 MHz. Generally, charge integration can be achieved at the pixel level with less silicon area, enabling larger arrays. An example of a large array was demonstrated in [8] with an array size of 176×144 with 40 μm pixel pitch.

In this work, the goal is to design and develop a 3-D imaging technology for gesture and identity recognition in living room

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The authors are with Microsoft, Mountain View, CA 94043 USA.

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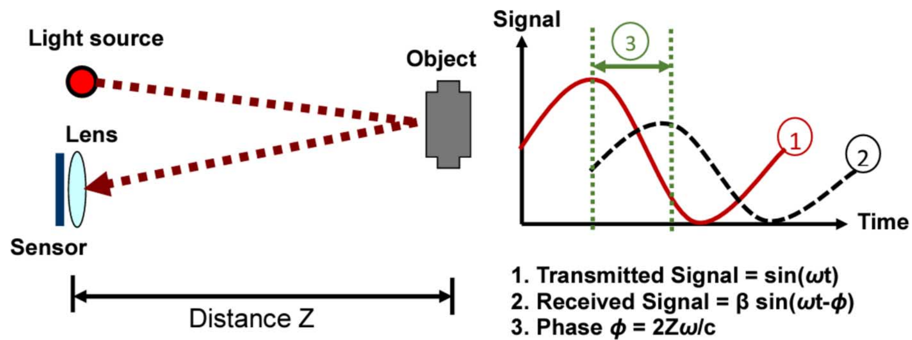

Fig. 1. Operation principle of TOF system.

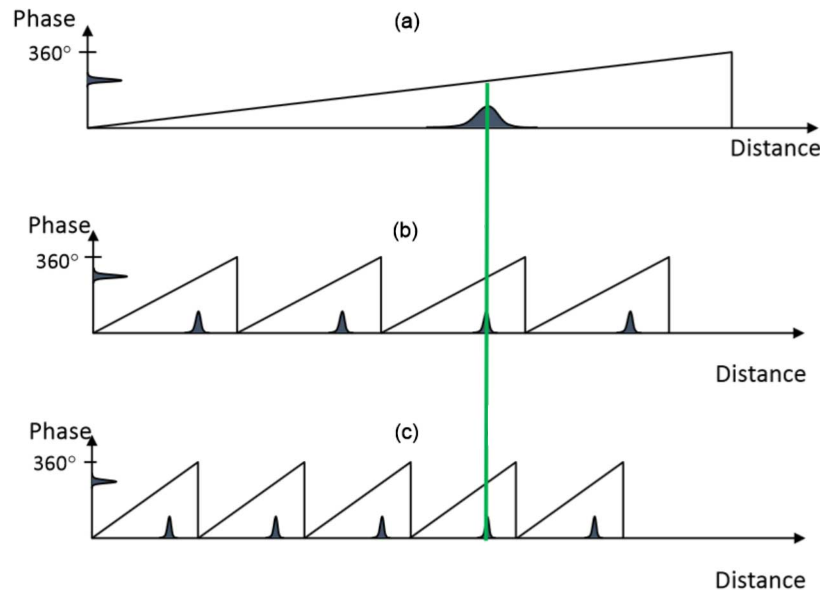

Fig. 2. ToF multi frequency operation. (a) Low-frequency f_0 has *no* ambiguity but large depth uncertainty. (b) High-frequency f_1 has more ambiguity but small depth uncertainty. (c) Another high-frequency f_2 with small depth uncertainty.

applications. The same components and techniques can be used in battery-operated devices with much lower power consumption because the area to be illuminated is far smaller resulting in lower power in both the light source and chip due to very short integration times. The requirements for the 3-D system include several difficult to meet constraints, such as a wide field of view (FOV) of $70^\circ \times 60^\circ$, and a small minimum detectable object size of 2 cm × 2 cm for detecting hand gestures at 3.5 m. Moreover, a large depth range of 0.8 m to 3.5 m and reflectivity between 10%–100% should be accommodated, and all objects that meet the minimum object size and reflectivity criteria anywhere in the scene, even in the presence of 3 Klx of bright indoor ambient light, should be imaged within an uncertainty spec of 1% of the object distance (and 1.5% accuracy error). To avoid excessive blurring, the data must be acquired in less than 20 msec. Calibration time must be kept to a minimum, and accuracy and performance must be maintained over millions of parts and over relatively uncontrolled operating conditions.

In this paper, we will present the detailed design of the 512×424 TOF system-on-chip (SoC) designed in a TSMC 0.13 μm CMOS process, suitable for use in Microsoft Kinect for XBOX ONE that meets the indoor requirements explained above. In the following sections, we will start with a brief introduction of the operating principle of our TOF system. Then, we will explain the sensor chip architecture focusing on the main blocks from pixel design to readout engine. Finally, we will show experimental results from the sensor system.

II. Phase Time-of-Flight

The operation principle of a TOF depth sensor is illustrated in Fig. 1. The signal amplitude transmitted by the optical source is represented as $\sin(\omega t)$, where $\omega = 2\pi f$ is the modulation frequency. The TOF required for this signal to traverse the distance z to the object, be reflected, and subsequently be detected by the TOF sensor introduces a phase shift $\varphi = 2z\omega/c$, where c is the speed of light in air. The amplitude of the received signal β is a function of several factors, such as input light power and reflectivity of the object, however, the phase shift φ depends only on the distance of the photodetector to the object and the refractive index of the medium where the imaging takes place.

In our TOF chip, the clocks driving the optical detector and the optical source are modulated in synchrony. The received signal $\beta \sin(\omega t - \varphi)$ is mixed with a phase-delayed form of the signal driving the optical source $\sin(\omega t - \varphi_{\text{offset}})$, which after low-pass filtering yields $0.5\beta\cos(\varphi - \varphi_{\text{offset}})$.

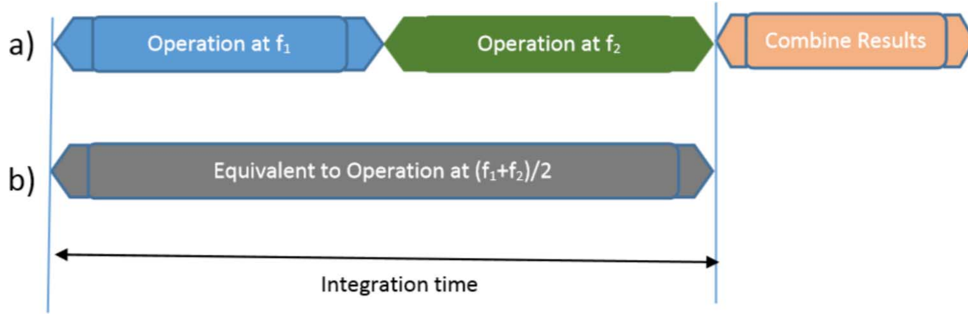

Fig. 3. TOF multifrequency operation sequence.

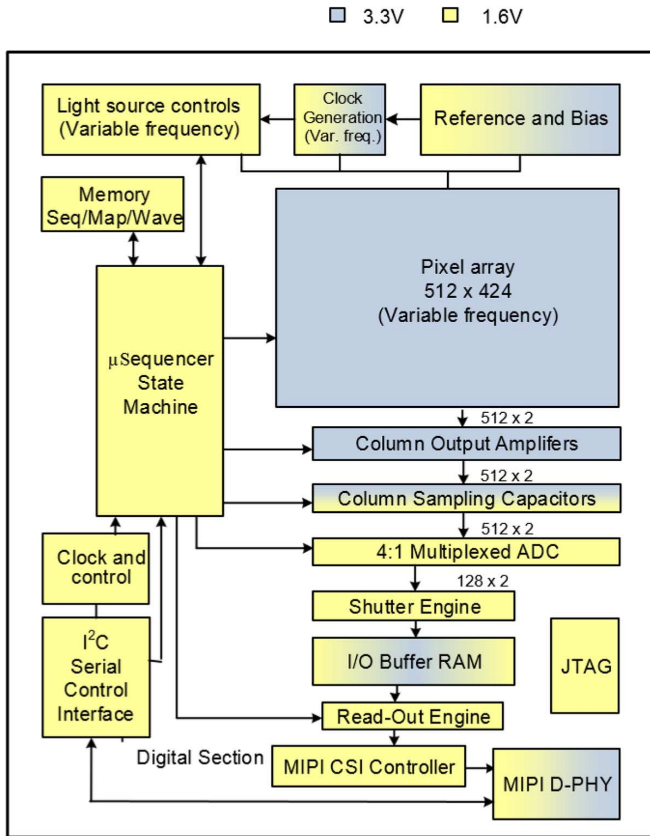

Fig. 4. Sensor architecture block diagram.

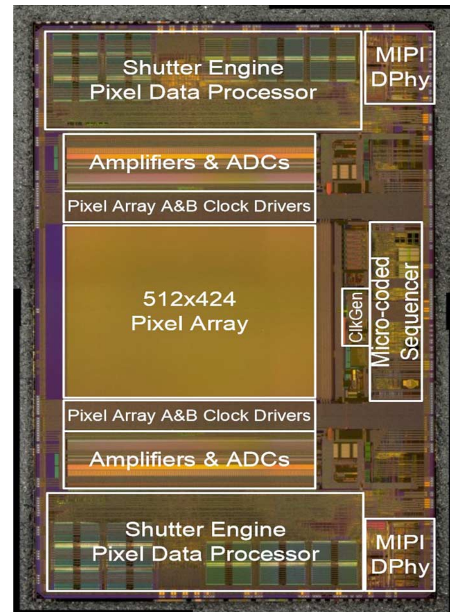

Fig. 5. Chip micrograph.

This on-chip mixing is achieved by differentially modulating the quantum efficiency of the detectors in the pixel array as described in Section III-A. The quantum-efficiency-modulation (QEM)-based detection can be performed at different input signal phases, such as 0°, 90°, 180°, 270°. This multi-phase measurement yields output values such as $\cos(\varphi+0°)$, $\cos(\varphi+90°)$, $\cos(\varphi+180°)$ and $\cos(\varphi+270°)$ and enables calculation of a unique phase angle φ for each distance independent of the received signal amplitude β. In theory, two phases are sufficient for this calculation; however, using more than two phases can cancel offsets, and reduce harmonics in the measurements thereby resulting in much better depth data.

Fig. 2 illustrates the phase φ, as a function of distance z for three different modulation frequencies. As shown in Fig. 2(a), at low frequency f_0, the phase wraparound takes place less frequently, allowing an extended range of operation without ambiguity in the measured distance. However, a given phase uncertainty yields a large depth uncertainty as shown. Fig. 2(b) shows a high-frequency f_1 operation, in which the phase wraparound takes place at shorter distances, causing more ambiguity (more possible solutions) in the distance measurement. However, depth uncertainty is smaller for a given phase uncertainty. Fig. 2(c) shows another high-frequency f_2 operation. Using two frequencies, for example, f_1 and f_2 shown in Fig. 2(b) and (c), it is possible to disambiguate the distance measurement by picking a consistent depth value across the two frequencies [12], [13], as shown in Fig. 2(b) and (c). The depth values for f_1 and f_2 are then averaged together to produce an even smaller depth uncertainty than either f_1 or f_2 alone. This uncertainty is approximately the uncertainty of the average frequency of f_1 and f_2 applied to the total integration time required.

Fig. 3(a) shows the sequence of operations. The first phase is obtained for frequency f_1 (e.g., 80 MHz) of Fig. 2(b), then the phase is obtained for frequency f_2 (e.g., 100 MHz) of Fig. 2(c). Finally, a formula that disambiguates and combines the phase from frequencies f_1 and f_2 is applied to yield the final depth

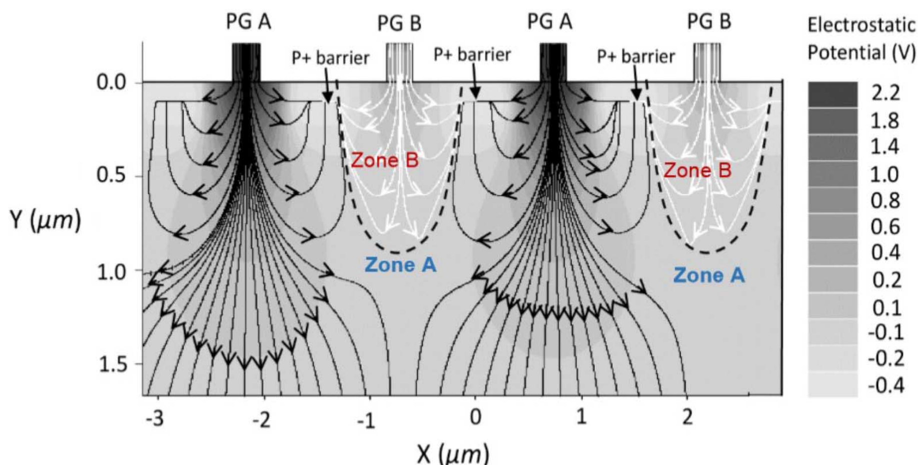

Fig. 6. Device simulation of TOF detector.

result. The uncertainty (jitter) of the final calculated depth is approximately the same as using a frequency $(f_1 + f_2)/2$ (e.g., 90 MHz) for the combined integration time as shown in Fig. 3(b). It can be shown that the range over which unambiguous operation is possible is many times greater than either f_1 or f_2 (e.g., the operating range is often proportional to f_1-f_2 which in this case is 100 MHz$-$80 MHz $=$ 20 MHz).

III. Sensor Chip Architecture

A block diagram of the TOF SoC architecture is illustrated in Fig. 4, and a chip micrograph is presented in Fig. 5. The sensor array is comprised of 512×424 fully differential TOF pixels. The pixel array is divided into a top and bottom half each driven by separate clock drivers and with pixel outputs read out from each half separately. A high-speed internal oscillator drives a clock generator, which generates the pixel clocks as well as the modulation signal to the light source. Modulation frequency and relative phase of the pixel clocks and the light source modulation signal are programmable. Programmable gain differential amplifiers (PGA), one for each of the 512 columns across both the top and bottom of the pixel array, are used to condition the array's analog output. The outputs of each of four adjacent PGAs are multiplexed into 256 10 bit ADCs (128 each on the top and bottom of the pixel array). Each of the 256 ADCs operates at a conversion rate of 8 MS/s, resulting in a row conversion rate of 2 GS/s.

The operation of the chip is managed by two shutter engines (top and bottom) and a micro-sequencer state machine. The shutter engines process the ADC outputs generated from the top and bottom halves of the pixel array normalizing for the correct integration time and gain. The programmable micro-sequencer maximizes flexibility in performance tuning of the sensor, by allowing adjustment of the sequencing and timing of the pixel and light source clocks, received light integration, array readout, and transfer of data to the external data interface. The micro-sequencer program is stored in the on-chip SRAM. The chip's pixel data output is controlled by the read-out engine, which reads shutter engine results from the FIFO in I/O Buffer RAM and packetizes them for transmission via a MIPI high speed serial interface. The main blocks of the sensor architecture are described in more detail below.

A. Pixel Design

Fig. 6 illustrates a cross-sectional view of the designed TOF detector, showing potential distribution and electrical field lines, while a top-view layout of the same TOF detector is shown in Fig. 7 integrated with a pixel schematic. Our TOF detector has positively biased polysilicon gates (PG A, B) connected to two substantially complementary clock signals (ClkA and ClkB). These poly gates create electric fields that attract and collect photo charges based on their arrival time under the gate oxide. Collected photo charges always remain under the gate where they are initially collected and ultimately diffuse slowly by self-repulsion under each poly gate to an n+ collection node (FD A, B). A p-type doped area between the gates creates a potential barrier that ensures charges collected by one poly gate are never transferred to an adjacent poly gate even if one is at a higher potential.

Fig. 6 shows the electric field lines for the case of A gates biased at 0 V and B gates at 3.3 V. The electric field lines run tangent to the boundary of the A and B zones (never from A to B), so charges never transfer from A to B. The large photonic charge collection region, ZoneA of A, is shown with dark electrical field lines. Most photo charges generated in ZoneA while ClkA is high are predominantly collected by poly gate A, and only a few photo charges generated in ZoneB, shown with light electrical field lines, are collected by poly gate B. When ClkB is high and ClkA is low, poly gate B will predominantly collect photogenerated charges. Thus, our TOF detector is collecting and assigning photocharges with their arrival time with respect to the modulation clocks ClkA and ClkB. As the sizes of ZoneA and ZoneB are modulated under the influence of ClkA and ClkB, this method is called differential Quantum Efficiency Modulation (QEM) [6].

The charge assignment (classification to PG A or B) in the above method occurs simultaneously with charge collection under the poly gates, and does not need the additional step of shifting charges from one gate to another, which is usually used

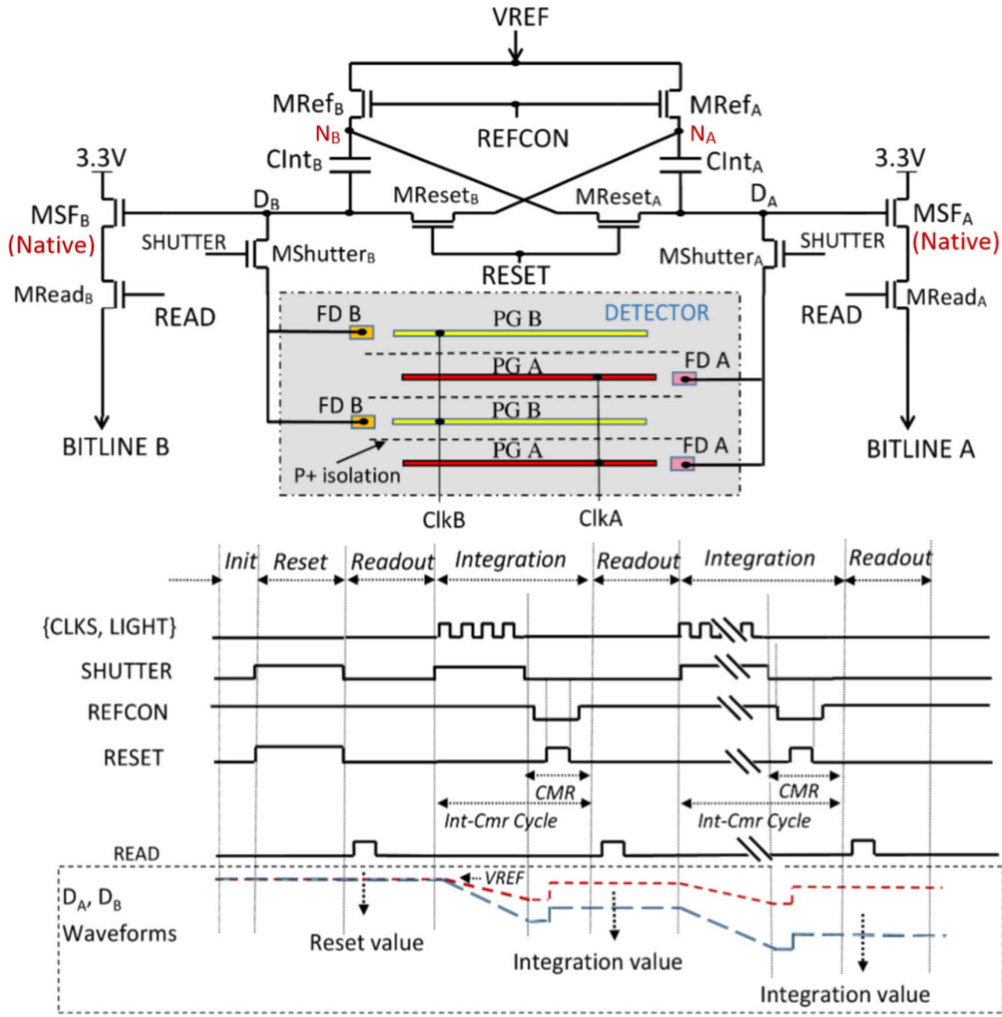

Fig. 7. Pixel schematics and timing diagram.

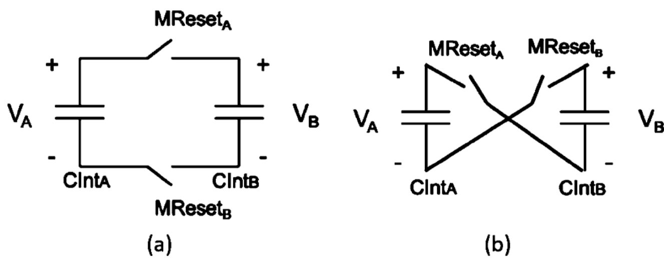

Fig. 8. CMR circuit concept.

in other TOF detector methods making it very well suited for high modulation frequency. Ultimately charges are collected at the (remote) n+ node, but timing of that operation does not need to be accomplished rapidly as it is completely decoupled from the critical charge assignment operation.

In order to achieve high modulation contrast (MC) at high frequencies, the chip was fabricated by using a 0.13 μm mixed-signal low-power CMOS process with minor modifications to support efficient TOF operation. Starting epi material was optimized in thickness and dopant concentration for maximum performance. Special attention was paid to produce a desirable doping gradient and avoid unintentional side effects such as auto-doping. Dedicated implant steps were adopted in pixels to set the required work functions, and provide suitable isolation and well profiles. Five layers of aluminum metal were used to enable front-side illumination and facilitate pixel design, power distribution and SoC integration. Microlenses are added after CMOS processing and are codesigned with the pixels to double the effective fill-factor. All optical interfaces were properly managed to minimize reflection.

The TOF pixels designed here operate with an MC of 67.5% at 50 MHz (and down to 56.5% at 130 MHz) and a responsivity of 0.14 A/W at 860 nm. The MC is calculated from the experimentally measured convolution curve of the pixel differential signal versus the complete cycle phase shift of the modulated light source, wherein MC is equal to maximum differential signal divided by common mode signal (after ambient subtraction): maximum of $(\mathrm{A}-\mathrm{B})/(\mathrm{A}+\mathrm{B})$. This MC measurement is independent of both active light source power and room ambient light. However the method measures the MC of the system taking into account the characteristics of the actual laser used in the production system (i.e., MC of the chip with a perfect laser is higher than stated here). Each pixel in the 512 × 424 array is 10 μm × 10 μm, and has a fill-factor of 31% without μlens, and 60% with μlens. The pixel is fully differential, which makes

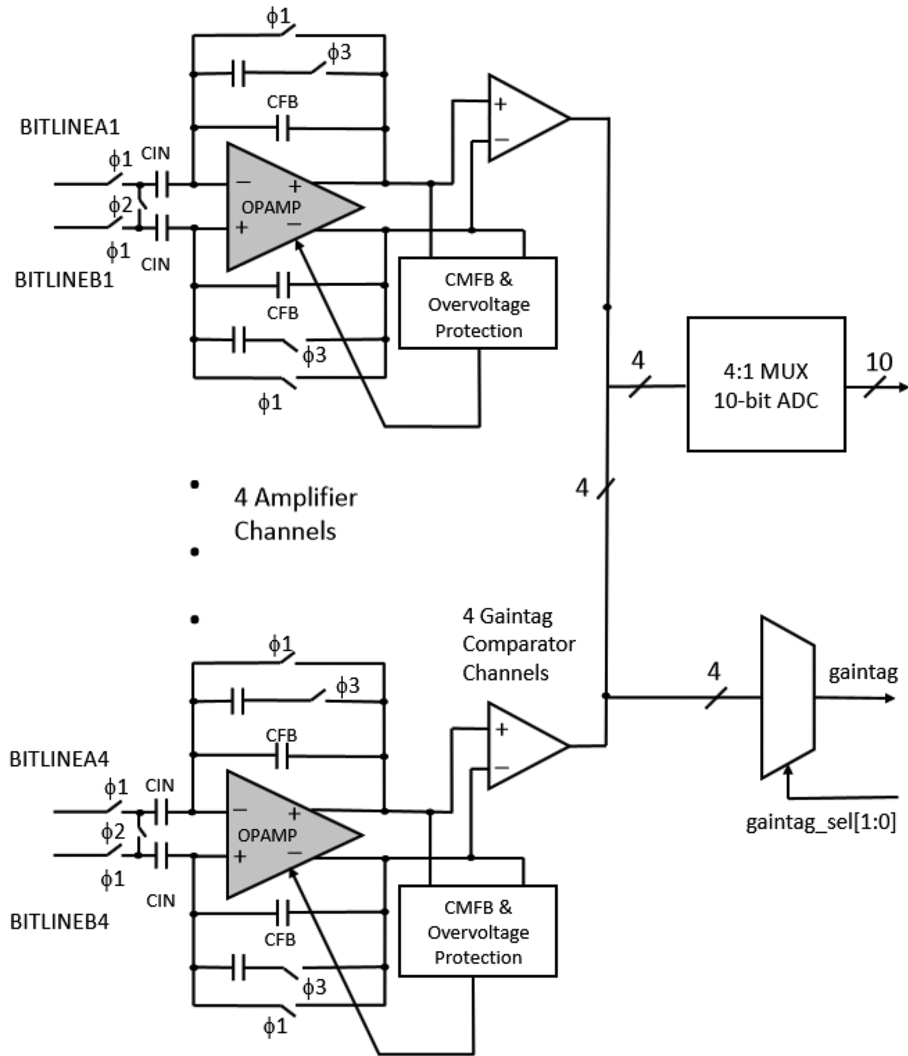

Fig. 9. Readout circuit block diagram.

it resistant to many design issues that plague single-ended designs, but makes matching and symmetry very important. As shown in the schematics in Fig. 7, the pixel is comprised of 10 NMOS transistors, which include a pair of native source followers and row-select for each side and 2 MIM Caps $\mathrm{CInt_A}$ and $\mathrm{CInt_B}$ to store the integrated signal. The sequence of operation for one particular frequency and phase is shown in the timing diagram of Fig. 7. Multiple captures are combined to detect depth information. To reset the detector and capacitors $\mathrm{CInt_A}$ and $\mathrm{CInt_B}$ the global signals Refcon, Shutter & Reset are high. Both plates of the capacitors are connected to voltage Vref as shown in plots for $\mathrm{D_A}$ & $\mathrm{D_B}$. Reset is then turned off and the row select signal Read is turned on to take a Reset sample $(\mathrm{BitlineA^{Reset}} - \mathrm{BitlineB^{Reset}})$ through the native source followers $\mathrm{MSF_A}$ & $\mathrm{MSF_B}$ for correlated double sampling (CDS). CDS cancels the reset kT/C noise, fixed pattern noise and offsets caused due to mismatches.

During integration, ClkA & ClkB are modulated 180 degrees out of phase for time $\mathrm{t^{Int1}}$ at the chosen modulation frequency. The phase of the received light with respect to ClkA & CLkB determines the integrated signals $\mathrm{D_A}$ and $\mathrm{D_B}$ as shown in Fig. 7. At the end of integration, ClkA & ClkB are turned OFF and Read is turned ON row-wise to sample the integrated signal $(\mathrm{BitlineA^{Int1}} - \mathrm{BitlineB^{Int1}})$. In a multi-shutter scenario, this sequence of operation is repeated with different exposure times (e.g., $\mathrm{t^{Int2}}$, $\mathrm{t^{Int3}}$) followed by sampling of the integration signal before the pixel is Reset again for the next light phase/frequency. To avoid pixel Common-Mode saturation in the presence of large amounts of ambient light e.g., sunlight while still remaining sensitive to the differential signal due to active modulated light, the common mode dynamic range of the pixel can be increased by an operation called common-mode-reset (CMR) [14]. The sequence of operation during CMR is shown in Fig. 7 which results in node $\mathrm{D_A}$ being connected to node $\mathrm{N_B}$ and $\mathrm{D_B}$ to $\mathrm{N_A}$. Using the theory of conservation of charges, if capacitors $\mathrm{Cint_A}$ and $\mathrm{Cint_B}$ are connected as shown in Fig. 8(a), $\Delta\mathrm{V_A} + \Delta\mathrm{V_B} = \mathrm{constant}$ while $\Delta\mathrm{V_A} - \Delta\mathrm{V_B} = 0$ resulting in common-mode being preserved while differential signal is destroyed. By cross-connecting the two storage MiM capacitors in the pixel [Fig. 8(b)], the common-mode signal $\Delta\mathrm{V_A} + \Delta\mathrm{V_B} = 0$ while the differential signal $\Delta\mathrm{V_A} - \Delta\mathrm{V_B} = \mathrm{constant}$. This results in the

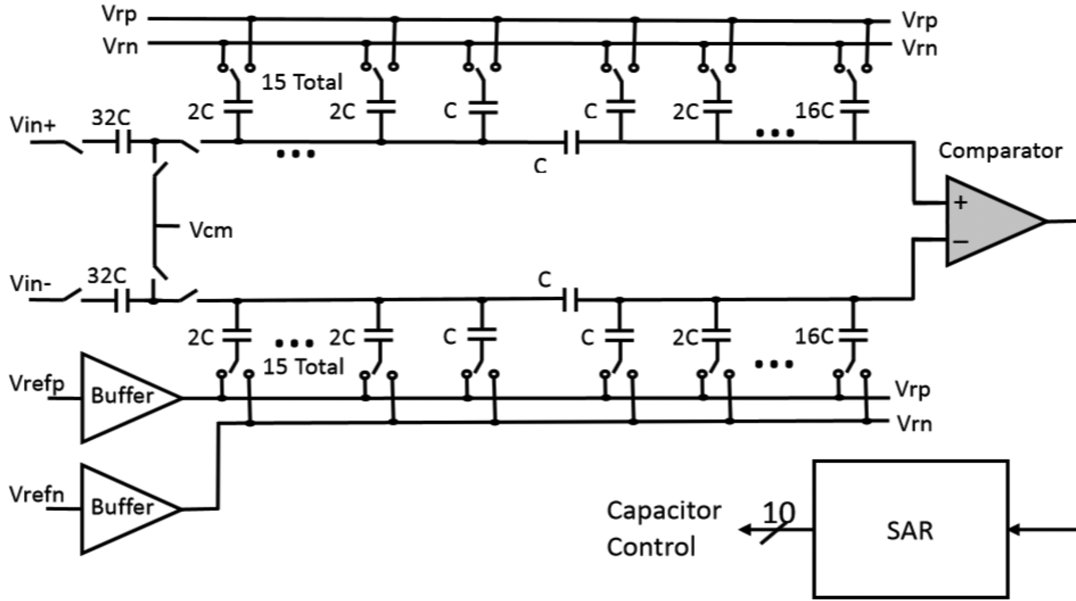

Fig. 10. ADC block diagram.

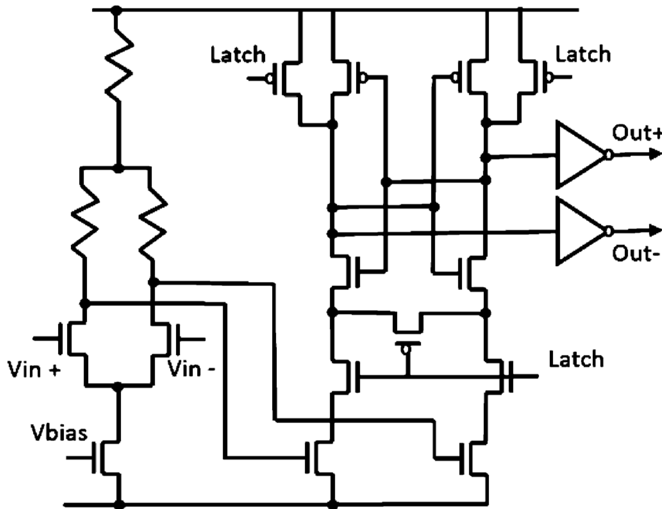

Fig. 11. Schematic of the latching comparator used in the ADC.

differential signal being preserved while the common-mode signal is cancelled thus increasing the common mode dynamic range without a need for reset. In the absence of circuit parasitics, the kT/C noise introduced by this operation is only in the common mode domain and does not affect the differential signal. However, in the presence of circuit parasitics, neither is the common-mode cancelled completely nor is the differential signal preserved fully nor kT/C cancelled fully. Thus the CMR operation should be used sparingly depending on the ambient light conditions to minimize differential signal loss.

B. Amplifiers and ADC

TOF creates constraints on readout circuits similar to those on higher frame rate cameras. Multi-phase, multi-frequency operations restrict the light exposure time available for each image capture. Readout time must be minimized so that available exposure time is maximized. Motion blur constraints further reduce the time available for exposure and readout.

The readout architecture shown in Fig. 9 achieves high throughput by combining a 10 μm pitch column amplifier with a 40 μm pitch 4:1 multiplexed ADC. Readout speed is further doubled by dedicating independent readout circuits to the top and bottom halves of the sensor array. A total of 256 ADCs and 1024 amplifiers produce over 2 GS/s and can perform a complete sensor array (differential) readout in approximately 100 us. This represents higher readout capacity/pixel than most other reported RGB cameras [15]–[17] and is comparable to high definition cameras.

An offset-cancelled switched-capacitor programmable-gain circuit amplifies the small differential voltages generated by the pixel to levels suitable for digital conversion. It also desensitizes the system performance from ADC noise while achieving a column gain mismatch of less than 1%. During the first phase of operation, the sensor outputs are connected to the bottom plates of C_{IN} while the amplifier offset is connected to the top plates. During the second phase, the input signal is amplified by shorting the C_{IN} bottom plates together and transferring the input capacitor charge to the feedback capacitors. The gain is then

$$A = \frac{C_{\rm IN}}{C_{\rm FB}}. \tag{1}$$

Multigain operation occurs during the third phase when the amplifier output is compared with the ADC reference voltage. If the output voltage is too large, then more feedback capacitance is added, thus decreasing the gain. This overflow event is reported to the system along with the ADC data.

It has been noted in [13] that most image sensor designs with more than 200 Mpixel/s readout capacity use column-parallel ADCs. The settling time constant in a CMOS circuit is generally

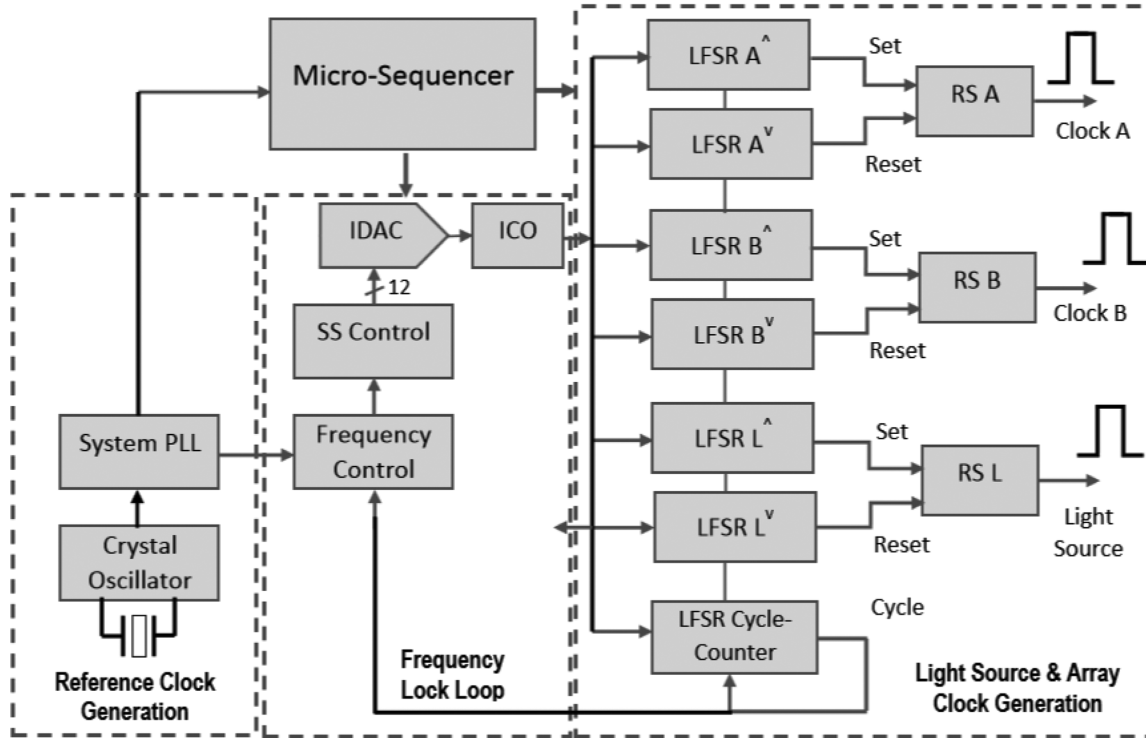

Fig. 12. Clock generation block diagram.

given by

$$\tau = \frac{g_m}{C} = \frac{\sqrt{2k'\frac{W}{L}I_D}}{C}. \tag{2}$$

Sampled kT/C noise limits the smallest allowable capacitance for a given noise floor. Since decreasing settling time requires quadratically more current, architectures with greater numbers of slower ADCs will usually use less power than architectures relying on a small number of very fast ADCs.

The most common column parallel ADC architectures are Single Slope (SS), Cyclic, and Successive Approximation (SAR). SS converters require 2^{N} clock cycles for conversion and are not suitable for the very high readout rates required in this TOF application. Cyclic converters require one or more precision opamps per converter. While SAR converters require a precision DAC, very fast charge redistribution DACs implemented in low voltage thin-oxide transistors make this a promising architecture for this application.

The block diagram of the ADC is shown in Fig. 10. The differential input is sampled on 192 fF sampling capacitors while a mid-scale value is selected on the capacitive charge redistribution DAC. Successive approximation logic then drives a binary search driven by decisions from a latching comparator with schematic shown in Fig. 11.

The DAC includes a 16-segment thermometer-coded main DAC coupled to a 6 bit binary weighted sub-DAC. All of the DAC capacitors are implemented as multiples of a 6 fF MIM unit-capacitor. Globally generated reference levels are locally buffered in each of the 256 converters to allow for fast settling. Thin-oxide transmission gates, small capacitance, and a high performance comparator allow an 80 MHz decision rate and 8 MS/s sampling rate for 10 bit conversions. The conversion speed is limited primarily by settling of the reference lines connected to the bottom plates of the DAC capacitors.

Each ADC is 40 μm wide matching 4 pixel widths and is 550 μm tall. Measured performance includes differential nonlinearity $(\mathrm{DNL}) = \pm 2$ LSB, integral nonlinearity $(\mathrm{INL}) = \pm 4$ LSB, and Noise Floor $= 0.8$ LSB. The ADC has a $\pm$650 mV differential full-scale range while operating from a 1.5 V supply and dissipating 750 μW. The local reference buffers are counted in both the area and power reported.

C. Clock Generation

The clock generation block creates the pixel array (A and B) and light source clocks from a common high speed *clock root*, the current controlled oscillator (ICO). Thus the relative phase (and frequency) of the clocks are precisely controlled. The block diagram of the clock generation is shown in Fig. 12. It takes a two-phase, high frequency input (up to 1.6 GHz), from the ICO and produces light-source, and pixel array clock outputs. The linear feedback shift registers (LFSRs) are loaded by the micro-sequencer (described later) and produce an output pulse when their programmed count is reached. They are composed of true single-phase clock (TSPC) dynamic flip-flops [18] shown in Fig. 13(a) which are capable of operating at frequencies of 1.6 GHz and are arranged in two 8 bit shift register stages each running at the ICO clock rate. The value loaded in the cycle counter LFSR determines the cycle count and the edges of the generated clocks are determined by the pattern loaded into the other LFSRs. Inserted between each 8 bit LFSR output and the RS-latch inputs is the half-cycle logic circuit shown in Fig. 13(b). This logic allows selectively adding a half-cycle of

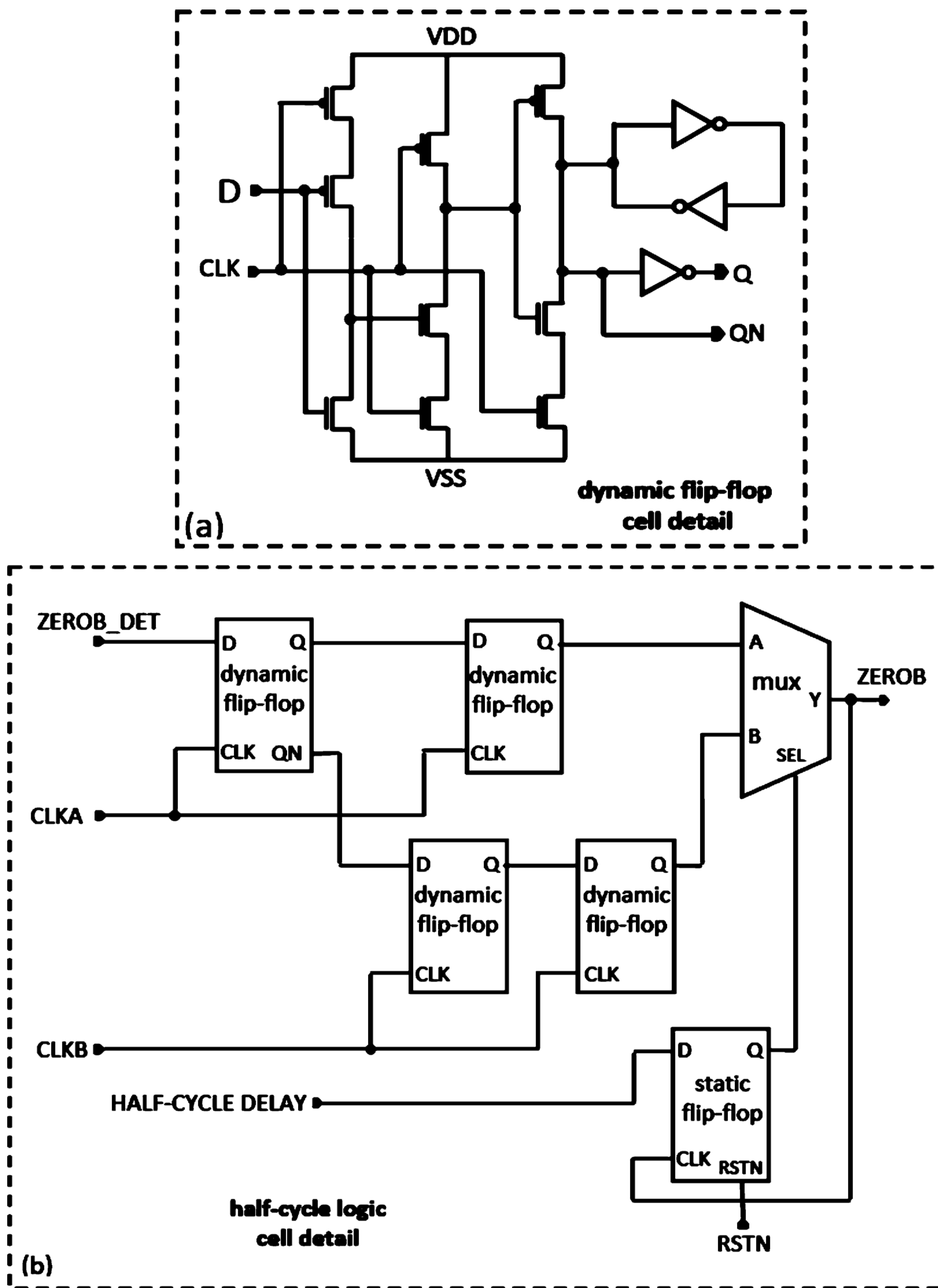

Fig. 13. TSPC. (a) Dynamic flip-flop. (b) Half-cycle logic.

the ICO clock to the output pulse by utilizing the other phase of the ICO clock, making half-cycle resolution possible.

The frequency-lock loop, depicted in Fig. 14, is composed of a high frequency divider, frequency control, spread spectrum (SS) control, 12 bit current-mode DAC, and a four stage differential ICO. The frequency-lock loop has both fast and slow lock modes. The digital feedback loop can be enabled and disabled on the fly by the micro-sequencer, more importantly the closed-loop DAC code can be stored and restored for each frequency to facilitate fast frequency switching. The closed-loop mode is employed during the time that the image sensor is not actively capturing an image in order to correct for slow frequency drift mechanisms. In a similar manner, the ICO frequency is intentionally dithered to spread the frequency spectrum. This is accomplished by putting the frequency-lock loop in open-loop mode and updating the DAC code with respect to the closed-loop value appropriately to generate a desired frequency dithering. To achieve a wide capture range, symmetric-load delay cells are employed with an optimized load biasing scheme. The ICO is a four-stage

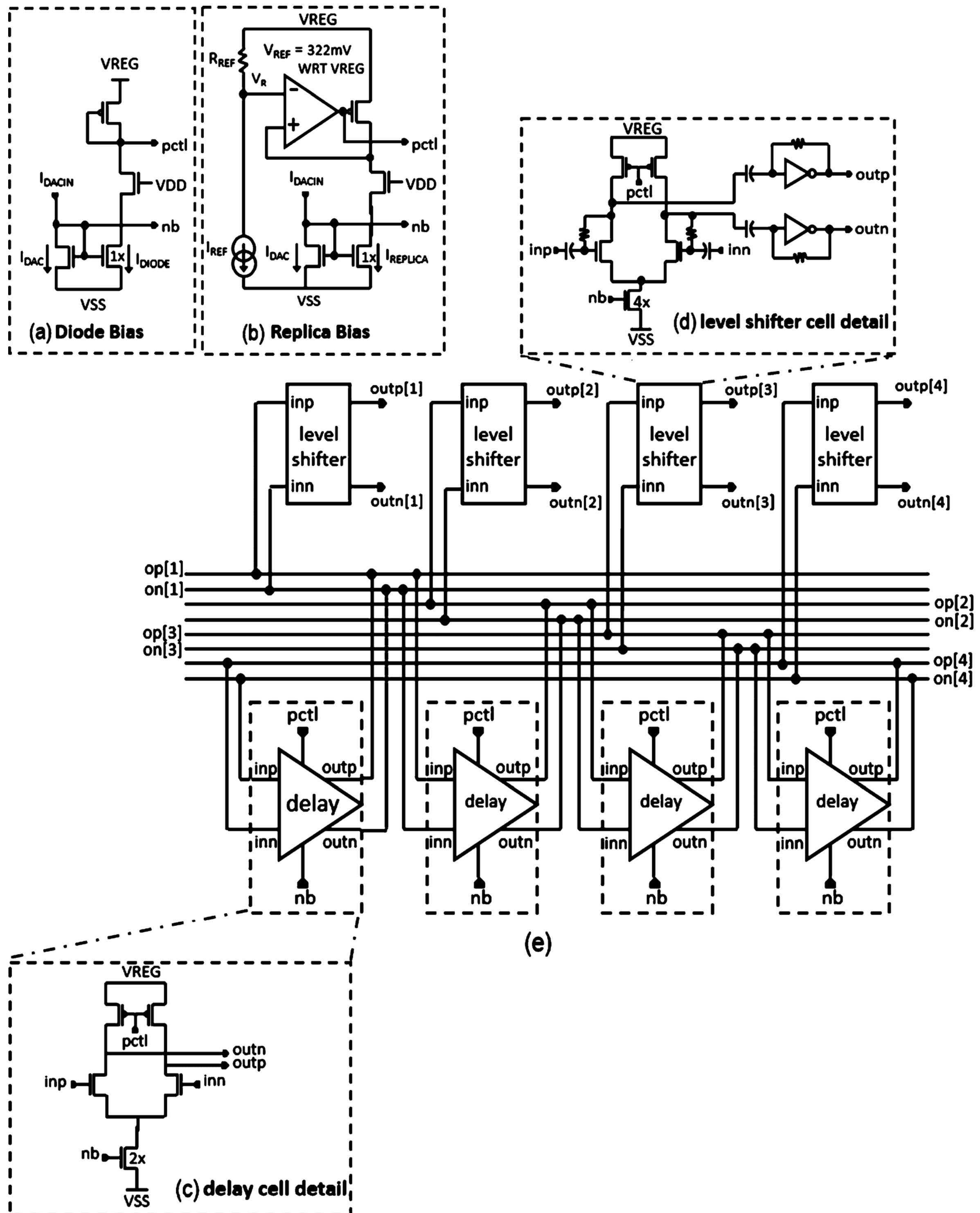

Fig. 14. Current controlled oscillator. (a) Diode-connected bias reference. (b) Replica bias reference. (c) Symmetric-load delay cell. (d) AC-coupled level-shifter. (e) Four-stage differential ring oscillator.

differential ring oscillator composed of symmetric-load delay cells shown in Fig. 14(e). The circuit is realized with replica biasing, shown in Fig. 14(b), and a symmetric-load delay cell, depicted in Fig. 14(c) and offset voltage insensitive ac-coupled level-shifter stages in Fig. 14(d) which have time-constants designed to support the lowest frequency required. The combination of the symmetric-load delay cell and the proposed replica biasing extends the frequency capture range. The replica bias circuit consists of a half delay-cell in a feedback loop which serves to keep the V_{DS} of the P-channel load transistors of the delay cell equal to V_{REF}. This arrangement forces the delay cell P_{CH} load impedance to be $R_{DS} = V_{REF}/I_{DS}$; where, I_{DS} is proportional to I_{DAC} and the voltage across R_{REF}, $V_{REF} = V_{REG} - V_R$. The frequency that the oscillator can

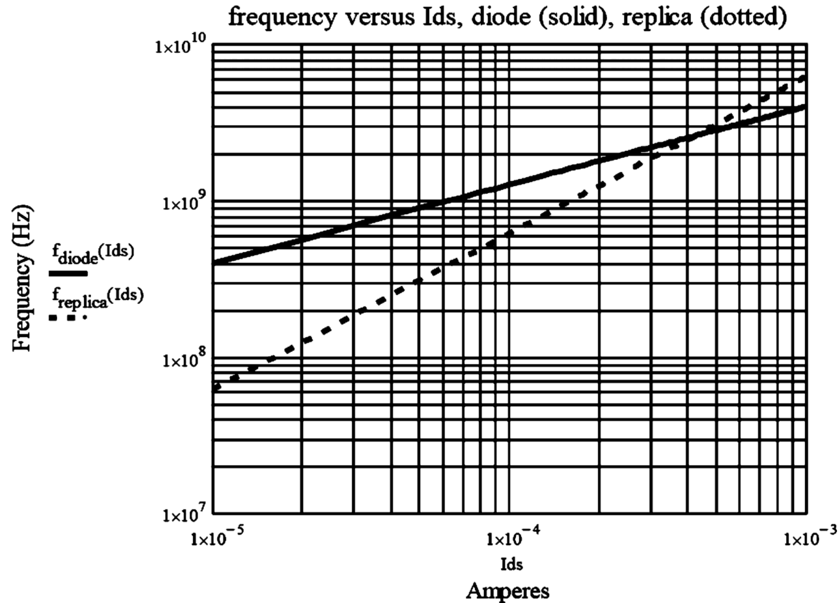

Fig. 15. Frequency versus I_{DS} for diode-connected versus replica bias.

support given the diode connected bias reference in Fig. 14(a) is given by

$$f_{diode} = \frac{1}{4} \frac{2\sqrt{I_{ds} \cdot k_p \cdot \frac{W_p}{L_p}}}{2\pi \cdot C_0} \tag{3}$$

where $kp \cdot (W_p)/(L_p) = 1 \times 10^{-3}$ (A/V^2), and $C_0 = 2.01 \times 10^{-14}$ (F) for this design.

The ICO frequency versus current for the proposed replica bias reference in Fig. 14(b) is given by

$$f_{replica} = \frac{1}{4} \cdot \frac{I_{ds}}{2\pi \cdot V_{ref} \cdot C_0} \tag{4}$$

where $V_{REF} = V_{REG} - V_R = 322$ mV for this design.

Fig. 15 shows a comparison of ICO frequency versus current given by (3) and (4) for the diode connected bias reference and proposed replica bias reference, respectively. The replica biasing circuit manipulates the R_{DS} curve of the P_{CH} loads of the differential delay cell to extend the frequency capture range of the ICO, at both low- and high-frequency extremes, well beyond what would normally be possible with comparable ICOs [19]; moreover, it can be tuned by the selection of the independent variable V_{REF}. The replica biasing keeps the P_{CH} loads in the linear region overcoming the drawbacks listed for the symmetric-load delay cell in [20] while drawing on its strength of good power supply noise rejection. Diode-connected N_{CH} clamps, not shown, are added in parallel with the loads to limit the swing at low frequency with minimal impact to the high-frequency performance. The replica bias circuit keeps the load $R_{DS} = V_{REF}/I_{DS}$, where I_{DS} is proportional to I_{DAC}. V_{REF} must be chosen to keep the V_{DS} sufficiently low to keep the P_{CH} load transistors in the triode region of operation while keeping the loop gain sufficiently high to sustain oscillation at the lowest R_{DS} targeted for the design. The typical capture range for this ICO design spans 320 MHz to >4 GHz; note that lower frequencies are possible, this design is intentionally limited by a pedestal current.

D. Shutter Engine

The shutter engine receives data from the ADC and performs three important functions. First, it performs differential CDS to remove differential reset kT/C noise in the Pixel. Differential CDS reset values are stored in on-chip RAM and are subtracted from the final values read from the Pixel.

Second, it normalizes (multiplies by a coefficient) the digital input data with respect to the amplifier gain, correcting for known amplifier gain variation using per amplifier calibration data. Two tag bits generated by the array column amplifiers in Fig. 9 are used to determine the gain used and the corresponding normalization coefficients.

Third, it merges the data from multiple shutters choosing the best shutter value for each Pixel. This selects the shutter with the highest valid signal value not corrupted by saturation. To select the best shutter for each pixel, the Shutter Engine extrapolates the correlated value of an earlier (shorter) shutter to the time of the current shutter. If the value of the current shutter is significantly below the expected value, it is assumed that the current value has been corrupted by saturation and the earlier value is used. All pixel values, regardless of the actual shutter time, are normalized (multiplied by a normalization factor) to the longest possible shutter.

The result is sent to the ReadOut engine, which serializes the data across the 4 serial MIPI channels. Since the MIPI throughput is only 1/3 of the maximum possible transfer rate from the Shutter Engine, the ReadOut engine maintains a small memory to temporarily buffer the data. Fig. 16 summarizes the flowchart of the shutter engine operation.

E. Micro-Sequencer

To allow late binding optimization of sensor operation for a particular application (e.g., number of shutters, gains, cap-

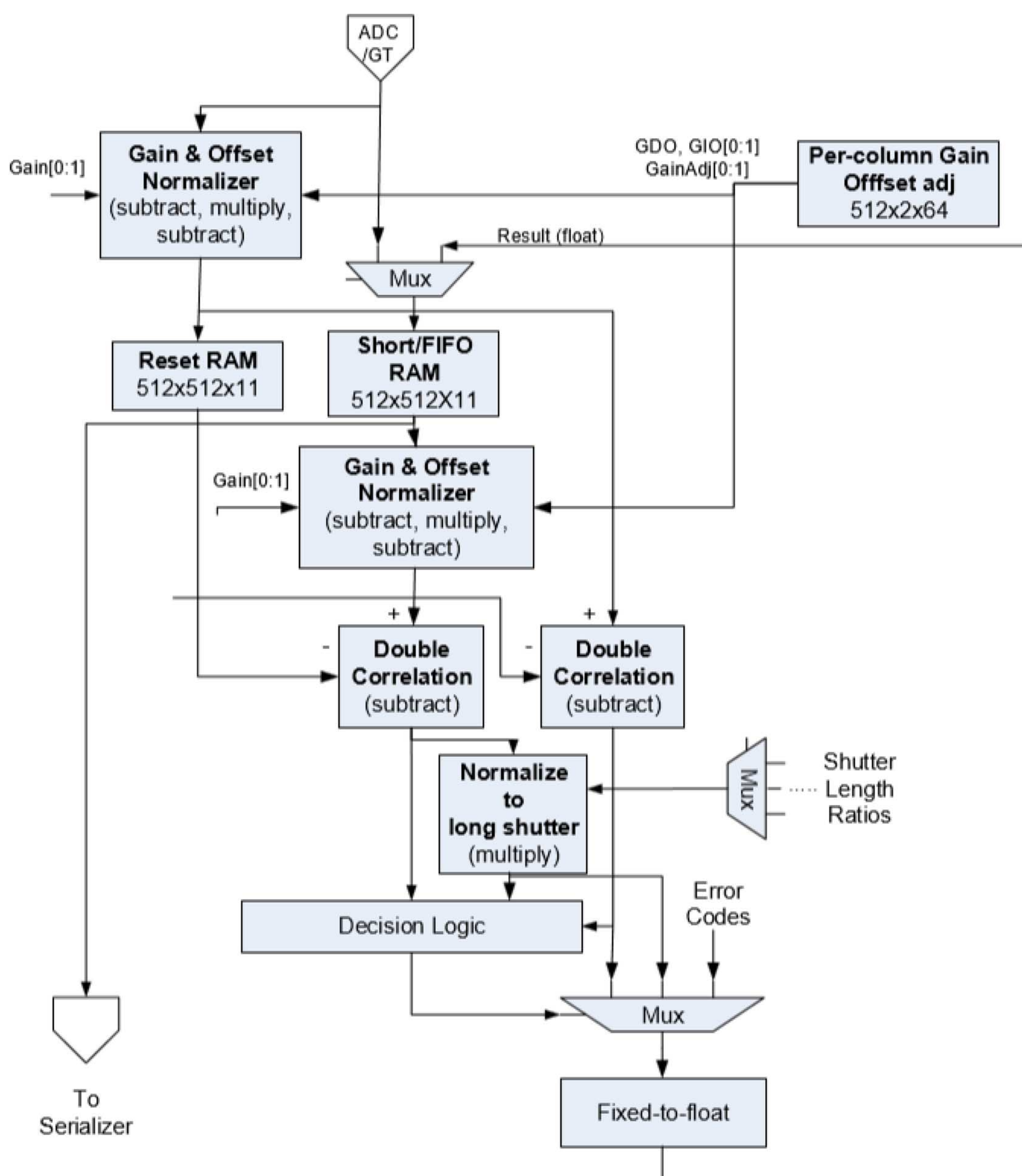

Fig. 16. Shutter engine flowchart.

tures, frequencies, or ordering of captures), the operation of the sensor is defined by a series of instructions downloaded into the sensor at boot time and interpreted by the micro-sequencer. The micro-sequencer uses a custom instruction set that can be divided into three categories; sequential instructions that provide arithmetic operations and flow control, sequential instructions that control analog and digital on-chip states, and custom ‘wave’ instructions that provide parallel generation of multiple pixel and analog control signals.

Wave instructions define a set of rising and falling edge timings for one or more of the pixel or analog control signals to allow generation of complicated control signal sequencing of practically any length. Wave instructions are user defined, and their definition is stored in a section of RAM called wave RAM. Wave instructions contain a pointer to the location in wave RAM where the definition of that wave instruction is stored.

IV. EXPERIMENTAL RESULTS

Our sensor is packaged in a chip-on-board (COB) module. This construction optimizes for thermal conductivity and optical performance while keeping costs in line for a consumer market product. The COB module consists of a 4 layer PC board with metal stiffener and offset-type thermal vias to help dissipate up to 2.5 W typical thermal load and keep below 5 μm of thermal-induced focus shift. A five-plastic-element F1.0 lens with $70^\circ \times 60^\circ$ FOV maximizes light gathering efficiency. A Near-IR narrowband-pass filter is integrated in the lens barrel to block all ambient light except in the narrow 860 nm wavelength range of the camera illumination system.

The phase shift measurement is proportional to the radial distance from the object to the center of the lens. The radial measurement is combined with the lens’ intrinsic parameters

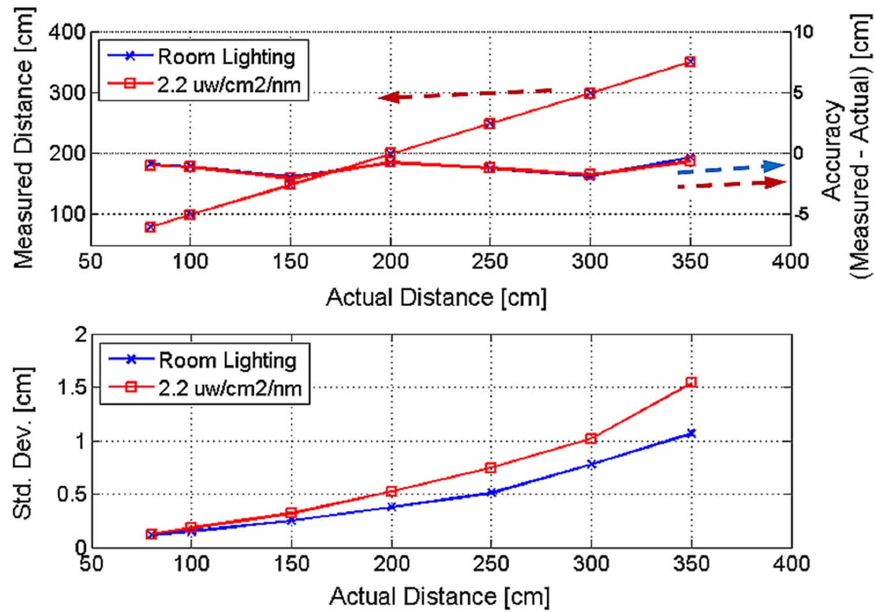

Fig. 17. Measured depth distance and accuracy.

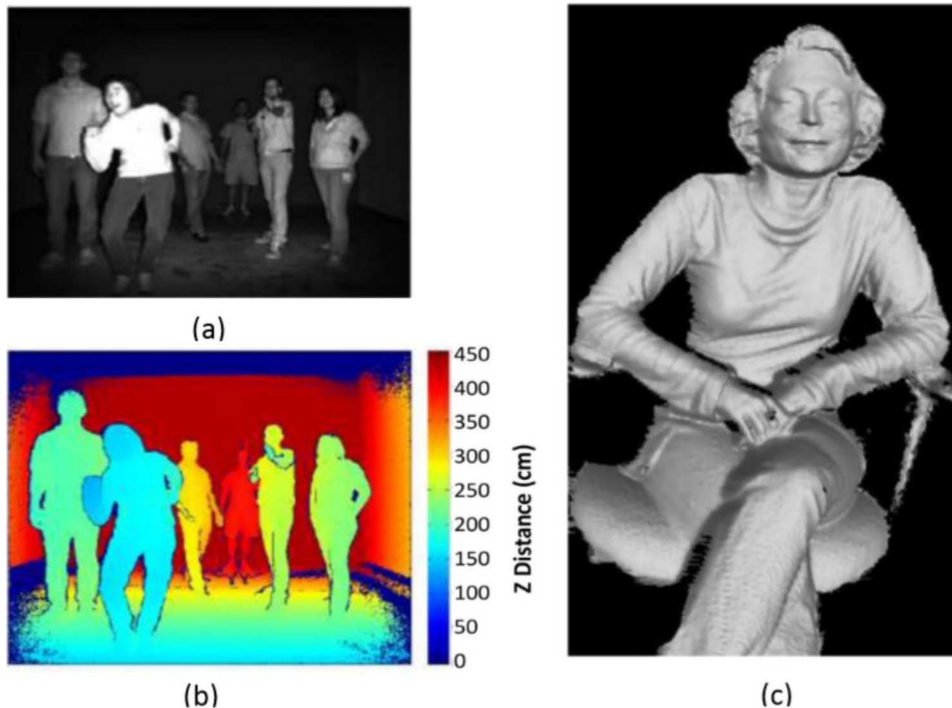

Fig. 18. Actual depth and active IR image.

to transform each pixel measurement into a point in (X, Y, Z) space. The active brightness image represents the amount modulated IR light returned to the sensor independent of ambient light. Various noise cancellation and filtering techniques are applied. Highly noisy and erroneous pixels are marked as invalid (shown in black).

In order to characterize the data, the camera is positioned on a rail in front of a Lambertian wall with 10% reflectivity perpendicular to the lens optical axes. The camera is positioned at seven discrete distances from the flat wall measured w.r.t. the principal point of the lens. At each of the seven distances 100 frames of the depth images are collected under normal room lighting and under ambient light at 2.2 μw/cm^2/nm. The mean of these images is plotted versus distance in Fig. 17 as well as depth accuracy and depth noise (standard deviation).

Fig. 18 shows examples of actual depth and active IR images produced by the sensor. Fig. 18(a) is a single active brightness (amount of IR light returned) image. Fig. 18(b) is a single Z-depth (proportional to the phase shift) image presented in a coarse color map. The wide 70° × 60° FOV of lens allows six

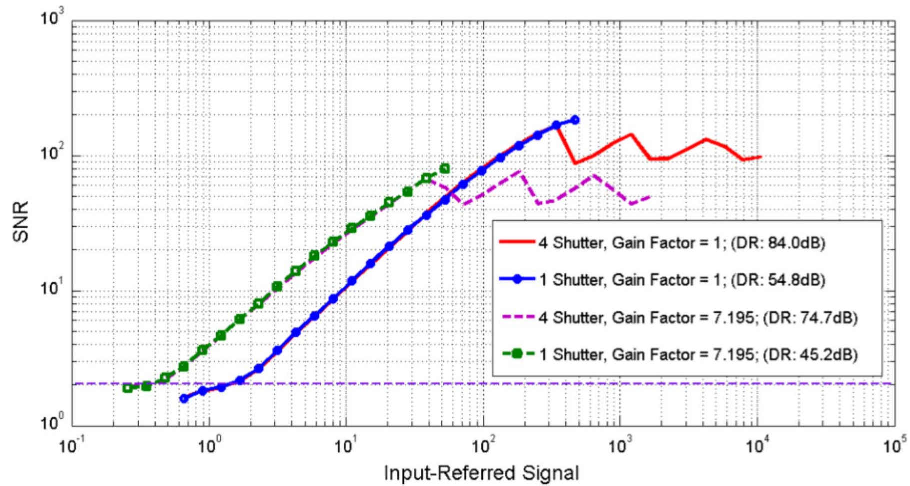

Fig. 19. Extended dynamic range using multi-shutter operation.

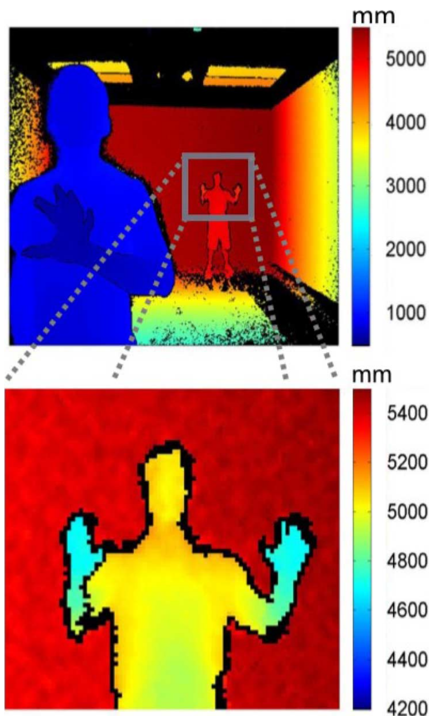

Fig. 20. Actual depth images demonstrates high dynamic range.

people to easily fit within the image. The high accuracy and sensor resolution of 512 × 424 makes it possible to detect fine features like clothes wrinkles as shown in Fig. 18(c) that displays the average of 100 frames data as a point cloud in a 3-D mesh. However, this high accuracy depth image requires taking the average of many frames at a near distance from the sensor, which might not be suitable for real time application.

Fig. 19 presents the measured IR signal versus SNR for a scene, which spans the dynamic range of the sensor for several configurations of amplifier gain and number of shutters. As shown in the two single-shutter plots, higher gain results in improved SNR but lower dynamic range. The multishutter figures illustrate the dynamic range improvement achievable by using a multishutter approach. A combined approach of multishutter and multigain can provide high sensitivity for low light conditions and a dynamic range of >75 dB.

TABLE I
SUMMARY OF CHIP PERFORMANCE PARAMETERS

Parameter	Value
Process Technology	TSMC 0.13 1P5M
Pixel Pitch	10u*10u
Pixel Array	512*424Pixels
Chip size	8.2mm*14.2mm
System Dynamic Range	> 2500 = 68db
Modulation Contrast	68% @ 860nm @50MHz
Pixel conversion gain	26µV/e
Full well Capacity	100Ke
Modulation Frequency	10-130MHz
Average Modulation Frequency	80MHz
FOV	70 (H) X 60 (V) degrees
Depth Uncertainty	< 0.5% of range
Distance Range	0.8-4.2m
Active Illumination source	Edge emitter laser
Operating Wavelength	860nm
Optical Bandwidth	45nm
Total exposure time	12.2msec
Frame Rate	max 60fps (typical 30fps)
ADC	2GS/s
Effective Fill Factor	60%
Reflectivity	15%-95%
Total Chip Power	2.1W
Pixel Array Clocks Power	1.2W
Column Amps/ADCs Power	0.11W
Clock Generation Power	0.07W
Misc. Analog Power	0.15W
Differential non-linearity	±2 LSB
Integral non-linearity	±4 LSB
Responsivity @ 860nm	0.144 A/W
Readout Noise	320 µV differential
Photo Response non-uniformity	1.47%
Dark Signal non-uniformity	3 mV
Column FPN	1.09 %
F#	1.07
ADC Resolution	10

TABLE II
COMPARISON OF THE STATE-OF-THE-ART TOF SENSORS

Parameter	Unit	Walker *et al.*, 2011 [22]	Stoppa *et al.*, 2011 [7]	Kim *et al.*, 2012 [23]	Niclass *et al.*, 2012 [24]	Niclass *et al.*, 2013 [21]	**This work**
Depth image resolution	Pixels	128x96	80x60	480x270	256x64	200x96	**512x424**
CMOS Technology	-	0.13µm Imaging	0.18µm Imaging	0.11µm Imaging	0.18µm HV	0.18µm HV	**0.13µm**
Pixel fill factor	%	3.2	24	34.5	13.9	70	**60***
Active light wavelength	nm	850	850	850	870	870	**860**
Active light power	mW	50	80	unknown	50	21	**600**
Modulation frequency	MHz	3.33	20	20	0.3	0.133	**72 Avg**
Field of View (HxV)	deg	40x40	7.6x5.7	24x14	45x11	55x9	**70x60**
Frame Rate	fps	20	5	11	10	10	**30**
Target reflectivity	-	white	white	white	white	9%	**15%**

*with microlens

The high dynamic range of the sensor is shown in real images presented in Fig. 20. The image on the top shows the full 512 × 424 resolution of the sensor with one person at about 80 cm and another at about 500 cm. The image at the bottom is zoomed in on the person 500 cm away to show more details. However very few pixels cover the zoomed area, which results in a lower image quality.

Table I summarizes our chip's main performance characteristics, and Table II compares our chip with other state of the art TOF image sensors in the literature [21]. This comparison highlights many strengths of our TOF chip. As far as we know our TOF sensor has the highest pixel resolution with the smallest pixel pitch among all published TOF sensors. It provides full frame rate operation, and operates at the highest modulation frequency (above 100 MHz) with excellent modulation contrast (above 55%). Our system achieves very good depth linearity at even low target reflectivity. Finally, our chip and system has been available commercially in millions of Kinect for XBOX ONE Systems.

V. CONCLUSION

We have introduced a high-performance, high-resolution TOF depth image sensor that meets the constraints of indoor natural user interface and gaming applications. The sensor was designed in a TSMC 0.13 μm CMOS process and consumes 2.1 W when used in the long-range large-FOV living-room scenario. The pixel design enables high MC (67%@50 MHz) at high modulation frequencies (up to 130 MHz) using a fully differential QEM TOF. The sensor allows for high-dynamic-range operation though the use of multigain and multishutter. A built-in programmable micro-sequencer maximizes operational flexibility allowing the sensor operating parameters to be tuned for maximum performance.

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Cyrus S. Bamji received the S.Bs. degree in mathematics and electrical engineering and computer science and the S.M. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA.

His early work was in the area of electronic design automation, where he won several best paper awards and wrote a book called *Leaf Cell and Hierarchical Compaction Techniques* (Springer, 1997 edition). He is the inventor of over 45 patents, most in the field of time of flight (TOF). He was the CTO and a cofounder of Canesta, a TOF company acquired by Microsoft in 2010. He now leads a team developing next generation TOF technologies at Microsoft, Mountain View, CA, USA.

Patrick O'Connor received the B.Sc. degree in Electrical & Electronic Engineering in 1984 from DIT and University of Dublin, Trinity College, Ireland.

He is a Partner Director of Engineering at Microsoft, Mountain View, Ca, USA, where he is responsible for hardware and software development of sensors and custom silicon in Microsoft's Natural User Interface platforms such as Kinect. Prior to joining Microsoft, he was Vice President of Engineering at Canesta Inc. and held engineering positions at Parthus Technologies, Aureal Inc., National Semiconductor, Rockwell Inc., and Analog Devices.

Tamer Elkhatib (S'09–A'09) received the B.Sc. degree in electronics and communication and the M.Sc. degree in engineering mathematics and physics (both with honors) from Cairo University, Cairo, Egypt, in 2002 and 2006, respectively, and the Ph.D. degree in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, USA, in 2010.

Currently, he is a Senior Scientist with Microsoft, Mountain View, CA, USA, developing the next-generation time-of-flight image sensor technology. His role includes semiconductor device physics analysis and modeling, device simulations, pixel architecture and development, and foundry process analysis. He is the author and coauthor of 16 scientific articles published in refereed journals and conference proceedings. He is also the inventor of three issued/pending US patents.

Swati Mehta (S'02–M'04) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Bombay, Mumbai, India, in 1999, and the M.S.E. and Ph.D. degrees in electrical and computer engineering from Johns Hopkins University, Baltimore, MD, USA, in 2001 and 2006 respectively.

She is currently a Principal Scientist with Microsoft, Mountain View, CA, USA, working on developing the pixel technology and chip architecture of the time-of-flight (ToF) image sensor. Her role includes researching and designing new pixels, circuit design and simulation, system analysis and test-setup and automation. In the past she has worked on motion detection image sensors and biologically inspired image sensors.

Barry Thompson (M'87) received the B.S. degree in electrical engineering and computer science from the University of California, Berkeley, CA, USA, and the S.M. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA.

He .has over 25 years of experience designing chips in the areas of network communications, RF circuits, OLED displays, and CMOS image sensors. He cofounded Sierra Research and Technology and held Vice President positions with TDK Semiconductor and Cambridge Display Technologies. His work on time-of-flight sensors started at Canesta and has continued at Microsoft, Mountain View, CA, USA, where he is a Principle Engineer.

Lawrence A. Prather (M'76) received the B.S. degree in electrical engineering technology from the Oregon Institute of Technology, Klamath Falls, OR, USA, in 1978.

He is currently a Principal Analog Design Engineer with Microsoft, Mountain View, CA, USA, where he is responsible for the design of a wide range of analog circuit content in time-of-flight image sensor chips. In his 36-year career, he has worked for nine companies in a variety of positions including nine years as Director of Analog Design at Genesis Microchip, where he was responsible for putting all flat-panel controller chips into full-scale production. He was a key contributor to the industry work group that developed the DisplayPort specification, now a VESA supported standard. His career focus is analog and mixed-signal design in standard CMOS ASIC process nodes. His research interests include, high-speed serial links, high-speed A/D and D/A converters, and DC-DC converters.

Dane Snow (M'76) received the B.S. and M.S. degrees in electrical engineering and computer science from the University of California, Berkeley, CA, USA, in 1975 and 1978, respectively.

He has held various analog IC design engineer and manager positions with Intersil, Harris, MicroUnity Systems Engineering, Epigram, Broadcom, and Canesta. Since November 2010, he has been a Principal Analog Design Lead with Microsoft, Mountain View, CA, USA. He holds more than ten patents and his current interests include analog IC design for CMOS image sensors.

Onur Can Akkaya received the B.S. degree in electrical and electronics engineering from Middle East Technical University, Ankara, Turkey, in 2006, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 2008 and 2012, respectively. His Ph.D. work focused on micro- and nano-scale devices that integrate photonics and MEMS, as well as interferometric sensor arrays.

He also worked on integrated electrochemical sensors at Intel Labs. He is currently a Scientist with Microsoft, Mountain View, CA, USA, and working on the next-generation time-of-flight image sensor technology. He holds seven issued/pending U.S. patents.

Andy Daniel received the M.Eng. degree from Rensselaer Polytechnic Institute, Troy, NY, USA, in 1982.

He has worked primarily in the fields of computer graphics hardware for the last 30 years. He led the development of the industry's first DRAM-based Windows accelerator for Western Digital in 1990 and the first video-in-a-window hardware for Alliance Semiconductor in 1995. A former Director of the Video Electronics Standards Association (VESA), he has taught video compression at SIGGRAPH and holds eight patents.

Andrew D. Payne (M'09) received the M.S. and Ph.D. degrees in physics from The University of Waikato, Hamilton, New Zealand, in 2004 and 2009, respectively.

After a three-year postdoctoral position with The University of Waikato, he is currently a Senior System Architect with Microsoft, Mountain View, CA, USA, where he is developing time-of-flight cameras for natural user interfaces. He holds three patents, and his current interests include opto-electronics, signal processing, and working with embedded controllers and sensors.

Travis Perry received the B.S. degree from University of California, Davis, CA, USA, in 2004, and the M.S. degree from Santa Clara University, Santa Clara, CA, USA, in 2007, both in electrical engineering.

He is currently a Senior System Architect with Microsoft, Mountain View, CA, USA, focusing on system and chip architecture and developing signal/image processing algorithms. Prior to joining Microsoft, he held various engineering positions with Canesta since 2006. In the last eight years at both Canesta and Microsoft, he has worked on nearly every aspect of time-of-flight systems, including high-volume camera calibration, system and chip characterization, chip bring up, algorithm development and implementation, system modeling, and chip and system architecture.

Mike Fenton (M'10) received the B.S. degree in computer engineering from the Pennsylvania State University, Colleg Park, PA. USA, in 2007, and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 2010.

He is currently a Senior System Architect with Microsoft, Mountain View, CA, USA, where he is primarily focused on system-on-chip modeling, specification, design, and execution. His previous experience spans nearly every aspect of time-of-flight systems including silicon verification, performance characterization, camera calibration, algorithm development, and chip bring-up.

Vei-Han Chan received the B.S. degree from National Taiwan University, Taipei, Taiwan, in 1986, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1991 and 1994, respectively, all in electrical engineering.

He worked on development of flash memory and logic technologies in various industrial capacities in the past. He is the author of over 10 publications and inventor of over 40 patents in various semiconductor areas. Currently, he is a Principal Technologist at Microsoft with focus on semiconductor technology development, foundry management, and product engineering in the areas of SoC and TOF image sensor.