A Fully Synthesizable All-Digital PLL With Interpolative Phase Coupled Oscillator, Current-Output DAC, and Fine-Resolution Digital Varactor Using Gated Edge Injection Technique

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***Abstract*—This paper presents a fully synthesizable phase-locked loop (PLL) based on injection locking, with an interpolative phase-coupled oscillator, a current output digital-to-analog converter (DAC), and a fine resolution digital varactor. All circuits that make up the PLL are designed and implemented using digital standard cells without any modification, and automatically Place-and-routed (P&R) by a digital design flow without any manual placement. Implemented in a 65 nm digital CMOS process, this work occupies only 110 µm × 60 µm layout area, which is the smallest PLL reported so far to the best knowledge of the authors. The measurement results show that this work achieves a 1.7 ps RMS jitter at 900 MHz output frequency while consuming 780 µW DC power.**

***Index Terms*—AD-PLL, CMOS, DAC, digital varactor, dual loop, edge injection, gated injection, injection-locking, logic synthesis, low jitter, low power, PLL, PVT, small area, standard cell, synthesizable.**

I. Introduction

As CMOS technology scaling advances, traditional analog circuits have moved towards digital-intensive or all-digital designs during the past few years. While taking advantage of digital circuits in scaled CMOS technology, digital-intensive or all-digital designs still cannot be absorbed in advanced design automation used by digital VLSI circuits. This paper investigates a design methodology for analog circuits that is defined as synthesizable analog design. In this design methodology, all circuit building blocks are implemented in all-digital architecture and expressed in a hardware description language, which can then be synthesized from commercial standard-cell libraries and automatically P&R using EDA tools. Comparing to conventional pure analog or digital-intensive analog implementations, synthesizable analog implementations significantly shorten the design time and cost. Also, synthesizable architectures enhance portability and scalability of analog circuits for various applications and different design nodes, since the functionality of cells remains unaltered between different process nodes, or between different process technologies. In addition, design rules in deep submicron technology node become much more complex and only allow restricted forms of circuit layout [1], which degrades the productivity of conventional analog design whereas synthesizable analog design has the potential to circumvent such restrictions on circuit layout. Design methodology for synthesizable analog circuits can be applied to various applications including all-digital transmitter [2], all-digital PLLs [3]–[6], time-to-digital converter (TDC) [7] and analog-to-digital converter (ADC) [8].

While a number of fully synthesizable PLLs have been reported recently [3]–[6] there is still considerable room for improvement in terms of power consumption and chip area. Moreover, considerable amount of custom-designed cells are required in the previous synthesizable PLLs, which introduce additional design and P&R procedures [4], [5]. These additional design procedures leads to performance degradation in terms of portability, integration and scalability. In order to address the above mentioned issues, this paper presents a low-power and compact fully synthesizable PLL [9], which does not use any custom design but purely designed by using a foundry-provided standard-cell library by a standard digital design flow. Several circuit techniques are proposed to overcome issues resulting from fully synthesizing a PLL system.

This paper is organized as follows. Section II describes the PLL overall architecture and considerations. Section III presents the details of important building blocks. Section IV demonstrates experimental results of the proposed fully synthesizable PLL. Finally, conclusions are summarized in Section V.

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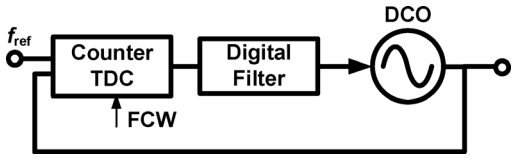

Fig. 1. Simplified diagram of conventional TDC-based all-digital PLL.

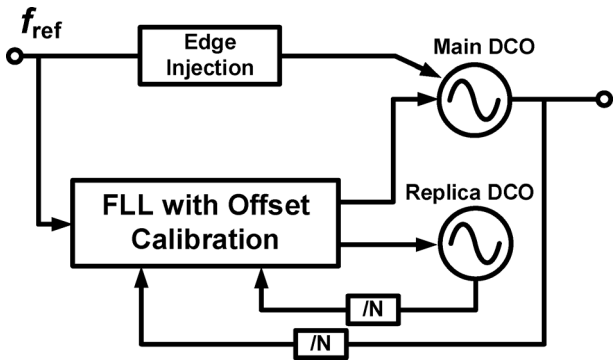

Fig. 2. Simplified diagram of the fully synthesized PLL.

II. PLL Architecture Consideration

All-digital PLLs, as shown in Fig. 1, are mostly TDC-based architecture [10]. While some all-digital PLLs [11] can be fully described in hardware description language (HDL), the layout designs, especially that of the digital-controlled oscillators (DCOs) and TDCs still has to be done by conventional custom layout drawing. This is because these critical building blocks are prone to layout uncertainty and impairment resulting from automatic P&R, which causes linearity degradation resulting in poor in-band and out-of-band phase noise in all-digital PLLs. To overcome this issue, authors in [5] proposes a plugin unit-cell technique but the additional procedures required in unit-cell design P&R negates any advantages promised by this method.

In this work, a fully synthesized PLL with a current output DAC and an interpolative phase-coupled oscillator based on standard digital library is presented. In comparison to the conventional works, the methodology presented in this paper requires neither any modifications in standard cell nor any manual layout steps. This PLL is based on injection-locking topology. Thus, TDC issues such as linearity and power-resolution trade-off can be avoided. Fig. 2 shows the simplified architecture of the proposed PLL. An interpolative-phase coupled oscillator incorporated in the design helps minimize output phase imbalance from automatic P&R, a current output DAC for reduces the power consumption and chip area, a standard-cell based varactor ensures fine resolution and a gated edge injection technique avoids issues related to injection-pulse width.

Different from conventional all-digital PLLs that adopt TDC for phase locking, feed-forward reference injection is adopted for phase locking in the design as illustrated in Fig. 3(a). A PLL suppresses the phase noise of a free-running oscillator only within its loop bandwidth, which is typically less than 0.1 times f_{ref} due to loop stability constrain. The limited loop bandwidth results in a poor in-band phase noise. On the other hand, the periodic phase alignment by injecting a clean reference to the oscillator makes use of the stable reference clock over a much wider

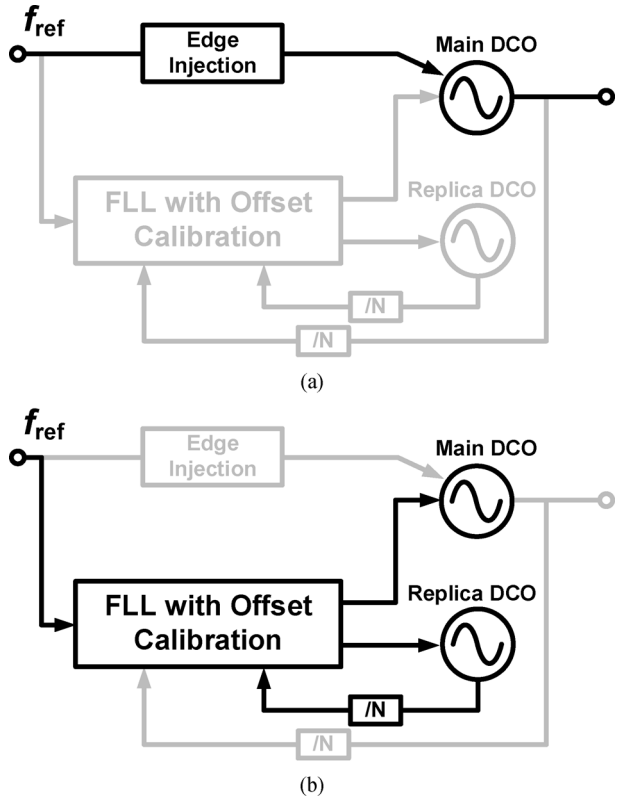

Fig. 3. (a) Phase locking and (b) frequency locking of the fully synthesized dual-loop IL-PLL.

bandwidth, thereby improving the suppression of free-running oscillator phase noise to obtain low in-band phase noise. Detailed phase noise analysis of this kind of edge injection locked oscillator was first performed in [12]. Further analysis by author in [13] reveals a 3 dB increase in high-frequency phase noise of the injection locked oscillator based on continuous time-domain approximation. In contrast, a different phase noise analysis method using discrete time-domain analysis is provided in [14] in which the phase noise expression is valid for any multiplication ratio N. Note that the single side band (SSB) phase noise power spectrum density (PSD) $\mathcal{L}(f)_{\mathrm{free-running}}$ of a free-running oscillator at frequency offset f is expressed as $\boldsymbol{\sigma_{\mathrm{p}}^2 N f_{\mathrm{ref}}}/(8\boldsymbol{\pi^2 f^2})$, the SSB phase noise PSD $\mathcal{L}(f)_{\mathrm{injection}}$ of an edge injection locked oscillator is given as

$$\mathcal{L}(f)_{\mathrm{injection}} = \mathcal{L}(f)_{\mathrm{free-running}} \cdot \frac{2\boldsymbol{\pi}^2(\boldsymbol{N}-1)(2\boldsymbol{N}-1)}{3\boldsymbol{f}_{\boldsymbol{ref}}^2\boldsymbol{N}^2} \cdot \frac{\boldsymbol{f}^2}{1+\left(\frac{\boldsymbol{f}}{\boldsymbol{f}_{\mathrm{inj}}}\right)^2} \quad (1)$$

and the injection locking bandwidth f_{inj} is

$$\boldsymbol{f}_{\mathrm{inj}} = \boldsymbol{f}_{\mathrm{ref}} \cdot \frac{1}{\boldsymbol{\pi}} \cdot \sqrt{\frac{1.5}{1-\frac{1}{\boldsymbol{N}}}} \quad (2)$$

where f_{ref} is the injection reference, N is the multiplication factor, and $\boldsymbol{\sigma_{\mathrm{p}}^2}$ is variances of Gaussian random variables of phase errors.

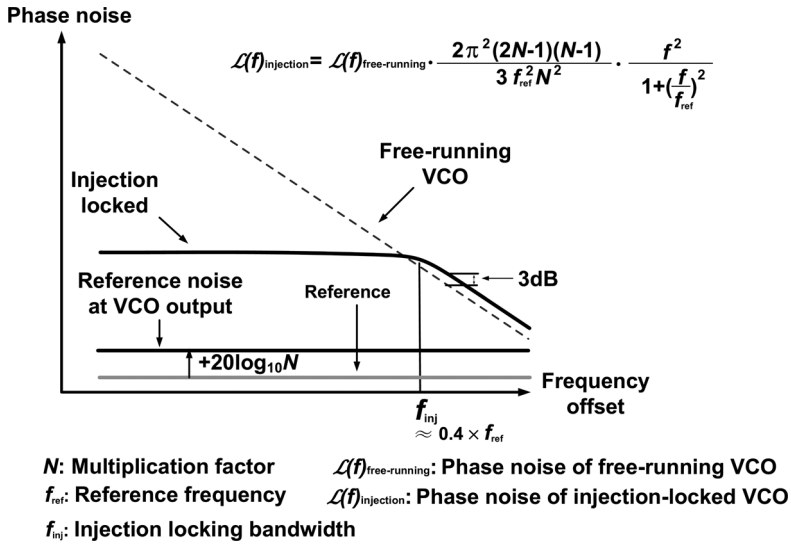

Fig. 4. Conceptual diagram of phase noise characteristics.

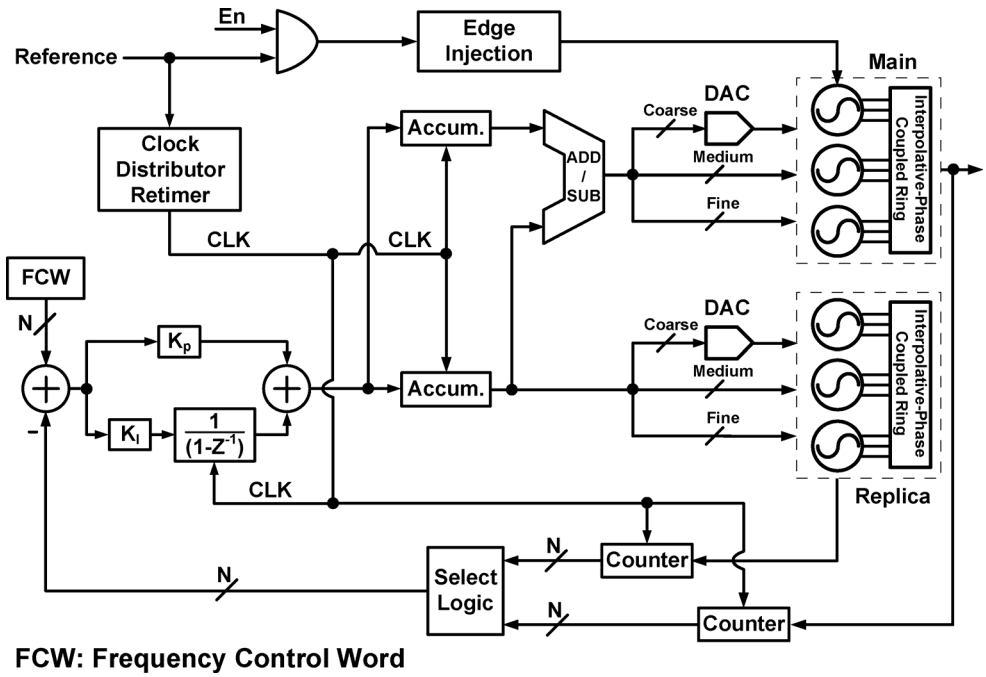

Fig. 5. Block diagram of the proposed fully synthesizable PLL with a DAC and an interpolative phase coupled oscillator.

At high frequency offset, (1) can be approximated as

$$\mathcal{L}(f)_{\text{injection}} = \mathcal{L}(f)_{\text{free-running}} \cdot \frac{2N-1}{N} \approx \mathcal{L}(f)_{\text{free-running}} \cdot 2. \quad (3)$$

Several inspections can be observed from (2) and (3). First of all, at a high value of N, f_{inj} is close to 0.4 times f_{ref}, which is much wider than PLL loop bandwidth. In addition, the phase noise of an edge-injection locked oscillator is approximately 3 dB higher than that of a free-running oscillator at high offset frequency.

It is necessary to point out that output phase noise due to the reference is increased by $20 \log N$. Fortunately, phase noise of reference clocks usually is much better than the intrinsic oscillator noise over the entire frequency range of interest, which will not affect the overall performance. The detail is shown in Fig. 4.

As for the injection method, conventional pulse injection [15] imposes severe timing requirements on the injection-pulse width whereas the proposed edge injection does not have any strict demands on its injection-window width, which considerably simplifies timing design issues. Regarding the frequency locking, a dual-loop PLL architecture [16], [17] is employed and improved in this design to provide continuous tracking of voltage and temperature variations and avoid timing problems in the conventional injection-locked PLL, as shown in Fig. 3(b).

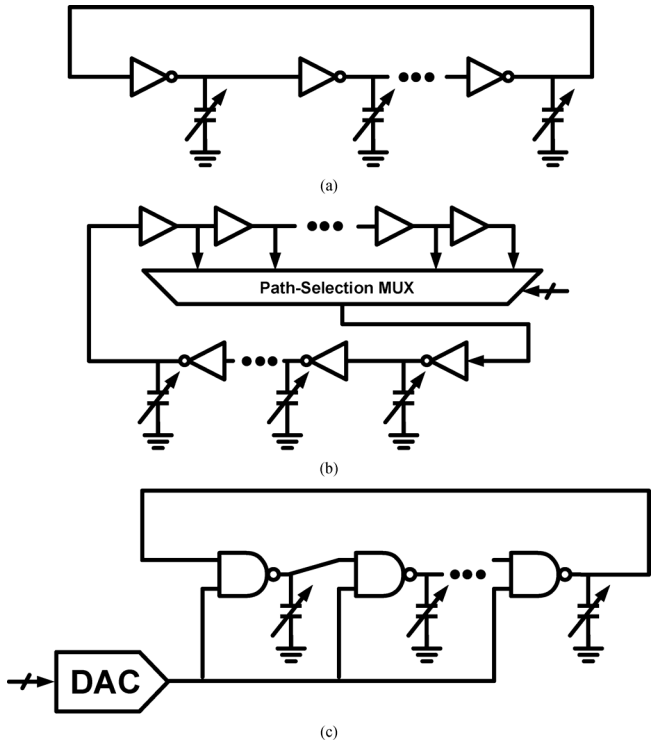

Fig. 6. Simplified diagram of synthesizable DCOs using (a) varactor, (b) varactor and path selection, and (c) varactor and DAC for frequency tuning.

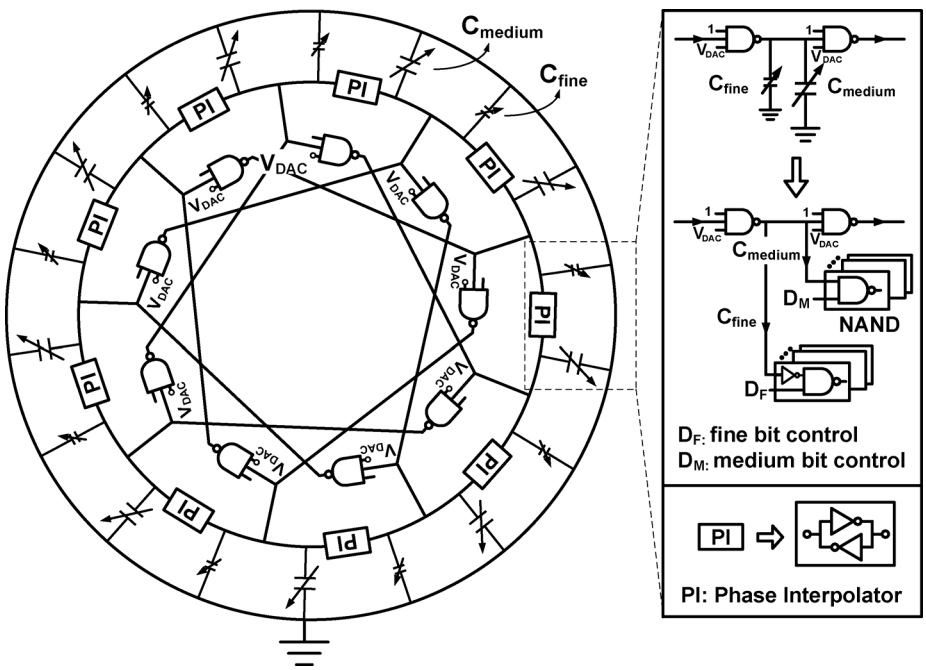

Fig. 7. Block diagram of the interpolative phase-coupled oscillator.

Detailed block diagram of the proposed PLL with a DAC and an interpolative phase-coupled oscillator is given in Fig. 5. All circuits that make up the PLL, including the DAC and DCO, are implemented using digital standard cells in the automated design procedure. Oscillation frequencies of two oscillators are digitized by two 14 bit counters. A digital signed adder/substractor with a dead-zone compares the digitized frequency with a predefined frequency control word (FCW) and generates frequency difference, which is then fed to a digital loop filter consisting of a proportional path and an integral path. The designed loop filter bandwidth is around 800 kHz. The filter output determines whether to increase, decrease, or hold the DCO oscillation frequency. Considering that the oscillator oscillates from 0.39 to 1.41 GHz, a 14 bit frequency control scheme, which is composed of 4 bit coarse, 6 bit medium, and 4 bit fine tuning leads to an oscillator LSB resolution of 100 kHz. Such fine resolution helps to achieve low spur level [17].

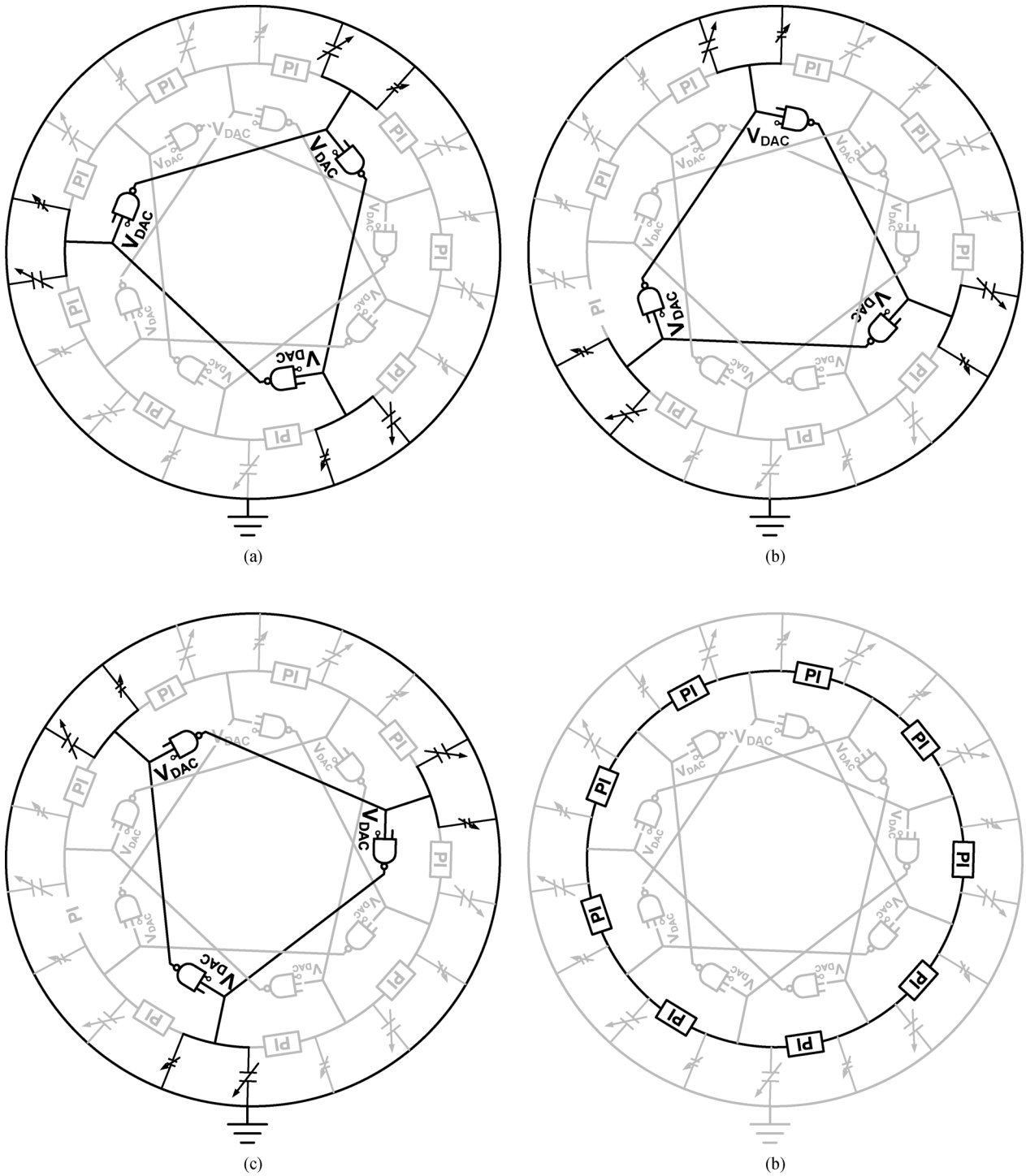

Fig. 8. Block diagram of (a)(b)(c) DCO built by NAND gates and digital varactors, and (d) phase-coupled ring.

III. Circuit Implementation

A. Interpolative Phase-Coupled Oscillator

Conventional standard-cell based DCO, as shown in Fig. 6(a), adopts digital varactor [18] for frequency tuning. While benefiting from high linearity, this method suffers from large power consumption and limited resolution. A path-selection method in Fig. 6(b) is proposed as the coarse tuning in synthesized oscillators [19] for reducing power consumption. However, this method suffers from poor linearity. To maintain the control code resolution and frequency linearity, the oscillator is designed to operate with a coarse tuning circuitry controlled by a DAC, a medium/fine tuning circuitry controlled by digital varactors, as shown in Fig. 6(c). The circuit will be revisited later for implementation details.

Recall that the PLL calibration system operates in three phases [17]. The first two phase are used upon start-up for compensating frequency offset between main and replica oscillators due to process variations at a certain temperature. The third calibration phase is continuously operating for tracking

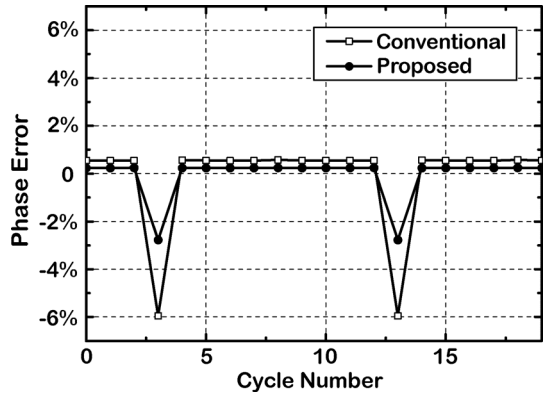

Fig. 9. Simulated phase error in the case of the conventional and proposed oscillator.

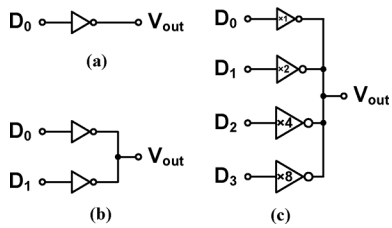

Fig. 10. Conceptual diagram of (a) 1 bit, (b) 2 bit, and (c) 4 bit binary coding voltage-linear DAC.

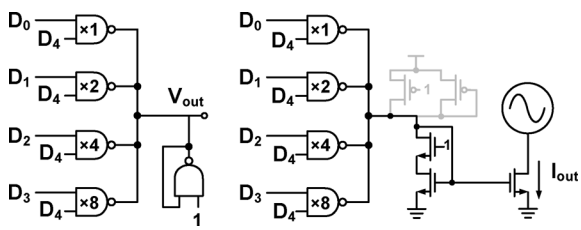

Fig. 11. Conceptual diagram of the proposed current output DAC.

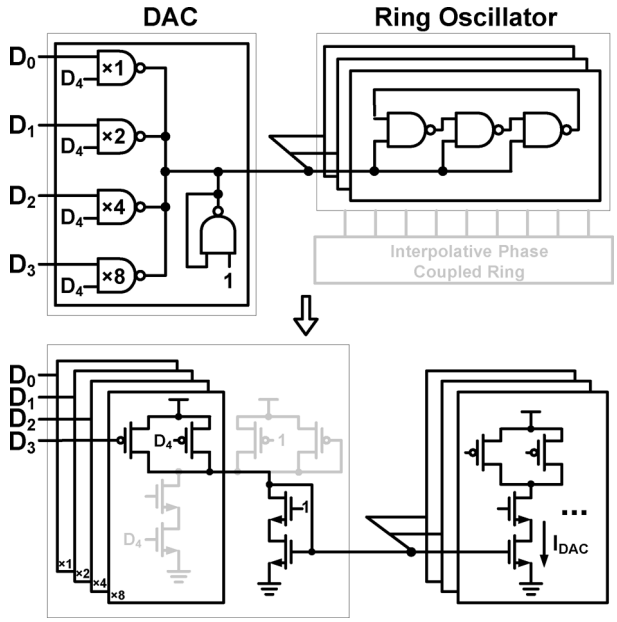

Fig. 12. Block diagram of the proposed synthesizable DAC with a current-linear output.

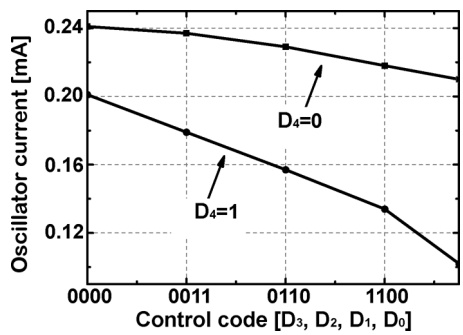

Fig. 13. Simulated current consumption of the oscillator using the current-output DAC.

voltage and temperature variations. However, a frequency mismatch between the main and replica oscillator might also occur, since the frequency of two automatic P&R-ed oscillators do not change equally in temperature effect. Such a frequency mismatch is not compensated in the third calibration phase [17], and, thus, there will be an increase in phase error of the main oscillator under injection locking. In order to relax this issue, an interpolative phase-coupled oscillator is developed that has its roots in the concept presented in [20]. Fig. 7 illustrates the proposed oscillator architecture built by three 3-stage oscillators that is used in both main and replica VCOs. Fig. 8(a)–(c) show the block diagram of the separated DCO. Fig. 8(d) shows the block diagram of the interpolative phase coupled ring. The phase interpolator is constructed using two inverters. If the oscillator does not have the auxiliary ring, the phase of three oscillators are independent of each other. The auxiliary ring couples every main oscillator to ensure accurate oscillation phase. As a result of its internal feedback and feed-forward control by the coupled interpolators, the phase difference within the ring and between all adjacent rings will remain fixed with time, leading to balanced output phases.

Simulation performed confirms the effectiveness of the proposed interpolative phase coupled oscillator. Assuming simulation conditions of a reference injection from a 200 MHz source, a multiplication ratio of 10, and 0.5% mismatch in free-running frequency, it can be observed in Fig. 9 that the maximum phase error is improved from 6% in the case of conventional 3-stage ring oscillator to 2.8% in the case of the proposed interpolative phase coupled oscillator, where the phase error is defined as deviation from its mean value in percentage.

B. Current Output DAC

Basically, a DAC can be used to control the coarse tuning part of oscillator. If the control code of the DAC is changed, the oscillator frequency can be changed accordingly. DAC control has the added advantage of balancing the loading at each node. Fig. 10(a) shows a simple inverter which can be considered as a 1 bit voltage-output DAC. If $\mathrm{D_0}$ is 0, then the output voltage $\mathrm{V_{out}}$ becomes $\mathrm{V_{DD}}$. Similarly, this concept can be extended to a 2 bit voltage-output DAC by voltage interpolation. If $\mathrm{D_0D_1}$ is 11, then $\mathrm{V_{out}}$ becomes 0. If $\mathrm{D_0D_1}$ is 10 or 01, $\mathrm{V_{out}}$ becomes $\mathrm{V_{DD}}/2$, if $\mathrm{D_0D_1}$ is 00, then $\mathrm{V_{out}}$ becomes

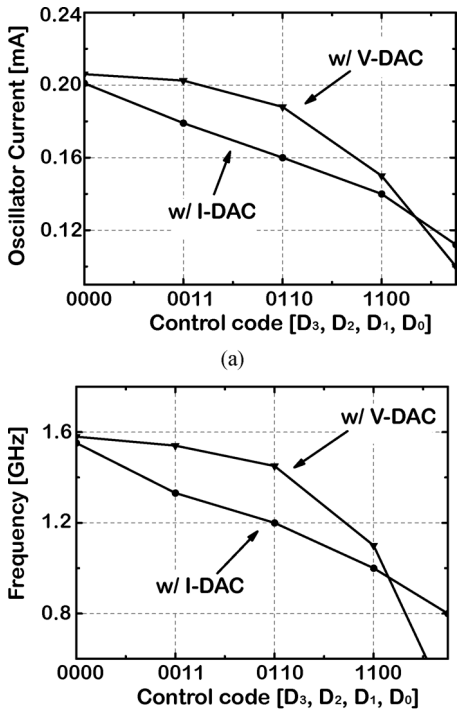

Fig. 14. Comparison of (a) current consumption (b) frequency of the oscillator using the current-output DAC and voltage-output DAC when D4 connects to logic HIGH.

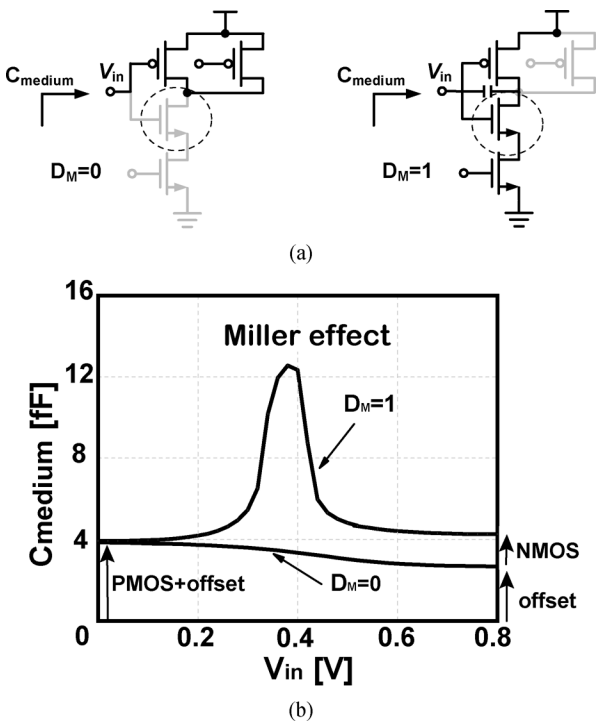

Fig. 15. (a) Equivalent circuit of the medium tuning capacitor and (b) Simulated medium tuning capacitance over $V_{\rm in}$.

$V_{\rm DD}$. By further extending this concept, a 4 bit DAC with binary coding can be designed as shown in Fig. 10(c). Thus an ideal voltage-linear DAC can be obtained by voltage interpolation. However, considering that the interpolative phase coupled

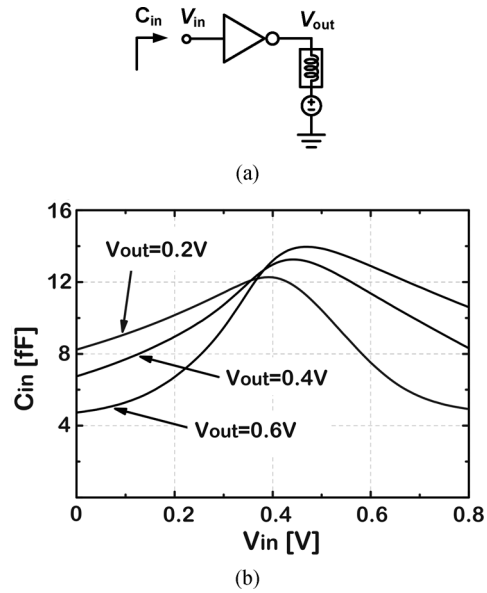

Fig. 16. (a) Test bench for the Miller effect sensitivity and (b) Simulated input capacitance against $V_{\rm in}$ at various $V_{\rm out}$.

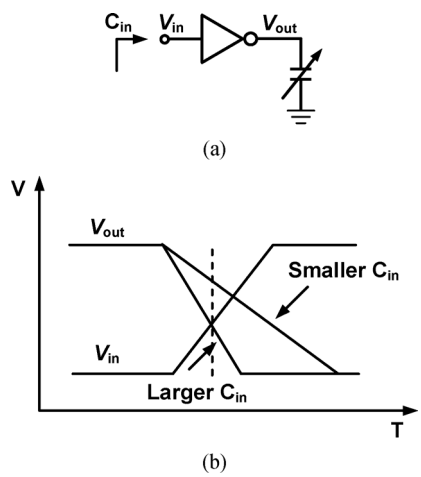

Fig. 17. (a) Equivalent circuit of fine tuning capacitor (b) conceptual diagram of time domain waveform of $V_{\rm out}$ and $V_{\rm in}$ indicating that a transient variation of $V_{\rm out}$ can make a fine capacitance difference in $\rm C_{in}$.

oscillator is based on current-starving topology, a current-linear rather than voltage-linear DAC is desired.

In this design, an equivalent current-output DAC built entirely from standard CMOS NAND gates is proposed as the coarse tuning circuitry. The proposed implementation contributes to the reduction of the overall power consumption and chip area without sacrificing phase balance. Tri-state buffers/inverters [3]–[5] are not used since they are sometimes not included in standard-cell libraries. For easier understanding, Fig. 11 depicts a conceptual diagram of a 4 bit current output DAC constructed from five two-input NAND gates. The proposed DAC consists of a PMOS-current-source array and an NMOS current mirror. The PMOS-current-source array is built by driving one of the two NAND gate inputs by a digital control word and the other input by D4 and by connecting outputs of 4 NAND gates together. The NMOS current mirror is built by connecting one input of NAND gate to its output and the

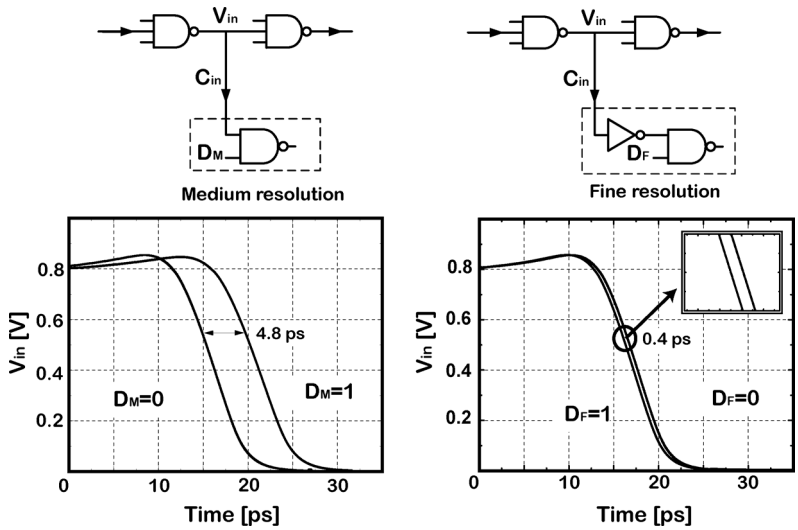

Fig. 18. Simulated input capacitances against input voltage $V_{\rm in}$ and the resulting delay resolutions for the medium tuning and proposed fine tuning varactors.

other input connects to logic HIGH. As illustrated in Fig. 12, the proposed current output DAC is combined with a current starved ring oscillator using a NAND logic gate as its delay cell to form a digitally controlled oscillator.

Several simulations are performed to verify the effectiveness of the proposed current-output DAC. Fig. 13 plots simulated current consumption of the current starved oscillator using the proposed current-output DAC. Fig. 14 compares simulated current consumption and frequency of the oscillator using current-output and voltage-output DAC when D4 connects to logic HIGH respectively. It can be seen from these two graphs that the proposed current output DAC stands out as a better option in terms of oscillator frequency linearity. The simulated DAC power consumption is less than 60 μW.

C. Standard-Cell Based Varactor

In order to achieve better resolution for reducing spurs, a medium and fine-tuning circuitry using standard-cell based varactor are required. Conventionally, standard-cell based varactor [18] is built by using NAND or NOR gate. In medium tuning circuitry, digitally-controlled varactor using NAND logic gate is adopted for introducing a capacitance difference between two delay stages. As illustrated in Fig. 15(a), the marked NMOS transistor under different $D_{\rm m}$ produces this capacitance difference. In general, the finer resolution can be achieved by reducing size of the marked NMOS transistor or increasing size of logic gate in the previous stage. However, the transistor size is limited in standard-cell based design. To deal with this issue, an improved standard-cell based varactor is developed for the fine tuning circuitry.

Fig. 15(b) shows the simulated medium capacitance $C_{\rm medium}$ against $V_{\rm in}$ at different $D_{\rm m}$. Interestingly but not surprisingly, the equivalent input capacitance $C_{\rm medium}$ increases due to the Miller effect, which happens around $V_{\rm in} = 0.4$ V for $D_{\rm m} = 1$. To investigate the possibility of achieving finer resolution using the Miller effect, a test bench is adopted as shown in Fig. 16(a). Simulation results in Fig. 16(b) indicate that the Miller effect sensitivity can be varied by varying $V_{\rm out}$, which cannot be controlled directly. However, if a varactor is placed at the output node, as illustrated in Fig. 17, the capacitance difference will cause a transient variation of $V_{\rm out}$, which in turn, changes the Miller effect sensitivity.

Based on this concept, the fine tuning circuitry is realized by another type of digitally controlled varactor using inverters and NAND gates. The digitally-controlled NAND gate introduces a capacitance difference at the inverter output node, which alters the rising and falling slopes thereby changing Miller effect sensitivity. Thus, the effective capacitance seen from the ring oscillator is also changed. This capacitance difference is used for the fine-tuning stage.

Fig. 18 shows input capacitances against input voltage $V_{\rm in}$ and the resulting delay resolutions for the medium tuning and proposed fine-tuning varactors. Digitally controlled varactor using NAND logic gates is adopted in the medium tuning circuitry providing a 4.8 ps delay resolution. As for the fine tuning circuitry, simulation results show that it achieves 0.4 ps delay resolution. It is known that the DCO non-monotonic response would introduce unlock phenomenon in the frequency-locked loop and increase spur level. While the monotonic characteristic of the medium tuning circuitry is studied in [18], the monotonic response of the proposed fine tuning circuitry is verified by the post-layout simulation. Fig. 19 shows that the simulated DNL ranges from -0.6 to 1.5 LSB and the DCO frequency varies from 1.234 to 1.237 GHz, which proves the monotonic response of the synthesized DCO.

D. Gated Edge Injection

Injecting a stream of narrow pulses to the oscillator is widely used to improve its jitter performance by resetting the oscillator at every reference cycle [15]. However, the injection pulse width requires an additional calibration to guarantee its robust operation over environmental variations, since excessively narrow pulse width causes a failure to lock or over-designed pulse width causes a strong periodical disturbance to oscillator

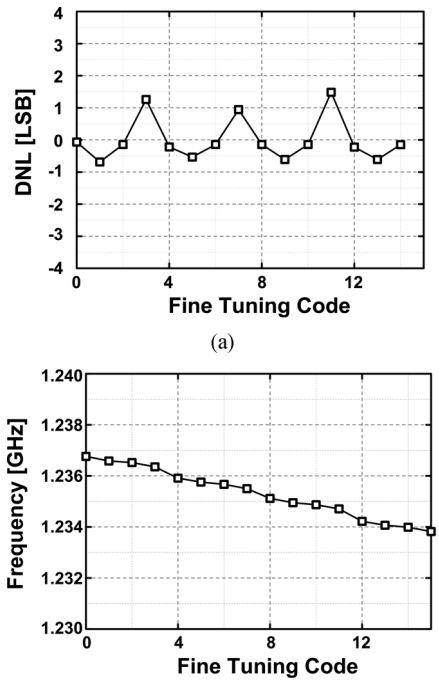

Fig. 19. Post-layout simulated (a) DNL and (b) DCO frequency against fine tuning code.

phase and amplitude degrading its deterministic jitter, as illustrated in Fig. 20. Conventional method uses a variable setting on the pulse generator for manually adjusting the injection pulse width, which inevitably lacks robust operation over process-voltage-temperature (PVT) variations. Performing background calibration on pulse injection technique necessities severe timing design for injection pulse width, which is not feasible for synthesizable analog circuits.

As shown in Fig. 21, a gated edge injection technique is proposed to avoid the injection pulse width issue [21]. Assuming that the oscillator frequency is N times higher than the reference frequency, an inverted injection-window signal forces the oscillator to stop oscillation at the rising edge of the injection-window signal. Then, an injection signal with clean edge is forwarded to the oscillator, which replaces the noisy edge V_y thus resetting the jitter accumulated for several cycles. Finally, the oscillator resumes normal operation after the falling edge of the injection-window signal with its phase aligned to the phase of injection signal. Comparing to the conventional pulse injection requiring severe timing design on the injection-pulse width, the proposed gated edge injection does not have strict demands on its injection-window width, which virtually eliminates the timing design issues. The whole phase replacement and alignment can be done in one reference cycle.

E. Design Procedure

Fig. 22 shows the design procedure using standard automated digital design flow. Gate-level Verilog netlists of DCO and DAC can be obtained directly from circuit schematics designed entirely from standard cell library. All other building blocks of the PLL are described by Verilog code, which can be used to generate gate-level netlists using commercially available logic synthesis tools such as Synopsys Design Compiler. Once all separated netlists including DCO and DAC are integrated to one netlist, the PLL layout can be directly obtained by using commercial P&R tools including Synopsys IC Compiler. During this step, the P&R tools assume that the whole PLL is a fully digital system and it might try to optimize the circuit by replacing/removing some of logic gates, or even changing the whole circuit while maintaining the identical digital functions. This optimization step might cause adverse effects in analog building blocks such as DCO and DAC. The adverse effects of optimization done by the EDA tool can be as insignificant as a slight degradation in performance or it can be serious enough to cause

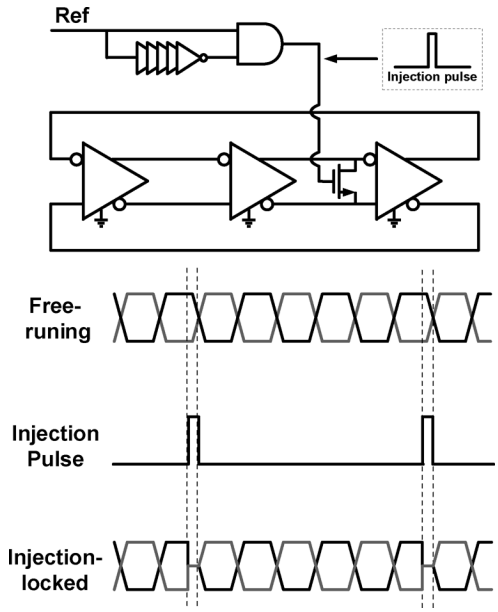

Fig. 20. Block diagram and locking transient of the conventional pulse injection locking.

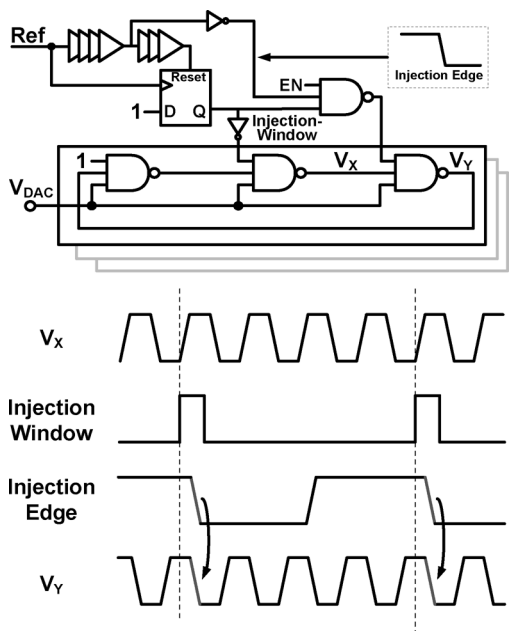

Fig. 21. Block diagram and locking transient of the proposed gated edge injection locking.

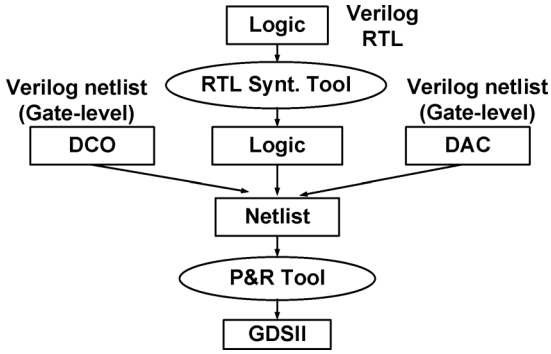

Fig. 22. The design method for the proposed fully synthesizable PLL.

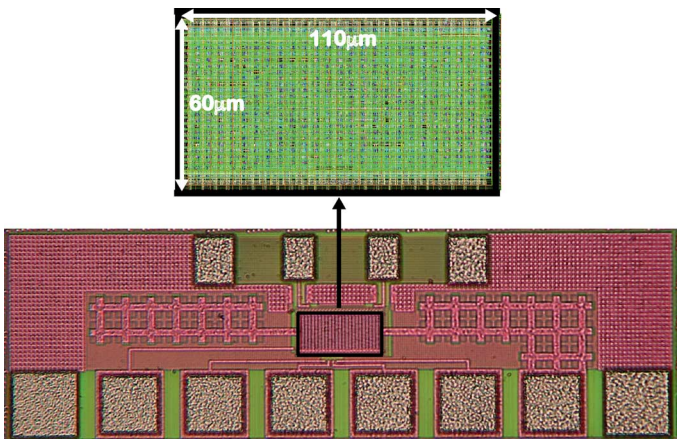

Fig. 23. Die microphoto.

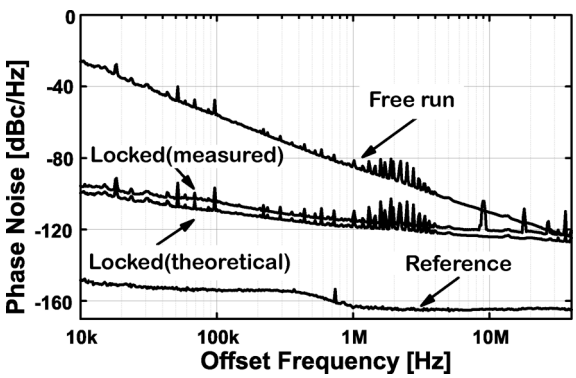

Fig. 24. Measured phase noise characteristic at a carrier of 0.9 GHz.

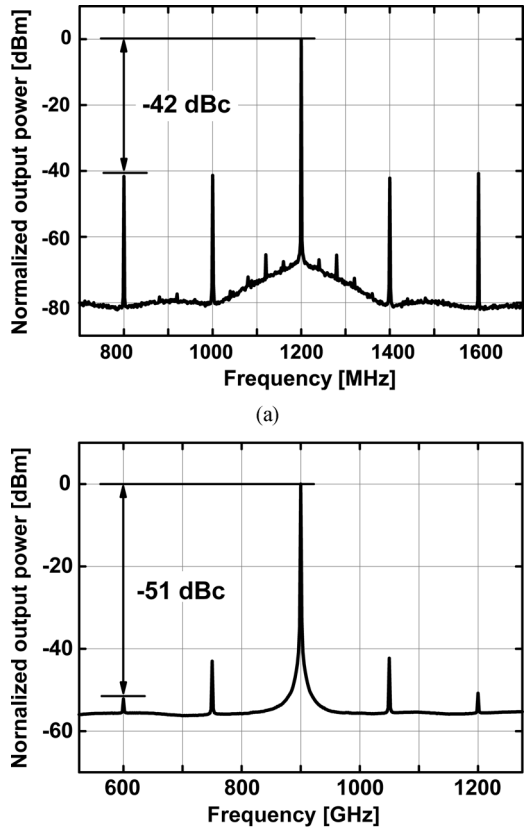

Fig. 25. Comparison of measured 2nd spur level between (a) conventional pulse injection and (b) edge injection at a multiplication factor of 6.

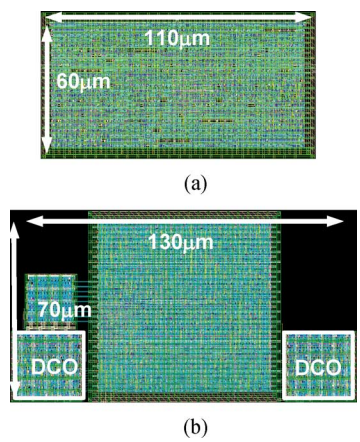

Fig. 26. Comparison of PLL with (a) the proposed fully synthesized layout and (b) hierarchical P&R with separated DCO layout.

a complete system failure. Thus, it is necessary to prevent the P&R tools from optimizing analog function building blocks.

IV. Measurement Results

The proposed fully synthesizable PLL is fabricated in a 65 nm digital CMOS technology. Fig. 23 shows a micrograph of the PLL which occupies only 110 μm$\times$ 60 μm layout area. The phase noise is evaluated by using a signal source analyzer (Agilent E5052B) and the spectrum is measured by using a spectrum analyzer (Agilent E4407B). The measured frequency tuning range of the PLL is 0.39 to 1.41 GHz. At a 0.9 GHz output, the power consumption is 780 μW excluding output buffers from a 0.8 V power supply. Fig. 24 shows the measured phase noise at 0.9 GHz output using a 150 MHz reference clock. The phase noise in free-running mode is measured in the third calibration phase with reference injection disabled. Considering (1) and assuming a 150 MHz reference clock, multiplication factor of 6 and output frequency of 900 MHz the theoretical phase noise is obtained. It can be seen from Fig. 23 that there is approximately a 3 dB difference between measured and theoretical calculated results. The phase noise maps to a 1.7 ps jitter when integrated from 10 kHz to 40 MHz. All

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART SYNTHESIZED PLLS.

	This work	[3]	[5]	[4]
Freq. [GHz]	0.39-1.41	1.5-2.7	0.25-1.65	0.4-0.46
Ref. [MHz]	40-350	10	25	40.3
Power [mW]	0.78 @900 MHz	13.7 @2.5 GHz	3.1 @250MHz	2.1 @403MHz
Area [mm^2]	**0.0066**	0.042	0.032	0.1
Normalized Area	1	6.36	4.84	15.15
Integ. Jitter [ps]	1.7*	N.A.	30	N.A.
Jitter RMS [ps]	2.8	3.2	N.A.	13.3
FOM [dB]	**-236.5**	-218.6**	-205.5	-214**
CMOS Technology	65nm	65nm	28nm	65nm
W/ custom cells?	No	No	Yes	Yes
Topology	Injection locking	TDC-based	TDC-based	TDC-based

*With a 150 MHz reference clock.
**FOM is calculated based on RMS jitter.

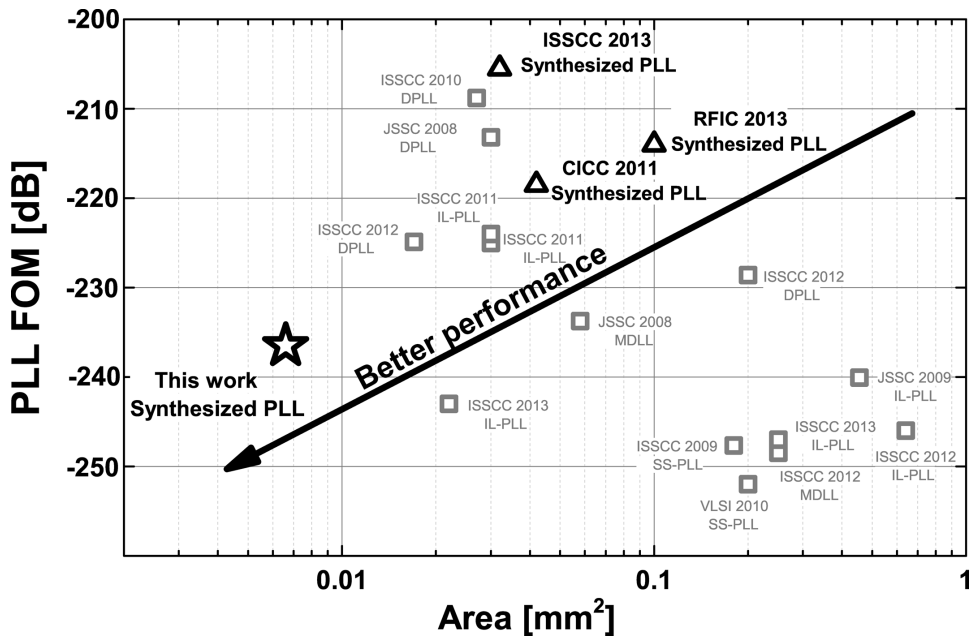

Fig. 27. Performance comparison with state-of-the-art prior work.

the above-mentioned measurements were performed at room temperature.

In order to assist the evaluation of spur level in edge injection, an injection-locked PLL using pulse injection method is chosen for comparison. The pulse width is tunable to achieve optimum performance for fair comparison. It is observed in Fig. 25 that both two injection method demonstrate similar 1st reference spur, which is around -41 dBc below the carrier. As for the 2nd reference spur at $2 \times f_{ref}$, the edge-injection PLL demonstrates -51 dBc spur level, while the pulse injection PLL achieves -42 dBc spur level. The reason is that the edge injection method introduces weaker periodical disturbance by replacing the oscillator noise edge.

Fig. 26(a) shows the fully synthesized layout of the whole PLL. On the other hand, Fig. 26(b) shows a different layout of the PLL. In this case, sub-blocks including DCOs and logics are P&R separately as macros, and then connected together to build the whole PLL. As mentioned before, the fully synthesized PLL achieves 1.7 ps RMS jitter while consuming 780 μW power resulting in an FOM of -236.5 dB, where FOM is defined as $10\log[(\sigma_{\rm t}/1{\rm s})^2 \cdot ({\rm P_{DC}}/1\ {\rm mW})]$, $\sigma_{\rm t}$ is the integrated jitter, and $\rm P_{DC}$ is the DC power consumption. The hierarchically synthesized PLL achieves 2.32 ps RMS jitter while have 640 μW power consumption resulting in an FOM of -234.6 dB, at the same output frequency. The difference in power consumption and jitter can be explained as follows. The oscillator in the fully synthesized PLL suffers from more parasitic capacitances from automatic P&R, which leads to lower oscillation frequency compared to that in the hierarchical synthesized PLL for the same power budget. Thus, larger current is necessary for the os-

cillator in the fully synthesized PLL to obtain the same oscillation frequency, which contributes to achieve lower phase noise. While there are some differences in power consumption and jitter due to parasitic capacitances from automatic P&R, both fully synthesized and hierarchically synthesized PLLs achieve similar performance in terms of FOM, which demonstrates that the fully synthesized design does not degrade overall performance. On the other hand, it is necessary to point out that the output jitter performance might vary from one layout synthesis procedure to another, due to parasitic capacitances variation as mentioned before. DCO phase noise can be simulated. Then the jitter of the PLL can be calculated from (1)–(3). Basically, the overall jitter performance is mainly determined by the DCO phase noise, which can be improved by adding more capacitances and increasing driving current.

Table I compares the results for synthesizable PLLs of previous studies [3]–[5] and that of this study. The proposed work achieves the best performance in terms of power, jitter, and area compared to previous work even those implemented using advanced technology.

Fig. 27 shows a comparison between the proposed and other work in terms of performance–area trade-off. It can be clearly seen that the proposed fully synthesized PLL achieves the best performance–area trade-off in terms of FOM and area when compared to other approaches.

V. Conclusion

To conclude, a fully synthesized PLL with a current output DAC and an interpolative-phase coupled oscillator based on standard digital library without any modification, which was designed using digital design flows, is presented in this paper. This design methodology significantly enhances productivity for all-digital PLLs. A standard cell based DAC is proposed to maintain frequency linearity and duty cycle balance. An interpolative-phase coupled oscillator is introduced to compensate the phase mismatch caused by automatic P&R. A gated edge injection technique is proposed to avoid the injection-pulse-width issue in conventional pulse injection-locking method.

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