

A 28 Gb/s 560 mW Multi-Standard SerDes With Single-Stage Analog Front-End and 14-Tap Decision Feedback Equalizer in 28 nm CMOS

Hiroshi Kimura, *Member, IEEE*, Pervez M. Aziz, *Senior Member, IEEE*, Tai Jing, *Member, IEEE*, Ashutosh Sinha, Shiva Prasad Kotagiri, Ram Narayan, Hairong Gao, Ping Jing, Gary Hom, Anshi Liang, Eric Zhang, Aniket Kadkol, Ruchi Kothari, Gordon Chan, Yehui Sun, Benjamin Ge, Jason Zeng, Kathy Ling, Michael C. Wang, Amaresh Malipatil, Lijun Li, Christopher Abel, and Freeman Zhong, *Member, IEEE*

Abstract—This paper presents a 28 Gb/s multistandard SerDes macro which is fabricated in TSMC 28 nm CMOS process. The transimpedance amplifier (TIA) base analog front-end achieved 15 dB high-frequency boost with an on-chip compact passive inductor. The adaptation loop for the boost is decoupled from the decision feedback equalizer (DFE) adaptation by the use of a group delay algorithm. The DFE is a half-rate 1-tap unrolled design with only two total error latches for power and area reduction. A two-stage sense amplifier-based latch achieved sensitivity of 15 mV. The high-speed clock buffer uses a PMOS active inductor circuit with common-mode feedback to optimize the circuit performance. The transceiver achieves error-free operation at 28 Gbps with 34 dB channel loss, consumes the worst case power of 560 mW/lane, and fully complies with multiple standards and applications.

Index Terms—Active inductor, group delay adaptation, TIA-based analog front end, unrolled DFE, 28 Gb/s SerDes.

I. INTRODUCTION

AS THE data center traffic increase by 20~30% a year, the demand for the high-speed SerDes is getting critical for deployments of new standards and protocols in communication systems to address increasing bandwidth demand. In order to meet new standards, such a OIF CEI-25G-LR, CEI-28G-MR/SR/VSR, IEEE802.3bj, and 32G-FC, data rate are increased to 25~28 Gbps that is more than 75% higher than previous generation of SerDes, which operates at 10~16 Gbps. A high-speed SerDes must meet multiple challenges including high-speed operation, intensive equalization techniques, low power consumption, small area, and robustness. Particularly for the SerDes applications with several hundreds of lanes integrated in single chip, the power consumption is a very important factor in maintaining high performance. There are several previous works at 28 Gbps or higher data rate [1]–[4]. Those use unrolled decision feedback equalizer (DFE) to meet the critical timing margin, but the unrolled DFE structure

Manuscript received April 22, 2014; revised July 02, 2014 and July 30, 2014; accepted August 01, 2014. Date of publication September 09, 2014; date of current version November 20, 2014. This paper was approved by Guest Editor Pavan Kumar Hanumolu.

The authors are with LSI Corporation, San Jose, CA 95131 USA (e-mail: hiroshi.kimura@avagotech.com).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2014.2349974

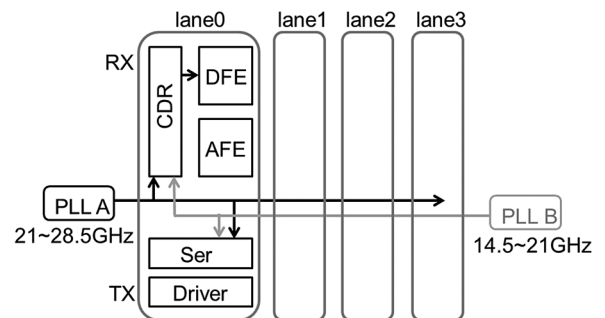


Fig. 1. SerDes system architecture.

increases the number of DFE slicers that increases the overall power and die area. In order to tackle these challenges, we introduced several circuits and architecture blocks.

One of the key design is an analog front-end (AFE) which achieve 15 dB high-frequency boost at 14 GHz. In order to do this, we used high-speed transimpedance amplifier (TIA) with on-chip compact inductor feedback. The TIA amplifier is very simple inverter-based structure with tail current for high bandwidth. The boost is adaptive and its adaptation loop is decoupled from the DFE adaptation loop by the use of a group delay adaptation algorithm. The DFE is a half-rate first-tap unrolled structure with only two total error latches for power and area reduction. A two-stage sense amplifier-based slicer is developed to achieve sensitivity of 15 mV with long degeneration sampling time and DFE timing closure. We also developed the high-speed clock buffer which uses a new active inductor circuit. This active inductor circuit has the capability to control output common-mode voltage to optimize circuit operating points.

II. SERDES SYSTEM ARCHITECTURE

A. SerDes Subsystem

The SerDes subsystem consists of four lanes and two PLLs as shown in Fig. 1. Each PLL has two LC tank VCOs to generate the low jitter clock for each lane. The PLLA covers the 21 to 28.8 GHz frequency range and the PLLB covers 14.5 to 21 GHz. Combining two PLLs, it covers multiple standards with 14.5 to 28.5 Gb/s native rate. Those PLL clocks are driven to each lane, and each lane has a clock mux to select clock source

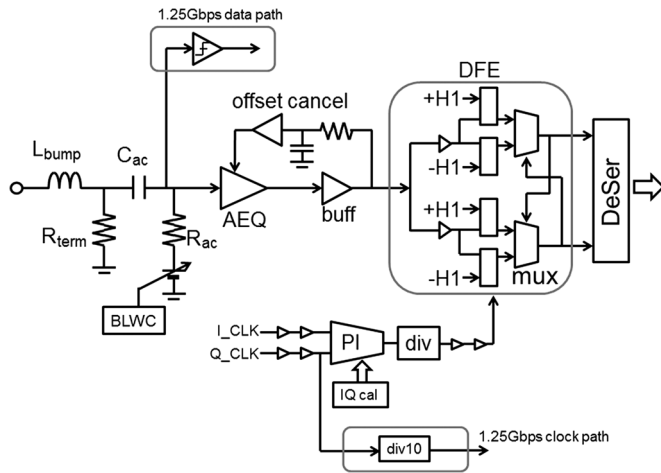


Fig. 2. RX block diagram.

either from PLLA or PLLB. With this configuration, it supports rate agility on a lane basis with dual PLLs and independent clock muxes. Also, it has half rate, quarter rate, and 1/8th rate mode to supports multiple standards.

B. Receiver Block

Fig. 2 shows the entire SerDes block diagram. For the receiver (RX) input stage, it has bump inductor L_{bump} followed by termination resistor R_{term} . The bump inductor is placed under the bump and there is no area penalty. Also it improves the return loss performance. Then the signal goes through on-chip ac coupling capacitor C_{ac} . The capacitance of C_{ac} is 4 pF, and the resistance of R_{ac} is 120 k Ω to form the high-pass filter (HPF). This HPF corner frequency is 330 kHz, and it is sufficiently low to support a wide frequency range.

When the ac-coupled capacitor is needed on a printed circuit board (PCB), it requires the through-hole on the PCB and it creates the impedance discontinuity. The impedance discontinuity causes the signal reflection and in order to compensate this reflection, the DFE needs to have a higher tap locations like 30~50 tap. This increases the overall SerDes power consumption and area. Thus, our approach is to put the on-chip ac-coupling cap on the die and it eliminates the reflections. We implemented this capacitor with metal-to-metal fringing cap and placed under bump to minimize the area penalty. Furthermore, on-chip ac-capacitance decouples the dc bias voltage from transmitter (TX) side and the AFE input common-mode voltage can be set for optimum bias voltage. After the signal goes through the ac-coupling capacitor, the differential signal of long run length data can droop and a base line wander correction (BLWC) circuit recover the low-frequency drift [5]. Fig. 3 shows a high-level analysis of the impact of ac coupling capacitor on the error induced on an ideal transmitted data stream. The error is a percentage of the transmitted amplitude. We plot the error percentage versus ac coupling corner or pole frequency for various PRBS patterns including PRBS7, 9, 11, and 15. The error is measured over the length of one PRBS pattern block. Plotted also are the results for the “CLS52TP2” pattern which is an IEEE 802.3AP recommended test pattern

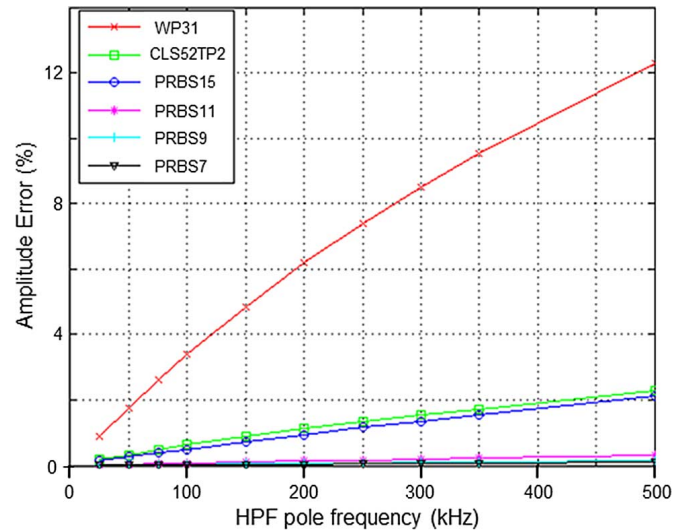


Fig. 3. BLW effect.

that emulates some of the run length properties of PRBS31. Since PRBS31 is an extremely long pattern, we isolated (through exhaustive search) a worst case section of this pattern, WP31, which provides the worst error from ac coupling. In reality, this section of the pattern occurs with low probability but we consider this here nonetheless to upper bound the effects of ac coupling. The plot also includes the results for WP31. For shorter length PRBS patterns up to 11, the effect of ac coupling of even up to 500 kHz is very small. For our corner frequency of 330 kHz, the error with PRBS15 and CLS52TP2 is less than 2%. Only for the low-probability worst case section of PRBS31, we see the error become much more significant up to 9%. The BLWC loop helps to cancel any residual error from PRBS15/CLS52TP2 or the worst case section of PRBS31. The overall baseline wander cancellation scheme is similar to that of [5], and the cancellation term depends on the received data pattern but the cancellation gain is independent of the data pattern.

The AFE is a single-stage circuit and incorporates both the variable gain adjustment (VGA) and linear equalizer (LEQ) functions in it. The buffer drives the DFE input stages and the buffer output is controlled by common mode feedback to control the common mode for the DFE input stage. The offset cancellation loop monitors the buffer output offset and feed back to the AFE. The DFE is a 14-tap half-rate design and it uses first-tap unrolled architecture with sign-sign least mean square (LMS) algorithm for tap adaptation. The DFE output data are deserialized and send to the digital block. The DFE is a half rate design and it has odd and even blocks. Each odd and even block uses a half-rate clock (2T clock) with in-phase (I) clock and quadrature phase (Q) clock which have 90 degree phase difference from each other. The I clock is used to sample the data and the Q clock is used for transition sampling. A phase interpolator (PI) block receives 2T I and Q quadrature phase clocks from the PLLs and generates the sampling clock for DFE.

The CDR consists of a bang-bang phase detector (BBPD) followed by a digital decimated loop filter similar to that described

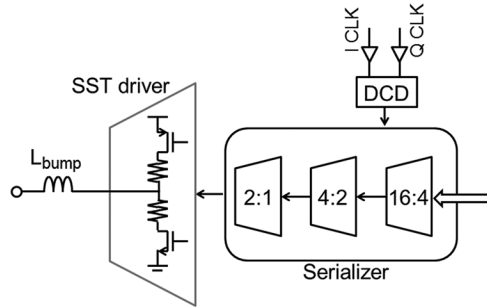


Fig. 4. TX block diagram.

in [21]. The loop filter is a second-order filter with a proportional path and an integral path. The proportional and integral paths are summed to obtain the overall loop filter output which is a 6-bit phase code that controls a PI with 1UI/64 spacing or resolution.

The linear range of PI is from 6 to 14 GHz, and it is followed by programmable divider 1, 1/2, and 1/4 (Fig. 2). With this configuration, it supports a data rate from 3 to 28 Gbps. For the 1.25 Gbps data rate, the data path and the clock path are treated differently. For 1.25 Gbps, the clock input to RX is 12.5 GHz, and it goes to dedicated divided-by-10 blocks to generate ten phases. For the 1.25 Gbps signal path, the input signal does not have much of an ISI effect, and the signal swing is relatively large. Thus, it does not require any equalization, and we have a separate signal path for this mode. The 1.25 Gbps input signal goes to dedicated comparator directory, and the output of the comparator is sent to digital block. The digital block receives the data and the ten-phase clock and the digital clock and data recovery (CDR) loop select the one phase out of ten phases.

There are several buffer stages before and after the PI to maintain the clock quality. These clock buffers employ active inductor circuits with common-mode feedback (CMFB) circuit. An IQ skew calibration circuit is employed to maintain the phase relationship between I and Q clocks before the clocks reach the DFE latches. The DFE latches are calibrated according to their dc value with forced value onto the first-tap unrolling muxes.

C. Transmitter Block

The TX block consists of serializer and source-series-terminated (SST) driver shown in Fig. 4. The serializer receives 16 bit parallel data from the digital block, and it has 16:4, 4:2, and 2:1 serializer in it. Then, serialized data are passed to driver. Since the data are serialized before the driver, the driver does not require any clock. This reduces the number of clock buffer and power consumption. The driver uses a SST driver structure with 3tap FIR filter [5], [6]. In order to achieve the low power consumption, we minimized the driver structure to 68 segments and we reduced the TX outputs loading by reducing the ESD devices as possible. The output of the driver is connected to bump inductor L_{bump} to improve the return loss performance. The clock path for TX has a duty cycle distortion (DCD) correction circuit. The clock duty cycle is one of the most important parameters because the duty cycle distortion directly degrades the TX eye opening so it is necessary to have a calibration or

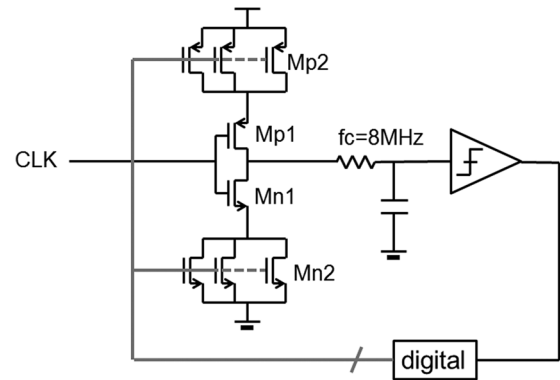


Fig. 5. Duty cycle distortion correction circuits.

real-time compensation. We implemented the duty cycle correction circuit and is shown in Fig. 5. The clock buffer with programmable duty cycle is configured with Mn1, Mn2, Mp1, and Mp2. The Mn2 and Mp2 are programmable devices, and they can control the duty cycle with this configuration. During the calibration mode, digital circuitry sweeps the control code for the programmable duty cycle circuit. The output of the programmable duty cycle buffer goes through the low-pass filter, and the duty cycle is converted to the voltage domain. Then, the comparator detects if its duty cycle is higher or lower than 50%, and the comparator output is sent to the digital block. Then, the digital block finds the optimum code. The comparator is connected after the low-pass filter and that corner frequency is set to 8 MHz to detect the lower frequency portion of the clock as possible. Thus, the comparator does not require the-high speed operation, and it uses the large device and careful layout to minimize the comparator offset.

III. ANALOG FRONT-END DESIGN

A. Analog Front-End Architecture

The AFE is an important block for not only equalization but also the robustness and power. In order to achieve those requirements, a simple and minimum stage of construction is preferable. For the high-speed application such as 28 Gbps or above, increasing the bias current with the simple differential pair circuit does not help after certain optimum bias because the output impedance of the differential pair degrade by increasing the bias current. Thus, even the gm will improve with higher current, it cannot achieve sufficient gain. It also degrades the bandwidth because the large device size is needed at the low-power supply voltage.

The TIA circuit is widely used in high-speed applications [7]–[10], and the TIA has an advantage to improve the high-frequency bandwidth. We developed a single-stage TIA-based LEQ with on-chip inductor feedback. The AFE needs to drive the DFE input stages where there are several data and error DFE slicer circuits connected. The TIA decouples the heavy loading capacitance and improves the high-frequency response. Also, we developed the compact inductor and made it possible to implement in a small silicon area. With the TIA structure plus compact inductor, we achieved 15 dB boost for a 28-Gbps data rate.

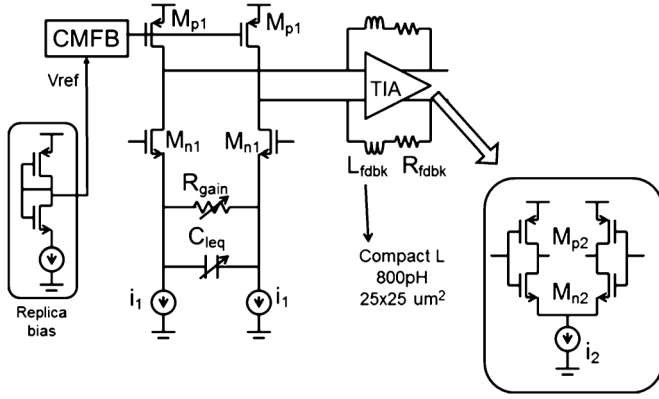


Fig. 6. AFE circuit diagram.

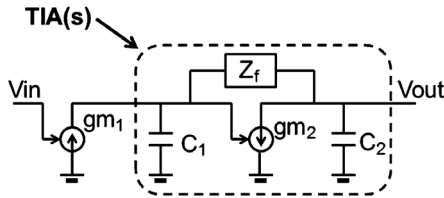


Fig. 7. TIA small-signal model.

The AFE input stage is shown in Fig. 6 and has NMOS differential pair M_{n1} with degeneration resistor R_{gain} and capacitor C_{leq} . The gain and the boost are controlled by tuning the R_{gain} and C_{leq} . The output current from the input differential pair is fed to the TIA stages. The TIA amplifier is configured by single stage inverter based circuit with M_{n2} , M_{p2} , and the tail current i_2 to maintain the dc bias. In order to keep the M_{n2} and M_{p2} in the TIA to be biased properly over the PVT, the reference voltage for CMFB is generated by the replica bias block in Fig. 6. The replica bias block is a half circuit of TIA, and the input and the output are shorted. This generates the reference bias voltage to be optimum over the PVT variation.

For the feedback path, we use the compact inductor L_{fdbk} and the resistor R_{fdbk} in series. This compact inductor uses top two metal layers and the inductance is 800 pH. The size of inductor is $25 \mu\text{m} \times 25 \mu\text{m}$. Also, the common-mode feedback circuit is implemented to make the dc operation point optimum for the TIA amplifier.

Fig. 7 shows the simplified small-signal model of the analog front-end circuit. The gm_1 represents transconductance of the input-stage differential pair, and gm_2 is the transconductance of TIA amplifier. C_1 and C_2 are the parasitic capacitors at the input and output node of TIA. The Z_f is the feedback path impedance. The transfer function of this small-signal model is expressed as

$$\frac{V_{out}}{V_{in}} = gm_1 TIA(s) \quad (1)$$

$$TIA(s) = \frac{1}{s^2 + \frac{C_1 + C_2}{C_1 C_2 Z_f} s + \frac{gm_2}{C_1 C_2 Z_f}} (1 - Z_f) \quad (2)$$

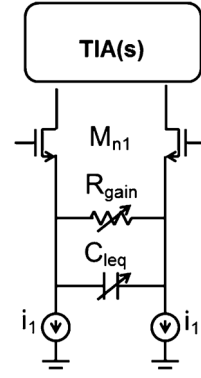


Fig. 8. AFE circuits.

and shows the second-order low-pass filter transfer function. The dc gain, pole frequency and Q are given by

$$dc_{gain} = -gm_1 \left(Z_f - \frac{1}{gm_2} \right) \quad (3)$$

$$\omega_p = \sqrt{\frac{gm_2}{C_1 C_2 Z_f}} \quad (4)$$

$$Q = \frac{\sqrt{gm_2 C_1 C_2 Z_f}}{C_1 + C_2} \quad (5)$$

To make gm_2 large in design, the pole frequency moves higher and the Q factor becomes high. Thus, it improves the high-frequency behavior. Also, the dc gain is simplified to $gm_1 Z_f$, and this improves the robustness.

B. Circuits Design

The AFE circuit is shown in Fig. 8 and the AFE configure the differential input pair with the TIA as a loading. The overall AFE transfer function can be expressed by (6).

$$\frac{V_{out}}{V_{in}} = \frac{gm_{n1}(1 + sC_{leq}R_{gain})}{sC_{leq}R_{gain} + 1 + gm_{n1}R_{gain}} TIA(s) \quad (6)$$

$$dc_{gain} = \frac{1}{R_{gain} \frac{1}{gm_{n1}}} \left(Z_f - \frac{1}{gm_2} \right) \quad (7)$$

$$zero = \frac{1}{C_{leq} R_{gain}} \quad (8)$$

where the Z_f is the feedback impedance of TIA block. By tuning the degeneration resistor R_{gain} , we can control the gain, and, by tuning C_{leq} , the high-frequency boost is controlled.

C. AFE Adaptation

The adaptation algorithm for the AFE peaking parameter is a simplified form of a least mean squared (LMS) type of algorithm [11]. Although this algorithm generally works well, the use of the error information at the data sampling phase and past decision terms which are also used by the DFE adaptation can in certain situations lead to coupling of the adaptation loops when they are jointly adapted, because both AFE and DFE adaptation

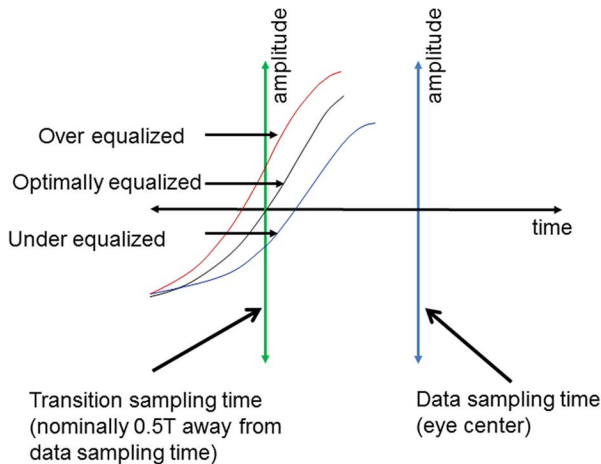


Fig. 9. Group-delay adaptation algorithm.

use same error information. The AFE peaking parameter control parameter $Ki(n)$ is updated as follows:

$$Ki(n+1) = Ki(n) - \mu_{afe} \text{sgn}[e(n)] \sum_{l=1}^{N_{afe}} d(n-l) \quad (9)$$

where μ_{afe} is an adaptation gain control parameter for the AFE. The parameter $Ki(n)$ is mapped through a look up table to the $Cleq$ value which controls the peaking. Note that this update equation uses the sign of the error weighted by an average of past N_{afe} sliced data samples. This update equation has an LMS-based analytical underpinning derived from the AFE formulaic representation of [11]. Although the AFE topology of [11] is somewhat different than here (here, the peaking control $Cleq$ affects the peaking magnitude as well as the peaking frequency to some extent, whereas in [11] the peaking frequency is independent of the peaking magnitude control), we empirically determined that (9) could be used to adapt the peaking control here as well. Another more *ad-hoc* view of the adaptation equation independent of the AFE topology is obtained by considering the role of the AFE in performing post-cursor intersymbol equalization across multiple symbol periods—a function which is also performed by the DFE of Section IV; albeit, in the case of the DFE, the equalization happens through feedback cancellation. Note that the LMS-based DFE equalizer tap adaptation of Section IV is governed by (13) which happens to be individual terms of the AFE update equation for up to the first N_{afe} taps of (9). Equation (9) for the AFE adaptation can be thought of as an composite or amalgamation of adaptation of multiple post-cursor equalization taps performed in a manner similar to the DFE taps of (13). Although the AFE update (9) allows the AFE peaking to converge adequately, the fact that (9) and (13) use common terms implies that the closely related or coupled adaptation metrics govern both AFE peaking and DFE tap adaptation which can sometimes lead to a suboptimal solution as the AFE and DFE adaptation are coupled and may “fight” to optimize the underlying minimum mean squared error criterion. Based on our simulation experience, we find that lower loss channels, the AFE may be somewhat suboptimally overequalized based on typical adaptation parameters.

TABLE I
AFE GROUP-DELAY ADAPTATION TABLE

$d(n-1)$	$d(n-1/2)$	$d(n)$	$\Delta(n)$
-1	-1	1	-1
-1	1	1	1
1	-1	-1	1
1	1	-1	-1

To alleviate this potential coupling, a group-delay algorithm that uses error information at the transition sample is also considered. Fig. 9 shows the concept of the heuristic group-delay algorithm, named as such because the algorithm considers waveforms corresponding to different group delays for different amounts of AFE peaking. The figure shows three waveform segments in the vicinity of the transition sampling time which is nominally $0.5T$ away from the data sampling time. When the AFE provides optimal equalization, the waveform segments would ideally have an average zero crossing threshold at the transition sampling point. If the AFE overequalizes the signal, the waveform zero crossing appears earlier than for optimal equalization, and the transition samples will tend to have a positive bias. If the AFE underequalizes the signal, the waveform zero crossing appears later than for optimal sampling, and the transition samples will tend to have a negative bias. Thus, we can correlate transition sample values to whether the AFE peaking should be increased or decreased. Let the binary sliced transition sample value be denoted by $d(n-1/2)$ and the sliced data value by $d(n)$. Then, we have Table I, which provides the increase/decrease $\Delta(n)$ resulting from correlating $d(n-1/2)$ when we have a transition between the prior data bit $d(n-1)$ and the current data bit $d(n)$. With this group-delay algorithm, the AFE peaking code is then updated as

$$Ki(n+1) = Ki(n) - \mu_{afe} \Delta(n). \quad (10)$$

Since this group delay algorithm does not use the signed error signal for adaptation, it significantly alleviates coupling with DFE adaptation.

Although the group-delay AFE adaptation uses transition samples as does the BBPD of the CDR loop, the CDR adaptation bandwidth is significantly larger than that of the LEQ adaptation bandwidth thereby further minimizing any interaction between the CDR and LEQ adaptation loops.

IV. DFE DESIGN

The DFE block is a half-rate design and has 14 feedback taps with the first tap unrolled. The first tap unrolling relaxes the critical timing [12]–[16]. Fig. 10 shows the DFE block diagram and, since this is a half-rate design, it has the same odd and even block. Each odd and even slice receives the analog signal from AFE, and the prebuffer drives five latches. Those latches are eye finder latch for eye monitoring, error latch for adaptation, transition latch for CDR, and two unrolled data latches. The DFE feedback is one of the critical paths and is shown in Fig. 11. This block diagram is the odd slice, and the even slice has the same structure. A half-rate DFE with first tap (H1) unrolled architecture is implemented to eliminate H1 tap timing from the critical path. Then, the H2 tap becomes one of the most critical

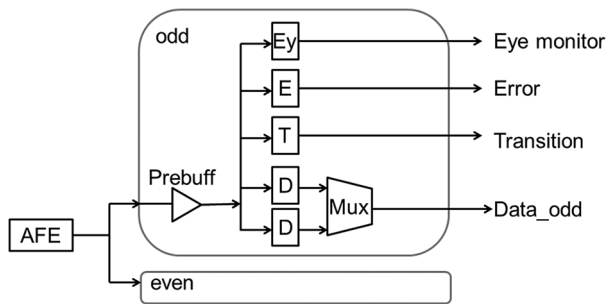


Fig. 10. DFE block diagram.

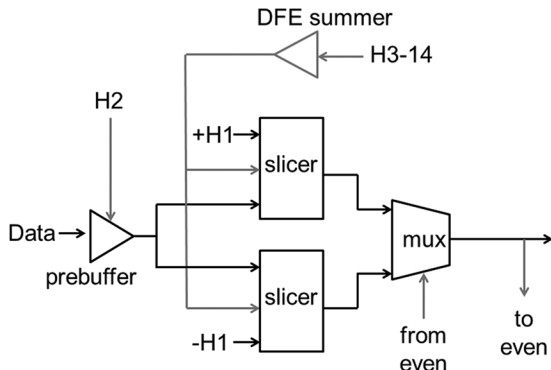


Fig. 11. DFE feedback path.

timing paths, and we treated this separately from other taps and the H2 tap is fed back to the DFE buffer. The rest of H3–H14 taps are combined at DFE summer and fed back to the slicer.

All of the DFE taps including unrolled 1st tap are adapted by LMS algorithm. Let $z(t)$ be the input to the DFE from the output of the AFE. The DFE equalized signal is then $w(t)$, which is the DFE input from which the DFE feedback terms are subtracted. Let $w(n)$ be the sampled version of the DFE equalized signal. In this design, only the second tap and higher are subtracted from the AFE output to obtain $w(n)$ due to first tap unrolling as follows:

$$w(n) = z(n) - \sum_{l=2}^N h(l)d(n-l). \quad (11)$$

With the first tap unrolling, the final decision $d(n)$ is made by slicing $w(n)$ at thresholds based on the unrolled tap1 value $h(1)$ and the prior data bit $d(n-1)$ as follows:

$$d(n) = \begin{cases} w(n) - h(1) & \text{if } d(n-1) = 1 \\ w(n) + h(1) & \text{if } d(n-1) = -1 \end{cases}. \quad (12)$$

The algorithmic LMS adaptation for unrolled tap1 is similar to the standard DFE tap1 adaptation with $l = 1$ for the first tap

$$h(n, l) = h(n-1, l) - \mu \text{sgn}[e(n)]d(n-l). \quad (13)$$

The only difference is that the sign of the error signal $e(n)$ is obtained from slicing signal amplitudes not relative to the equalization target amplitude $h(0)$ but at an error latch threshold obtained from a combination of $h(0)$ and $h(1)$.

For the first tap unrolled DFE, there are four error latches per odd and even slice in general, which is shown Fig. 12(a). The

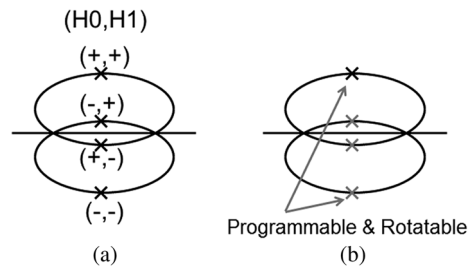


Fig. 12. Error position for unrolled DFE.

error latch threshold positions are the combination of $+/-$ H0 and $+/-$ H1. The error latch slicer output is determined based on the following equations:

$$\text{sgn}[e(n)] = \begin{cases} w(n) - h(0) - h(1) & \text{if } d(n) = -1, d(n-1) = -1 \\ w(n) - h(0) + h(1) & \text{if } d(n) = -1, d(n-1) = 1 \\ w(n) + h(0) - h(1) & \text{if } d(n) = 1, d(n-1) = -1 \\ w(n) + h(0) + h(1) & \text{if } d(n) = 1, d(n-1) = 1. \end{cases} \quad (14)$$

Thus, the unrolled DFE structure increased the number of latches and increased the overall power and area. In our architecture shown in Fig. 12(b), we use only one error latch instead of four per even and odd slice. This error latch position is programmable (static mode) and dynamically rotatable to minimize sensitivity to pattern variations (dynamic mode). There are four possible positions for each odd and even error latch. Thus, there are 16 combinations for those error positions, and we can choose any combination by programming for the static mode. For the dynamic mode, we rotate several combinations of positions periodically. The period of each position can be programmable from 512 T to 32 768 T. With this structure, we could reduce the power and complexity without losing any performance.

A slicer circuit design is the most challenging part of the DFE implementation as link performance directly depends on the slicer sensitivity. Fig. 13(a) shows the slicer circuit diagram, and Fig. 13(b) shows the sampling clock generation circuit and its output clock phases. In order to increase the DFE slicer sensitivity, it requires a long degeneration time. The sampling period is minimized by inverter gate delay, and it increases the degeneration time. With this sampling phase generation, we achieved 15 mV sensitivity. For this sampling clock, the duty cycle is not necessary to be 50% in our design.

The slicer has three differential inputs for the data, the H3–H14 feedback, and the offset. The CK1 and CK2 generate the three phases, sampling phase, regeneration phase, and preset phase. When the CK1 is high, it samples the data. Then, CK1 goes to low, and the positive feedback circuits start regeneration. After CK 2 goes to low, it will do preset. The following mux stage also has the same circuit topology with slicer circuits, and this architecture achieved 15 mV sensitivity. The error latch, transition latch, and eye monitor latch are all same circuit structure as data latch.

V. CLOCK BUFFER DESIGN

The high-speed clock buffer is a key building block component and is used in many blocks in the SerDes. The clock

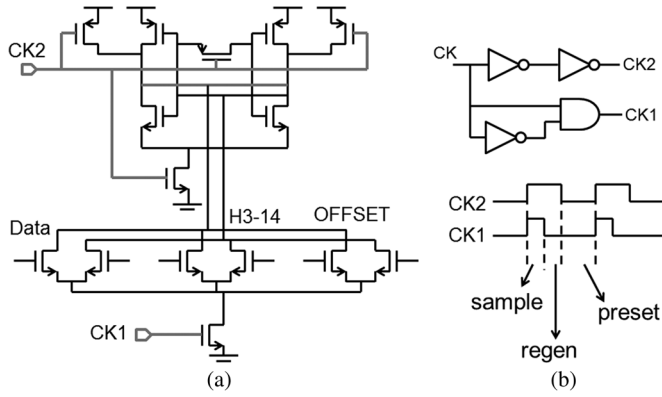


Fig. 13. (a) DFE slicer circuit diagram. (b) Sampling clock phase.

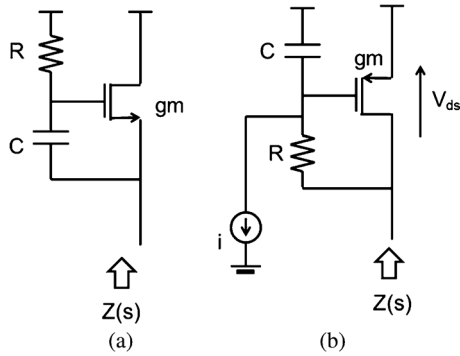


Fig. 14. (a) Conventional active inductor load. (b) PMOS active inductor load with improved headroom.

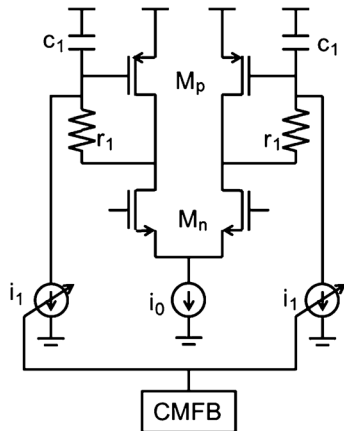


Fig. 15. Active inductor clock buffer circuits.

buffer performance and power are very important for overall the SerDes power consumption. In order to achieve low power and high-frequency bandwidth, the active inductor circuit is widely used in many applications [17]–[20]. Fig. 14(a) shows the conventional active inductor load circuit and the NMOS transistor with the resistor connected between the gate of NMOS transistor and low impedance node, like power supply. The capacitor is connected between the source and the gate of the NMOS transistor. The impedance of this active inductor loading is given by

$$Z(s) = \frac{sCR + 1}{gm} \quad (15)$$

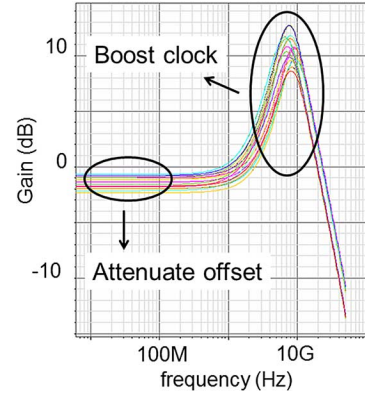


Fig. 16. Simulated frequency response of active inductor clock buffer circuit.

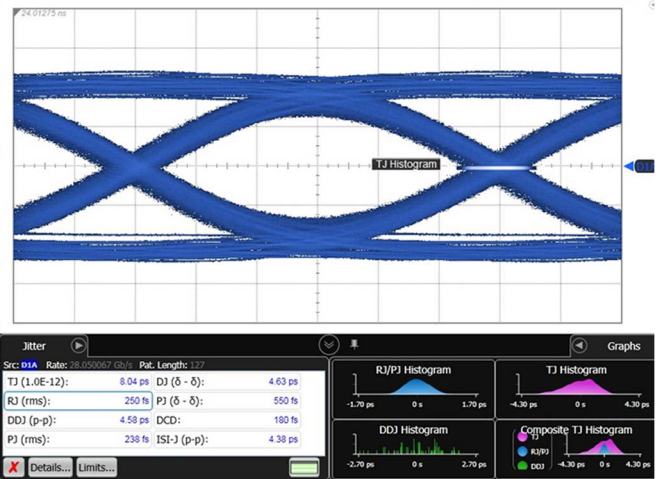


Fig. 17. TX eye diagram of 28 G PRBS7: RJ = 250 fs, TJ = 8 ps.

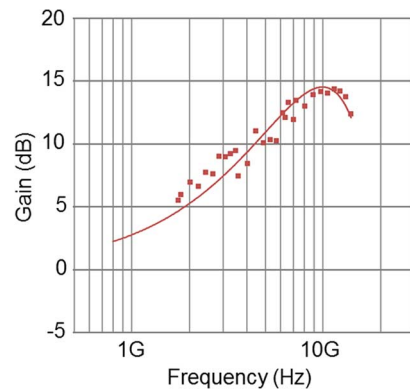


Fig. 18. Digitally measured AFE+buffer+DFE prebuffer frequency response.

where the gm is the transconductance of the NMOS transistor. The advantage of this active inductor load is that the bandwidth is improved by adding the zero. However, it requires the V_{gs} as a head room. In order to relax the head room, the native device can be used. However, usually minimum channel length of native device is limited by process and is not applicable for high-speed applications with low-power supply voltage application. Fig. 14(b) shows the PMOS active inductor load circuit. The PMOS, capacitor and resistor are connected similar

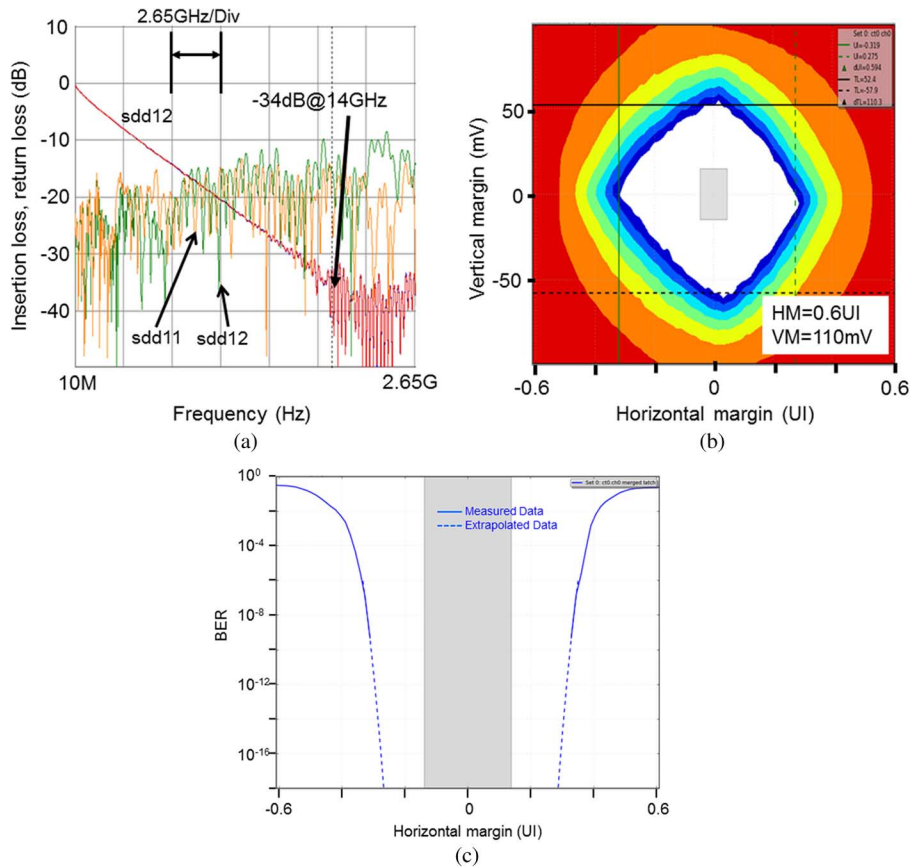


Fig. 19. (a) Test channel. (b) Measured eye diagram @10E⁻⁹. (c) Measured bathtub curve.

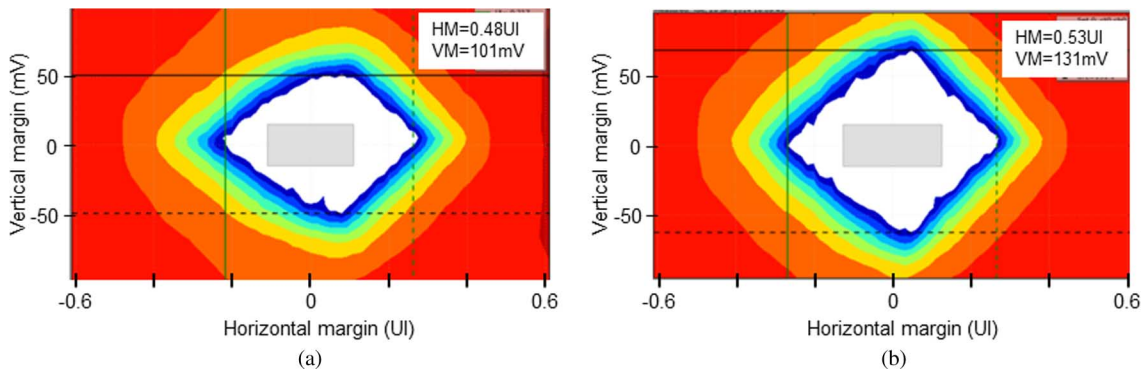


Fig. 20. Eye margin with error latch. (a) Static mode. (b) Dynamic mode.

to NMOS active inductor circuit. The current source is connected to make the V_{ds} become $V_{gs} - iR$ and the head room is improved by iR . Furthermore, by controlling the current i , the common-mode voltage can be adjusted. The output common mode voltage can be expressed by $VDD - V_{gs} + iR$. The current source i is controlled by common mode feedback circuit to maintain the optimum output voltage.

The complete clock buffer circuit with this active inductor loading is shown in the Fig. 15. M_{in} is the input differential pair and M_p , r_1 , and c_1 configure the active inductor loading. The common mode feedback circuit controls the current i_1 . Fig. 16 is the simulated frequency response of this active inductor clock buffer circuit over the PVT sweeps. One additional benefit of this clock buffer circuit is that it doesn't amplify the dc input. In

other words, it attenuates the input offset whereas it amplifies the amplitude at the clock frequency.

VI. MEASUREMENT RESULTS AND CHIP MICROGRAPH

The silicon measured TX output waveform is shown in Fig. 17. This measurement is done at 28 Gbps with PRBS7 pattern and it shows the 250 fs random jitter and 8 ps total jitter. A digitally measured AFE frequency response is shown in Fig. 18. For this measurement, we applied a sinusoidal wave at the RX input and sweep that frequency. We then let CDR lock to the waveform and run the target amplitude adaptation without DFE. After the adaptation completes, we monitor the mean target amplitude from reading the H0 value. Then we calculated the gain from H0 compared with the input signal

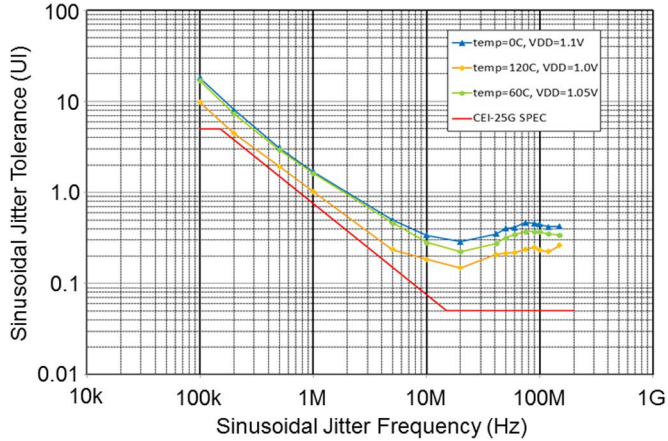


Fig. 21. Sinusoidal jitter tolerance with 31.5 dB channel loss (at 12.9 GHz) which exceeds CEI-25LR channel loss compliance spec.

amplitude. This measurement includes AFE, a buffer, and DFE prebuffer response and a 2~3 dB loss from the package and PCB trace.

Fig. 19(a) is a frequency response of the measured test channel. It shows the insertion loss measurement *sdd12* and return loss measurements *sdd11* and *sdd22*. The total insertion loss is 34 dB at 14 GHz which is the Nyquist frequency. Fig. 19(b) is the measured eye diagram at 28 Gbps and the bit error rate (BER) is $10E^{-9}$ bit. The vertical eye margin is 110 mV and the horizontal margin is 0.6UI. Fig. 19(c) is the measured bathtub data up to $10E^{-9}$ and extrapolated data to $1E^{-18}$. Fig. 20 shows the eye opening test for static mode and dynamic mode of error latch positioning with PRBS31 pattern at 25 Gbps. The horizontal margin with dynamic mode is 30% larger and the horizontal margin is 0.05UI wider than that of static mode.

The sinusoidal jitter tolerance measurements over temperature and power supply voltage variations are shown in Fig. 21. The test channel is 31.5 dB loss at 12.9 GHz. The test channel includes all other impairments, like cross talk and random noise interference. The tested data rate is 25.8 Gbps and the BER is $10E^{-12}$ with PRBS31 pattern. The power supply voltage is swept from 1.0 to 1.1 V and temperature from 0 to 120 °C.

Fig. 22 is the chip microphotograph that consists of four lanes and two PLLs in subsystem macro. The PLLA is placed between lane 0 and 1, and the PLLB is placed between lane 2 and 3. The clock tree path is located between the analog TX and analog RX. The size of each lane is 300 μm wide and 1854 μm long. The total SerDes subsystem macro area is 3.34 mm^2 .

The worst case power breakdown for four-lane one-PLL configuration SerDes is shown in Fig. 23. The measured worst case power consumption per lane is 560 mW under conditions of 28 Gbps, three sigma fast silicon die material, and temperature of 125 degree. The SerDes use three power supply voltages. The 1.5-V supply is used only for the regulator used for PLL VCO and high-speed divider. The 0.85 V is used for static logic, deserializer, and serializer except final 2:1 mux. The remaining high-speed blocks use 1.05 V. The SerDes transceiver summary and comparison table is shown in Table II.

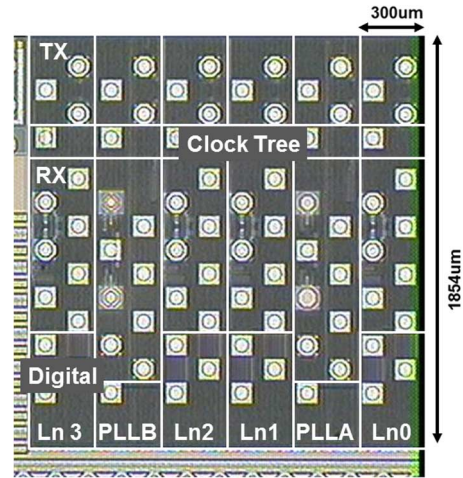


Fig. 22. Chip microphotograph.

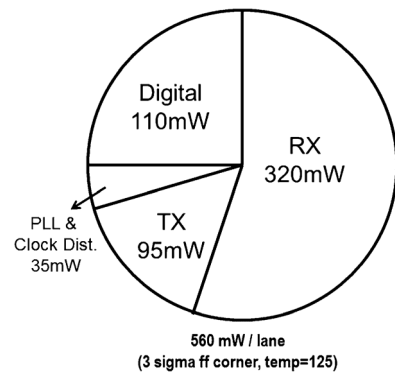


Fig. 23. SerDes power breakdown. 28 Gbps four-lane one-PLL configuration.

TABLE II
TRANSCIEVER PERFORMANCE COMPARISON

Reference	[1]	[2] *RX only	This work
Technology	32nm SOI CMOS	28nm CMOS	28nm CMOS
Power Supply	1.2V / 1.05V / 0.85V	0.9V	1.5V / 1.05V / 0.85V
Area / lane	0.81 mm^2	(0.33 mm^2)*	0.83 mm^2
Data Rate Range	~28.5 Gbps	32Gbps	1.25 ~ 28.5 Gbps
Channel Loss	35dB @ 14GHz	37dB @ 16GHz	34dB @ 14GHz
TX output RJ@28Gbps	450fs	—	250fs
Power @28Gbps	693 mW	(240 mW)*	560 mW
Power @1.25Gbps	—	—	170 mW

Fig. 24 is the picture of the 100 G Ethernet system implementation. The each chip has eight lanes and there are eight chips in the each card. The total 64 channels are communicating with one another 64 channels with error-free operation. This backplane insertion loss and cross talk are shown in Fig. 25. The insertion loss is 29.43 dB and the insertion loss to crosstalk ratio is 13.53 dB at 12.89 GHz.

Net	Backplane Length	Fabre Length	Line Length	Total
Longest Net	16"	10"	5.5"	31.5"
Shortest Net	16"	5.56"	1.76"	23.41"



Fig. 24. 100 G Ethernet system implementation.

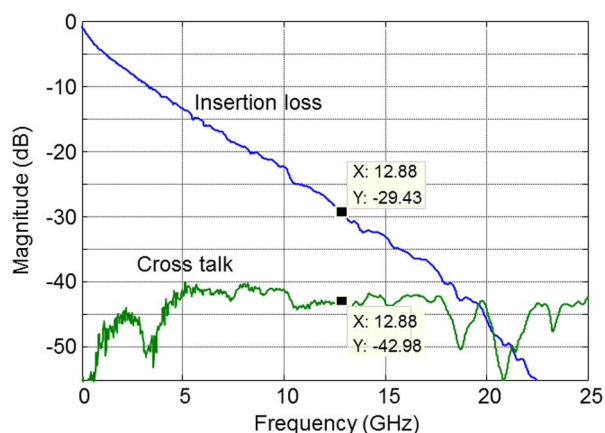


Fig. 25. Insertion loss and cross talk of victim channel. IL = 29.43 dB, ICR = 13.53 dB at 12.89 GHz.

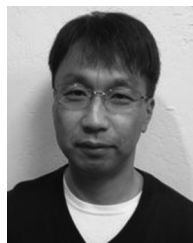
VII. CONCLUSION

We developed a 28 Gbps SerDes macro which has four lanes and two PLLs and fabricated it in TSMC 28 nm CMOS process. The TIA-based AFE achieves 15-dB high-frequency boost with single pair of on-chip inductor. The half-rate unrolled DFE with two rotatable error latches achieves DFE timing closure, less hardware, and robust adaptation. The group-delay algorithm for AEQ adaptation eliminates potential coupling between AEQ and DFE adaptation. The active inductor clock buffer circuit with CMFB extends bandwidth without major power penalty. The transceiver achieves error-free operation at 28 Gbps with 34 dB channel loss with the worst case power of 560 mW/lane and it fully complies with multiple standards and applications.

REFERENCES

[1] J. Bulzacchelli *et al.*, "A 28-Gb/s 4-Tap FFE/15-Tap DFE serial link transceiver in 32-nm SOI CMOS technology," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 324–325.

- [2] S. Parikh *et al.*, "A 32 Gb/s wireline receiver with a low-frequency equalizer, CTLE and 2-Tap DFE in 28 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 28–29.
- [3] Y. Doi *et al.*, "A 32 Gb/s data-interpolator receiver with two-tap DFE fabricated with 28-nm CMOS process," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3258–3267, Dec. 2013.
- [4] M. Harwood *et al.*, "A 225 mW 28 Gb/s SerDes in 40 nm CMOS with 13 dB of analog equalization for 100GBASE-LR4 and optical transport lane 4.4 applications," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 326–327.
- [5] F. Zhong *et al.*, "A 1.0625 ~ 14.025 Gb/s multi-media transceiver with full-rate source-series-terminated transmit driver and floating-tap decision-feedback equalizer in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3126–3139, Dec. 2011.
- [6] M. Kossel *et al.*, "A T-coil-enhanced 8.5 Gb/s high-swing SST transmitter in 65 nm bulk CMOS with <16 dB return loss over 10 GHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2905–2920, Dec. 2008.
- [7] R. G. Meyer and R. A. Blauschild, "A wide-band low-noise monolithic transimpedance amplifier," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 4, pp. 530–533, Aug. 1986.
- [8] W. Lin *et al.*, "3–10-GHz ultra-wideband low-noise amplifier utilizing miller effect and inductive shunt-shunt feedback technique," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 9, pp. 1832–1843, Sep. 2007.
- [9] O. Ghasemi *et al.*, "A low power transimpedance amplifier using inductive feedback approach in 90 nm CMOS," in *IEEE ISCAS Dig. Tech. Papers*, 2009, pp. 1937–1940.
- [10] B. Razavi, *Design of Integrated Circuits for Optical Communications*. New York, NY, USA: McGraw-Hill, 2003, pp. 87–88.
- [11] P. Aziz and A. Malipatil, "Adaptation algorithms for a class of continuous time analog equalizers with application to serial links," in *IEEE ISCAS Dig. Tech. Papers*, 2011, pp. 1383–1386.
- [12] V. Stojanovic *et al.*, "Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 1012–1026, Apr. 2005.
- [13] S. Kasturia and J. H. Winters, "Techniques for high-speed implementation of nonlinear cancellation," *IEEE J. Sel. Areas Commun.*, vol. 9, no. 5, pp. 711–717, Jun. 1991.
- [14] A. Garg, A. C. Carusone, and S. P. Voignescu, "A 1-tap 40-Gbps lookahead decision feedback equalizer in 0.18 m SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2224–2232, Oct. 2006.
- [15] S. Ibrahim and B. Razavi, "Low-power CMOS equalizer design for 20-Gb/s systems," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1321–1336, Jun. 2011.
- [16] G. R. Gangasani *et al.*, "A 16-Gb/s backplane transceiver with 12-tap current integrating DFE and dynamic adaptation of voltage offset and timing drifts in 45-nm SOI CMOS technology," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1828–1841, Aug. 2012.
- [17] E. Sackinger and W. C. Fischer, "A 3 GHz, 32 dB CMOS limiting amplifier for SONET OC-48 receivers," in *IEEE ISSCC Dig. Tech. Papers*, 2000, pp. 158–159.
- [18] C. Wu *et al.*, "A 1 V 4.2 mW fully integrated 2.5 Gb/s CMOS limiting amplifier using folded active inductors," in *IEEE ISCAS Dig. Tech. Papers*, 2004, pp. I-1044–I-1047.
- [19] Y. M. Lee *et al.*, "A 10 Gb/s active-inductor structure with peaking control in 90 nm CMOS," in *IEEE ASSCC Dig. Tech. Papers*, 2008, pp. 229–232.
- [20] P. Payandehnia *et al.*, "A 12.5 Gb/s active-inductor based transmitter for I/O applications," in *IEEE ECCTD Dig. Tech. Papers*, 2011, pp. 186–189.
- [21] P. Aziz and A. Malipatil, "Analysis of a class of decimated clock/data recovery architectures for serial links," in *IEEE ISCAS Dig. Tech. Papers*, 2013, pp. 1175–1178.



Hiroshi Kimura (M'94) received the B.S. degree in electrical engineering from Chiba University, Chiba, Japan, in 1990.

He joined the System Development Laboratory, Hitachi Ltd., Yokohama, Japan, in 1990, where he worked on the research and development of read-channel analog circuits for hard disk drives. From 1999 to 2004, he was with DataPath Systems, Santa Clara, CA, USA, where he worked on read-channel, DSL, and high-speed interface analog circuits design. From 2004 to 2009, he was

with Link-A-Media Devices Corporation, Santa Clara, where he worked on read-channel analog circuits design. Since 2009, he has been with LSI Corporation (an Avago Technologies company), San Jose, CA, USA, where he is currently a Distinguished Engineer/Senior Manager and leads the development of high-speed SerDes analog circuits design.



Pervez M. Aziz (S'87–M'96–SM'11) received the B.S., M.S., and Ph.D. degrees from the University of Pennsylvania, Philadelphia, PA, USA, in 1990, 1991, and 1996, respectively.

After working on delta-sigma A/D converter architectures for his doctoral thesis, he joined AT&T Microelectronics Group/Bell Laboratories in 1995 to work on architecture development for magnetic recording read channels. This group subsequently became part of Lucent Technologies, then Agere Systems, and LSI Corporation in 2007. LSI Corporation was acquired by Avago Technologies in May 2014. From 1995 to 2003, while contributing to several generations of commercially designed read channels, he worked on various aspects of architecture development and analysis including equalization, timing recovery, servo signal processing, construction, and implementation of modulation and distance enhancing codes, as well as Viterbi and postprocessor-based detection. In 2003, he joined the SerDes architecture group where he has been working on adaptive equalization and clock/data recovery architecture/algorithm development and analysis for commercially designed high-speed multi-gigabit SerDes channels. His interests also include bit cycle accurate modeling and functional verification of digital signal processing circuits and modeling of analog circuits. He has authored or coauthored six book chapters, 11 journal papers, 24 conference papers, and numerous internal technical documents and architecture specifications. He is currently a Distinguished Engineer at Avago Technologies.

Dr. Aziz is a member of Eta Kappa Nu and Tau Beta Pi. He was a recipient of the Electronics Letters Premium Award. He holds about 40 U.S. patents.



Tai Jing (M'96) received the B.S.E.E. degree from the California Institute of Technology, Pasadena, CA, USA, in 1994, and the M.S.E.E. degree from Stanford University, Stanford, CA, USA, in 1996.

Since 2008, he has been with LSI Corporation (recently acquired by Avago) working on high-speed SerDes products. His main interests are low power, high scalability, and digital signal processing. He is currently a Senior Design Manager in the area of SerDes digital design.



Ashutosh Sinha received the B.Tech. degree from the Indian Institute of Technology, Delhi, India, in 1996, and the M.S. degree from Stanford University, Stanford, CA, USA, in 2007, both in electrical engineering.

Since 2008, he has been a Principal Analog Design Engineer with LSI Corporation, Milpitas, CA, USA, working on high-speed SerDes. His research interests are in the area of analog/mixed-signal integrated-circuit design, with special emphasis on high-speed data links.



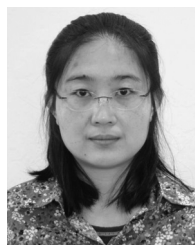
Shiva Prasad Kotagiri received the M.S. degree from the University of Missouri-Rolla, Rolla, MO, USA, in 2003, and the Ph.D. degree in electrical engineering from the University of Notre Dame, South Bend, IN, USA, in 2008.

He is a System Architect for high-speed SerDes transceiver design at LSI Corporation (acquired by Avago), San Jose, CA, USA. He was with Xilinx from 2008 to 2011 as a System Architect for high-speed SerDes transceiver design.



Ram Narayan received the B.Tech degree from the Indian Institute of Technology, Bombay, India, in 2000, and the M.S. degree from University of Virginia, Charlottesville, VA, USA, in 2003, both in electrical engineering.

From 2003 to 2008, he was a Staff Engineer with Agere Systems (merged with LSI Corporation in 2007) in Mendota Heights, MN, USA. During this period, he worked on preamplifier design for disk drive applications. Since 2008, he has been with the SerDes design group at LSI Corporation (acquired by Avago Technologies), San Jose, CA, USA, where he has been designing transmitters and analog front-ends for receivers.



Hairong Gao received the B.S.E.E. degree from the University of Science and Technology of China, Hefei, China, in 1995, and the M.S.E.E. degree from Oregon State University, Corvallis, OR, USA, in 1997.

From 1997 to 1999, she was with Datapath Systems Inc., working on analog and mixed-signal designs for hard disk drive (HDD) read-channel ICs. From 1999 to 2007, she was with the Consumer Product Group Division, LSI Corporation (acquired by Avago), Milpitas, CA, USA. During this period, she worked on analog front-end designs for various consumer ICs, including HDD read channel, terrestrial and cable tuner and DVD R/W drive. Since 2007, she has been with the Custom Silicon Division of LSI Corporation, Milpitas. Her current focus is on analog and mixed-signal designs for high-speed SerDes.



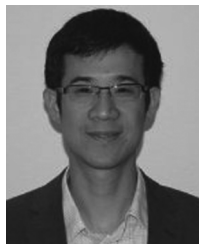
Ping Jing received the B.S. degree from Nankai University, Tianjin, China, in 1986, and the M.S. degree in electrical and computer engineering from the University of Florida, Gainesville, FL, USA, in 1999.

In 1999, she joined Cirrus Logic, Inc., Broomfield, CO, USA, as an Analog Circuit Design Engineer, where she was involved with circuits design for hard disk drive read-channel devices. In 2004, she joined LSI Corporation, Milpitas, CA, USA, where she designed analog circuits for DVD controllers. In 2008, she joined Telegent Technology, Inc., Sunnyvale, CA, USA, where she designed circuits in analog TV tuner for mobile devices. She has been with LSI Corporation (acquired by Avago), San Jose, CA, USA, since 2011, working on high-speed SerDes. She holds one U.S. patent.



Gary Hom received the B.S. and M.S. degrees in electrical engineering from San Jose State University, San Jose, CA, USA, in 1987 and 1993, respectively.

He has worked in high-speed I/O circuit library development since 1993 in both LSI Logic and VLSI Technology. In 2006, he joined the Serdes Analog Design Group at LSI Logic, where he has been involved with high-speed analog front-end circuit designs, and in the development of PLL. His current research interests are in variable-gain amplifiers, linear equalizer, decision feedback equalization, clock-and-data recovery, and PLL circuits for high-speed I/O interface.



Anshi Liang received the B.Eng. degree (*summa cum laude*) from Stony Brook University, Stony Brook, NY, USA, in 2001, and the M.S. degree from the University of California, Berkeley, CA, USA, in 2004.

In 2011, he joined LSI Corporation, where he worked on CMOS integrated circuit design for high-speed serial IOs. He is currently with Apple Inc., Cupertino, CA, USA.



Eric Zhang received the M.S. and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, MD, USA, in 1992 and 1996, respectively.

From 1996 to 2000, he was a Senior Analog Design Engineer with Integrated Device Technology, where his major responsibilities included transistor-level design of analog circuitry, such as PLLs, high-speed transmitters and receivers for twist-pairs, and coaxial and fiber optic cables. He joined LSI Corporation (acquired by Avago) in 2000, where he

worked in analog and mixed-signal design of high-speed SerDes for networking and communication applications. He is currently working on the design and development of SerDes for storage network products. His primary areas of interest include system architecture, high-speed and low-power analog circuit design for transceivers, mixed-signal system verifications, and applications.



Aniket Kadkol received the B.E. degree from Sardar Patel College of Engineering, Mumbai, India, in 2001, and the M.S. degree from the University of Southern California, Los Angeles, CA, USA, in 2004, both in electrical engineering.

From 2005 to 2011, he was an Analog design Engineer with Altera Corporation, San Jose, CA, USA. During this period he worked on amplifiers, comparators and clock distribution circuits for FPGAs. Since 2011, he has been with the SerDes design group with LSI Corporation (acquired by Avago), San Jose, CA,

USA. He has been an analog/mixed signal designer working on Gb/s serdes for high-speed communication. His technical interests include SerDes, low-power design, low-phase-noise VCOs, and wideband amplifiers.

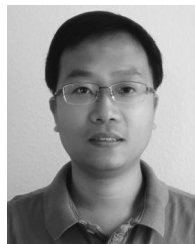


Ruchi Kothari received the B.E. degree in electronics engineering from Ramdeo Baba Kamla Nehru Engineering College, India, in 2000, the M.E. degree in electrical engineering from the University of Virginia, Charlottesville, VA, USA, in 2003, and the M.S. degree in electrical engineering from Case Western Reserve University, Cleveland, OH, USA, in 2006.

In 2007, she joined LSI Corporation (acquired by Avago), Milpitas, CA, USA, where she has been working on Transmitter design for Gb/s Serdes. Her current technical interests include Serdes, high-speed design, and PLLs.

Gordon Chan received the Ph.D. degree in engineering science from the University of Oxford, Oxford, U.K., in 1995.

He joined LSI Corporation (acquired by Avago), San Jose, CA, USA, in 2011, where he is a Mixed-Signal Circuit Designer. He is currently working on the design and integration of high-speed serial links. He has authored or coauthored three papers in conferences and journals related to circuit design.



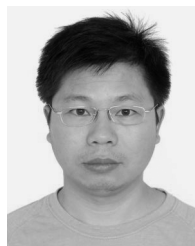
Yehui Sun received the B.S., M.S., and Ph.D. degrees in electrical engineering from Nankai University, Tianjin, China, in 2002, 2005, and 2008, respectively.

From 2005 to 2010, he was a Senior Analog Design Engineer with Integrated Device Technology, Shanghai, China, where he worked on SerDes and clock-data-recovery (CDR) circuit design. From 2010 to 2013, he was with LSI Corporation, Shanghai, China, as a Staff Analog/Mixed-Signal Design Engineer, where he worked on high-speed slicer and decision feedback equalization. Since 2013, he has been with Avago Technology, San Jose, CA, working on multi-GHz SerDes for optical and high-speed communications. His current research interests include design of high-speed multi-level SerDes, decision feedback equalization, and CDR.



Benjamin Ge received B.S. degree and M.S. degree in electronic engineering from Shanghai Jiaotong University, Shanghai, China, in 2003 and 2006, respectively.

From 2006 to 2007, he was with STMicroelectronics, working on the design of automotive ICs. In 2007, he joined Agere Systems in 2007, later acquired by LSI Corporation, San Jose, CA, USA, where he has worked on the design of Ethernet PHYs and high-speed SerDes.



Jason Zeng received the B.S. and M.S. degrees in electronics science and technology from Xi'an Jiaotong University, ShaanXi, China.

He joined HyperPHY team of LSI Corporation (acquired by Avago), San Jose, CA, USA, in 2010 and has worked as a Digital IC Design Engineer for high-speed SerDes products since then.



Kathy Ling received the B.S. degree from Soochow University, Taiwan, the M.S. degree in physics from the University of Oregon, Corvallis, OR, USA, and the M.S. degree in electrical engineering from San Jose State University, San Jose, CA, USA, in 1992.

From 1993 to 1995, she worked with Noller Communication on telecommunications ASIC designs. Then, from 1995 to 1998 she worked with Opti and S3 on MPEG2 decoders. Since 1998, she has been a Staff Design Engineer with Avago/LSI Technologies, San Jose, CA, USA, where she develops and designs high-speed digital SerDes.



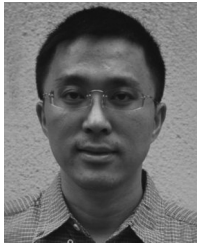
Michael C. Wang was born in 1986. He received the B.S. degree in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 2008, and the M.E. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2009.

Since then, he has been with LSI Corporation (acquired by Avago), where he is currently a Senior IC Design Engineer.



Amaresh Malipatil received the B.Eng. degree in electronics and communications engineering from the National Institute of Technology, Karnataka, India, and the Ph.D. degree in electrical engineering from the University of Notre Dame, South Bend, IN, USA.

He has been a SerDes System Architect with Avago Technology, San Jose, CA, USA, since 2005, where he is involved with developing system architectures for high-speed SerDes. His research interests include signal processing and communications over high-speed links and wireless channels, linear and nonlinear signal processing with applications in communications, and distributed signal processing over sensor networks.



Lijun Li received the B.S. degree in electronics engineering from Tsinghua University, Beijing, China, in 1998, the M.S. degree in electrical engineering from Northeastern University, Boston, MA, USA, in 2002, and the Ph.D. degree in electrical engineering from the University of California, Irvine, CA, USA, in 2006.

From 2000 to 2002, he was a Hardware Design Engineer with Lucent Technologies, Westford, MA, USA, working on multi-service ATM WAN switch service cards. In 2006, he was a Member of Technical Staff with Ambarella Inc., working on high-speed interface circuits. Since 2006, he has been an Analog/Mixed-Signal Designer working on Gb/s SerDes for optical and high-speed communications. His current research interests include the design of high-speed serdes, clock data recovery, and phase-locked loop circuits.



Christopher Abel received the B.S. degree and Ph.D. degree in electrical engineering from The Ohio State University, Columbus, OH, USA, in 1989 and 1995, respectively.

From 1995 to 1997, he was with Rosemount Inc., where he designed sigma-delta A/D converters for industrial process control products. He joined the Microelectronics Division of Lucent Technologies in 1997, where he focused on the design of continuous-time filters and A/D converters for DSL products, and remained with the Division when it spun off to form Agere Systems. He joined the SerDes design team at Agere in 2001 and has been actively involved in SerDes design and management since that time. He is currently the Director of SerDes Analog Design in the Data Controller Division at Avago Technologies, San Jose, CA, USA.



Freeman Zhong (M'00) received the B.S. degree from Guangzhou University, Guangzhou, China, the M.S. degree in physics from Jinan University, Jinan, China, and the M.S. degree in electrical engineering from San Jose State University, San Jose, CA, USA, in 1995.

From 1995 to 1998, he was with National Semiconductor Corporation, Santa Clara, CA, USA, as a Senior Design Engineer working on analog and mixed-signal IC designs. From 1998 to 2000, he worked with NEC Corporation, Santa Clara, as a Staff Design Engineer working on mixed-signal IC design for storage SOC products. Since 2000, he has been a Senior Design Manager/Design Director with LSI Corporation (acquired by Avago), San Jose, CA, USA, where he leads the developments of Ethernet PHY and high-speed SerDes. His current research interests include high-speed SerDes and DSP-based transceiver.