A Compact and Low-Power Fractionally Injection-Locked Quadrature Frequency Synthesizer Using a Self-Synchronized Gating Injection Technique for Software-Defined Radios

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***Abstract*—This paper describes a compact and low-power frequency synthesizer with quadrature phase output for software-defined radios (SDRs). The proposed synthesizer is constructed using a core phase-locked loop (PLL), which is coupled with a fractional-*N* injection-locked frequency divider (ILFD). The fractional-*N* injection-locking operation is achieved by the proposed self-synchronized gating injection technique. The principle of a fractional-*N* injection locking operation and the concept of the proposed circuits are described in detail. Analysis for predicting the locking range of the proposed fractional-*N* ILFD is investigated. A digital calibration scheme is adopted in order to compensate for process, voltage, and temperature (PVT) variations. Implemented in a 65 nm CMOS process, this work demonstrates continuous frequency coverage from 10 MHz to 6.6 GHz with quadrature phase output while occupying a small area of 0.38 mm^2 and consuming 16 to 26 mW, depending on the output frequency. The normalized phase noise achieves -135.3 dBc/Hz at an offset of 3 MHz and -95.1 dBc/Hz at an offset of 10 kHz, both from a carrier frequency of 1.7 GHz.**

***Index Terms*—Synthesizer, PLL, SDR, CMOS, injection-locking, fractional-*N*, quadrature multi-band.**

I. Introduction

RECENT years have witnessed enormous progress in the development, implementation, and commercialization of multiple wireless communication systems in a low-cost CMOS technology. At present, commercial multi-band mobile devices usually adopt multiple transceivers, each of which is dedicated to an individual wireless communication standard. Building separate RF front-ends for individual operation modes in parallel is straightforward and also provides the optimal performance for each mode. However, this approach significantly increases power consumption, the implementation cost, and the overall system complexity. A more desirable solution is to adopt a flexible multi-standard, multi-mode, multi-function radio system with high configurability and programmability, which is usually defined as software-defined radios (SDRs) [1]–[8].

One of the challenging building blocks of such a SDR RF front-end is the multi-radio frequency synthesizer, which must provide all necessary carrier signals in a pre-allocated frequency range with a proper channel spacing that corresponds to the channel bandwidth or to the frequency raster of a given wireless communication standard. Several approaches have been proposed in the literature for multi-band and multi-mode frequency synthesizers [9]–[17]. Among these publications, there are mainly two frequency synthesizer architectures available when it comes to a multi-band carrier synthesis. Each architecture has its advantages in terms of phase noise, implementation cost, spur level, and power consumption.

Fig. 1 illustrates two approaches to the design of a SDR frequency synthesizer with quadrature outputs. In the first topology (Fig. 1(a)), multi-band carrier generation is accomplished using quadrature voltage-controlled oscillators (QVCOs). Single-side band (SSB) mixing and dividing the QVCO frequency division are then performed [9]–[12]. Quadrature voltage-controlled oscillators are constructed by cross-coupling two differential voltage-controlled oscillators (VCOs), thereby doubling the required chip area. The power consumption of the QVCO is also significantly increased compared to a single differential VCO. In the second topology, multi-band carrier generation is achieved using a set of differential VCOs, followed by VCO frequency division [13], [15]–[17]. This approach benefits from the absence of SSB mixing, thus avoiding undesired sidebands. In addition, frequency division also has the advantage of providing I/Q signals. However, this architecture requires multiple LC resonators, which significantly increase the chip area and power consumption.

In this paper, a compact and low-power frequency synthesizer using a fractional-*N* injection-locking technique is investigated [18], [19]. Fig. 2 shows a conceptual diagram of the proposed SDR frequency synthesizer. Unlike the present SDR

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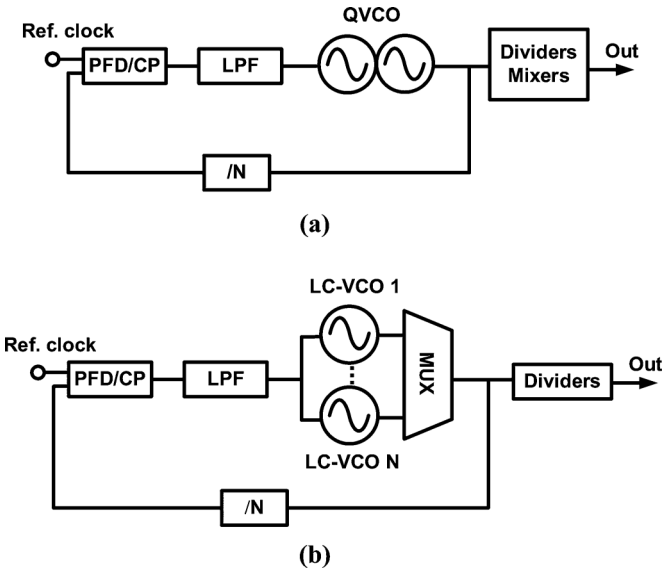

Fig. 1. Conceptual diagram of conventional SDR frequency synthesizers (a) using QVCO, SSB mixers and dividers, and (b) using multiple LC resonators and dividers.

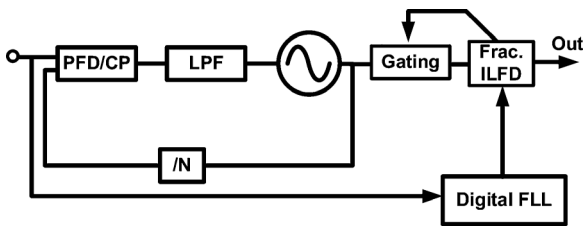

Fig. 2. Conceptual diagram of the proposed SDR frequency synthesizer using the fractional-N injection-locking technique.

frequency synthesizers, which contain two, or sometimes four, LC resonators [15], only one LC VCO is used in the core-PLL, which considerably reduces the occupied chip area. Moreover, a quadrature fractional-N ILFD is proposed for quadrature output generation that avoids the use of poly-phase filters, which are narrow band with poor phase accuracy, and QVCOs, which degrade the phase noise characteristics. A digital calibration scheme using a frequency-locked loop is used to guarantee the proper operation of the fractional-N injection-locked operation over PVT variations. A compact and low-power quadrature frequency synthesizer with continuous frequency coverage from 10 MHz to 6.6 GHz is demonstrated as a proof-of-concept prototype.

The remainder of this paper is organized as follows. Section II describes the frequency planning and the overall synthesizer architecture. Section III presents the detailed synthesizer architecture and important building blocks. Section IV demonstrates experimental results for the proposed SDR frequency synthesizer. Finally, the conclusions are presented in Section V.

II. Frequency Planning and Synthesizer Architecture

A. Frequency Planning

The basic method in this work adopts a low-phase noise VCO oscillating at a frequency that is higher than the required carrier frequency. The targeted output frequencies are generated by dividing the VCO frequency. Fig. 3 shows the proposed synthesizer architecture, which uses a fractional-N ILFD to extend the frequency tuning range. As shown in Table I, the fractional-N division ratios in addition to the integer-N division ratios are very helpful because they help to reduce the required frequency range of the core-PLL to $\pm 14.3\%$, which can be accomplished by only one LC VCO and leads to a significant reduction in area. On the other hand, the upper frequency limitation of the core-PLL is also relaxed from 12 GHz (6 GHz $\times$ 2 in the case of integer-N) to 8 GHz (6 GHz $\times$ 4/3 in the case of fractional-N) for a target frequency coverage of up to 6 GHz. Such a core-PLL operating at a relatively low frequency helps to reduce the overall power consumption.

Fig. 4 illustrates the frequency planning of the proposed synthesizer architecture, and frequency division by 1.33 (4/3), 1.5 (3/2), 1.67(5/3), 2, 2.5 (5/2), 3, 4, and 5 are generated by the quadrature ILFD. Note that the upper boundary of the synthesizer quadrature output range is subjected to the highest free-running frequency of the fractional-N ILFD.

B. Synthesizer Architecture

Fig. 5 shows the detailed architecture of the frequency synthesizer. The core PLL has a frequency coverage from 7.2 to 10.3 GHz and uses only one LC resonator oscillating at high frequencies, where small inductors are used, leading to a significant reduction in the chip area. For frequencies between 1.6 GHz and 6.6 GHz, a fractional-N ILFD is used to divide the frequency of the core PLL output signal. Then, lower frequencies are generated by a programmable digital divider chain with a modulus of $2N$ $(N = 0, 1, \ldots 7)$. Using a 16-bit delta-sigma modulator in the core PLL, a frequency resolution lower than 10 kHz can be achieved over the entire frequency range.

In the proposed frequency synthesizer, the core PLL with a minimum tuning range of 14.3% is sufficient because the following fractional-N ILFD relaxes the requirement for the tuning range. In order to compensate for the limited locking range due to the fractional-N operation, a digital calibration scheme is adopted that guarantees the functionality of fractional-N ILFD over the entire PLL frequency range.

The proposed SDR synthesizer using the fractional-N injection-locking technique has the following four advantages. 1) Only $\pm 14.3\%$ of the frequency tuning range is required for the core-PLL. Such a frequency tuning range can be achieved by using only one LC resonator, which helps to considerably reduce the chip area and power consumption. 2) Quadrature phase outputs without the adoption of narrowband poly-phase filters or phase-noise-degrading QVCOs. 3) There is no large spurious content because SSB mixing is avoided [14]. (4) Higher frequency oscillation for core-PLL also contributes to the reduction in the overall chip area.

III. Circuit Implementation

A. Fractional-N ILFD Using Self-Synchronized Gating

Generally speaking, a direct injection ILFD has a wide locking range for divide-by-2 operation and a limited locking range for higher division ratios, such as divide-by-3, -4, and

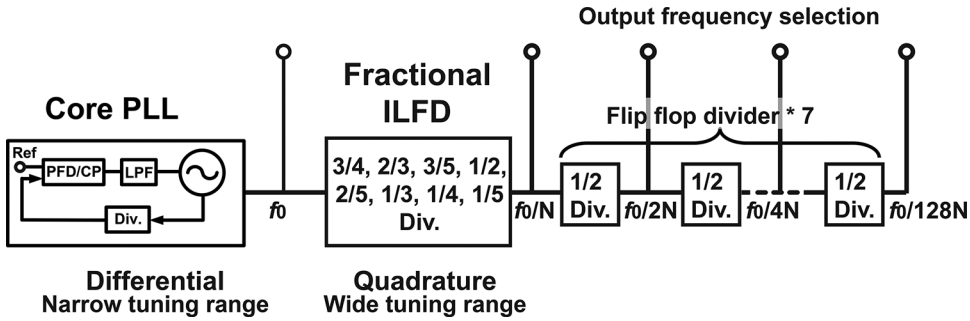

Fig. 3. Simplified diagram of the core-PLL with frequency extension circuits using the fractional-N injection-locking technique.

TABLE I
COMPARISON OF SDR SYNTHESIZER WITH INTEGER-N AND FRACTIONAL-N DIVISION RATIOS IN THE DIVIDER CASCADE

	[12][15][16]	[13]	This work
Architecture	Integer-*N* Division Ratio		Fractional-*N* Division Ratio
Division ratio	2, 4, 8, 16, 32, …	2, 3, 4, 5, 6, 8, …	4/3, 3/2, 5/3, 2, 3, 4, 5, …
Minimum required frequency range of core LC-VCOs	±33.3%	±20%	±14.3%
Normalized frequency range of core LC-VCOs[1]	6-to-12 GHz	8-to-12 GHz	6-to-8 GHz
Numbers of LC resonator	2, 4	2	1

[1]The minimum required frequency tuning range of core LC-VCOs in order to achieve 0.01 - 6 GHz continuous frequency range.

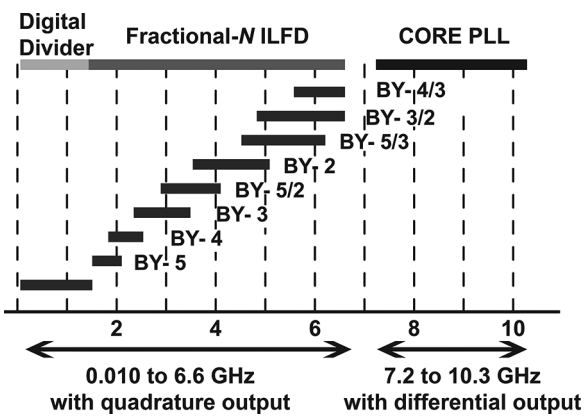

Fig. 4. Frequency planning of the proposed SDR frequency synthesizer.

-5 operation. Fig. 6 shows the ILFD time domain waveform $f_{\rm o}$ and injection signals at $2f_{\rm o}$ and $3f_{\rm o}$ from the core PLL. The vertical dotted line indicates the ideal injection moment, which is at the zero crossing of the ILFD output waveform. The injection signal at $2f_{\rm o}$ can ideally inject at the correct timing. However, in the case of the injection signal at $3f_{\rm o}$, only one injection signal is in phase and injects at the correct timing, whereas the other two injections are out-of-phase and disrupt the injection locking state, thereby degrading the injection efficiency. The locking range of divide-by-3 operation is improved if these two undesired injection signals are eliminated. Similarly, other division ratios, including fractional-N, can be realized by rejecting these out-of-phase injections.

Fig. 7 shows the circuit implementation of the proposed fractional-N ILFD with a self-synchronized gating to eliminate unwanted injections. The direct-injection topology is adopted for the ILFD. Quadrature outputs are generated by a dual-coupled differential ring oscillator with a 3-bit current digital-to-analog converter (DAC). Injection signals from the core PLL are input to the I-channel through a gating block. The 90-degree shifted gating function is realized by connecting the Q+ signal of the ILFD and a PMOS switch in series. As an example, Fig. 8 illustrates the cases of divide-by-3 and $-3/2$ operation. The conduction angle, Φ, determines the injection power from the core PLL, which must be optimized, because too large of a power can lead to an unstable locking state and too small of a power causes a narrow locking range or even failure to lock. The conduction angle Φ can be adjusted by the control voltage $V_{\rm ctrl}$, which is brought off-chip in this design as a feasibility study of the fractional-N injection locking. In order to make this technique more attractive for use in practical applications, calibration on $V_{\rm ctrl}$ is necessary in order to mitigate the effect of PVT variations.

The proposed gating injection technique can also be explained in the phase domain. Recall that in an injection-locked frequency divider, the total current is the sum of the original current $I_{\rm osc}$ and injection current $I_{\rm inj}$, which causes the phase shift of the total current $I_{\rm T}$. In a locked state, this phase shift φ compensates the difference from the original oscillation frequency [20]. Fig. 9 shows the current phasor diagram of an ILFD with and without gating for the divide-by-3 operation. In the case of conventional direct-injection ILFDs, there are three non-overlapped injection opportunities during every

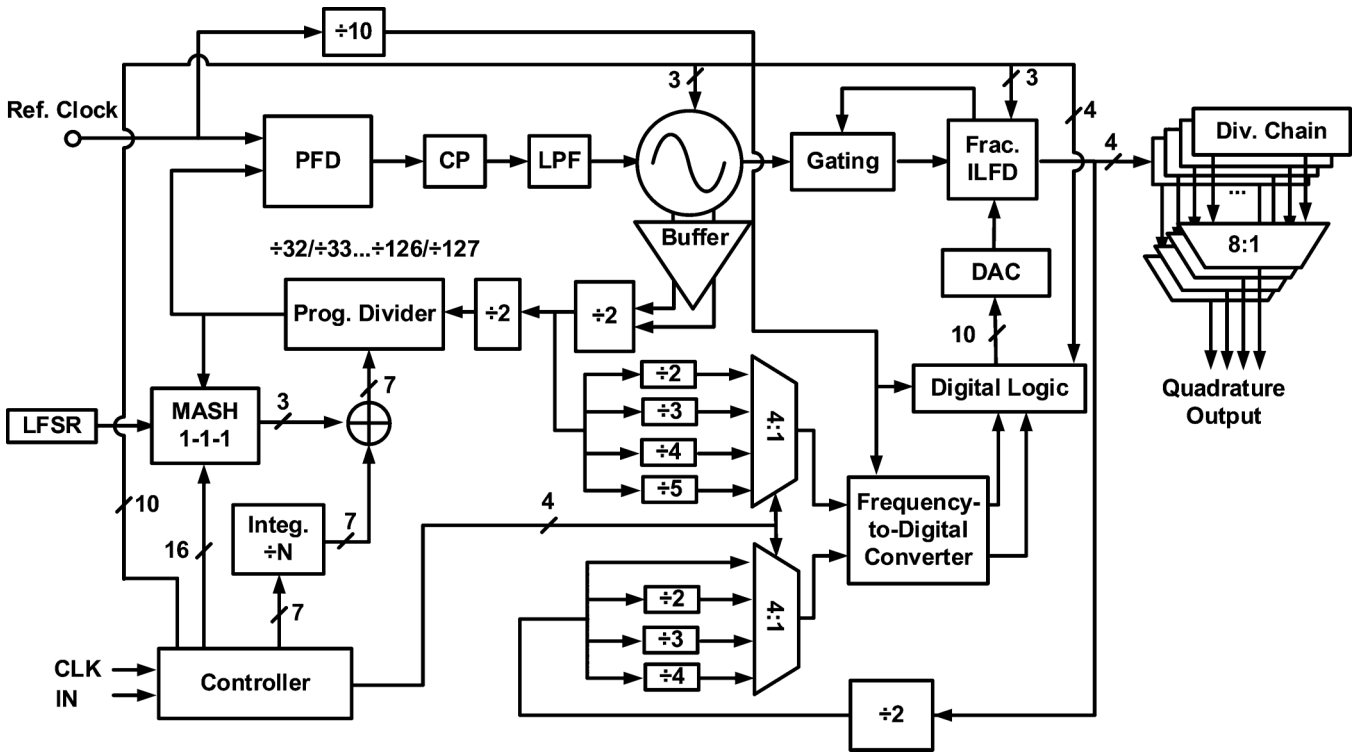

Fig. 5. Detailed block diagram of the proposed SDR frequency synthesizer.

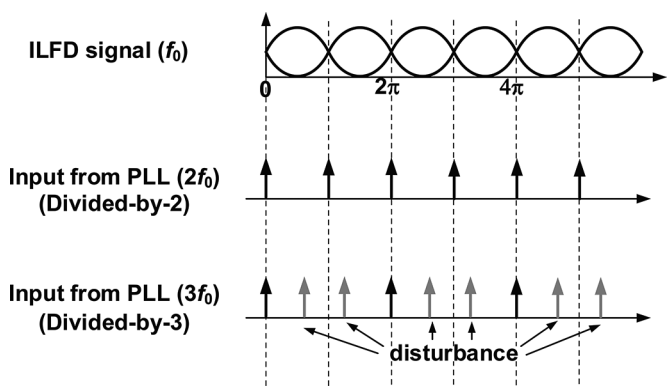

Fig. 6. Time domain waveforms demonstrating injection efficiency degrades at higher division ratios due to multiple out-of-phase injections.

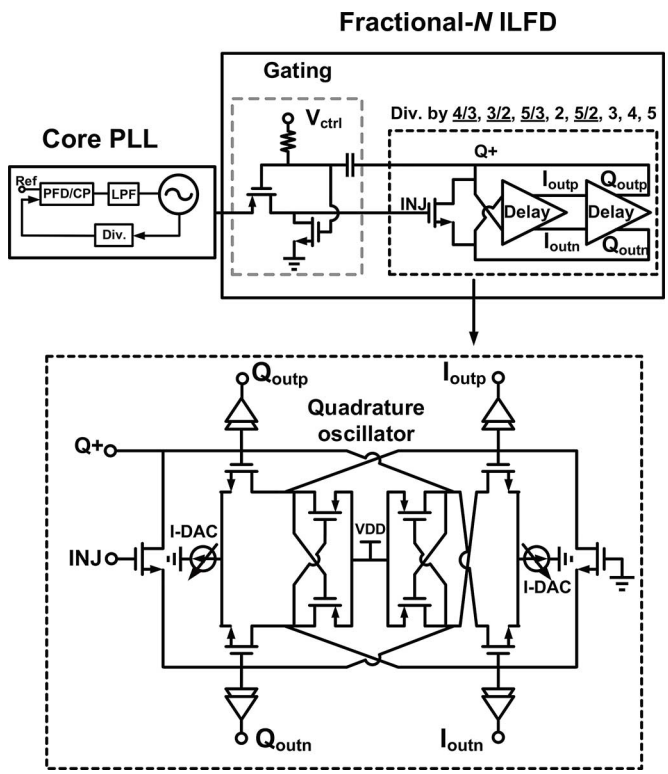

Fig. 7. Detailed schematic of the proposed fractional-N injection-locked frequency divider using the gating injection technique.

period. Unfortunately, these injection currents would disturb each other. Thus, the conventional ILFD does not have the divide-by-3 mode if it is in an ideal small-signal region. On the other hand, out-of-phase injection currents can be eliminated by the self-synchronized gating function in the proposed ILFD, which contributes to maximizing the locking range for the non-divide-by-2 operation. The self-synchronized gating circuit in this implementation periodically modulates the injection signal from the core PLL, producing the effective gated injection signal together with undesired intermodulation (IM) products, which generates harmonics at the fractional-N ILFD output. These IM products can become weaker with a smaller conduction angle Φ (by choosing a high V_{ctrl}); however, this is at the expense of narrower injection locking range. Future work can be placed on the re-design of the self-synchronized gating circuit with harmonic rejection function.

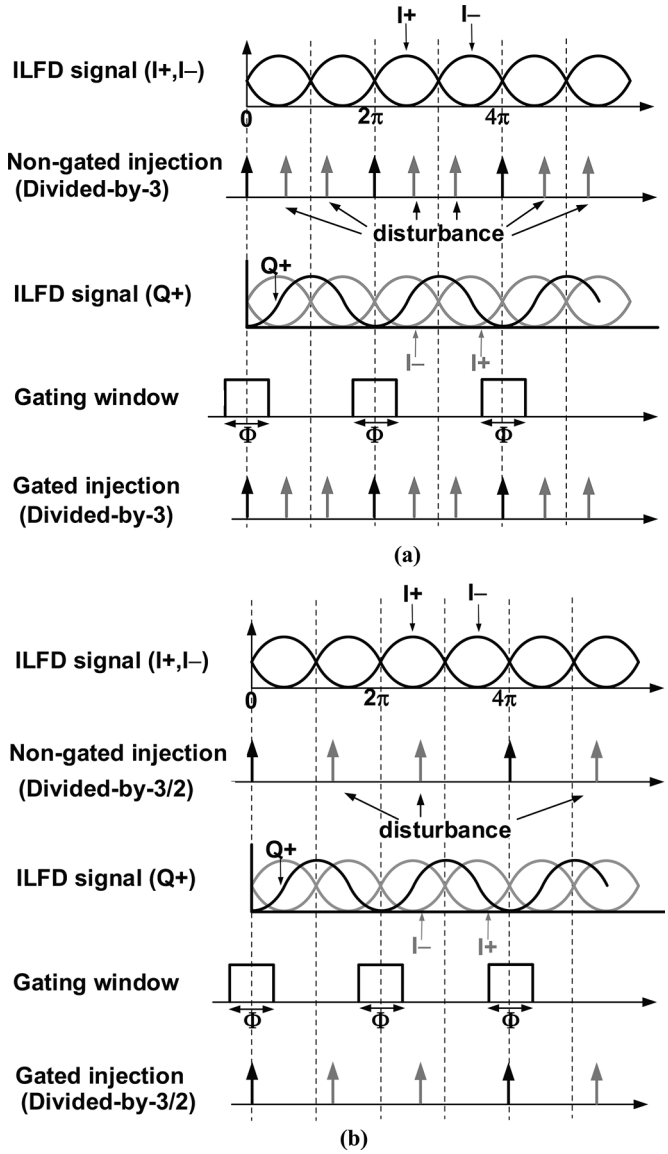

Fig. 8. ILFD time domain waveforms for (a) divide-by-3 and (b) divide-by-1.5.

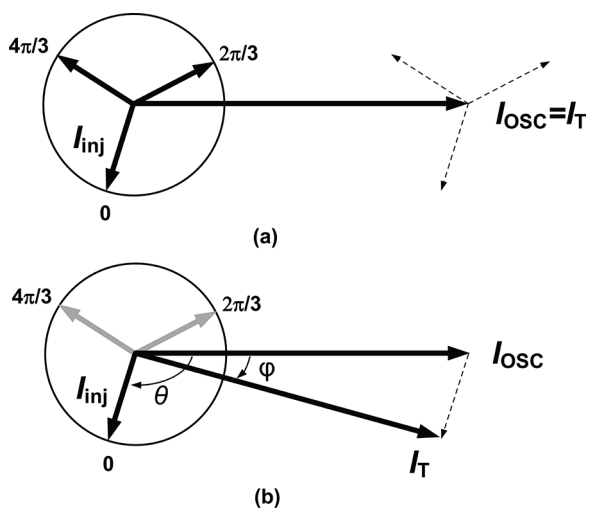

Fig. 9. Current phasor diagram of (a) the conventional ILFD and (b) the proposed ILFD using self-synchronized gating technique for divide-by-3 operation.

The locking range of the proposed ILFD is investigated as follows. By applying Euler's formula to $I_{\rm T}e^{j(\omega t-\varphi)} = I_{\rm osc}e^{j\omega t} + I_{\rm inj}e^{j(\omega_{\rm inj}t-\theta)}$, it can be shown that $I_{\rm T}\sin\varphi = I_{\rm inj}\sin(\omega t+\theta-\omega_{inj}t)$, where ω is the ILFD angular frequency and $\omega_{\rm inj}$ is the injection signal angular frequency. The injection current $I_{\rm inj}$ is not constant and depends on the ILFD output voltage difference. Here, the following equation is assumed:

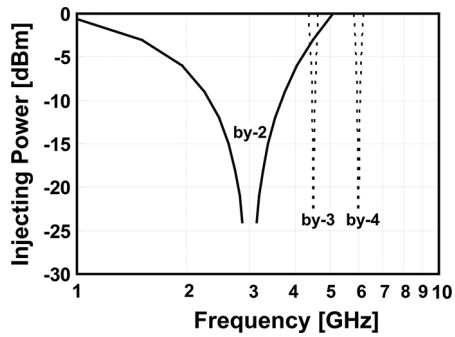

Fig. 10. Theoretically calculated locking range of the conventional ILFD at different division ratios.

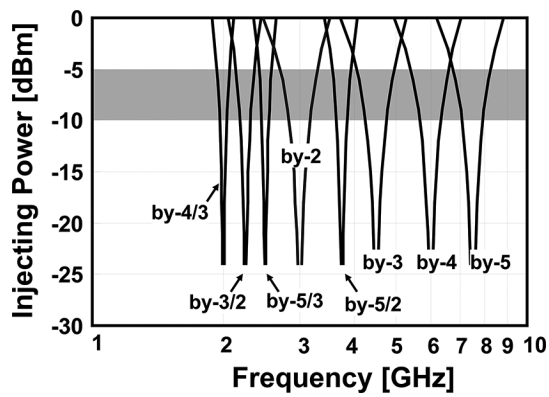

Fig. 11. Theoretically calculated locking range of the proposed ILFD at different division ratios.

$$I_{\rm inj} = I_{\rm inj0}\sin(\omega t-\theta) \tag{1}$$

where $I_{\rm inj0}$ is the injection current amplitude.

Then, we have:

$$\begin{aligned} I_{\rm T}\sin\Phi &= I_{\rm inj0}\sin(\omega t-\theta)\sin(\omega t+\theta-\omega_{\rm inj}t) \\ &= \frac{I_{\rm injo}}{2}\{\cos(\omega_{inj}t-2\theta)-\cos(2\omega t-\omega_{\rm inj}t)\}. \end{aligned} \tag{2}$$

i) Basically, the locking range is proportional to the average current $\overline{I_T\sin\varphi}$ over a given period T. In the case of the conventional ILFD, it can be shown that

$$\begin{aligned} &\overline{I_T\sin\varphi} \\ &= \frac{1}{T}\int_0^T \frac{I_{\rm injo}}{2}\{\cos(\omega_{inj}t-2\theta)-\cos(2\omega t-\omega_{\rm inj}t)\}\,dt. \end{aligned} \tag{3}$$

When $2\omega-\omega_{inj}=0$,

$$\begin{aligned} \overline{I_T\sin\varphi} &= \frac{1}{T}\int_0^T \frac{I_{\rm injo}}{2}\{\cos(\omega_{\rm inj}t-2\theta)-1\}\,dt \\ &= -\frac{I_{\rm injo}}{2}. \end{aligned} \tag{4}$$

TABLE II
THEORETICAL NORMALIZED LOCKING RANGE BETWEEN THE CONVENTIONAL AND PROPOSED ILFD AT DIFFERENT DIVISION RATIOS

Divide-by-n/N				Locking range without gating	This work	
					Locking range with gating (Output referred)	Locking range with gating (Input referred)
	n/N	n	N		$\frac{\Phi}{\pi}\frac{1}{N}$	$\frac{\Phi}{\pi}\frac{n}{N^2}$
1.3333	4/3	4	3	0	$\frac{\Phi}{\pi}\frac{1}{3}$	$\frac{\Phi}{\pi}\frac{4}{9}$
1.5	3/2	3	2	0	$\frac{\Phi}{\pi}\frac{1}{2}$	$\frac{\Phi}{\pi}\frac{3}{4}$
1.6667	5/3	5	3	0	$\frac{\Phi}{\pi}\frac{1}{3}$	$\frac{\Phi}{\pi}\frac{5}{9}$
2	2/1	2	1	1	$\frac{\Phi}{\pi}$	$\frac{\Phi}{\pi}2$
2.5	5/2	5	2	0	$\frac{\Phi}{\pi}\frac{1}{2}$	$\frac{\Phi}{\pi}\frac{5}{4}$
3	3/1	3	1	0	$\frac{\Phi}{\pi}$	$\frac{\Phi}{\pi}3$
4	4/1	4	1	0	$\frac{\Phi}{\pi}$	$\frac{\Phi}{\pi}4$
5	5/1	5	1	0	$\frac{\Phi}{\pi}$	$\frac{\Phi}{\pi}5$

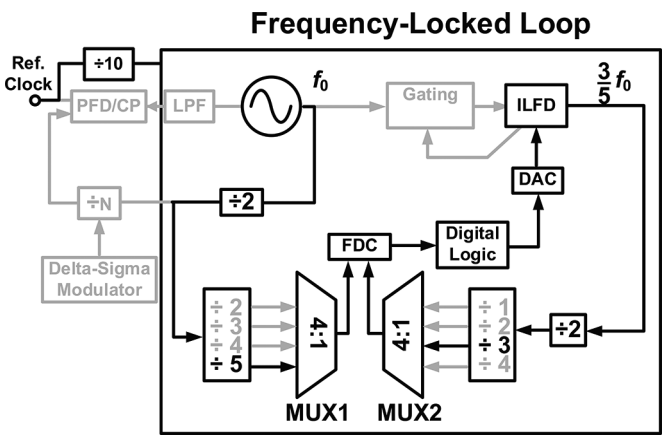

Fig. 12. Block diagram of digital calibration circuits.

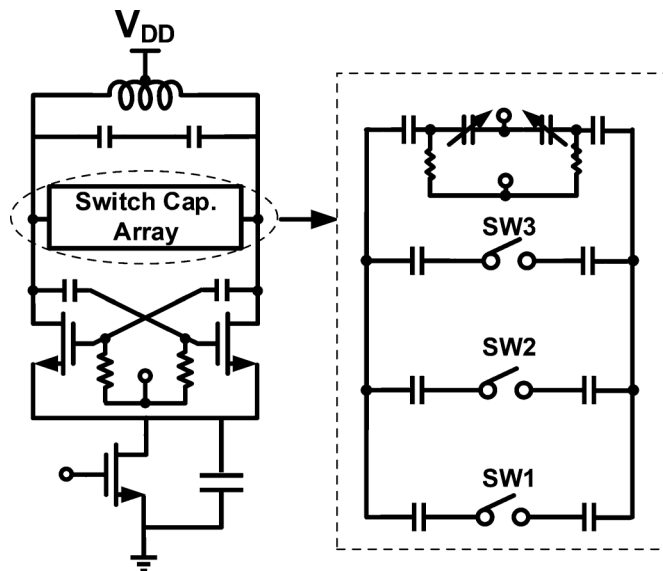

Fig. 13. Circuit implementation of the core-VCO.

When $2\omega - \omega_{\rm inj} \neq 0$,

$$\begin{aligned}\overline{I_T \sin\Phi} &= \frac{1}{T}\frac{I_{\rm injo}}{2}\left|\frac{\sin(\omega_{\rm inj}t-2\theta)}{\omega_{\rm inj}} - \frac{\sin(2\omega t-\omega_{\rm inj}t)}{2\omega t-\omega_{\rm inj}t}\right|_0^T \\ &= 0. \end{aligned} \tag{5}$$

These results reveal that linear ILFDs can be locked by an injection signal only two times higher $(2\omega - \omega_{\rm inj} = 0)$ and cannot be locked by divide-by-3, -4, -5, etc. operation, whereas actual ILFDs are usually locked practically due to the non-linear operation of the ILFD.

ii) On the other hand, the proposed feedback-gated ILFD can work as a fractional-N ILFD. The average of $I_{\rm T}\sin\varphi$ is calculated as follows:

$$\overline{I_T \sin\varphi} = \frac{1}{T}\int_{-t_0/2}^{t_0/2}\frac{I_{\rm injo}}{2}\{\cos(\omega_{\rm inj}t-2\theta)-\cos(2\omega t-\omega_{\rm inj}t)\}dt \tag{6}$$

where t_0 is the current conduction time in a given period and can also be defined as Φ/ω, where Φ is the conduction angle, as shown in Fig. 9.

When $2\omega - \omega_{\rm inj} = 0$,

$$\begin{aligned}\overline{I_T \sin\varphi} &= \frac{1}{T}\int_{-t_0/2}^{t_0/2}\frac{I_{\rm injo}}{2}\{\cos(\omega_{\rm inj}t-2\theta)-1\}\,dt \\ &= \frac{I_{\rm injo}}{2}\left\{\frac{2\sin(\omega_{\rm inj}t_0/2)\cos 2\theta}{\omega_{\rm inj}T} - \frac{t_0}{T}\right\}. \end{aligned} \tag{7}$$

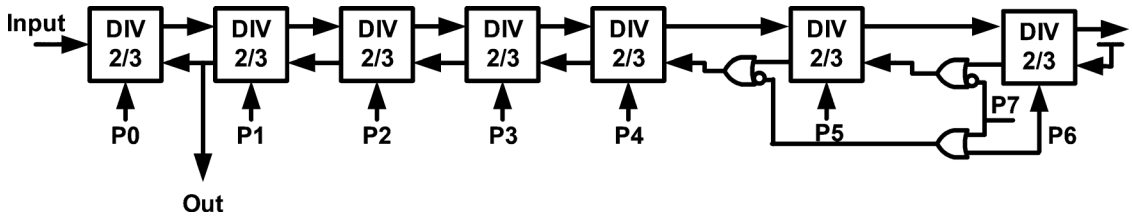

Fig. 14. Circuit implementation of the programmable divider with extended division range.

By defining $\omega_{\rm inj} = (n)/(N)\omega$, where n and N are numerator and denominator, respectively, of the fractional ratio, (7) can be rewritten as

$$\begin{aligned}\overline{I_T \sin\varphi} &= \frac{I_{\rm injo}}{2}\left\{\frac{2\sin(n\Phi/2N)\cos 2\theta}{2\pi n} - \frac{t_0}{T}\right\} \\ &= -\frac{I_{\rm injo}}{2}\frac{\Phi}{2\pi N}\left\{1 - \cos 2\theta \frac{\sin(n\Phi/2N)\cos 2\theta}{n\Phi/2N}\right\} \\ &\approx -\frac{I_{\rm injo}}{2}\frac{\Phi}{2\pi N}\{1-\cos 2\theta\}. \end{aligned} \tag{8}$$

Assuming that $\cos 2\theta = 1$, the above equation reaches the maximum value. In the case of divide-by-2 operation, n is equal to 2 and N is equal to 1. Thus, (8) is simplified to

$$\overline{I_T \sin\varphi} \approx -\frac{I_{\rm injo}}{2}\frac{\Phi}{\pi}. \tag{9}$$

When $2\omega - \omega_{\rm inj} \neq 0$,

$$\begin{aligned}\overline{I_T \sin\varphi} &= \frac{1}{T}\frac{I_{\rm injo}}{2}\left|\frac{\sin(\omega_{\rm inj}t - 2\theta)}{\omega_{\rm inj}} - \frac{\sin(2\omega t - \omega_{\rm inj}t)}{2\omega t - \omega_{\rm inj}t}\right|_{-t_0/2}^{t_0/2} \\ &= \frac{I_{\rm injo}}{2}\left\{\frac{\sin(\omega_{\rm inj}t_0/2)\cos 2\theta}{\omega_{\rm inj}T/2} - \frac{\sin(2\omega t - \omega_{\rm inj})t_0/2)}{(2\omega t - \omega_{\rm inj)T/2}}\right\} \end{aligned} \tag{10}$$

$$\approx -\frac{I_{\rm injo}}{2}\frac{\Phi}{2\pi N}\{1-\cos 2\theta\}. \tag{11}$$

In this case, there is no difference between (8) and (11).

Assuming that $\cos 2\theta = 1$, the above equation (11) reaches the maximum value:

$$\overline{I_T \sin\varphi} \approx -\frac{I_{\rm injo}}{2}\frac{\Phi}{\pi N}. \tag{12}$$

Note that $N = 1$ for divide-by-2 operation, where (4) and (9) indicate that the locking range of the proposed ILFD becomes $\Phi/\pi N = \Phi/\pi$ times smaller than that of the conventional ILFD. For divide-by-n/N operations, (5) and (12) indicate that the locking range of the proposed ILFD varies from 0 to $(I_{\rm injo}/2)(\Phi/\pi N)$, which is an output-referred value. Table II summarizes the theoretical locking range between the conventional ILFD and the proposed ILFD at different division ratios. Figs. 10 and 11 show the theoretically calculated locking range of the conventional and proposed ILFDs, respectively. If the injection power (for example, in the range of -10 to -5 dBm, as illustrated in Fig. 11) is properly controlled by setting $V_{\rm ctrl}$, false locking will not be a concern.

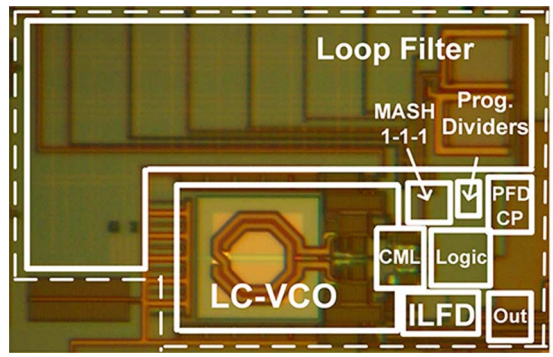

Fig. 15. Chip microphotograph.

In summary, the conventional ILFD has only a divide-by-2 state in an ideal small-signal operation. In actual designs, the conventional ILFD can have, for example, divide-by-3, -4, and -5 states due to the non-linearity of the injection signals. However, the locking range is very narrow and unstable. On the other hand, the proposed ILFD has several stable locking states, including fractional division ratios. Since each locking range is balanced, locking states can be chosen by controlling the free-running frequency of the ILFD.

B. Digital Calibration

In order to guarantee proper operation of the fractional-N injection, especially including PVT variations, a digital foreground calibration scheme [21] is adopted in order to initially calibrate the frequency, as shown in Fig. 12. The digital calibration circuitry consists of a frequency-to-digital converter (FDC), a path selector, a digital logic circuit, and a 10-bit DAC. Note that the injection from the core PLL is disabled, and the fractional division ratio is preset by activating the corresponding path in MUX1 and MUX2. The frequencies from the output of the core PLL and the ILFD are measured using counters. The outputs of the two counters, in the form of binary numbers, are compared and processed in the following logic circuit during each reference cycle. The output of the logic circuit directly controls the code for the DAC, giving rise to adjust the ILFD free-running frequency. If the derivative frequency from ILFD is greater (less) than that coming from the core PLL, the output code of the digital logic circuit is decremented (incremented) to spend down (up) the ILFD free running frequency. The calibration circuit works as a frequency-locked loop (FLL). After several divided reference cycles when the FLL is settled, the ratio between the core PLL frequency and the ILFD free-running frequency is approximately equal to the preset fractional division ratio. The calibration algorithm in this implementation

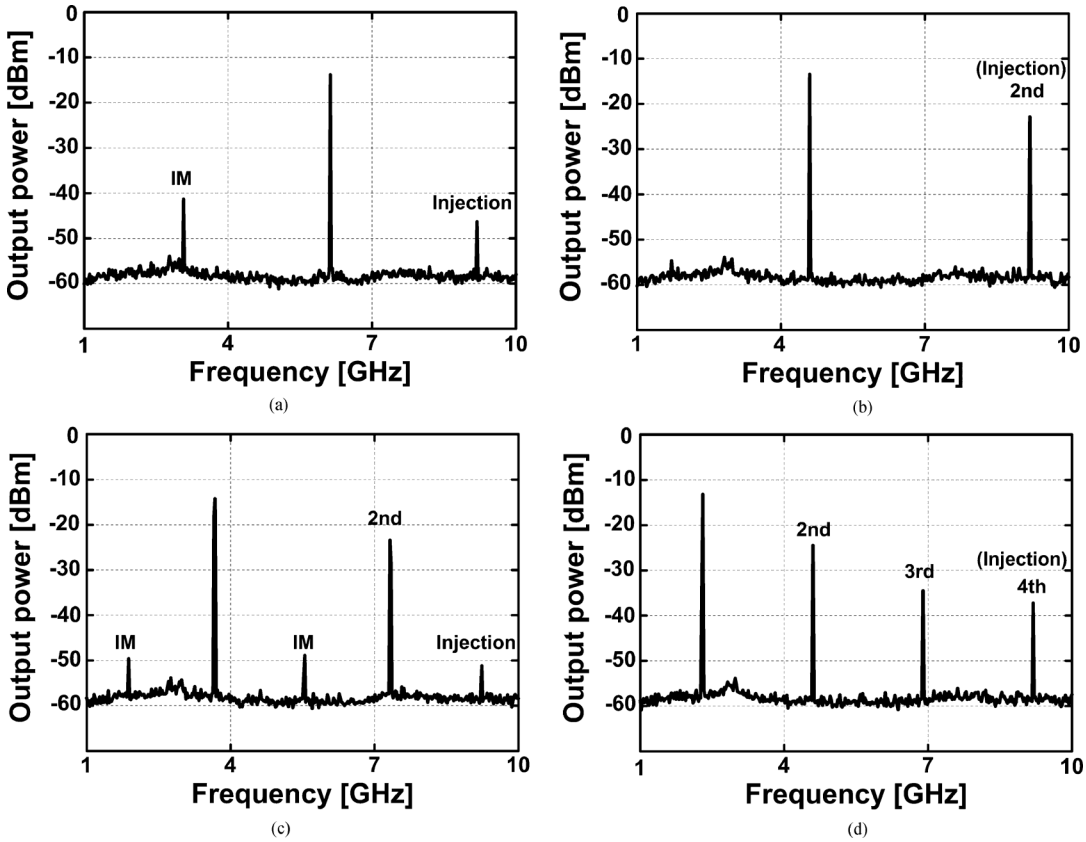

Fig. 16. Measured spectrums for (a) divide-by-1.5, (b) divide-by-2, (c) divide-by-2.5, and (4) divide-by-4 state.

is a simple up-down based scheme. Thus, the worst-case settling time is 1 023 cycles of the FDC clock. More sophisticated calibration algorithms can be adopted if a faster locking time is desired.

Another issue for consideration is that the proposed ILFD free-running frequency might drift away from the locking-range center or even fall out of lock (and then pull back to the border of the locking range by the FLL) due to environmental variations. Both cases lead to undesired phase noise and spur deterioration [20]. The calibration method using the FLL cannot detect this state because frequency errors are reset at every injection cycle. Fortunately, this issue can be solved by a dual-loop calibration mechanism [22], [23], with one free-running ILFD as a replica placed inside the FLL for tracking temperature and voltage drift, and the other ILFD is injection locked for producing a low-phase-noise output.

C. Class-C VCO

The core LC VCO uses the class-C topology [24], as shown in Fig. 13. This topology uses the advantages resulting from biasing the cross-coupled transistors in a class-C condition, generating more efficient oscillation currents, and thereby considerably lower power consumption, for the same phase noise level. However, the class-C VCO suffers from a trade-off between the maximum oscillation amplitude and robust start-up. Fortunately, this issue can be improved by means of a negative feedback circuit [25], [26], which adaptively adjusts the gate bias voltage of cross-coupled pairs.

D. Other Circuit Blocks

For a reference clock operating at a few tens of MHz, a divider with a wide programmable range of from 32 to 127, is required for the core PLL. The programmable divider adopts a modular, adaptable architecture [27] consisting of a cascade of divided-by-2/3 cells with an extended division range, as shown in Fig. 14. Divide-by-2/3 cells and additional control circuits are constructed by CMOS logic. The programmable divider is dynamically controlled by the delta-sigma modulator.

The phase frequency detector consists of two latches and a delay path. The charge pump adopts a cascaded current source to improve current matching. A second-order loop filter is adopted, followed by another filtering stage to further suppress ripples. MOS capacitors are adopted for the large capacitors in the loop filter, because these capacitors benefit from a higher capacitance density per area compared to MIM capacitors.

IV. Experimental Results

The proposed SDR synthesizer is designed and implemented using a 65 nm CMOS technology, with all circuit blocks integrated on the chip. Fig. 15 shows the chip microphotograph. The core chip area without decoupling capacitors is 0.38 mm^2. Phase noise performance is measured using a signal source analyzer (Agilent E5052B), and the spectrum is evaluated using a spectrum analyzer (Agilent E4448A).

The measured tuning range of the core PLL is 7.2 GHz to 10.3 GHz and is covered with sufficient overlap by neighboring bands. The measured output of the SDR synthesizer is 0.01

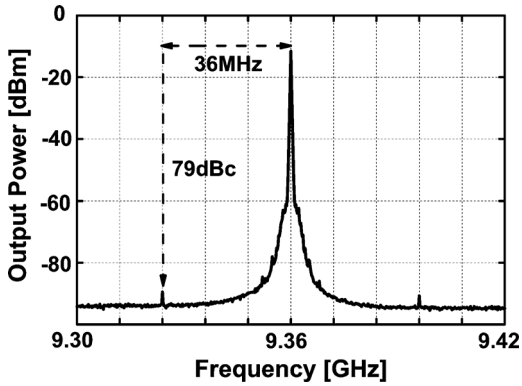

Fig. 17. Measured spectrum at 9.36 GHz.

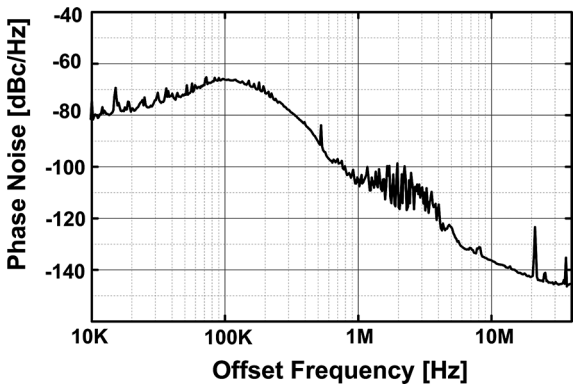

Fig. 18. Measured phase noise at 8.928 GHz.

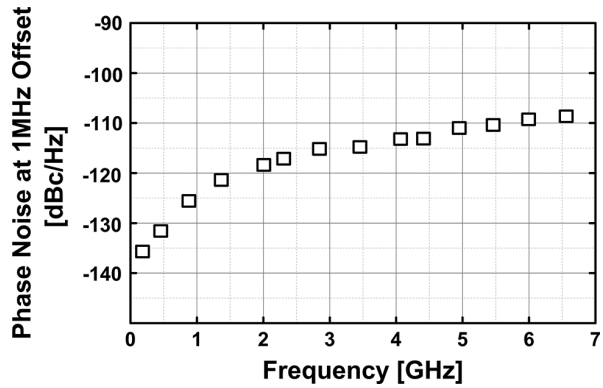

Fig. 19. Measured phase noise characteristics at 1 MHz offset against operating frequency.

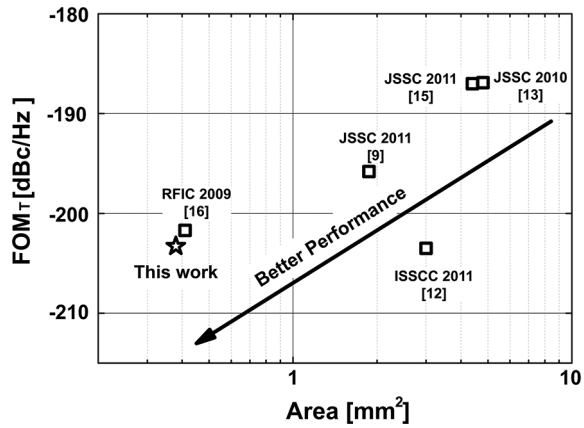

Fig. 20. Performance comparison with state-of-the-art prior work.

GHz to 6.6 GHz without any gaps. Fig. 16(a)–(d) shows the output spectra for divided-by-1.5, -2, -2.5, and -4 operations, respectively. Intermodulation products located far from carrier frequencies are observed at outputs, which might lead to undesired harmonic mixing in frequency bands that are assigned to other wireless standards. Fig. 17 shows the measured output spectrum at 9.36 GHz. The level of reference spurs is as low as -79 dBc. Fig. 18 shows the measured core PLL phase noise performance. The phase noise maps to a 2.2 ps jitter when integrated from 10 kHz to 40 MHz. Phase noise regrowth between 1 and 5 MHz offset is caused by noise from the power supply, whereas low-frequency noise is suppressed by a built-in low-drop out regulator, and high frequency noise is suppressed by on-chip decoupling capacitors. On the other hand, resistors in the loop filter add thermal noise, which is band-pass filtered by the loop transfer function, leading to relatively high in-band peaking of the PLL loop.

At a carrier frequency of 8.928 GHz, the core PLL achieves a phase noise of -120.9 dBc/Hz at 3 MHz offset. Fig. 19 shows the measured phase noise at an 1 MHz offset against with respect to the operation frequency. The phase noise characteristics have a slope of $+20$ dB/dec with respect to the output frequency in a logarithm coordinate system. The total power consumption varies from 16 to 26 mW, depending on the output frequency.

The $\mathrm{FOM_T}$, which allows comparison of the output frequency range, the power consumption, and the phase noise characteristic between multi-band PLLs, is unitized in order to evaluate the performances of these PLLs. The $\mathrm{FOM_T}$ is defined by the following equation [28]:

$$\mathrm{FOM_T} = \mathcal{L}(f_{\mathrm{offset}}) - 20\log_{10}\left(\frac{f_{\mathrm{o}}}{f_{\mathrm{offset}}}\frac{\mathrm{FTR}}{10}\right) + 10\log_{10}(\mathrm{P_{DC}}/1\ \mathrm{mW}). \quad (13)$$

where $\mathcal{L}(\mathrm{f_{offset}})$ is the phase noise, $\mathrm{f_{offset}}$ is the offset frequency, $\mathrm{f_0}$ is the oscillation frequency, $\mathrm{P_{DC}}$ is the power consumption, and FTR is the generated frequency range, which is defined as $(\mathrm{f_{max}} - \mathrm{f_{min}})/((\mathrm{f_{max}} + \mathrm{f_{min}})/2)[\%]$. Fig. 20 compares the $\mathrm{FOM_T}$ and the occupied chip area of analog-PLL-based frequency synthesizers reported in the literature [9], [12], [13], [15], [16]. Although the proposed SDR frequency synthesizer is not implemented in the most advanced technology, the proposed synthesizer achieves the best performance in terms of power consumption and chip area. Note that a previous study [16] involving two LC VCOs achieves a similar occupied chip area, compared to this work, mainly by two custom-designed inductors and shrinking loop filter area. If the proposed self-synchronized gating injection technique is applied to [16], only one LC VCO is required in the core-PLL. Therefore, removal of the other LC VCO contributes to an approximately 26.5% reduction in the total chip area, which further validates the effectiveness of the proposed method with respect to area reduction. Table III shows the performance of the SDR frequency synthesizer and the performances of state-of-the-art analog-PLL-based

TABLE III
PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART ANALOG PLL BASED SDR FREQUENCY SYNTHESIZERS

	Frequency	Tech.	phase noise[3] @ 10kHz offset	phase noise[2,3] @ 3 MHz offset	Area	Power	FOM_T[3]	Numbers of LC resonators	Output type
Unit	GHz	nm	dBc/Hz		mm^2	mW	[dBc/Hz]		
[9]	1.8-6	130 CMOS	-93	-136.8	1.87	36-53	-195.8	2	Quad.
[12]	0.05-10, 19-22, 38-44	130 CMOS	-91-98	-139.6	3.0	33-83	-203.5	2	Quad.
[13]	0.6-4.6, 5-7, 10-14, 20-28	250 BiCMOS	-109.9	-136.5	4.8[1]	680	-186.9	2	Diff.
[15]	0.125-32	180 BiCMOS	-91.6	-137.2	4.4[1]	1283	-187	4	Diff.
[16]	0.1-5	45 CMOS	-94	-136	0.41[5]	21.4-31.3[4]	-201.7	2	Quad.
This work	0.01-6.6	65 CMOS	-95.1	-135.3	0.38	16-26	-203.3	**1**	Quad.

[1]Area including pads.
[2]Normalized to 3 MHz from values reported at other frequency offsets.
[3]Normalized to 1.7 GHz from values reported at other carrier frequencies.
[4]Power consumption of the core PLL only.
[5]Area of the core PLL only.

frequency synthesizers in the literature [9], [12], [13], [15], [16]. To the best of our knowledge, this is the only frequency synthesizer that uses one LC resonator to cover a wide frequency tuning range.

V. CONCLUSION

This paper proposes a compact and low-power frequency synthesizer with a quadrature phase output using a fractional-N injection locking technique. The locking range of the proposed fractional-N ILFD is analyzed. Through careful design, the proposed frequency synthesizer can be well adapted to software-defined radios and cognitive radios.

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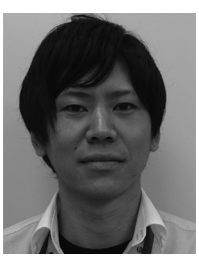

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