A Fully Digital 8 × 16 SiPM Array for PET Applications With Per-Pixel TDCs and Real-Time Energy Output

Leo H. C. Braga, *Student Member, IEEE*, Leonardo Gasparini, *Member, IEEE*, Lindsay Grant, *Member, IEEE*, Robert K. Henderson, *Member, IEEE*, Nicola Massari, *Member, IEEE*, Matteo Perenzoni, *Member, IEEE*, David Stoppa, *Senior Member, IEEE*, and Richard Walker, *Member, IEEE*

Abstract—An 8 × 16 pixel array based on CMOS small-area silicon photomultipliers (mini-SiPMs) detectors for PET applications is reported. Each pixel is 570 × 610 μ m² in size and contains four digital mini-SiPMs, for a total of 720 SPADs, resulting in a full chip fill-factor of 35.7%. For each gamma detection, the pixel provides the total detected energy and a timestamp, obtained through two 7-b counters and two 12-b 64-ps TDCs. An adder tree overlaid on top of the pixel array sums the sensor total counts at up to 100 Msamples/s, which are then used for detecting the asynchronous gamma events on-chip, while also being output in realtime. Characterization of gamma detection performance with an $3 \times 3 \times 5$ mm³ LYSO scintillator at 20 °C is reported, showing a 511-keV gamma energy resolution of 10.9% and a coincidence timing resolution of 399 ps.

Index Terms—Biomedical sensors, CMOS, digital silicon photomultiplier (SiPM), image sensors, mini-SiPM, positron emission tomography (PET), single-photon avalanche photodiode (SPAD), spatial and temporal compression.

I. INTRODUCTION

P OSITRON emission tomography (PET) is a nuclear imaging technique that utilizes annihilation gamma photons from positron decay to generate three-dimensional functional images of the body. Its main applications are preclinical research, clinical oncology, and brain function analyses [1]. PET is fundamentally different from other body imaging techniques such as computed tomography (CT) and magnetic resonance imaging (MRI) as it can provide metabolic information of the body. To this end, PET uses the emission from radioactive compounds (tracers) to localize tissues where a specific cell function is occurring as, for instance, the elevated glucose metabolism in cancer cells [1].

L. H. C. Braga is with the University of Trento, Trento 38123, Italy.

L. Gasparini, N. Massari, M. Perenzoni, and D. Stoppa are with Fondazione Bruno Kessler, Trento 38123, Italy.

L. Grant is with STMicroelectronics, Edinburgh EH12 7BF, U.K.

R. K. Henderson and R. Walker are with the University of Edinburgh, Edinburgh EH8 9YL, U.K.

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The working principle of PET is briefly illustrated in Fig. 1. When a radioactive atom of the tracer injected in the patient decays, a positron is emitted from the nucleus and, after travelling a short distance (typically between 0.1 to 1 mm [2]), an annihilation process occurs. In this process, the positron combines with an electron, both are annihilated and a pair of 511-keV gamma photons is emitted in opposite directions (180° apart). The PET scanner needs to detect both emitted photons of the pair to establish the line of response (LOR) along which the annihilation took place. After millions of LORs are acquired, a tomographic 3-D image of the subject is formed, revealing the tracer concentration.

To enable the detection of the photon pairs, PET scanners are normally constructed in the form of a ring of detectors, each of which needs to determine the energy, position, and time of arrival (ToA) of the incoming gamma photons. This data is then fed to a coincidence unit, which is responsible for determining if any two detected photons are from a unique annihilation process. This is done by first selecting the photons with the correct energy and then employing a coincidence timing window, usually a few nanoseconds wide [3]. Finally, the LORs are generated based on the photons position information.

The detectors most widely used in PET scanners are scintillation detectors. These detectors comprise a dense crystalline scintillator material which absorbs gamma photons and emits light as a result, coupled to photosensors. The scintillation light is emitted isotropically in a short pulse in time, typically a couple of hundred nanoseconds long [4], as shown in Fig. 2. The typical number of light photons emitted from a single 511-keV gamma scintillation is between 1 to 30 k, depending on the scintillator material [4]. Therefore, the first requirement for PET photosensors is to possess a very high sensitivity in order to achieve a good signal-to-noise ratio (SNR).

Another important requirement for the photosensor concerns its timing performance. The recent development of bright and fast scintillators such as LSO, LYSO, and LaBr₃ has enabled the usage of time-of-flight PET (ToF-PET), which explores the difference between the arrival times of the gamma pair to estimate the position along the line-of-response (LOR) where the annihilation took place. Therefore, to actually improve the SNR and image contrast with ToF-PET, the employed detectors must feature sub-ns timing performance [5].

Moreover, as PET detectors can be up to tens of centimeters in size [1], the photosensors must also provide spatial information so as to localize the scintillation point inside the crystal or crystal matrix. Finally, an additional desired feature of the

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Fig. 1. PET working principle.

photosensors is the compatibility with magnetic fields, so as to enable the close integration of PET with MRI (instead of CT). The main advantages that MRI offers over CT are better soft tissue differentiation [6] and lack of radiation dosage to the patient.

Historically, the most commonly used photosensors in PET scanners were photomultiplier tubes (PMTs) [7]. This was mainly due to their very high gain, low noise, and fast response. However, PMTs are formed by a vacuum tube, and, as such, they are somewhat bulky and fragile. In addition, they also require power supplies of up to thousands of volts and are sensitive to magnetic fields. Due to these disadvantages, solid-state detectors (SSDs) have long been proposed as an alternative to PMTs [8].

SSDs are intrinsically compact and rugged, besides being insensitive to magnetic fields and usually requiring lower operating voltages. One type of SSD that has been showing promising results in the field of PET is the silicon photomultiplier (SiPM) [9]. SiPMs comprise large arrays of single-photon avalanche diodes (SPADs) connected in parallel. When a light photon is detected by the SPAD, a very fast avalanche is triggered, generating a current pulse. Therefore, when a scintillation event occurs, a current signal builds up at the SiPM output proportional to the number of SPADs triggered.

The PET performance of state-of-the-art SiPMs heavily depends on the type and dimension of the scintillator crystal used in the measurements. Nonetheless, a figure-of-merit (FOM) comparison can be made by taking, for instance, an LYSO crystal with $3 \times 3 \times 5$ mm³ size as a standard [10]–[15]. Focusing first on the detectors coincidence resolving time (CRT, also known as timing resolution), [10] reports a CRT of 138 ps using Hamamatsu SiPMs, while [11] reports 183 ps using SensL devices and [12] obtained 186 ps with FBK-SRS SiPMs. Other works have focused on energy resolution characterization, another important FOM for PET, with [13] reporting 10.2% also with FBK-SRS SiPMs, and [14] reporting 10.5% with Hamamatsu sensors (with a $5 \times 5 \times 5$ mm³ crystal, however).

Still, the intrinsic photon counting capability of SPADs is not fully exploited with SiPMs, as the analog-to-digital (A/D) conversion is only performed on the final summed current output, through external electronics and is therefore subject to electronic noise. Since the SPAD output is only able to distinguish between a photon and no photon (i.e., it is an intrinsically binary output), performing the A/D conversion at each individual SPAD can significantly improve the noise performance of the system. This approach has been recently pursued in [16], with the so-called "digital SiPM."

The digital SiPM takes advantage of CMOS technology to perform a 1-b A/D conversion per SPAD and to integrate an on-chip digital accumulator that produces the sensor energy output. In addition, the timing information is also generated on-chip, by a time-to-digital converter (TDC), and there are per-SPAD memories that can disable noisy devices, further improving performance and device yield. Up to now, only one group has successfully developed and characterized a digital SiPM for PET, reporting a CRT of 153 ps and an energy resolution of 10.4% [17]. Other groups have also been pursuing the digital SiPM approach [18], [19] without, however, having reported PET characterization results yet. Finally, CMOS SiPMs have also been reported for different applications, such as fluorescence lifetime imaging [20].

In this work, we present a digital SiPM for ToF-PET applications developed in 0.13- μ m 1P4M CMOS imaging technology [21]. The sensor is composed of an 8 × 16 pixel array and incorporates spatio-temporal compression of SPAD pulses for increased fill-factor, per-pixel timestamping of photons for improved timing resolution, and top-level monitoring of the photon flux for efficient scintillation detection. The sensor also offers a real-time output of the total detected energy at up to 100 MSamples/s.

The remainder of this paper is organized as follows. Section II details the sensor architecture, Section III presents the sensor characterization, including both electrooptical and scintillation measurements. Finally, Section IV lays the conclusions of this work.

II. SENSOR ARCHITECTURE

Deep-submicron CMOS technology enables the integration of processing circuits into sensors with minimum area overhead. Our main goal when designing the sensor was to exploit this advantage to not only create a digital version of the



Fig. 2. Scintillation light pulse hitting the photosensor and its respective outputs.



Fig. 3. Mini-SiPM (detector cell) complete schematic

SiPM, but to extract as much information as possible from the gamma scintillation events. Three features that could provide valuable information in PET applications were identified: multiple photon timestamping, increased spatial resolution, and scintillation decay time determination. Multiple photon timestamps can be combined to provide a better CRT [22], [23], more refined spatial information can lead to improved scintillation positioning [24], [25], while scintillation decay time information can be used to distinguish between different crystal types [26].

Concurrently, the sensor needs a high fill-factor (FF) and to perform asynchronous exposure, as the integration period needs to be started at the beginning of a scintillation event, which occurs randomly in time. To achieve these goals, the sensor architecture is divided in three levels: 1) a detector cell, which consists of many SPADs connected to a counter; 2) the pixel, which is the smallest structure that preserves spatial information of detected photons and is also responsible for timestamping photons; and 3) the top-level, which controls the sensor exposure, the pixel array readout and the external I/O. In the following subsections, each hierarchy level is explained in detail.

A. Detector Cell: The Mini-SIPM

The typical operation of passively quenched SPADs implemented in CMOS technology can be briefly described as follows: when a photon is detected, an avalanche is triggered and a voltage pulse builds up on one of the SPAD nodes, which is then digitized by an inverter. During the inverter pulse width, any further avalanches generated by the SPAD will not produce a new output pulse, and thus this width is commonly referred to as the SPAD dead time. Furthermore, spurious avalanches can occur due to thermally generated carriers or band-to-band electron tunneling, which will generate digital pulses as if a photon had been detected. Therefore, these pulses are the main noise source of digital SPAD-based sensors, and they are characterized by their occurrence rate, known as the dark count rate (DCR) [27].

As both the average DCR and the SPAD yield (i.e., the percentage of SPADs with DCR below a certain threshold) can be severely compromised in large CMOS SPADs, practical SPAD diameters are limited to a few dozen micrometers ([17] is one of the largest CMOS SPAD reported, with 59.4 × 64 μ m² size with 78% FF), which is much less than the desired spatial resolution. To improve the DCR versus FF compromise while at the same time reducing the required electronics for reading out the SPAD array, we implemented spatio-temporally compressed fully digital small-area SiPMs [28] (mini-SiPMs).

The mini-SiPM schematic is shown in Fig. 3. At a high level, it is composed of 180 SPADs and their respective front-ends, connected to a compression circuit and then to a counter. The key advantage of the mini-SiPM with respect to other digital SiPM implementations comes from the compression circuit, which is divided in two parts. First, three SPADs are OR'd together so that, if any of them trigger during another one's dead time, only one will be counted. The main benefit of this

column bus



Fig. 4. Pixel block diagram with DAMAC simplified schematic.

topology is that the required readout circuit per SPAD is reduced, meaning the FF is increased, while, as the SPADs have the same size, the DCR scales linearly with area and the yield is kept constant. On the other hand, the possible disadvantage of compression loss is minimized by the combination of the SPADs small size with the low photon surface density in PET scintillator detectors. Since the feasibility of this architecture depends on the distribution of photons in space, we call it spatial compression.

Next, a monostable is used to reduce the SPAD pulses width to subnanosecond, effectively removing the SPAD dead time and allowing many more SPADs to be compressed together. By connecting many monostables through an OR tree, a singlewire GHz channel for transmitting the SPAD triggers is created, which is then directly fed into a counter clock input. This approach provides a substantial area gain compared to other digital summing solutions as, for instance, a full parallel adder. Again, the potential disadvantage of compression loss is minimized by the relatively low photon arrival rate with respect to the high speed digital blocks of deep-submicron CMOS, which enable monostable pulses as short as 250 ps in the actual implementation. As this second technique takes advantage of the distribution of photons in time, we call it temporal compression.

The implemented SPADs have a structure similar to [29], with a circular shape and an active diameter of 16.27 μ m. They are organized in a 12×15 honeycomb-like array with well sharing [30], having their cathodes connected to a common bias line (V_{SPAD}) and their anodes individually fed into passive quenching transistors (M1). The SPADs front-end circuit is further composed by a Schmitt trigger inverter, which digitizes the SPAD pulse and prevents the slow recharge of the SPAD from affecting the compression circuit, and by a 6T SRAM, which allows disabling high-DCR SPADs.

Finally, the counting stage is implemented with two 7-b ripple counters working in ping-pong mode. This is done to avoid any dead time in the system, so that, when one counter is being read and reset, the other is performing the counting operation. The counter selection is performed by the pipeline select signal



Fig. 5. TDC block diagram.

(*PIPE*), which also separates the pulse train into trains A and B, each containing the pulses of its respective counter.

B. Pixel

Moving up the hierarchy, the pixel is responsible for aggregating data from the mini-SiPMs and timestamping photons. As the mini-SiPM size is limited by the compression losses, a compromise between high spatial resolution (i.e., small pixel size) and high FF was achieved by designing the pixel as a 2×2 mini-SiPM array, as shown in the diagram of Fig. 4. The main block in the pixel is the data managing circuit (DAMAC), and its simplified schematic is also shown in Fig. 4.

The DAMAC manages two types of data: counts (energy) and timestamps. The energy data comes from the four mini-SiPM outputs, which are summed together and then fed to a 3×9 -b FIFO memory for storage. This FIFO has two duties. First, it stores the pixel counts while waiting for the top-level exposure control (ACCUM). Then, when ACCUM is set high, the last register starts acting as an accumulator so that, when the pixel is readout, the total energy accumulated during the exposure period is provided in a single register. Additionally, a real-time output is continuously fed to the top-level discriminator after the first register, the purpose of which will be explained in the next subsection.

The timestamping subsystem, on the other hand, is responsible for both generating the timestamps from the mini-SiPM pulse trains and storing them for later readout. For timestamp generation, two 12-b TDCs were implemented based on a ring



Fig. 6. Top-level block diagram.

oscillator architecture [31], and their block diagram is shown in Fig. 5. The ring oscillator has four pseudo-differential stages, and it triggers a 9-b ripple counter at each period, providing the coarse output, while the 3-b fine output is obtained by encoding its four internal nodes. In order to minimize the TDCs power consumption, the ring oscillator is started only when a pulse arrives from the mini-SiPMs, while being stopped by the system clock.

Similarly to the mini-SiPM counters, the TDCs also work in ping-pong mode, with the active block being selected by the pipeline signal *PIPE*. Each phase of PIPE defines a time window, in which the enabled TDC is able to timestamp the first pulse that reaches it. Special attention has been paid in the layout of the mini-SiPM so as to minimize the skew added by the compression tree since, at the pixel level, the timestamped pulse may have come from any of the 720 SPADs.

Due to DCR, the TDCs may also be triggered even when there are no impinging photons. Therefore, to minimize the probability that the TDC was already triggered by a dark count when a photon arrives, the time windows defined by PIPE must be relatively short. In other words, the clock—which is distributed from the top-level—should have a high frequency with respect to the total DCR of the pixel. The clock frequency also affects other sensor features at the top-level, as will be shown later, and in this design 100 MHz was targeted. However, as a safety margin, the depth of both the mini-SiPM counters (7 b) and the TDCs (12 b) were chosen to also cope with lower clock speeds (e.g., 5 MHz, when one cycle equates to the event integration time), avoiding any counter saturation and providing enough time range, respectively.

C. Top-Level

As mentioned in Section I, gamma photons arrive asynchronously in time at the detector, and the resulting light photons emitted from the scintillation reach the sensor spread in space, but close in time. Therefore, the sensor must be able to recognize the occurrence of a scintillation event and start the exposure accordingly. To this aim, the photon counting function has been divided in short, consecutive time bins defined by the clock signal, resulting in a discrete photon flux estimation, which can then be used to discriminate incoming gamma events.

At the pixel level, each register of the accumulator FIFO contains a sample of the photon flux. However, since the scintillation photons are spread over the array, these counts still need to be gathered at the top-level, in real time. To achieve this, a distributed adder was designed in a H-tree-like topology and superimposed over the pixel array, in which each node performs the addition of the counts from its leaf cells (the pixels). Since all pixel counts must be synchronized for this scheme to work, the clock signal is distributed through the tree in the opposite direction of the count data flow, resulting in equalized propagation delays. Hence, at the top-level, the total chip photon count for each time bin, i.e., the discrete photon flux, is obtained. From this point, a discriminator can monitor this value to determine when an event occurred. The complete top-level diagram of the sensor, including the discriminator state diagram, is shown in Fig. 6.

The discrimination logic compares two consecutive photon flux samples against two configurable thresholds to distinguish the fast light pulse generated by a gamma event from noise



Fig. 7. Sensor timing diagram.

(dark counts and spurious photons). When an event is detected, the in-pixel accumulator will start integration from the time bin compared to the first threshold, while the last two stages of the TDC FIFOs will contain the timestamp of the first pulses in the bins corresponding to the first and second thresholds, respectively (see the timing diagram in Fig. 7). The goal of the double threshold algorithm is to retain the timestamps of the very first photons of the scintillation, which are the most important for a precise gamma ToA estimation [23]. With this algorithm, the first threshold can be made small, slightly above the noise level, so that even in the case of an event arriving very close to the end of the time bin, the very first timestamps that were taken in that bin will still be saved. The second threshold, on the other hand, can be made large, so as to clearly distinguish between the desired gamma events and noise/scattered events.

An important feature of this architecture is that the ToA estimation is completely decoupled from the discrimination function, as the relevant event timestamps are saved for postprocessing. This means that the discriminator can be configured with the sole purpose of increasing the sensor efficiency, i.e., of reducing the number of triggers due to noise or scattered events, without regarding the effects on the timing resolution.

The timing diagram of the sensor is shown in Fig. 7. In time bin "1," the pulses generated by all mini-SiPMs of the chip are being counted in their respective A counters, while the timestamp of the first pulse in each pixel will be saved by TDC A. During the next time bin, the B counters and TDCs will start operating, while the A blocks will be frozen for half clock cycle. After this half cycle, the FIFOs are clocked, thus saving the sum of the A counters and the timestamp at TDC A, and the A blocks are then reset. From this moment on, the pixel counts will flow through the adder tree, reaching the top-level output after one and a half clock cycles. As an example, the diagram shows a gamma event arriving during bin "2". The counts will propagate to the top-level such that while bin "5" is being counted at the pixel level, the discriminator will process the total array count value from bin "2" (which is above the first threshold) and enter the discriminate state. Following this, in bin "6" the discriminator will enter the *integrate* state (i.e., bin "3" counts above second threshold), sending the accumulate signal ACCUM to the pixel, which will both freeze the TDC FIFOs and start integration in the accumulator FIFO. This way, the timestamps generated at bin "2" are stored at the last TDC FIFO register, while the sum at the accumulator is started also from



Fig. 8. Chip micrograph.

bin "2." The duration of *integrate* is externally configurable, so that the sensor integration time (comprised by the *discriminate* and *integrate* states) can be optimized for each setup. Finally, after *integrate*, the sensor will go into the *readout* state, stopping the pixel accumulators and then waiting to be readout by an external controller. Each pixel energy and timestamp information is readout by accessing the sensor in a standard row-wise mode, resulting in a full chip readout time of 2.84 μ s at a 100-MHz clock, during which the sensor cannot detect further events.

During all states before *readout*, the sensor is constantly outputting the chip-level count, i.e., the discrete photon flux, which can be monitored externally in real-time, at the same sampling frequency as the clock (i.e., 100 MSamples/s). Additionally, the internal discriminator can be completely bypassed in favour of an external one, since both the *integrate* and *readout* state signals can be provided externally.

The sensor was implemented in a $0.13 \ \mu m$ 1P4M CMOS imaging technology, achieving a pixel FF of 42.6% with pixel dimensions of $570 \times 610 \ \mu m^2$ The full die is $9.85 \times 5.45 \ mm^2$, as shown in the micrograph in Fig. 8, resulting in a total FF of 35.7%. The top pads are for testing purposes only, and the full sensor operation has been verified using only the bottom pads. A production re-spin of the chip, therefore, could lose the top pads for an improved total FF of about 38%. Furthermore, the fabrication process features Through-Silicon Vias (TSV), allowing all pads to be connected via a ball grid array on the back of the die. Compared with wire-bonded devices, this solution greatly reduces the chip-to-chip spacing in a PET detector, thus increasing the overall FF.

III. EXPERIMENTAL RESULTS

To control and readout the sensor, a Xilinx SP605 board—which contains a Spartan-6 FPGA—was used. The characterization of the sensor was done in two phases. First, the electrooptical performance of each relevant block was characterized, and, next, measurements using a scintillator were made. For the later, the crystal of choice was a $3 \times 3 \times 5$ mm³ LYSO wrapped in Teflon and optically coupled to the sensor using Cargille Meltmount glue. To emulate a PET experiment, a Na²² gamma source with 370 kBq of activity was used. This source emits 511-keV photons, as in PET, and also 1275-keV photons, which can be used to calibrate the sensor response. In



Fig. 9. SPAD characterization results at 1.5-V excess bias. (a) DCR distribution. (b) Average PDP. (c) Timing resolution.

the following subsections, the results from both characterization phases are reported.

A. Electrooptical Characterization

The results of the SPAD characterization are plotted in Fig. 9. All measurements were performed with an excess bias of 1.5 V and at room temperature. The figure shows the three most important SPAD characteristics to our system: the dark count rate, the photon detection probability (PDP), and the timing resolution.

DCR may affect the sensor performance in three distinct ways. First, its shot noise will reduce the SNR of the energy output. Second, dark pulses may trigger some TDCs in a clock cycle before a real event arrives, preventing an actual photon from being timestamped. Finally, many dark counts occurring in a small time interval could deceive the discriminator into



Fig. 10. TDC characterization results. (a) LSB uniformity. (b) DNL. (c) INL.

registering an event, thus reducing the sensor efficiency. Even if low DCR is always desired, the sensor architecture features different mechanisms to mitigate these issues, e.g., fine-grained spatial information enabling optimization of the integration area for better SNR, or per-pixel TDCs, increasing the probability of having at least a few real photon timestamps in an event.

The measured DCR has a median of 13.7 kHz, while the average is 42.1 kHz. The effect of these values on both the energy SNR and discriminator efficiency will depend on the number of photons detected in a scintillation event, and thus will be discussed in the next subsection. The probability of a TDC being triggered by a dark count, however, can already be calculated: taking the average pixel DCR of circa 30 MHz and assuming a 100-MHz clock (10-ns time bins) results in a probability of about 25%. However, taking into account that gamma events will arrive randomly in time—and thus the average time between the clock edge and an event arrival is 5 ns—and that the photons will spread across at least 3×3 pixels, the probability of all TDCs being triggered by darks when an event arrives is reduced to 2×10^{-8} .

Concerning the SPAD PDP, measurements were made with a Horiba Jobin Yvon TRIAX 180 monochromator. The curve in Fig. 9(b) shows a peak at around 45% which, given the pixel FF of 42.6%, results in a sensor photon detection efficiency of 19.1%. There is a sharp drop in PDP at around 440 nm, which was not expected given previous results in this technology [29]. An analysis of this phenomenon has shown that it is caused by interference in the nitride layer, which then creates a peak in the sensor reflectivity.



Fig. 11. System timing resolution (jitter) compared with a commercial TCSPC system.



Fig. 12. Experimental setup for PET emulation.

Finally, the single-photon SPAD timing resolution was measured with a 470-nm, 70-ps pulsed laser (PicoQuant LDH-P-C-470) and a time-correlated single photon couting (TCSPC) module (PicoHarp 300) connected to the SPAD after the inverter stage. The results show a full-width at half-maximum (FWHM) timing resolution of 171 ps, not discounting the laser intrinsic timing resolution. Further increasing the SPAD excess bias to 3 V improves the resolution to 142 ps.

The next block to be characterized was the TDC, which mainly affects the final CRT performance. However, the CRT performance in PET systems is usually heavily limited by the photon statistics and not by the TDC resolution [32], and, thus, the TDC implementation targeted low area occupancy and power consumption more than absolute resolution. The obtained results are shown in Fig. 10. The average resolution is approximately 64.5 ps, with less than 1 ps of standard deviation between all of the TDCs in the array. The differential non-linearity (DNL) and integral nonlinearity (INL) performance was measured through a code density test using the SPADs dark counts, and a typical TDC performance is shown, with DNL <0.28 LSB in a 50-ns (20-MHz) range. The INL performance, even if not as good as DNL, can be fully corrected in postprocessing.



Fig. 13. Examples of typical 511-keV, 1275-keV, and pile-up events. (a)-(c) Real-time energy output. (d)-(f) Pixel counts.

Finally, the full system jitter was measured, which includes not only the SPAD jitter, but also all jitter contributions from the mini-SiPM compression circuit, the TDCs and the clock distribution. For this measurement, the same 70-ps laser was used, but the photon timestamp was taken from the in-pixel TDCs. The results are shown in Fig. 11, including a reference system based on the previously mentioned TCSPC module and a MPD PDM 50ct SPAD. The timing histogram of a typical pixel is plotted, highlighting a 263-ps FWHM resolution. The inset shows the distribution of all pixels, with an average of around 266 ps and a standard deviation of around 16 ps.

B. Characterization With LYSO Scintillator

The experimental setup used for the PET emulation characterization phase is pictured in Fig. 12, showing the SP605 board, a custom PCB to interface the sensor and the SP605 and the TSV-bonded sensor coupled to the LYSO crystal. During the experiments, the sensor is covered by a small black box, and the Na²² source is placed above this box. The whole setup is placed inside a temperature chamber, which was kept at 20 °C during all measurements. Finally, the sensor is configured for an integration time of 150 ns per event and around 8% of the highest DCR SPADs were disabled [i.e., all SPADs with DCR above 135 kHz, as per Fig. 9(a)], resulting in a total chip DCR of circa 1.8 GHz. The applied SPAD excess bias was the same as for the electrooptical characterization, 1.5 V.

To demonstrate the sensor functionality, the real-time energy output and the pixel counts of three typical events are plotted on Fig. 13: a 511-keV gamma, a 1275-keV gamma, and a pile-up event. For instance, from Fig. 13(c), one can understand how the real-time energy output can be used to detect these pile-up events. Additionally, Fig. 13(d) and (e) illustrate the fine-grained pixel pitch ($\sim 0.6 \times 0.6 \text{ mm}^2$) and the resulting photon distribution, which can be used to optimize the integration area. Also interesting to note is that the photons are spread in a larger area than the crystal itself, which can be

mainly attributed to the 500- μ m-thick glass that is attached to the wafer front-side in the TSV process.

As mentioned in Section I, one of the main FOMs of PET detectors is the energy resolution, which can be seen as a measure of the SNR of the energy output. To calculate it, we first need to convert the sensor output (counts) to gamma energy. In a typical SiPM, this conversion is nonlinear mostly due to the SPAD dead time, since a photon that hits a SPAD that was recently triggered will not be counted. The amount of compression (i.e., the photon loss with respect to an infinitesimally small dead time) depends on the quenching circuit (which affects the dead time) and the SPAD size (which affects the probability of a photon hitting an already triggered SPAD). However, in the case of our sensor, the photon loss may be further increased due to the mini-SiPM compression schemes.

To estimate the sensor response in the desired range, the average counts for the 511- and 1275-keV gammas and the measured sensor DCR are used to fit an approximated compression curve, based on analog SiPMs [33], as shown in Fig. 14. This model does not take into account crosstalk or after-pulsing, which, however, do not have major effects on our system: measurements with a mini-SiPM-like structure and the same SPADs reported in [30] showed less than 2% total crosstalk, while afterpulsing is removed by making the dead time longer than the integration time.

Finally, the obtained compression curve is used to transform the total counts into gamma energy, providing the Na²² energy spectrum shown in Fig. 15. Besides the Na²² gamma emission peaks (511 and 1275 keV) and pile-up events, the spectrum is composed by several other features, such as LYSO self-emission and partial gamma absorptions due to scattering. Therefore, Fig. 15 shows a number of scattered and LYSO-emitted events below 400 keV, the photo peak at 511 keV, then a second set of events that are due to 1275-keV gamma scattering and lower energy events pile-up, and, finally, the 1275-keV peak.

The energy resolution is defined as the ratio between the FWHM and the mean of the 511-keV photo peak. However,



Fig. 14. Total sensor counts versus gamma energy, highlighting the sensor compression curve.



Fig. 15. Obtained energy spectrum with photo peak Gaussian fit, showing a 10.9% energy resolution.

the actual measured peak has two further components that must be taken into account before calculating the sensor resolution. One is the pile-up and scattered events that are spread all over the spectrum, while the other is the so-called escape peak. The escape peak is due to events where the 54-keV X-ray that is generated during the photoelectric interaction in LYSO escapes the crystal, thus reducing the detected energy. Therefore, we fit the measured peak with a sum of three functions: a Gaussian for the 511-keV photo peak, another Gaussian for the 457-keV escape peak, and a first-degree polynomial for the scattered events [15]. Finally, the FWHM of the fitted photo peak Gaussian is obtained, resulting in an energy resolution of 10.9%. To fully appreciate this number, one must take into consideration the LYSO intrinsic resolution, which has been reported to be of the order of 8% [34].

The fitting procedure used to obtain the compression curve also allows us to estimate the number of detected photons if no compression was present (i.e., no dead time or spatial and temporal compression), which is plotted as the dashed line in Fig. 14. This shows that, for a 511-keV scintillation event, the sensor loses about 10% of the photons due to the various compression schemes. To understand how the spatial and temporal compression contribute to the total loss, the following measurements were performed. First, a single SPAD was enabled each



Fig. 16. CRT results. (a) Comparison between the single timestamp and the multiple timestamp estimator using different photon indices/different number of timestamps. (b) Obtained histogram for the single timestamp estimator using the third timestamp. (c) Obtained histogram for the multiple timestamp estimator using the first seven timestamps.

three spatially compressed SPADs, and then all SPADs in one third of the total groups, illustrating zero and maximum spatial compression, respectively, with equal PDE. The results showed that around 4% loss is due to the implemented spatial compression. For the temporal compression, we swept the externally controllable monostable pulse width, which indicated around 2%–3% of loss at the minimum pulse width of 250 ps.

The other key FOM for PET detectors is the coincidence resolving time. To measure it, two identical acquisitions setups (i.e., FPGA board, sensor, and LYSO crystal) were placed on top of each other, with the Na^{22} source closer to the bottom sensor. On average, each sensor had a total of 45 timestamps for each 511-keV gamma event. To estimate a single time of arrival for



Fig. 17. Total sensor counts histogram for different discriminator thresholds.

Sensor			
Process technology	CMOS 1P4M 0.13µm Imaging	Maximum clock frequency	100MHz
Array Size	8×16 pixels	Output data rate	1.6Gb/s
In-pixel photodetectors	4 mini-SiPMs of 180 16.27μm SPADs each	Chip size	9.85×5.452 mm ²
Array fill factor	42.6%	Supply voltage	3.3V for digital 1.2V for core
Pixel pitch	$610.5{\times}571.2\mu\text{m}^2$	Chip power consumption	200 mW (dark) 300 mW (light)
TDC			
TDC range (12b)	261.59ns	TDC DNL (50 ns range)	-0.24 +0.28LSB
TDC resolution (1 LSB)	64.56ps	TDCs spatial uniformity (σ across a chip)	0.81ps
TDC INL (50 ns range)	-3.9 +2.3LSB	TDC current consumption (for a single running TDC)	0.79mA
SPAD (@ 1.5V excess bias)			
Jitter (incl. 70 ps laser)	171 ps (142 ps @ 3V)	Peak PDP	45%
Median DCR	13.7 kHz	Average DCR	42.1 kHz
System jitter			
Single photon, average of all pixels jitter		$266 \text{ ps} (\sigma = 16 \text{ ps})$	
Gamma detection performance (using 3×3×5 mm ³ LYSO scintillator, @ 20° C)			
511 keV peak energy resolution		10.9%	
Compression loss with 511 keV gammas		~ 10%	
CRT (using 7 timestamps w/ estimator in [22])		399 ps	

 TABLE I

 SUMMARY OF THE SENSOR PERFORMANCE AND MAIN CHARACTERISTICS

each event, the first step is to process the timestamps intervals, so that early dark-generated timestamps can be removed. Then, two different algorithms were compared for ToA estimation: a simple, single timestamp estimator, and the hardware-friendly, multiple timestamp estimator described in [22]. The results of both are shown in Fig. 16(a), where the *x*-axis represents the

index of the photon being used for single timestamp estimation and the range of photons (first to the *n*th) for the multiple timestamp estimator. The best CRT obtained for the single timestamp estimator was 427 ps at the third timestamp, with its histogram shown in Fig. 16(b), while the best CRT for the multiple timestamp estimator was 399 ps by combining seven photons, with its histogram shown in Fig. 16(c).

Finally, the efficiency improvement due to the discriminator can be verified by changing its thresholds, as shown in Fig. 17. Starting with both thresholds very close to the DCR level, at 35 counts, the curve marked as "th 1" was obtained. In this case, a lot of events read out by the sensor which are purely due to noise, as evidenced by the low energy, out of scale, peak. However, by sequentially increasing threshold B, first the noise peak can be greatly reduced ("th 2", 40 counts), then completely removed ("th 3", 45 counts), followed by also filtering out the unwanted scattered events, and finally leaving only the 511-keV peak and above ("th 6", 180 counts). In all cases, the total number of acquired events was the same, and thus the increase in height of the photo peak highlights the increased efficiency. Converting the obtained sensor counts to gamma energy shows that the minimum discerned gamma energy is below 40 keV.

IV. CONCLUSION

A fully digital silicon photomultiplier for ToF-PET applications with per-pixel photon timestamping has been presented and its main characteristics and performance are summarized in Table I. The sensor contains 92 k SPADs, arranged in 8×16 pixels, each of size around $0.6 \times 0.6 \text{ mm}^2$, resulting in a 42.6% fill-factor. The in-pixel 12-b TDCs have an average resolution of 64.5 ps, and a DNL below 0.28 LSB, while the complete system jitter, measured by timestamping single photons, has an average of 266 ps across all pixels. The implemented adder tree is able to provide a real-time output of the detected energy in the array at up to 100 Msamples/s, which is also internally used by the discriminator. Analyzing the sensor in a PET-like setup demonstrated an energy resolution of 10.9%, with a total compression loss of circa 10%, and a timing resolution of 399 ps obtained by a ToA estimator combining seven timestamps. Finally, the discriminator was shown to greatly improve the sensor efficiency, while at the same time being able to correctly validate events below 40 keV, which is essential in PET detectors where the scintillation light may be spread across different sensors.

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Leonardo Gasparini (S'10–M'12) received the B.Sc. degree, M.Sc. degree in telecommunication engineering, and Ph.D. degree in information and communication technologies from the University of Trento, Trento, Italy, in 2004, 2007, and 2011, respectively.

For his doctoral studies, he worked on the development and the metrological characterization of an ultralow-power wireless system equipped with a camera. In 2010, he joined the Integrated Optical Sensors and Interfaces Group, Fondazione Bruno

Kessler, Trento, Italy, where he is involved with the design and characterization of integrated optical sensors fabricated in deep-submicron CMOS technology. His research interests include the design and the metrological characterization of advanced CMOS sensors for biomedical applications, and the modeling of complex optical systems.



Lindsay Grant (M'03) received the degree in physics from St. Andrews University, Scotland.

He is a Pixel Technology Expert with STMicroelectronics with more than 25 years of experience in semiconductor R&D. Since 1999, he has worked on multiple generations of CMOS image sensor pixel and process technology from 5.6 to 1.1 μ m pitch, including TSV and BSI developments. Since 2006, his R&D interest has also covered embedded SPAD devices in CMOS. He has been a member of the steering committee for two European-funded

programs in SPAD development. He has authored or coauthored more than 40 technical papers and conference presentations and has been an invited speaker on imaging technology at the ISSCC Forum on Image Sensors, at the Fraunhofer IMS Workshop, and at ESSDERC. Currently, he manages a team working on pixel characterization, runs a program of sponsored Ph.D. studentships, and is a Director of STMicroelectronics R&D, UK Ltd.

Mr. Grant sits on the Technical Program Committee for IISW since 2009 and has cochaired the Image Sensors Europe Conference, London, U.K., since 2008.



Robert K. Henderson (M'84) received the Ph.D. degree from the University of Glasgow, Glasgow, U.K., in 1990.

He is a Reader with the School of Engineering, Institute for Microelectronics and Nanosystems, University of Edinburgh, Edinburgh, Scotland. From 1991, he was a Research Engineer with the Swiss Centre for Microelectronics, Neuchatel, Switzerland, working on low-power sigma-delta ADCs and DACs for portable electronic systems. In 1996, he was appointed a Senior VLSI Engineer with VLSI Vision

Ltd., Edinburgh, U.K., where he worked on the world's first single-chip video camera and was a Project Leader for numerous other CMOS image sensors. From 2000, as principal VLSI engineer in ST Microelectronics Imaging Division he designed some of the first image sensors for mobile phones. He joined Edinburgh University in 2005 to pursue his research interests in CMOS integrated circuit design, imaging and biosensors. He is the author of 113 papers and 17 patents.

Dr. Henderson was the recipient of Best Paper Award at the 1996 European Solid-State Circuits Conference as well as the 1990 IEE J. J. Thomson Premium.



Leo H. C. Braga (S'09) received the B.Sc. degree in electronic and computer engineering (*cum laude*) and M.S. degree in electrical engineering from the Federal University of Rio de Janeiro (UFRJ), Rio de Janeiro, Brazil, in 2008 and 2009, respectively, and the Second Level Master degree in nano and micro systems from the University of Trento, Trento, Italy, in 2010, where he is currently working toward the Ph.D. degree in electronics in partnership with Fondazione Bruno Kessler (FBK).

His thesis topic is CMOS photodetectors for positron emission tomography (PET), while his more broad research interests include image sensors, mixed-signal circuit design, and system architectures.



Nicola Massari (M'08) received the Laurea degree in electronic engineering from the University of Padova, Padova, Italy.

Since 2000, he has worked with FBK as a Researcher with the Optical Sensor and Interface Group, a fabless design center developing smart image sensors and sensor interfaces. His main interests are ultralow-power vision sensors with processing capability and special sensor architecture based on single-photon avalanche diodes.



Matteo Perenzoni (M'09) was born in Rovereto, Trento, Italy, in August 1977. He received the degree in electronic engineering from the University of Padua, Padua, Italy, in 2002 work on analog integrated circuit design.

In 2002, he worked with the University of Padua on the design of an integrated circuit implementing an analog channel decoder. Since January 2004, he has been with Fondazione Bruno Kessler (FBK, formerly ITC-IRST), Trento, Italy, as a Researcher working in the Smart Optical Sensors and Interfaces Group of

the Materials & Microsystems Area. He collaborates on teaching courses of electronics and sensors for the NanoMicro Master, Trento, Italy. His research interests are design of advanced vision sensors for X-ray, infrared and THz, modeling, and optimization of analog integrated circuits.

teaching courses of analog electronics and microelectronics as a member of the Telecommunications Engineering faculty of the University of Trento, Trento, Italy. His research interests are mainly in the field of CMOS integrated circuit design, image sensors and biosensors. He has authored or coauthored more than 100 papers in international journals and presentations at international conferences and holds several patents in the field of image sensors.

Dr. Stoppa was the recipient of the 2006 European Solid-State Circuits Conference Best Paper Award. Since 2011, he has served as a program committee member of the International Solid-State Circuits Conference and the SPIE Videometrics, Range Imaging and Applications Conference and was a technical committee member of the International Image Sensors Workshop in 2009 and 2013.



David Stoppa (M'97–SM'12) received the Laurea degree in electronics engineering from Politecnico of Milan, Milan, Italy, in 1998, and the Ph.D. degree in microelectronics from the University of Trento, Trento, Italy, in 2002.

In 2010, he became Head of the Smart Optical Sensors and Interfaces research unit at Fondazione Bruno Kessler (FBK, formerly ITC-IRST), Trento, Italy, where he has been a Research Scientist since 2002, working on the development of CMOS sensors for advanced applications. Since 2000, he has been



imaging project.

Richard Walker (S'08–M'13) received the M.Eng. degree in electrical engineering and electronics and Ph.D. degree from the University of Edinburgh, Edinburgh, U.K., in 2007 and 2012, respectively.

His doctoral research focused on time-correlated imaging for 3-D and bio-imaging applications in collaboration with the Imaging Division of STMicroelectronics. He is now a Post-Doctoral Research Fellow with the University of Edinburgh, Edinburgh, U.K., as a Sensor Designer working on the EC FP7-funded SPADnet CMOS-PET medical