A Sub-Harmonic Injection-Locked Quadrature Frequency Synthesizer With Frequency Calibration Scheme for Millimeter-Wave TDD Transceivers

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***Abstract*—This paper proposes a sub-harmonic injection-locked frequency synthesizer with frequency calibration scheme for millimeter-wave Time-division Duplexing (TDD) transceivers. The proposed synthesizer is capable of supporting all 60 GHz channels (58.1–65 GHz) including channel-bonding defined by 60 GHz wireless standards for short-range high-speed wireless communications. In order to guarantee a robust performance over process-voltage-temperature (PVT) variations of the conventional frequency synthesizer, a frequency calibration scheme is proposed to automatically correct a frequency drift of quadrature injection locked oscillators. Implemented by a 65 nm CMOS process, the frequency synthesizer achieves a typical phase noise of −117 dBc/Hz @ 10 MHz offset from a carrier frequency of 61.56 GHz while consuming 72 mW from a 1.2 V supply. The calibration system consumes 65 mW additionally.**

***Index Terms*—Channel bonding, CMOS, frequency calibration, injection locking, millimeter-wave, PLL, PVT, sub-harmonic, synthesizer, TDD, 60 GHz.**

I. Introduction

THE unlicensed bandwidth between 57 and 66 GHz is released for broadband short-distance communications. As it is known, this is the widest portion of radio-frequency spectrum ever allocated in an exclusive way for wireless unlicensed application which allows multi-gigabit-per-second wireless communications [1]–[7]. Moreover, significant advancements in CMOS technology permit one to consider utilizing the 60 GHz band for high data rate applications including short range, wireless transmission.

There are already several standards for 60 GHz wireless communication, including IEEE 802.15.3c [8], IEEE 802.11ad [9], ECMA-387 [10], WirelessHD [11] and WiGig (Wireless Gigabit Alliance) [12]. Each is formed by a different community of potential users of technology. For example, IEEE802.11ad is one of standards for implementing WLAN computer communication for Gb/s speed utilizing 60 GHz frequency band, and WirelessHD and ECMA are developed to for streaming high-definition content between source and display devices. Most of the standards are focusing on very high speed communication (1–5 Gb/s) to enable wireless HDMI replacement.

Even though different standards are needed for different applications, an ability to operate across different standards is more preferable. These standards define 4 bands centered at 58.32 GHz/60.48 GHz/62.64 GHz/64.8 GHz, and ECMA-387 additionally defines channel-bonding bands centered at 59.4 GHz/61.56 GHz/63.72 GHz for higher data rates and more efficient constellations. In order to be compliant with these standards, mm-wave frequency synthesizers are required to generate each of these carrier frequencies. Moreover, as systems move away from single-carrier modulation and adopt more complex schemes, the design of mm-wave frequency synthesizers with quadrature output will become increasingly challenging.

Recently, for 60-GHz wireless communication system, the authors in [13] propose a 60 GHz PLL using a QVCO oscillating at the fundamental frequency. Another PLL with push-push VCO followed by a hybrid coupler [5] is published. In [14], a PLL with a sub-harmonic VCO which is used to inject a sub-harmonics quadrature Injection Locked Oscillator (ILO) [15], [16] is proposed. Among these publications, PLL using sub-harmonics quadrature ILO is preferred due to the best phase noise performance at 60 GHz. As shown in Fig. 1, a sub-harmonic injection-locked quadrature frequency synthesizer is used to generate these carrier frequencies for a direct-conversion TDD transceiver. However, due to inaccurate active/passive device modeling at mm-wave frequency band, it is difficult to guarantee the proper operation of the 60 GHz ILO, especially including PVT variations. The typical locking range of QILO is only several hundred MHz. As a result, a small shift of free-running frequency caused by PVT variations can lead the QILO unable to lock to the input signal. In addition, the undesired free-running frequency drift also causes considerable I/Q mismatch [14]. Therefore, a calibration scheme is needed to tune the free-running frequency of QILO for robustness of its operation and small I/Q mismatch in various conditions.

A conventional calibration technique [13], [17], which is operated only at start-up, cannot track ILO frequency drift as temperature varies, thus, another method, which would automatically correct frequency drift by frequency feedback, is

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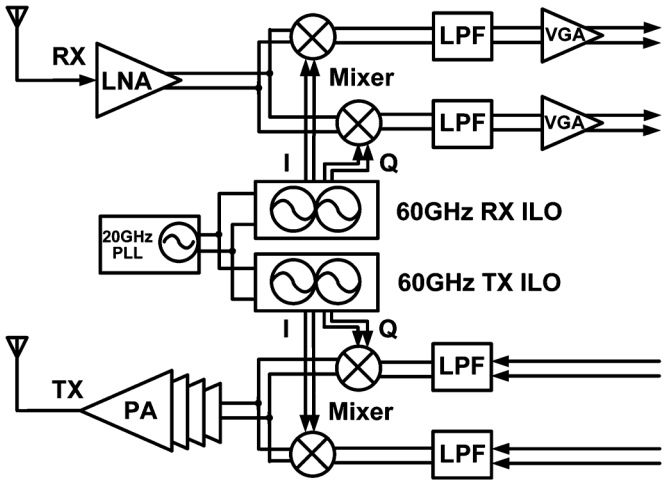

Fig. 1. Diagram of a 60 GHz direct conversion TDD transceiver using a sub-harmonic injection-locked quadrature frequency synthesizer.

needed inevitably. In this paper, a 60 GHz frequency synthesizer with frequency calibration scheme [18] is proposed for millimeter-wave TDD transceivers. The proposed frequency synthesizer operates for a wide frequency range from 58.1 to 65.0 GHz, which supports all 60 GHz channels defined by the 60 GHz wireless communication standards. This paper is organized as follows. In Section II, a calibration scheme for a 60 GHz frequency synthesizer is introduced. The following section describes the circuit implementation in details. Section IV demonstrates experimental results of the proposed 60 GHz frequency synthesizer. Finally, a conclusion is summarized in Section V.

II. Calibration Scheme for 60 GHz Synthesizer

A. Calibration Operation and Timing Between TDD Transceivers

A typical millimeter-wave TDD transceiver is composed of a transmitter (TX) and a receiver (RX) which has separate 60 GHz ILOs for their own operation as shown in Fig. 1. It is noted that the TX and the RX operate in different time slots, thus, the calibration of the 60 GHz ILO for the TX can be performed during RX time slots, and the calibration of the 60 GHz ILO for the RX can be performed during TX time slots. Fig. 2 shows the calibration operation and timing between TDD transceivers. If a transceiver A (TRX A) is transferring data stream to a transceiver B (TRX B), the data stream is divided into small packets. After the first packet is transmitted to the TRX B, an acknowledged packet will be transmitted from the TRX B back to the TRX A to confirm that the first packet was received successfully. The TRX A will wait until the acknowledged packet is received completely before starting to transfer the next packet. In this case, the most crucial part of timing that poses a time restriction for calibration occurs when an acknowledged packet is being sent and received from TRX B and TRX A respectively. Typically this length of time is composed of two shortest inter-frame spaces (SIFS) and one ACK packet length, which is limited to several μs. For example, in IEEE 802.11ad, the SIFS length is 3 μs and ACK length including preamble is 1.2 μs, thus the maximum available duration for ILO calibration is limited to

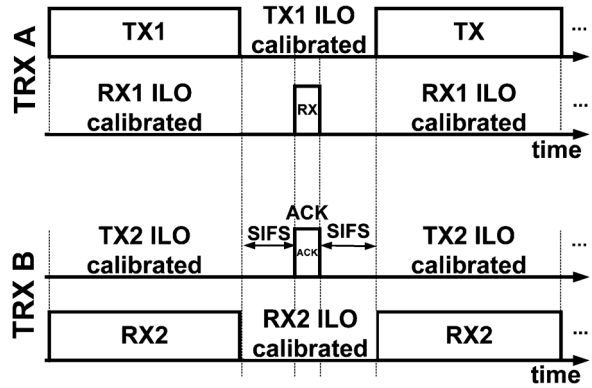

Fig. 2. Calibration operation and timing between TDD transceivers.

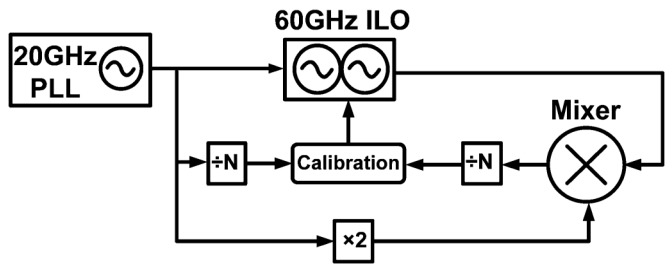

Fig. 3. Conceptual diagram of the 60 GHz frequency synthesizer with the proposed frequency calibration scheme.

7.2 μs. Such a short interval imposes a strict requirement for the calibration time of the 60 GHz ILO. Fortunately, noted that TDD systems allow foreground calibration, it is feasible to calibrate the ILO frequency to the target frequency initially. Next, considering the fact that the ILO frequency drift caused by component aging and environmental changes is usually a gradual and slow process (compared to the time duration of μs level), a small frequency drift can be corrected easily within several calibration steps, which relaxes the severe requirement for the calibration time. Meanwhile, it is possible to monitor the frequency drift at regular intervals, which helps to reduce the overall power consumption.

B. Proposed Calibration Scheme

Fig. 3 shows a simplified diagram of the proposed synthesizer with the frequency calibration scheme. For the adoption of a down converting mixer, the 20 GHz PLL can be used as a reference for mixing 60 GHz output to lower frequency. However, directly mixing 20 GHz signal with 60 GHz signal is not feasible since the IF output frequency still requires a 40 GHz divider. Therefore, a better solution is to use a doubler or push-push amplifier to utilize the second harmonic of 20 GHz PLL to mix with the output of the ILO. Thereby, the output of mixer will be around 20 GHz where we can use dividers chain for further digital comparison.

The process of calibration is carried out when the 20 GHz PLL is locked. At the initial state or during TX time slots, the ILO for RX outputs its free-running frequency, and the output of ILO for RX is down-converted to a frequency around 20 GHz by a mixer, through doubling of the 20 GHz PLL injection signal. After two separate divider chains, the frequency coming from the output of mixer and the 20 GHz PLL are compared using

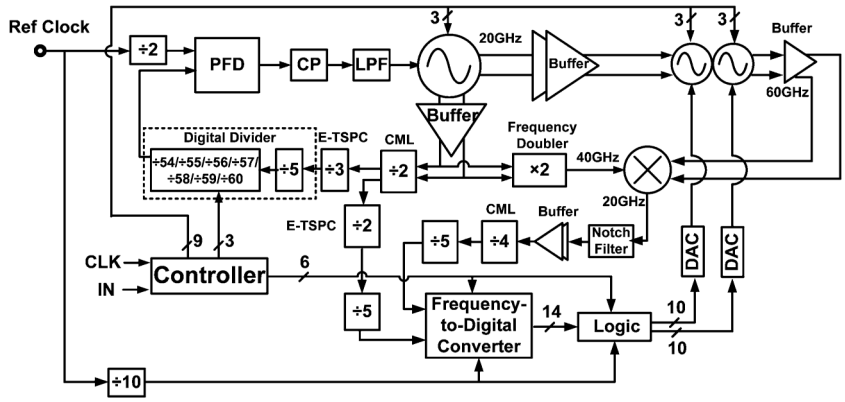

Fig. 4. Block diagram of the proposed 60 GHz frequency synthesizer with frequency calibration.

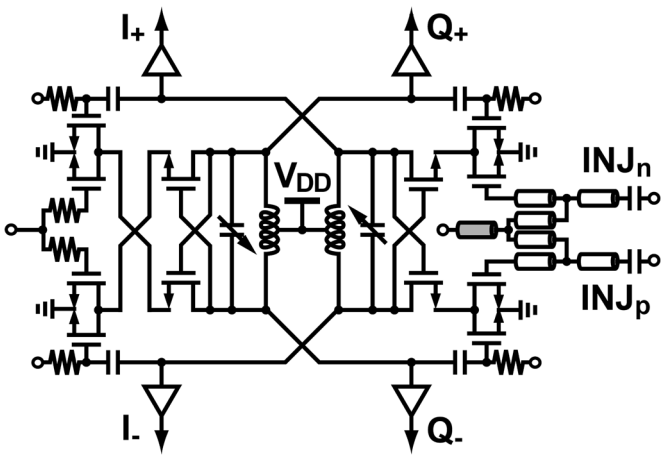

Fig. 5. Circuit schematic of the quadrature ILO.

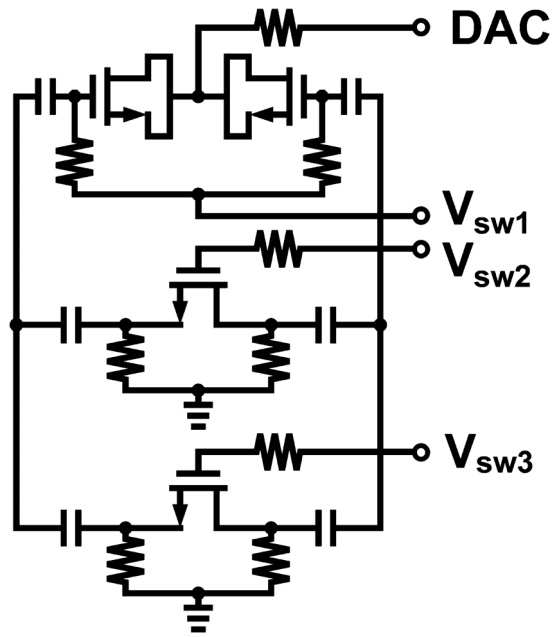

Fig. 6. Circuit schematic of the variable capacitor part.

digital calibration circuits. The output of digital calibration circuit directly controls the digital code for a digital-to-analog converter, giving rise to adjust the ILO free running frequency. After several reference cycles, the 60 GHz ILO free-running frequency is close to 3 times the 20 GHz PLL output.

III. 60 GHz Synthesizer Topology

The proposed 60 GHz frequency synthesizer mainly consists of a 20 GHz PLL, a 60 GHz quadrature ILO, a frequency down-converting circuit, and a digital calibration circuit. The block diagram of proposed 60 GHz synthesizer is depicted in Fig. 4.

A. 20 GHz PLL

The 20 GHz PLL consists of a phase-frequency detector (PFD), a current-steering charge pump, a 2nd-order on-chip low pass filter, an LC-VCO with a tuning range of 17.9-to-21.7 GHz, followed by a divide-by-2 CML divider, an divide-by-3 E-TSPC divider, a digital divide-by-5 divider, and a digital multi-modulus divider. The whole divide ratio can be controlled from 1620 to 1800 in steps of 30. This divide ratio combing with a 12 MHz frequency resulting from a halved off-chip 24 MHz reference enables synthesis of the required tones.

B. 60 GHz ILO

The circuit schematic of 60 GHz ILO is shown in Fig. 5. A quadrature 60 GHz LO signal can be obtained due to a quadrature I/Q configuration. The free-running frequency can be adjusted by a switched capacitor bank for coarse tuning, and a varactor which is controlled by the calibration circuit for fine tuning. The 20 GHz PLL signal is injected through the tail transistor of I oscillator. Fig. 6 shows the circuit schematic of the variable capacitor part, which consists of a MOS varactor providing continuous and fine tuning ability, and switched capacitor array allowing discrete and coarse tuning steps. By tuning QILO to be at the center of the locking range, the output I/Q mismatch can be minimized. However, as the free-running frequency of QILO shifts from being 3 times the injected frequency, a considerable I/Q mismatch will be occurred [14]. A simulated sensitivity of I/Q phase error as a function of control voltage of a varactor in the QILO is approximated to be 0.6 degree/mV [14]. This demonstrates the necessity of the ILO frequency calibration.

C. Down-Converting System

The down-converting system is composed of a frequency doubler, a mixer, and two notch filters. There are mainly two design considerations for the down-converting system. First of all, the occupied chip area should be minimized for low cost.

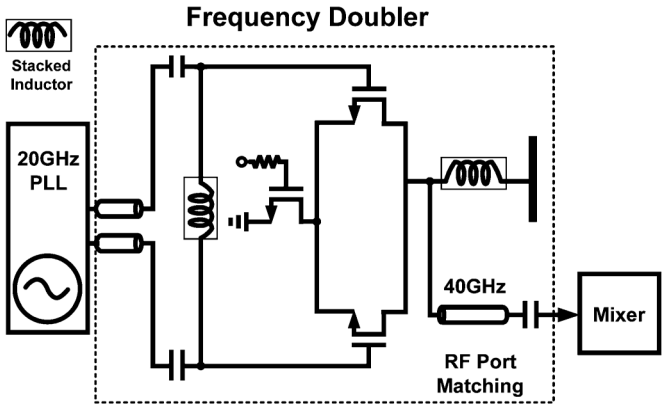

Fig. 7. Circuit schematic of the frequency doubler, along with other building blocks.

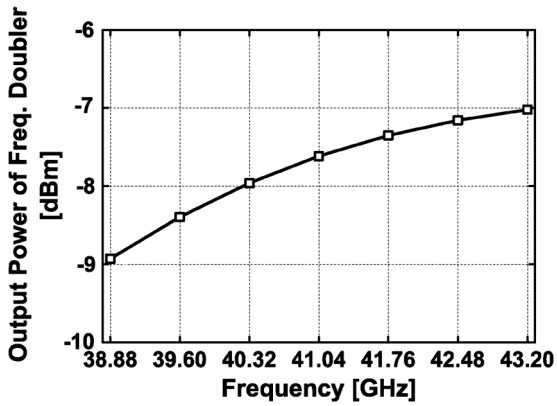

Fig. 8. Simulated output power of the frequency doubler.

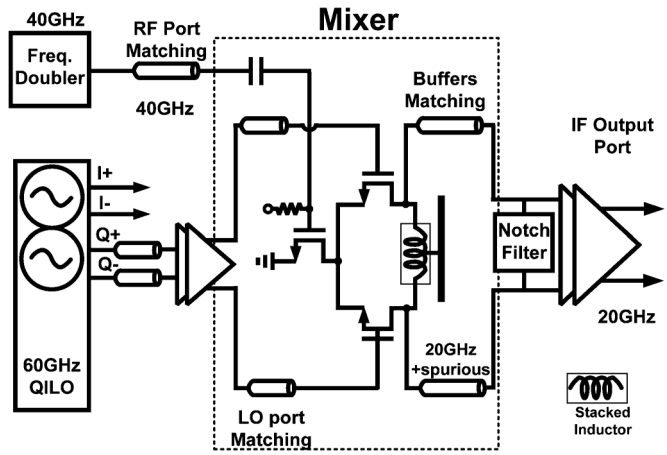

Fig. 9. Circuit schematic of SSB mixer, along with other building blocks.

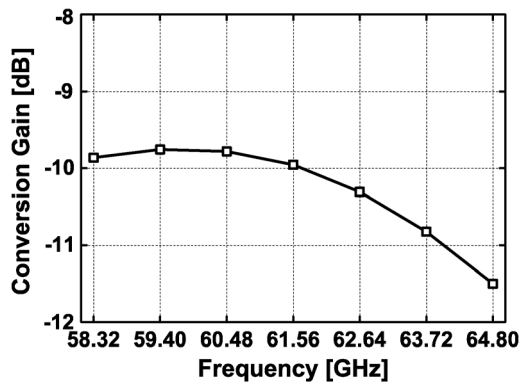

Fig. 10. Simulated conversion gain of the single-balanced mixer.

Considering building blocks for the down-converting system are operated in the millimeter-wave regime, on-chip impedance match and inductive peaking are necessary to improve the gain and output power of active circuits. In this work, miniaturized transmission line and custom-designed inductors help to reduce the whole chip area. Secondly, a sufficient large output power is critical to driving the following divider stage. In this section, detailed circuit implementations together with their simulation results are introduced.

1) Frequency Doubler: The frequency doubler operates as a push-push amplifier which combines 2 phases with 180 degrees phase shift by combining output nodes. As a result, odd harmonics components are cancelled out and the second harmonic component survives. In this implementation, a simple differential amplifier is used as shown in Fig. 7, where output nodes are shorted. Even though the output signal is single-ended, it is enough to carry frequency information for calibration. In order to transfer maximum power to load, the input impedance of this frequency doubler is matched to the output impedance of 20 GHz PLL buffers at 50 Ω. This is done by the use of transmission line, and a custom-designed stacked inductor. The size of differential pair also affects the output amplitude. In this case, the width of transistors is chosen as 2×20 μm. Another stacked inductor is utilized at the output node to peak at high frequency. Meanwhile, the transmission line is utilized to match output node to RF port of the next-stage mixer.

With 0 dBm input power from 20 GHz PLL, the simulated output power of the frequency multiplier is shown in Fig. 8. The output power varies from about -9 dBm to -7 dBm over the output frequency range from 38.88 GHz to 43.2 GHz.

2) Mixer: A double-balanced mixer is widely used due to its excellent port-to-port isolations while maintain reasonable conversion gain and noise performance. However, it requires differential RF inputs which would further complicate the topology of a frequency doubler or an additional Balun might be needed. In this work, the mixer is designed using a single-balanced topology which mixes the single-ended RF output from the frequency doubler at frequency around 40 GHz, with the differential LO output signal from the ILO at frequency around 60 GHz. The detailed schematic of the single-balanced mixer with other building circuits is shown in Fig. 9.

As mentioned earlier, a combination of stacked inductor at output node of the frequency doubler and transmission line is utilized to match the input impedance of RF port at the frequency of around 40 GHz. On the other hand, for matching the LO port, only transmission line is utilized since it is for higher frequency of 60 GHz. Another stacked inductor is used for the mixer core. The stacked inductor and transmission line are designed to match the impedance of notch filter and input impedance of buffers at the frequency around 20 GHz which maintain 20 GHz signals and attenuates 60 GHz LO feed-through and other spurious signals. The size of differential pair is chosen at 2×10 μm and the size of tail transistor is chosen as 2×26 μm. As shown in Fig. 10, the simulated power

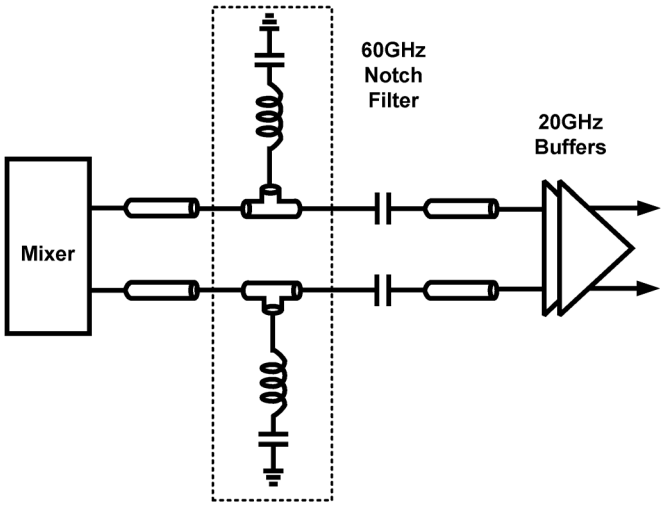

Fig. 11. Schematic of the notch filter, along with other building blocks.

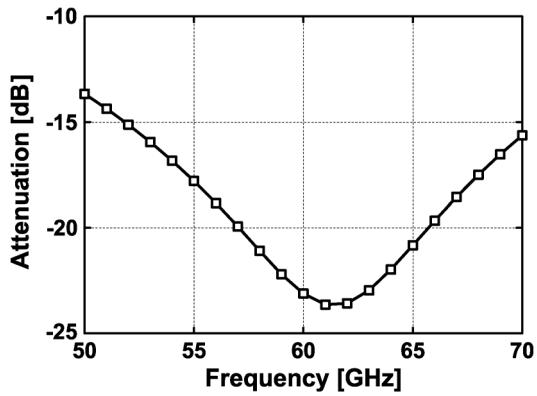

Fig. 12. Simulated attenuation of the notch filter.

conversion gain varies from −9.7 to −11.5 dB over the range of frequency from 58.32 to 64.8 GHz.

3) Notch Filter: Output signals of the mixer carry a 20 GHz output signal and undesirable signals caused by a strong LO input power. Thus, a passive *LC* band-rejection filter is implemented to attenuate the LO feed-through signal as shown in Fig. 11. The inductor used in this filter is custom-designed with an inductance of 92 pH and a quality factor of 9. The capacitor is chosen as 75 fF. The resultant attenuation of this notch filter is shown in Fig. 12. It shows an attenuation of about −20 dB at the frequency around 60 GHz to reduce the LO feed-through signal.

4) Transmission Line: Transmission line is mainly adopted for impedance match since it benefits from low loss. However, this method proves to be area intensive. As can be seen in [1], considerable chip area is occupied by matching blocks using a transmission line with a 10 μm signal line width. In order to reduce the chip area, a 6 μm-width transmission is utilized for designing match blocks in this work [2]. Fig. 13 shows a top and cross-sectional view of the guided micro-strip line. It has a 6 μm signal-line width and a 7-μm gap between the signal and ground line. The distance between the side grounds is 20 μm.

For an accurate device modeling, a careful de-embedding method has been carried out to remove the parasitics of the pad and interconnection. Fig. 14 shows the modeled and measured

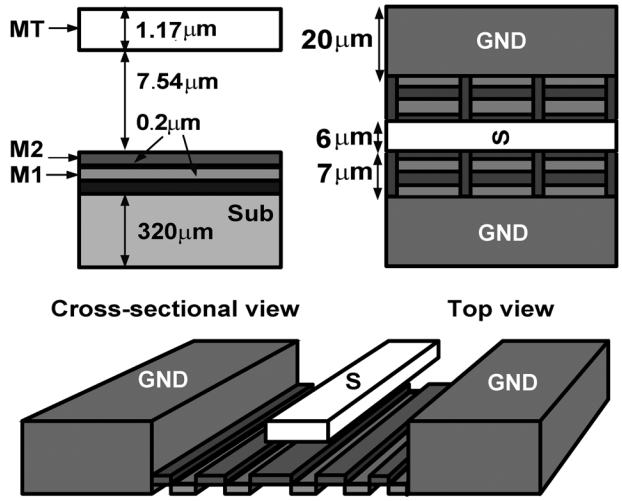

Fig. 13. Structure of the transmission line.

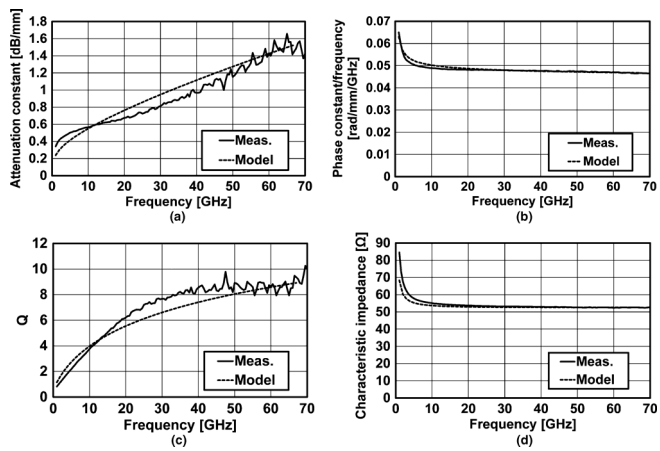

Fig. 14. Modeling results of (a) attenuation constant, (b) phase constant/frequency, (c) Q, and (d) characteristic impedance.

results including attenuation constant, phase constant, quality factor and characteristics impedance, of the transmission line adopted in this work. Measured and modeled results were calculated from S-parameter in measurement and HFSS simulation, respectively. A careful simulation for impedance matching between input and output ports of different blocks, e.g., RF and LO input ports and output port of mixer, has been carried out using an accurate transmission line model. The detailed length of transmission line of impedance matching is shown in Fig. 15.

5) Summary: The full down-conversion system is composed of three main blocks as discussed in details in the previous sub-chapters. The input impedance of the frequency doubler is designed to match the output impedance of PLL buffers through the use of transmission line and a stacked inductor. The single-ended output of the frequency doubler feeds to the RF port of the mixer. The matching between two ports is also done with the use of transmission line. The differential LO signals is input to one-stage buffers before input the LO ports of the mixer. The LO feed-through at the output of the mixer is filtered out by a notch filter. The output at frequency around 20 GHz is amplified by two-staged buffers. Then, it is divided to lower frequency by a divider chain and compare with the reference signal from the 20 GHz PLL.

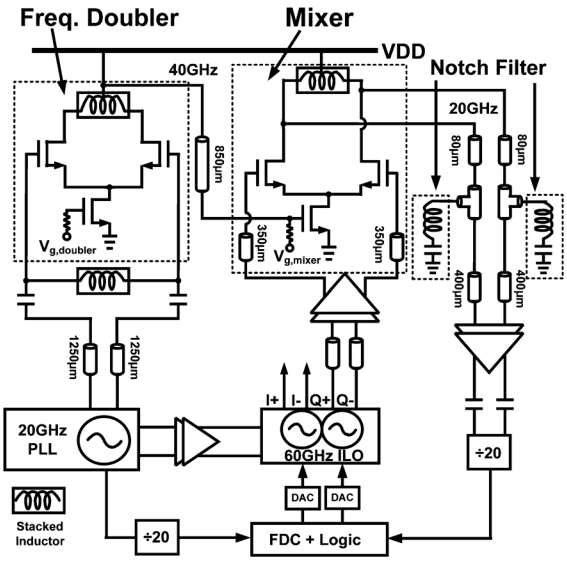

Fig. 15. Full schematic of down-converting circuits, along with other building blocks.

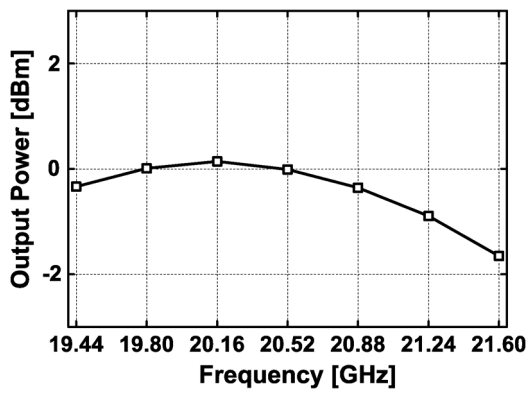

Fig. 16. Simulated output power of the down-conversion system.

The amplitude of output signals from the mixer carrying the 20 GHz output frequency is enhanced by two-stage buffers which are also designed using stacked inductors for gain peaking. From simulation, under a normal case of having 0 dBm input power from the 20 GHz PLL and −10 dBm input from the ILO, the output power over the range of frequency around 20 GHz is shown in Fig. 16. The output power varies from −1.7 to 0.14 dBm in the range of frequency from 19.44 to 21.6 GHz. The strongest spurious frequency is lower than −21 dBm at the frequency around 60 GHz. These output power levels are high enough to drive the next-stage dividers for digital calibration. Simulation results indicate that the calibration system introduces negligible phase noise degradation.

D. Digital Calibration Circuit

The digital calibration circuit consists of a frequency-to-digital converter, and digital logics. In order to increase the frequency resolution, digital calibration circuits are triggered at 1/10 of the reference clock. Derivative frequency signals coming from the 60 GHz ILO and 20 GHz PLL are measured using digital counters, respectively. Outputs of the digital counters, in the form of binary numbers, are compared in the following logic circuit during each reference cycle for digital circuits. The output of logic circuit directly controls the code

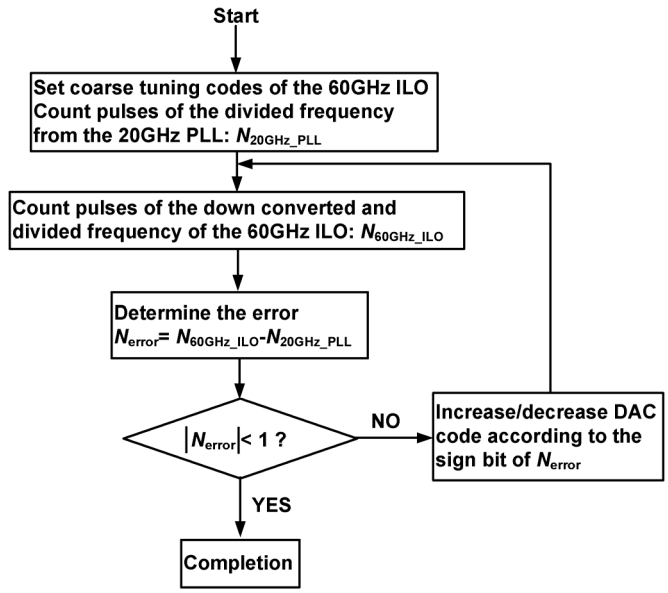

Fig. 17. Flow chart of the ILO frequency calibration process.

for DAC, giving rise to adjust the ILO free-running frequency. If the derivative frequency coming from the 60 GHz ILO is greater than that coming from the 20 GHz PLL, the output code of digital logic circuit is decremented to speed down the 60 GHz ILO free-running frequency. Similarity, if the derivative frequency coming from the 60 GHz ILO is less than that coming from the 20 GHz PLL, the output code of digital logic circuit is incremented to speed up the 60 GHz ILO free-running frequency. The flowchart of the above ILO frequency calibration procedure is summarized in Fig. 17, where $N_{20\ \mathrm{GHz\_PLL}}$ is the number of pulses of the divided frequency from 20 GHz PLL, $N_{60\ \mathrm{GHz\_ILO}}$ is the number of pulses of the down converted frequency from 60 GHz ILO, and N_{error} is the difference in the number of pulses between down-converted signals from 20 GHz PLL and 60 GHz ILO.

A possible calibration algorithm is outlined as follows. It is noted that TDD system allows foreground calibration. Thus, the entire calibration procedure can be divided into initial and intermittent calibration. Initially, ILO free-running frequencies are measured in the foreground by down-converting system and all-digital calibration circuits, and digital DAC codes representing the information of each frequency band (e.g., 58.32 GHz, 61.56 GHz, etc.) can be stored in a memory. Thus, process variation can be calibrated during initial calibration. When millimeter-wave transceivers operate in TDD mode, the calibration system can monitor ILO free-running frequency drift mainly caused by temperature variation. In a short interval of time duration, the ILO free-running frequency shift is regarded as gradual and subtle changes. As a result, such a small frequency drift can be corrected easily within several calibration steps.

In order to demonstrate the feasibility of the proposed method, the initial and intermittent calibration is implemented in this design. However, the memory for the store and recall of the DAC and capacitor bank codes is not implemented in this design, and only one state can be recorded for the intermittent operation. The detail of calibration algorithm is shown in

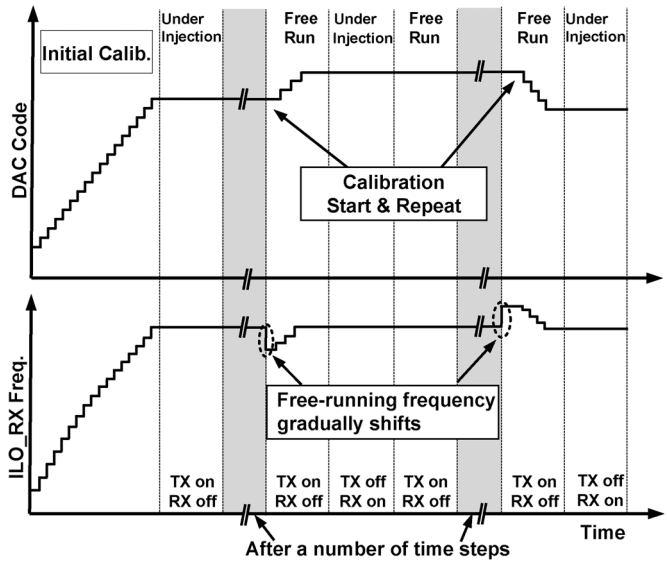

Fig. 18. DAC code and output frequency of ILO for RX against time.

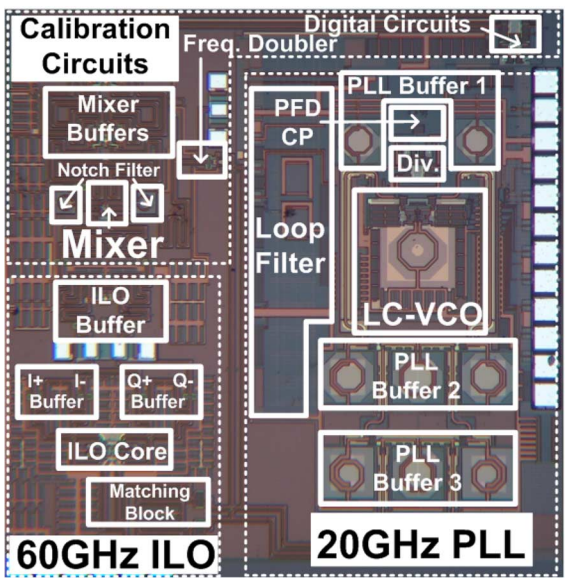

Fig. 19. Chip microphotograph.

Fig. 18. After presenting the capacitor bank codes for coarse tuning, the calibration loop will calibrate the free-running frequency of the ILO for RX to the desired frequency and monitor the ILO free-running frequency drift at regular intervals afterwards. As a result, the proposed calibration system can always adjust the ILO free-running frequency as environment changes to be at the middle of the locking range at the target frequency band.

IV. Experimental Results

The proposed 60 GHz frequency synthesizer is implemented in a standard 65 nm CMOS process. The microphotograph of the fabricated synthesizer is shown in Fig. 19. The total chip area is 1.9 mm × 2 mm. PLL spectrum is measured with an Agilent E4448A PSA spectrum analyzer and a 50-to-75 GHz external mixer. The phase noise is evaluated using an Agilent E5052B SSA signal source analyzer and a 50-to-75 GHz external mixer.

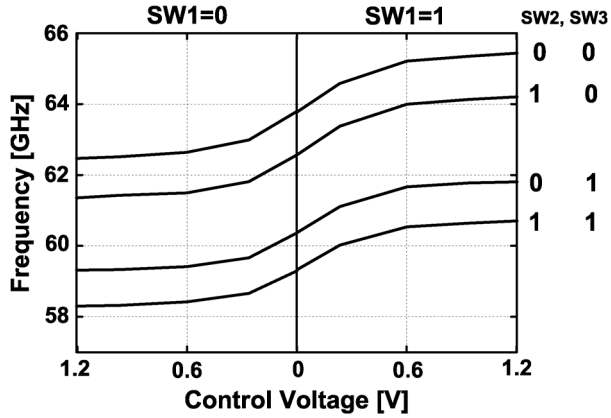

Fig. 20. Measured free-running frequency range of the ILO TEG.

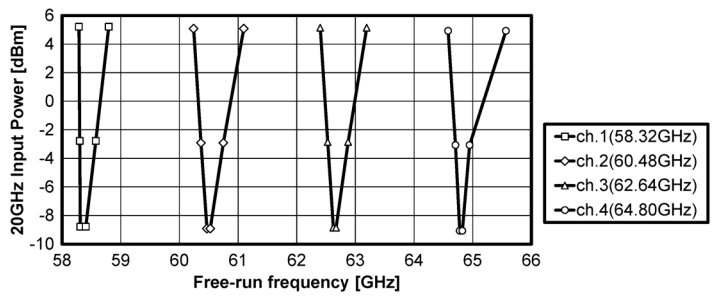

Fig. 21. Measured locking range of the quadrature ILO at centered frequency of each channel.

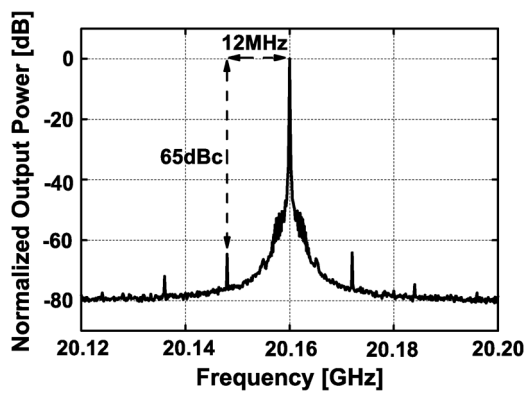

Fig. 22. Measured spectrum at 20.16 GHz.

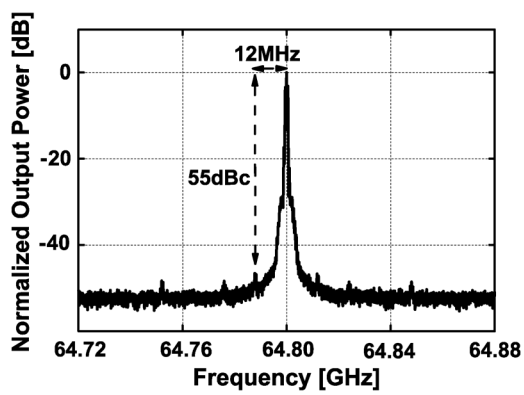

Fig. 23. Measured spectrum at 64.80 GHz.

In order to assist the evaluation of 60 GHz frequency synthesizer, a 60 GHz ILO TEG chip is also fabricated on the same

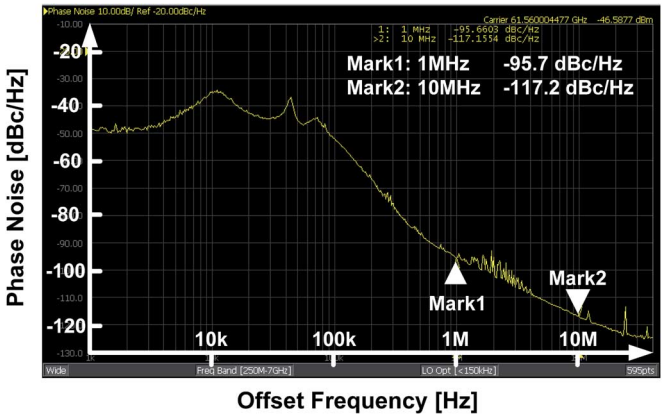

Fig. 24. Measured phase noise at a carrier of 61.56 GHz.

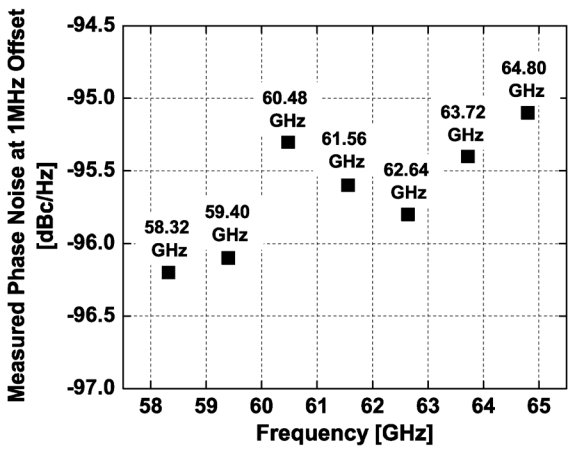

Fig. 25. Measured phase noise performance across the entire frequency band.

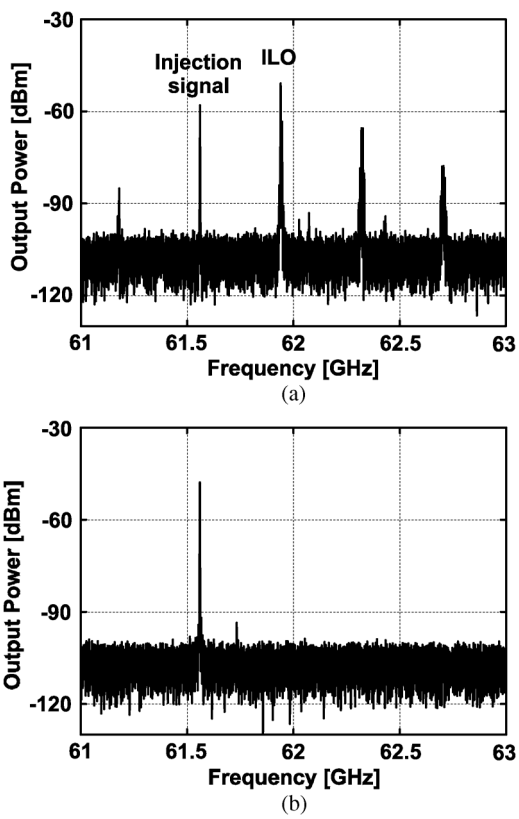

Fig. 26. Measured 60 GHz output spectrum when (a) disabling the calibration and (b) enabling the calibration.

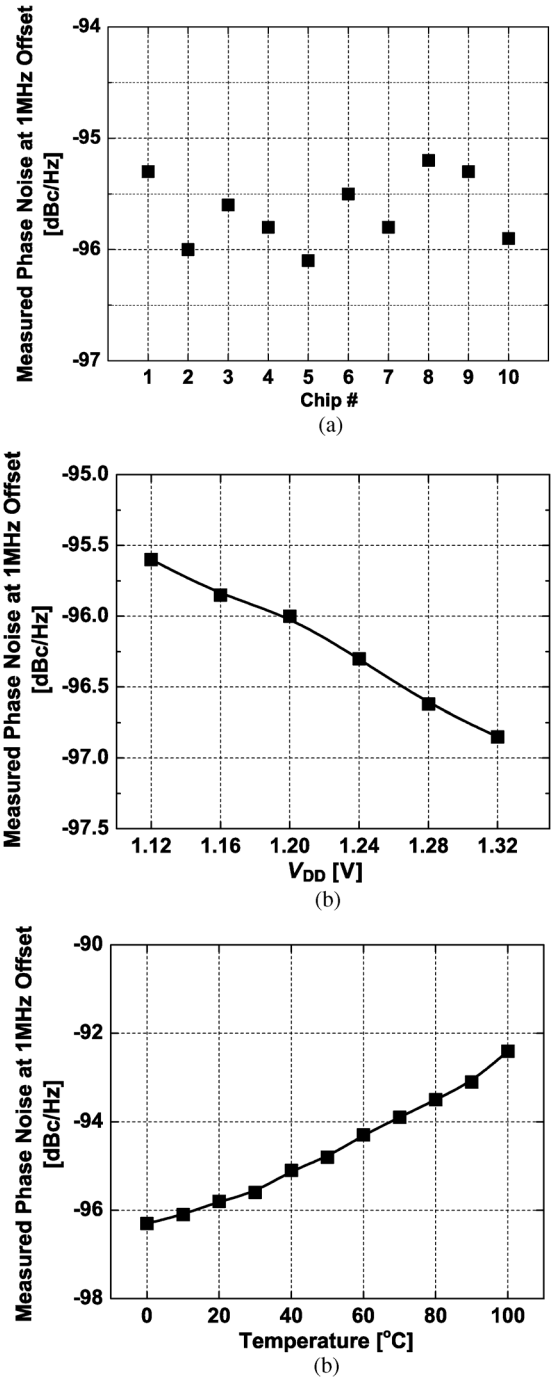

Fig. 27. Measured phase noise characteristics (a) from 10 samples, (b) as a function of power supply, and (c) over temperature, at a carrier frequency of 62.64 GHz.

die. As shown in Fig. 20, the measured ILO free-running frequency range is 58.3 GHz–65.4 GHz, and is covered with sufficient overlap between neighboring bands. The resulting frequency tuning range can cover all 60 GHz bands. Even though the free-running frequency of ILO in the complete frequency synthesizer is slightly dropped due to undesired parasitic capacitances, the measured tuning range of 58.1 GHz–65.0 GHz is still sufficient to cover all 60 GHz bands. As shown in Fig. 21, the measurement results indicate that the ILO has a locking range of about 180–380 MHz at 60 GHz bands, when the input power less than -2 dBm.

TABLE I
PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART 60 GHz CMOS PLLs/VCOs

	[13] PLL	[5] PLL	[14] PLL	[2] PLL	[19] PLL	[20] VCO	[21] PLL	This work PLL
Feature	QVCO @60GHz	Push-push VCO @30GHz + Coupler	Sub-harmonic Injection	Sub-harmonic Injection	Diff. VCO @60GHz	Mag. Coupled	VCO @ 48GHz	Sub-harmonic Injection + Frequency Calibration
CMOS Tech [nm]	45	90	65	65	90	65	65	65
f_{ref} [MHz]	100	203.2	36	36	60	-	54	24
Frequency [GHz]	57-66	59.4-64	58-63	58 - 64.8	61-63	56-60.35	42.1 - 53	58.1-65.0
Phase Noise [dBc/MHz]	-75@1	-73@1 -112@10	-96@1 -113@10	-95@1	-80@1 -110@10	-95@1 -117@10	[1]-95.6@1	-96@1 -117@10
Power [mW]	78	76	80	68	78	22	72	137 (Initial only) 72
Output type	Quad.	Quad.	Quad.	Quad.	Diff.	Quad.	Diff.	Quad.
Voltage/ Temperature Tracking	No	-	No	No	No	-	No	**Yes**
Channel bonding supporting	No	No	No	No	No	-	No	**Yes**
60GHz band coverage	All 4 Bands	3 Bands	3 Bands	All 4 Bands	1 Band	2 Bands	All 4 Bands	All 4 Bands

[1] Normalized to 62.64 GHz from 50.112 GHz measurement.

When the frequency of input reference clock is 24 MHz, the synthesizer can generate all 60 GHz channel bands (including channel bonding): 58.32 GHz, 59.4 GHz, 60.48 GHz, 61.56 GHz, 62.64 GHz, 63.72 GHz, and 64.8 GHz, which are defined by current 60 GHz wireless standards. The frequency synthesizer consumes 72 mW from a 1.2 V power supply. If the intermittent operation is disabled, the calibration circuits including down-converting circuits and digital circuits consume 65 mW additionally.

The measured phase noise characteristic of the 20 GHz PLL is less than -105.6 dBc/Hz at 1 MHz offset across the entire frequency channel. The measured phase noise characteristic of the 60 GHz frequency synthesizer is less than -95 dBc/Hz at 1 MHz offset across the entire frequency channel. The measured reference spur level varies from -52 dBc to -70 dBc. The output spectrum at 20.16 GHz is graphed in Fig. 22 displaying the typical locked spectrum for the 20 GHz PLL. The graph demonstrates that the 12 MHz reference spur are kept 65 dB below the carrier frequency, showing good matching between charge pump currents. The output spectrum at 64.80 GHz is illustrated in Fig. 23 indicating the typical locked spectrum for the 60 GHz frequency synthesizer. As shown in Fig. 24, the typical measured phase noise is -95.6 dBc/Hz at 1 MHz offset, from a carrier frequency of 61.56 GHz. Fig. 25 shows the measured phase noise across the entire frequency band. It is worthwhile to mention that the phase noise of the 20-GHz PLL is -107 dBc/Hz at 1 MHz offset at 20.52 GHz. Theoretically, the phase noise should become 9.54 dB higher at the 60 GHz ILO output. Noted that the calibration system introduces negligible noise, the 2-dB degradation at 1 MHz offset is caused by a limited locking bandwidth. Due to the absence of on-chip I/Q mixers, an I/Q imbalance of this millimeter-wave frequency synthesizer cannot be accurately measured since any connectors and cables can further introduce significant delays.

Fig. 26 shows the 60 GHz output spectra disabling and enabling the calibration. As can be seen, without carrying out calibration the ILO free-running frequency is far from the third harmonic of the 20.52 GHz injected signal, causing failure of injection-locking operation. When enabling the calibration, the ILO free-running frequency is corrected to vicinity of 61.56 GHz, thus guaranteeing the injection-locking operation. The DAC signals were not brought off-chip and could not be measured. It is noted that the output power indicated in Fig. 24 do not account for losses from cables and an external 50-to-75 GHz down-conversion mixer. The calibrated output power is -8 dBm. Fig. 27 shows the measured phase noise characteristic in various PVT conditions at a carrier frequency of 62.64 GHz, which shows that the proposed circuit can be successfully calibrated for any PVT conditions. Fig. 27(a) shows the measured phase noise from 10 different chips. Fig. 27(b) shows the effect of a variation of supply voltage on measured phase noise. Fig. 27(c) shows the effect of temperature variation from 0–100° C on the measured phase noise performance.

Table I compares the present 60 GHz frequency synthesizers/VCOs with the state-of-art publications [2], [5], [13], [14], [19]–[21]. This work could cover all 60 GHz channels and demonstrates a very good phase noise performance with quadrature output phase. To the best knowledge of authors', it is the first 60 GHz frequency synthesizer with frequency calibration for TDD transceivers.

V. Conclusion

A 60 GHz frequency synthesizer with frequency calibration scheme which can support IEEE 802.15.3c, wirelessHD, IEEE 802.11ad, and ECMA-387 TX/RX front end is reported. A frequency calibration scheme is proposed to monitor the frequency drift caused by environmental variations. With carful design, the proposed synthesizer can be suited for millimeter-wave TDD transceivers.

Acknowledgment

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References

[1] K. Okada, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, N. Li, and S. Ito, "A 60 GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE 802.15. 3c," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2011, pp. 160–161.

[2] K. Okada, K. Kondou, M. Miyahara, M. Shinagawa, H. Asada, R. Minami, T. Yamaguchi, A. Musa, Y. Tsukui, Y. Asakura, S. Tamonoki, H. Yamagishi, Y. Hino, T. Sato, H. Sakaguchi, N. Shimasaki, T. Ito, Y. Takeuchi, N. Li, Q. Bu, R. Murakami, K. Bunsen, K. Matsushita, M. Noda, and A. Matsuzawa, "A full 4-channel 6.3 Gb/s 60 GHz direct-conversion transceiver with low-power analog and digital baseband circuitry," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2012, pp. 218–219.

[3] S. Emami, R. F. Wiser, E. Ali, M. G. Forbes, M. Q. Gordon, X. Guan, S. Lo, P. T. McElwee, J. Parker, and J. R. Tani, "A 60 GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2011, pp. 164–165.

[4] A. Siligaris, O. Richard, B. Martineau, C. Mounet, F. Chaix, R. Ferragut, C. Dehos, J. Lanteri, L. Dussopt, and S. D. Yamamoto, "A 65 nm CMOS fully integrated transceiver module for 60 GHz wireless HD applications," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2011, pp. 162–163.

[5] C. Marcu, D. Chowdhury, C. Thakkar, J. D. Park, L. K. Kong, M. Tabesh, Y. Wang, B. Afshar, A. Gupta, and A. Arbabian, "A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry," *IEEE J. Solid-State Circuits*, vol. 44, pp. 3434–3447, Dec. 2009.

[6] G. M. V. Vidojkovic, K. Khalaf, V. Szortyka, K. Vaesen, W. V. Thillo, B. Parvais, M. Libois, S. Thijs, J. R. Long, C. Soens, and P. Wambacq, "A low-power 57-to-66 GHz transceiver in 40 nm LP CMOS with −17 dB EVM at 7 gb/s," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2012, pp. 268–269.

[7] T. Tsukizawa, N. S. Hirakata, T. Morita, K. Takana, J. Sato, Y. Morishita, M. Kanemaru, R. Kitamura, T. Shima, T. Nakatani, K. Miyanaga, T. Urushihara, H. Yoshikawa, T. Sakamoto, H. Motozuka, Y. Shirakawa, N. Yosoku, A. Yamamoto, R. Shiozaki, and N. Saito, "A fully integrated 60 GHz CMOS transceiver chipset based WiGig/IEEE802.11ad with build-in self calibration for mobile applications," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2013, pp. 230–231.

[8] *802.15.3c-2009*, IEEE Std., Oct. 2009 [Online]. Available: http://standards.ieee.org/getieee802/download/802.15.3c-2009.pdf

[9] *IEEE802.11ad*, IEEE Std. [Online]. Available: http://standards.ieee.org/develop/project/802.11ad.html

[10] ECMA [Online]. Available: http://www.ecma-international.org/publications/files/ECMA-ST/ECMA-387.pdf

[11] WirelessHD. [Online]. Available: http://www.wirelesshd.org/pdfs/WirelessHD-Specification-Overview-v1.1May2010.pdf

[12] WiGig. [Online]. Available: http://wirelessgigabitalliance.org/specifications/

[13] K. Scheir, G. Vandersteen, Y. Rolain, and P. Wambacq, "A 57-to-66 GHz quadrature PLL in 45 nm digital CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2009, pp. 494–495.

[14] A. Musa, R. Murakami, T. Sato, W. Chaivipas, K. Okada, and A. Matsuzawa, "A low phase noise quadrature injection locked frequency synthesizer for MM-wave applications," *IEEE J. Solid-State Circuits*, vol. 46, pp. 2635–2649, Nov. 2011.

[15] W. L. Chan and J. R. Long, "A 56–65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, pp. 2739–2746, Dec. 2008.

[16] J. R. Long, Y. Zhao, W. H. Wu, M. Spirito, L. Vera, and E. Gordon, "Passive circuit technologies for mm-wave wireless system on silicon," *IEEE Trans. Circuits Syst. I, Regular Papers*, vol. 59, pp. 1680–1693, Aug. 2012.

[17] S. Pellerano, R. Mukhopadhyay, A. Ravi, J. Laskar, and Y. Palaskas, "A 39.1-to-41.6 GHz $\Delta\Sigma$ fractional-N frequency synthesizer in 90 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2008, pp. 484–485.

[18] W. Deng, T. Siriburanon, A. Musa, K. Okada, and A. Matsuzawa, "A 58.1-to-65.0GHz frequency synthesizer with background calibration for millimeter-wave TDD transceivers," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, 2012, pp. 201–204.

[19] H. Hoshino, R. Tachibana, T. Mitomo, N. Ono, Y. Yoshihara, and R. Fujimoto, "A 60-GHz phase-locked loop with inductor-less prescaler in 90-nm CMOS," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, 2007, pp. 472–475.

[20] U. Decanis, A. Ghilioni, E. Monaco, A. Mazzanti, and F. Svelto, "A mm-wave quadrature VCO based on magnetically coupled resonators," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2011, pp. 280–281.

[21] D. Murphy, Q. J. Gu, Y. C. Wu, H. Y. Jian, Z. Xu, A. Tang, F. Wang, and M. C. F. Chang, "A low phase noise, wideband and compact CMOS PLL for use in a heterodyne 802.15. 3c transceiver," *IEEE J. Solid-State Circuits*, vol. 46, pp. 1606–1617, Jul. 2011.

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