A 125–600-MHz IF 75-dB DR Partially Time-Interleaved Bandpass DSM Based on Passive N-Path Filters

Wei Jin, *Member, IEEE*, and Kong-Pang Pun, *Senior Member, IEEE*

***Abstract*— This work presents a sixth-order partially time-interleaved bandpass delta-sigma modulator (BP DSM) for direct intermediate-frequency (IF) digitization. There are three resonators, and each of them is built with a passive N-path filter; while two open-loop operational transconductance amplifiers (OTAs) are inserted in between to realize the loop filter. The partially time-interleaved implementation enables a wide IF tuning range from 125 to 600 MHz. Besides, the OTAs are free of bandwidth limitation by deploying their equivalent large output resistors as the input resistors of the load N-path filters. Therefore, the BP DSM is power-efficient without compromising its performance. As a validation on the design, a prototype is fabricated in a 65-nm general-purpose (GP) CMOS technology. For a fixed 2-MHz bandwidth, the prototype achieves over 70-dB signal-to-noise-and-distortion ratio (SNDR) from 150- to 250-MHz IF; and it achieves over 60-dB SNDR from 125- to 550-MHz IF. The prototype achieves a peak SNDR of 72.0 dB and a maximal dynamic range (DR) of 75.1 dB at 150-MHz IF, while dissipating only 0.42 mW (including the clock generator) from a 1-V supply. This results in a Walden's figure of merits (FoM) of 32.3 fJ/conversion-step and a Schreier's FoM of 168.8 dB.**

***Index Terms*— Bandpass delta-sigma modulator (BP DSM), direct intermediate-frequency (IF) digitization, linear periodically time-variant (LPTV) system, N-path filter, programmable IF, time-interleaving.**

I. Introduction

THE concept of software-defined radio (SDR) has emerged as an attractive and universal solution with the tremendous advancement of wireless communication and CMOS technology. Lots of investigations and attempts are made in direct intermediate-frequency (IF) or radio frequency (RF) digitization, which aims to bring digital interfaces forward and reduce analog modules in the receiver. Compared with the traditional superheterodyne receiver, as is shown in Fig. 1, there are mainly two aspects of benefits with this highly digital architecture. First, a reconfigurable receiver is more efficiently implemented in the digital domain [1]; second, the receiver is less sensitive to the analog circuit impairments such as unbalanced I/Q downmixing, flicker noise, and dc offset [2]. However, direct IF/RF digitization demands high-quality analog-to-digital conversion, which emphasizes on both high sampling rate and high dynamic range (DR). Besides, the potentially high power dissipation would be a significant issue when pursuing enhanced flexibility in such an architecture. These factors make SDR a promising but challenging field in the development of next-generation RF system.

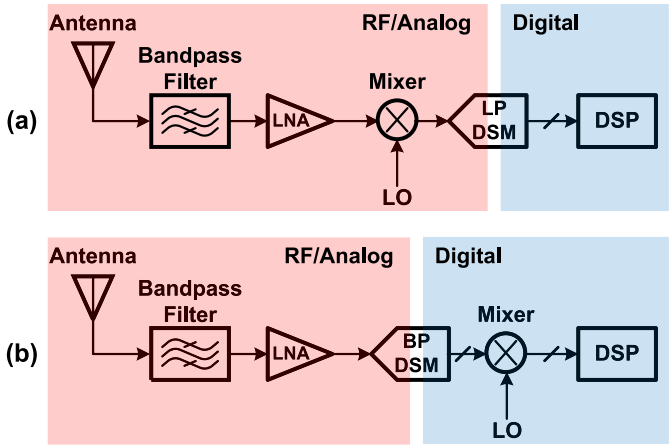

Fig. 1. Simplified block diagrams of (a) traditional superheterodyne receiver with an LP DSM and (b) direct IF/RF digitization receiver with a BP DSM.

Bandpass delta-sigma modulators (BP DSMs), which provide inherent channel-selectivity, serve as a competitive candidate in the SDR receiver front-end. Although the performance metrics of BP DSMs are less efficient than their low-pass (LP) counterpart, they can move the operation of downconversion and LP filtering to the more robust digital domain. In particular, continuous-time (CT) BP DSMs are capable of digitizing signals in the sub-GHz or GHz IF range [2]. The loop filter of conventional CT BP DSMs can be realized either with active resonators (active-RC or G_m-C) or with passive LC resonators. The active resonators demand operational transconductance amplifiers (OTAs) with high unit-gain bandwidth (UGB), which makes them power-hungry. In contrast, passive LC resonators typically support discrete-step resonance frequencies with quite limited tuning range by using a capacitor array. Besides, the bulky LC-tank tends to occupy large areas in IF design.

A resonator based on passive N-path filter was first proposed in [3] to address the issues mentioned above. It achieves an IF tuning range between 100 and 200 MHz, with a maximal signal-to-noise-and-distortion ratio (SNDR) of 60.5 dB over a

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The authors are with the Department of Electronic Engineering, The Chinese University of Hong Kong, Hong Kong SAR, China (e-mail: kppun@cuhk.edu.hk).

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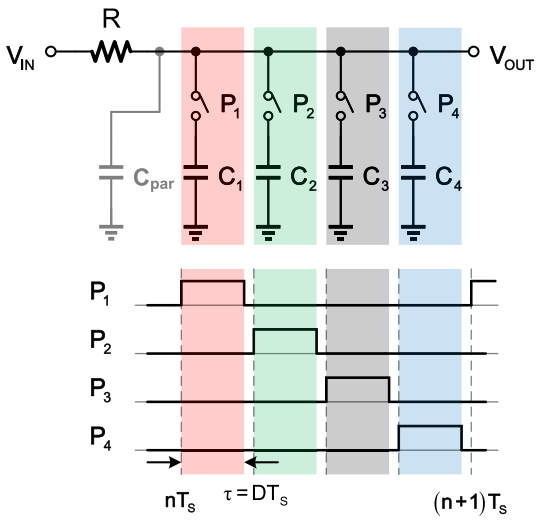

Fig. 2. Schematic of a passive N-path filter ($N = 4$) and the timing diagram.

fixed 2-MHz bandwidth. The center frequencies of the filter's passbands, and thus the noise transfer function (NTF) notches, are proportional to the clock frequency. Therewith, the in-band IF digitization performed by the BP DSM can be accurately controlled and flexibly configured.

In this work, we demonstrate a partially time-interleaved BP DSM architecture to further take advantage of the passive N-path filter resonator. In the proposed BP DSM, the feedback digital-to-analog converter (DAC) and the single-bit quantizer are time-interleaved, while the OTAs are shared by all the paths. Thanks to the partially time-interleaved implementation, the IF tuning range of the modulator is greatly expanded without consuming excess power or degrading its performance. To better illustrate the properties of the signal transfer function (STF) and the NTF, a CT analysis is conducted on this linear periodically time-variant (LPTV) circuit. The proposed modulator is fabricated in a 65-nm CMOS technology. It achieves high DR, wide IF tuning range, high power efficiency, and robust loop stability in the measurement, which validates the proposed design methodology.

This article is organized as follows. Section II introduces the properties of the N-path filter. Section III demonstrates the proposed partially time-interleaved BP DSM with design considerations. Section IV discusses the detailed circuit implementation, and Section V presents the experimental results. The conclusion is drawn in Section VI.

II. Resonator Based on Passive N-Path Filter

N-path filter is an attractive on-chip bandpass filtering solution for RF receiver front-ends [4], [5], [6], thanks to its flexible channel-selectivity, high linearity, and high-Q bandpass characteristics. The passive N-path filter consists of N switched-RC branches, with each branch referred to as a kernel [7]. The properties of the switched-RC circuits have been discussed with insights in [7], [8], and [9], in terms of frequency response, noise performance, input impedance, and nonidealities. Depending on the operation mode, a switched-RC circuit could be configured as a mixer with a large RC-constant (in the mixing region) or as a sampler with a small RC-constant (in the sampling region) [7]. In this section, the N-path filter will be discussed only in the mixing region, with consideration on resonator design in the BP DSM.

A. Property of the Passive N-Path Filter

Fig. 2 shows the schematic of a passive N-path filter ($N = 4$) with the timing diagram. Typically the capacitors C_1–C_4 are set equal, and each of them is switched on for a quarter of the clock period T_s. C_{par} is the total parasitic capacitance at the output node. The four phases of the clock P_1–P_4 are nonoverlapped to avoid charge redistribution between any two of the capacitors. Then, the duty cycle D of each branch is slightly smaller than $1/N$ in a practical implementation. Therewith, the output node periodically and sequentially sees the voltage on each capacitor from C_1 to C_4. In particular, the time-constant of RC should be much larger than $\tau(= DT_s)$, such that the circuit is in the mixing region and presents bandpass characteristics.

The passband of an ideal N-path filter is centered on the clock frequency f_s, and the 3-dB bandwidth f_b of the N-path filter is given by [10]

$$f_b = \frac{1}{N\pi RC} \tag{1}$$

which depends on the number of branches N and the RC-constant. Then, the quality factor Q of the bandpass filter is derived as

$$Q = \frac{f_s}{f_b} = N\pi RCf_s. \tag{2}$$

Due to the relatively large RC value in the mixing region, the N-path filter is intrinsically capable of narrow bandpass filtering with high quality factor. The parasitic capacitance C_{par} will cause the peak frequency to shift down slightly from f_s and attenuate the peak gain [3], [11], [12], which should be taken into account in the design.

With the configuration mentioned above, the N paths take turns to process the input signal in a time-interleaved manner. To illustrate the mechanism of the N-path filter, we may zoomed-in view to observe one path of the switched-RC circuit. As is shown in Fig. 3(a), there are two nodes that deliver the processed output signal: a high-frequency IF voltage node $V_{\text{OUT, IF}}$ and a low-frequency baseband voltage node $V_{\text{OUT, BB}}$. Either node could be picked as the input of the subsequent stage, depending on the specific implementation. The equivalent signal transfer diagram for input signal near the clock frequency is depicted in Fig. 3(b). The implicit downmixing and upmixing are realized with a simple switch. As a result, the LP filter at the baseband is transferred to the bandpass filter centered on the clock frequency. The bandwidth of the LP filter is determined by the capacitance of C_1 and the equivalent resistance $N \cdot R$ seen by it, which is consistent with the bandwidth derived for the N-path filter.

B. Passive N-Path Filter Cascaded With OTA

According to the analysis above, the bandpass filtering is efficiently performed by the time-interleaved branches of the passive N-path filter. However, the gain stages are still required

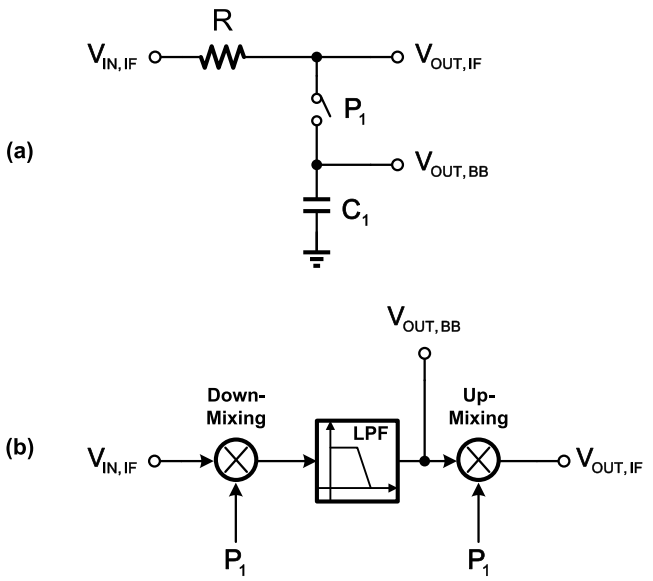

Fig. 3. (a) Switched-RC kernel of an N-path filter and (b) its equivalent signal transfer diagram (for input signal near the clock frequency) in the mixing-region.

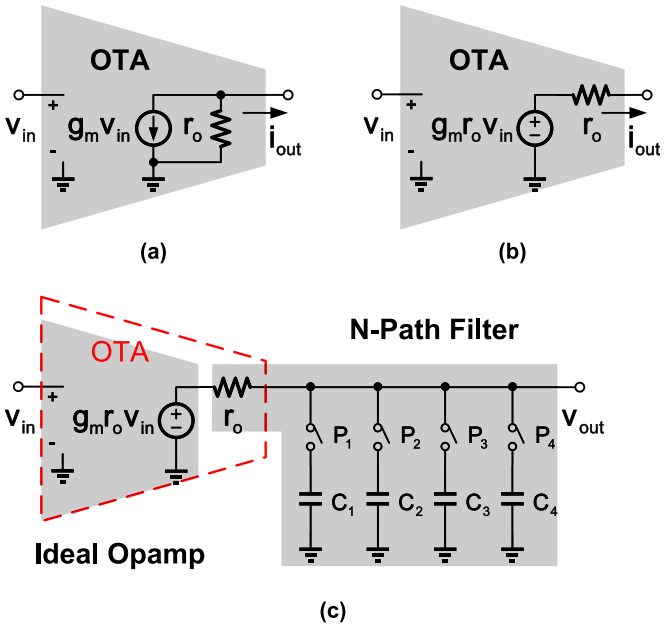

Fig. 4. (a) Small-signal model of an OTA and (b) its Thevenin's equivalent. (c) Equivalent small-signal model of the open-loop OTA and the cascaded N-path filter.

by the loop filter of the BP DSM to realize the desired NTF notches. Since the gain stages need to cover a wide frequency tuning range, it would be too power-hungry to drive the N-path filter directly with an opamp.

Despite the seemingly high power budget, an OTA with large output resistance provides an efficient solution in this case, as will be discussed below. Fig. 4(a) shows the small signal model of an OTA, while Fig. 4(b) shows its Thevenin's equivalent. From this perspective, the OTA is equivalent to a gain stage $A = g_m r_o$ in series with the output resistor r_o. When an OTA is cascaded with an N-path filter, the OTA's output resistor r_o serves as the large input resistor R of the N-path filter. Then, the combined stage could be regarded as an N-path filter driven by an ideal opamp subject to no bandwidth limitation, as shown in Fig. 4(c). It should be noted that the equivalence assumes a small voltage swing at the OTA's output, thus an almost unvaried small-signal output resistance. As will be discussed in Section III, this condition can be easily satisfied with appropriate design. From another perspective, the four switched capacitors are high-ohmic near f_s (the IF) and low-ohmic outside the IF passband [10]; hence, the voltage gain of the OTA is high at IF and drops significantly outside the IF passband. This gives an intuitive explanation as to why the OTA in Fig. 4(c) offers IF amplification without a demanding bandwidth requirement. As part of the parasitic capacitance at v_{out}, it would slightly downshift the center frequency [3], [11], [12] but not impose a limit on the IF range.

III. Proposed Architecture of the BP DSM

The analysis in Section II shows that the OTA bandwidth does not dominantly limit the frequency tuning range of the BP DSM. Compared with the relaxed design requirement of the resonators, the quantizer and the digital blocks in [3] need to operate at four times of the IF frequency. To get rid of this restriction and further expand the IF tuning range, a time-interleaved implementation is favored in such a design. Because the N-path filter itself is subject to mismatch due to imperfect fabrication, the time-interleaved paths do not introduce more types of nonidealities. In the meanwhile, a foreground digital calibration, based on a least-mean-square (LMS) algorithm similar to [13], is developed to address this issue. The detail of the calibration scheme is described in Appendix B.

A. Fully Time-Interleaving Versus Partially Time-Interleaving

The BP DSM could be implemented either in a fully time-interleaved architecture or in a partially time-interleaved architecture. Without loss of generality, the simplified circuit diagrams of the fourth-order examples are shown in Fig. 5 to demonstrate the proposed time-interleaving techniques. In Fig. 5(a), the fully time-interleaved BP DSM employs baseband amplification with four OTAs ($g_m/4$); in contrast, the partially time-interleaved BP DSM in Fig. 5(b) employs IF amplification with only one OTA (g_m). All the OTAs are designed with the same output resistance. In each period, the amount of charge transferred to the load capacitor C_2 is equal in both cases (respectively, $(1/4)g_m \cdot v_{c1} \cdot T_s$ and $g_m \cdot v_{c1} \cdot (1/4)T_s$), which could be regarded as a first-order equivalence. Recall the analysis in Section II, the bandwidth requirements of the OTAs in both cases are highly relaxed with the cascaded N-path filter load. Therefore, a similar operation frequency span (and similar power dissipation) could be achieved with appropriate design in both cases. While the OTAs do not dominantly limit the bandwidth of the BP DSM, both architectures allow the dynamic blocks to operate four times slower than the previous design [3].

Next, a further comparison should be made between these two architectures. In the proposed BP DSM, IF amplification is favored over baseband amplification due to the immunity to

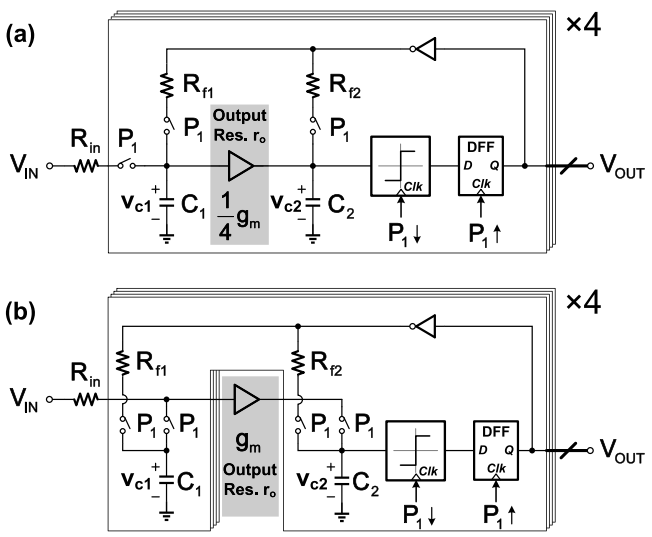

Fig. 5. (a) Fully time-interleaved and (b) proposed partially time-interleaved implementation of a BP DSM based on passive N-path filters. A fourth-order example is shown for simplicity, while our actual design is of sixth order.

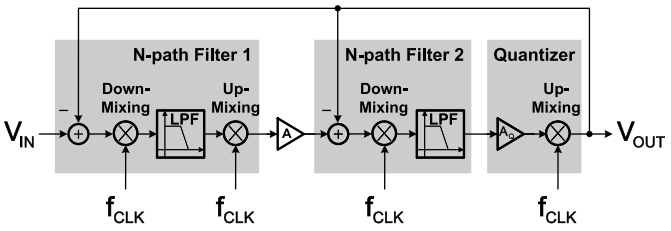

Fig. 6. System block diagram (for input signal near the clock frequency) of the partially time-interleaved fourth-order BP DSM example in Fig. 5. $A = g_m r_o$, A_q is the quantizer's voltage gain.

flicker noise, which is especially beneficial in the narrow-band scenes. In Fig. 5(a), the IF signal is mixed down to the baseband in each path (at v_{c1} and v_{c2}) and will thus be corrupted by the flicker noise of the OTAs. Then, the in-band signal and the flicker noise are upconverted to the IF band in the output spectrum when the four quantizers' outputs are deinterleaved into a single stream of final output. In contrast, the IF amplifier in Fig. 5(b) does not expose the high-frequency input/output signal to the flicker noise, which leads to the separation of these two components in the output spectrum. A macromodel simulation is conducted to validate this advantage, where the flicker noise is modeled at the input of each OTA and the other noise sources (except for quantization noise) are disabled. For the baseband amplification case, the signal-to-noise ratio (SNR) decreases by 7.1 dB (from 85.8 to 78.7 dB); while for the IF amplification case, the SNR decreases by only 0.3 dB (from 88.1 to 87.8 dB).

In addition, a single shared OTA provides inherently better matching for the different paths and improves the robustness of the loop filter. Taking these merits into account, the partially time-interleaved architecture is advantageous over its fully time-interleaved counterpart. Fig. 6 shows the system block diagram of the partially time-interleaved fourth-order BP DSM. The gain stage A is obtained with the Thevenin's equivalent of the OTA (as shown in Fig. 4(c), $A = g_m r_o$). Note that all the downmixing and upmixing processes are implicitly performed by the switches or the deinterleaving of the quantizers' outputs. Despite the fact that the IF amplifier has to handle high-frequency signal, its performance does not compromise, as will be discussed in Section II-B.

B. Proposed Sixth-Order BP DSM

To improve the DR with more aggressive noise shaping (more in-band loop gain), improve the robustness against OTA gain variation, and relax the gain requirement for the comparators, a sixth-order BP DSM is proposed in this work. Fig. 7 shows the circuit implementation of the main blocks with the timing diagram. G_{m1} and G_{m2} represent the two OTAs shared by the four paths. Each time-interleaved comparator samples the capacitor voltage at the falling edge of the respective clock phase. Since the outputs of the resistive feedback DACs are directly clocked by the switches, the D flip-flops (DFFs) in Fig. 5 are redundant and therefore removed in the implementation. The time-interleaved digital outputs V_{D1}, V_{D2}, V_{D3}, and V_{D4} are orderly combined off-chip to form the final output bit-stream V_{Dout}, in the manner of $V_{Dout}[4k+i-1] = V_{Di}[k]$ with the time index $k(= 0, 1, 2, \ldots)$ and the path index $i(= 1, 2, 3, 4)$.

In each path of the resonators, a pair of identical MIM capacitors are implemented in parallel to reduce the area and conserve symmetry. The capacitance is programmable to guarantee the loop stability within the IF tuning range. Nonreturn-to-zero (NRZ)-resistive DACs are employed in the feedback paths to minimize the peak DAC current and jitter effect. For each N-path filter, the feedback resistance is set equal to the respective input resistance ($R_{f1} = R_{in}$, $R_{f2} = R_{o1}$ and $R_{f3} = R_{o2}$) to deliver a unity feedback. With the time-interleaved implementation, the adjacent samples of V_{Dout} are essentially separated and then allocated to different sub-DACs. For each individual path, the sub-DAC (clocked by the switches) returns to zero for $(3/4)T_s$ in each period T_s. Therefore, despite being NRZ (within the respective duty cycle), the DACs do not suffer from intersymbol-interference (ISI) in this partially time-interleaved BP DSM.

Fig. 8 shows the equivalent block diagram of the proposed sixth-order BP DSM, and the derivation is based on analyzing the LPTV system. The transfer function derivation tracks the complete waveforms of each stage and the sampling is performed by the quantizer, which is similar to the case of a CT DSM. The transfer function of the first stage [3], [7], [8] is derived as

$$H_{NPF1}(z) = \left(\frac{1}{4}\omega_1 T_s\right)\frac{z^{-4}}{1-\beta_1 z^{-4}} \tag{3}$$

where the angular frequency ω_1 is given by $\omega_1 = 1/(R_{in}||R_{f1})C_1$, and the attenuation coefficient β_1 is given by $\beta_1 = \exp(-\omega_1 T_s/4)$. The transfer function of the subsequent resonators is in the same form. Provided that $RC \gg \tau$ in the mixing region, the passband of the resonators would occur at the multiples of the clock frequency $(nf_s, n = 0, 1, 2, \ldots)$. When cascading multiple N-path filters in the loop filter, several feedforward paths would arise due to the propagation of the continuous waveform. The detailed derivation procedure

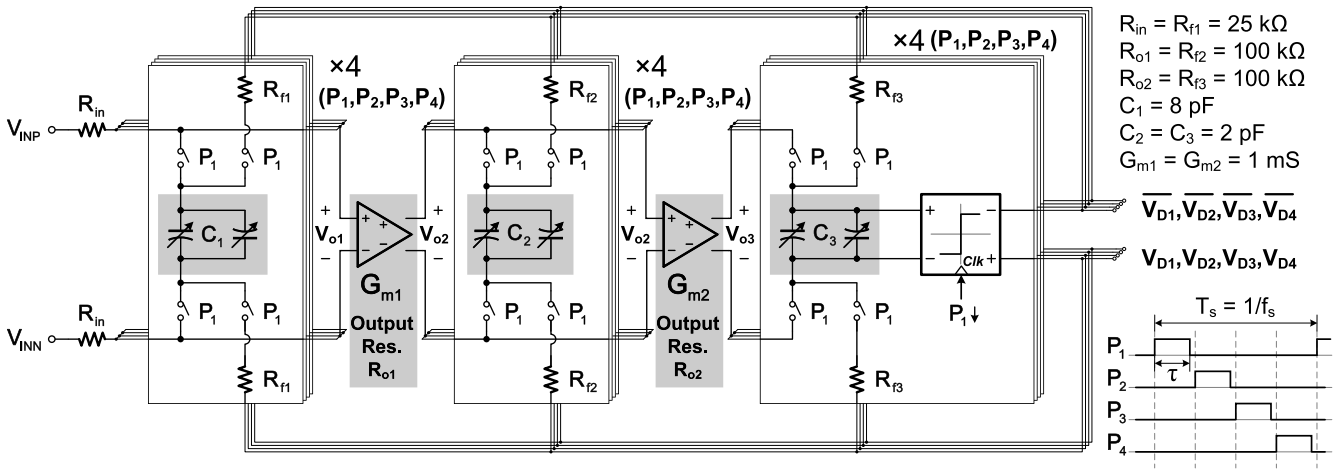

Fig. 7. Circuit implementation of the proposed sixth-order partially time-interleaved BP DSM and the timing diagram.

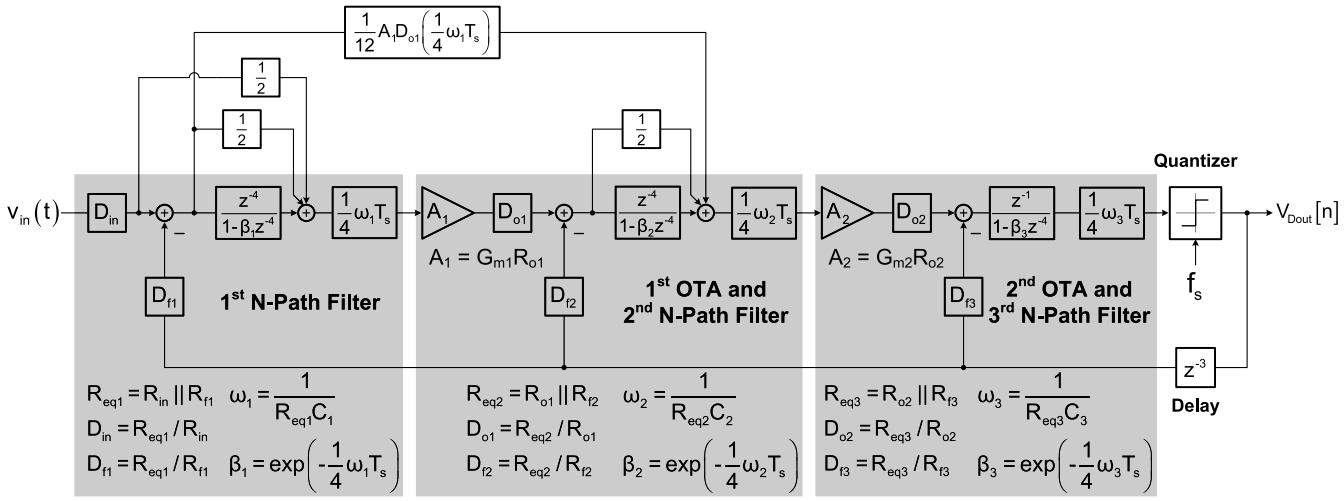

Fig. 8. Equivalent z-domain model of the sixth-order BP DSM in Fig. 7.

is attached in Appendix A, together with a unified method that can be applied to similar LPTV systems.

Fig. 9 shows the simulated waveform at the output of each N-path filter (with a −2-dBFS sinewave input at 200-MHz IF). When inspecting the input and the output of the OTAs, the in-band signal is canceled out to a minimum due to the large in-band loop gain; while the out-of-band components are suppressed by the N-path filters. Thanks to this passive-filter-first architecture and a proper design of the modulator coefficients, the output voltage swing of the N-path filters (including the IF output nodes and the baseband output nodes) is effectively limited to a few tens of millivolts. This small signal swing leads to a relatively constant OTA output resistance and enables the design tentatively discussed in Section II. Additionally, it relaxes the design requirements of the OTAs and guarantees the linearity of the MOSFET switches. Recall that the bandwidth of the OTAs is not a major limitation in the modulator. As a result, IF amplification can be naturally realized without any demanding circuitry.

The analysis above shows that the N-path filters in the modulator provide the desired frequency response of a BP DSM, while the OTAs buffer the passive filter with adequate loop gain. Since the gain (or G_m) of the open-loop OTA is subjected to process variation, the loop stability of the proposed modulator is checked with transistor-level simulations. Fig. 10 plots the simulated OTA gain histogram and the corresponding SNDR. The two OTAs on the same chip are assumed to deliver similar voltage gain. Monte-Carlo simulations (including mismatch and process variation) are conducted on the OTA to obtain the gain histogram and variation range. Then, the OTAs are replaced by ideal gain stages (the other blocks remain to be transistor-level) to check the SNDR variation. As shown in Fig. 10, the modulator is stable over a wide gain variation range and could achieve relatively high SNDR in a majority of the cases.

As is discussed in [3], nonidealities involved in the design are briefly evaluated here. First of all, the ON-resistance of the switches, which limits the out-of-band suppression of the N-path filters, is designed to be significantly smaller than the input resistances of the N-path filters. Indeed, the net out-of-band suppression in this architecture will almost always be sufficient due to the cascade of three N-path filters. Second, the path mismatch, which includes the effects of switches, feedback DACs, and timing skew, could be

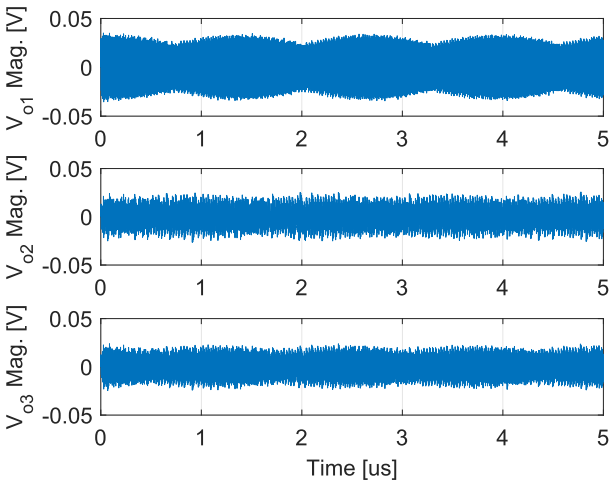

Fig. 9. Voltage swing at the output of each N-path filter.

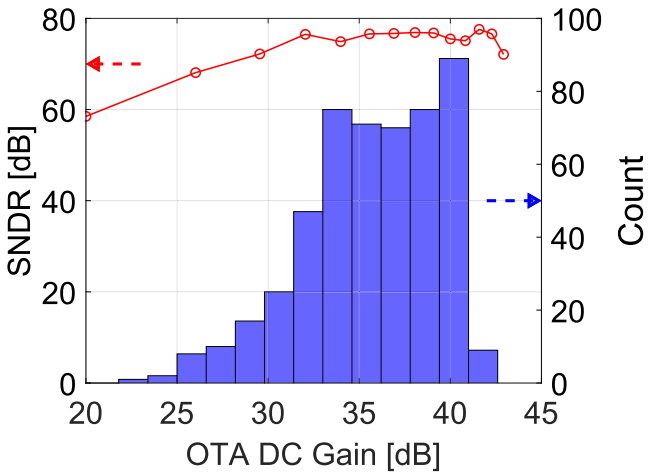

Fig. 10. OTA gain histogram (with Monte-Carlo simulation) and the corresponding SNDR (with transistor-level simulation).

effectively compensated through the foreground calibration. Besides, the NTF notches would slightly shift to the low-frequency side, due to the parasitic capacitance at the output of the N-path filter. This imperfection could be mitigated with appropriate transistor sizing and compact layout floorplan.

C. Thermal Noise Analysis

In order to present the bandpass characteristics of the proposed BP DSM, the z-domain block diagram is demonstrated in the previous section. Although the input stage of the modulator is a switched-RC circuit, it does not sample the input signal directly. It functions as a CT DSM since the complete waveform should be evaluated in the transfer function derivation. Therewith, the noise analysis of the input stage goes back to the s-domain. Thanks to the large in-band gain provided by the first OTA, the in-band thermal noise is dominant by the input stage. Following the annotation in Fig. 8, the s-domain transfer function is given by [9]:

$$H_{\mathrm{NPF1}}(s) = \frac{D_{\mathrm{in}}}{1+sR_{\mathrm{eq1}}C_1}\left\{1-\frac{R_{\mathrm{eq1}}C_1}{\tau}H_{\mathrm{eq1}}(s)\cdot\left[1-e^{-s(T_s-\tau)}\right]\right\} \quad (4)$$

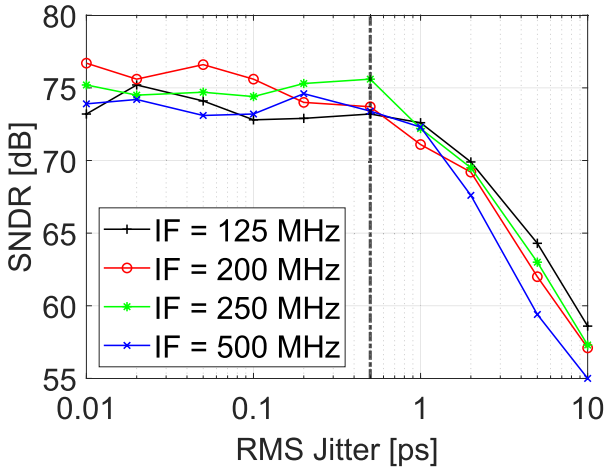

Fig. 11. SNDR versus rms clock jitter (transistor-level simulation).

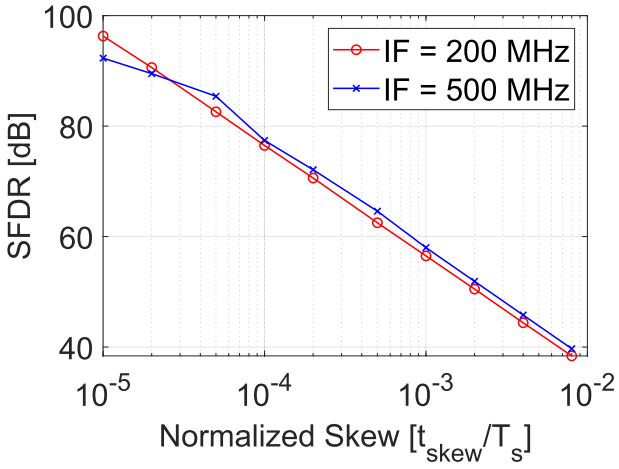

Fig. 12. SFDR versus normalized timing skew (transistor-level simulation).

where $H_{\mathrm{eq1}}(s)$ is given by

$$H_{\mathrm{eq1}}(s) = \frac{1}{1+sR_{\mathrm{eq1}}C_1}\cdot\frac{1-\beta_1 e^{-s\tau}}{1-\beta_1 e^{-sT_s}}. \quad (5)$$

As shown in [3] and [9], the thermal noise folded back from higher frequencies is an insignificant portion and could be ignored here for brevity. Then, the input-referred noise spectral density is derived as

$$\overline{V_{n,\mathrm{in}}^2}(\omega) \approx 8kTR_{\mathrm{in}}\left(1+\frac{R_{\mathrm{in}}}{R_{f1}}\right)+\frac{8kT\gamma}{g_{m1}}\cdot\frac{1}{|H_{\mathrm{NPF1}}(j\omega)|^2} \quad (6)$$

with a differential implementation. When setting $R_{\mathrm{in}} = R_{f1} = 25\ k\Omega$ and $g_{m1} = 1$ mS in the design, the calculated SNR is 77.4 dB ($\gamma = 2/3$) with a -2-dBFS input, which is consistent with the simulation result. The contributions of the thermal noise from the input/feedback resistors and the first OTA are 57% and 43%, respectively.

D. Clock Jitter and Timing Skew

The nonideal clock signal that drives the N-path filters may degrade the performance of the time-interleaved modulator. The clock jitter would equivalently lead to the rising of the spectral noise floor, while the timing skew in different paths

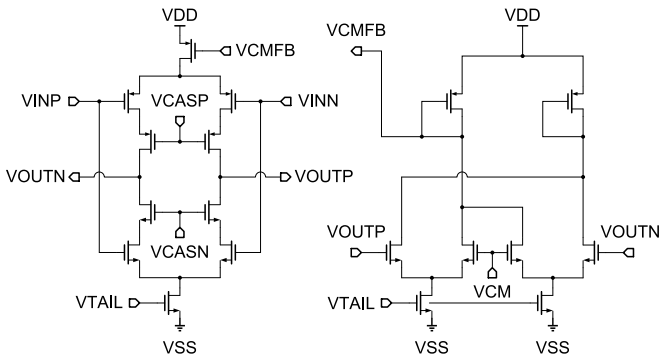

Fig. 13. Schematics of the class-AB OTA and the common-mode feedback circuitry.

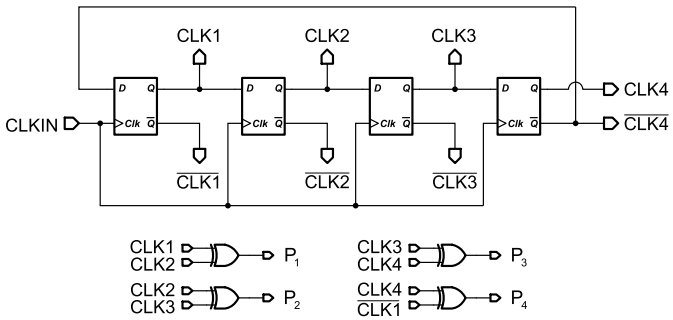

Fig. 14. Schematic of the four-phase clock generator.

would introduce the image tones [3]. Both aspects of clock nonidealities should be carefully evaluated in the design phase.

Fig. 11 shows the SNDR versus clock jitter curves plotted with transistor-level simulation. When the jitter-induced noise contribution is dominant over the thermal noise and quantization noise of the modulator, the SNDR would severely decrease. As shown in the plot, the proposed BP DSM can tolerate approximately 0.5-ps root-mean-square (rms) jitter with the single-bit feedback DAC. Fig. 12 shows the simulated spurious-free DR (SFDR) versus the timing skew normalized to the clock period T_s. According to the analysis in Appendix B, the timing skew among the four paths is mainly manifested in gain mismatch, which is similar to the case of RC mismatch. Therefore, timing skew could be compensated through the proposed calibration scheme.

IV. Building Block Circuits

In this section, the circuit implementation of each block is discussed according to the system requirements. The system-level parameter optimization is briefly discussed here to illustrate the design process. The first step is to determine a design starting point for the attenuation coefficient β and the gain stage A in the modulator. The attenuation coefficient β determines the NTF zeros ($\pm\beta^{1/4}$, $\pm i\beta^{1/4}$) and could be derived based on the in-band SQNR optimization. A large gain could suppress the input voltage swing of the amplifier and relax its linearity requirement. Hence, a nearly maximal A is picked and the upper limit of A is mainly set by loop stability requirement. The second step is to determine the parameters (R_{in}, C_1 and G_{m1}) of the input stage. Since the RC-constant is typically large (in the mixing region and determined by β_1),

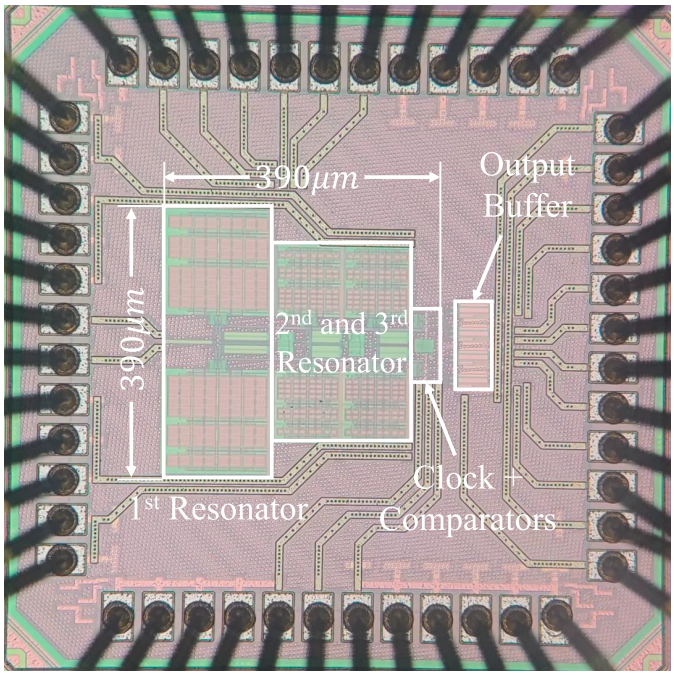

Fig. 15. Chip micrograph of the sixth-order BP DSM prototype.

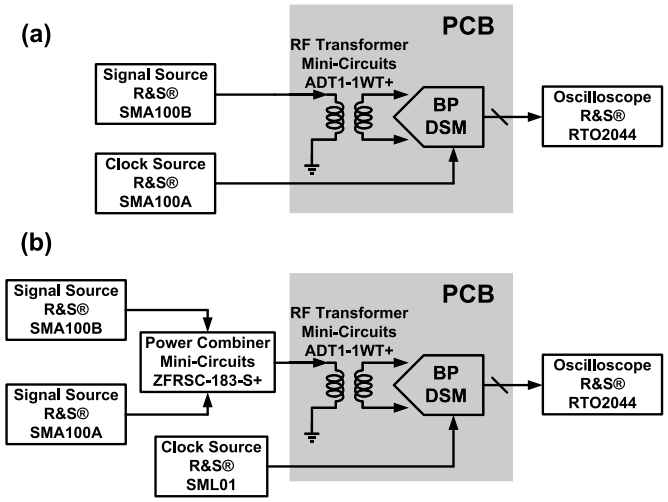

Fig. 16. Measurement setup for (a) single-tone test and (b) two-tone test.

the area occupied by the input stage is a critical issue. It is practical to determine R_{in} with consideration on both thermal noise and the area occupied by the large capacitor C_1. G_{m1} is thereby derived with (6) for a similar noise contribution. The third step is to check the system robustness against parameter variation. With the parameters derived above as a reference, it is feasible to slightly adjust them through parameter sweeps. After determining these key parameters in the design, we can proceed to implement the circuit design.

Before diving into the topology choice of the OTA, we observe that its input and output swing is limited to a few tens of millivolts. Therefore, the linearity and slewing requirement of the OTAs is effectively relaxed and the main design consideration is focused on the noise performance. Class-AB amplifier is a good candidate here, which can achieve high current efficiency and low thermal noise simultaneously [14].

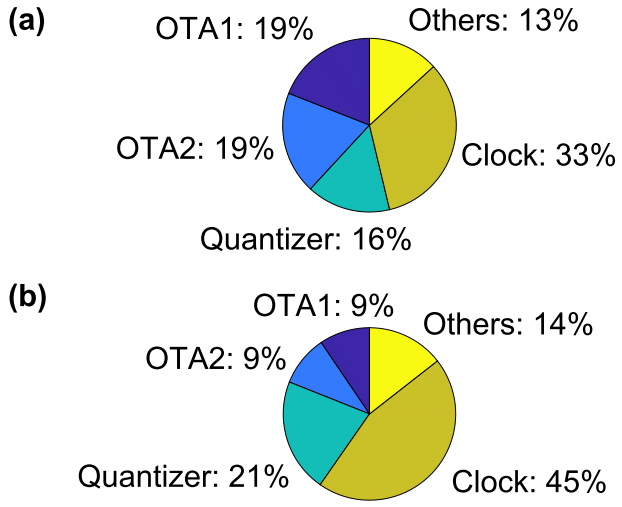

Fig. 17. Power breakdown at (a) 150- and (b) 550-MHz IF.

Fig. 13 shows the schematics of the class-AB OTA and its common-mode feedback circuitry. Considering the parasitic capacitance, however, the transistors should be appropriately sized to alleviate the shifting of the NTF notches.

With the time-interleaved BP DSM architecture, the design requirement of the quantizer is also highly relaxed in terms of settling time and propagation delay. To maintain the loop stability, adequate voltage gain should be provided for the most inner feedback loop. A single-bit quantizer fits well from the perspective of power-efficiency, which offers an undefined but self-adaptive voltage gain. In each path, a strong-arm comparator followed by a NAND-based latch [15], [16], [17] is employed as the single-bit quantizer. The strong-arm comparator consists of a preamplifier and an inverter-based latch in cascode. Driven by a single-phase clock signal, it produces the output at the clock rising edge. Since the comparators are directly connected to the large capacitors of the N-path filter, the parasitic capacitance at the input nodes is negligible. The transistor size can be freely optimized to cover the entire IF tuning range. Besides, the kick-back noise is significantly absorbed and attenuated by the large capacitors.

Another key block in the BP DSM is the four-phase nonoverlapped clock generator. With a passive N-path filter implemented as the input stage, the nonidealities of the clock signal will directly degrade the DR of the BP DSM. Fig. 14 shows the schematic of the four-phase clock generator. The DFFs are based on NAND gates with differential outputs. The DFF chain in a loop divides the input clock signal by four. Then, each XOR gate combines two adjacent DFF outputs and their differential supplements (not shown in Fig. 14 for simplicity) to generate the desired clock phase. With this configuration, the systematic symmetry is guaranteed and the sensitivity to the input interference is minimized.

V. Experimental Results

As a validation on the proposed design methodology, a sixth-order BP DSM prototype is fabricated in a 65-nm general-purpose (GP) CMOS technology. The chip micrograph is shown in Fig. 15 and the core occupies an active area of

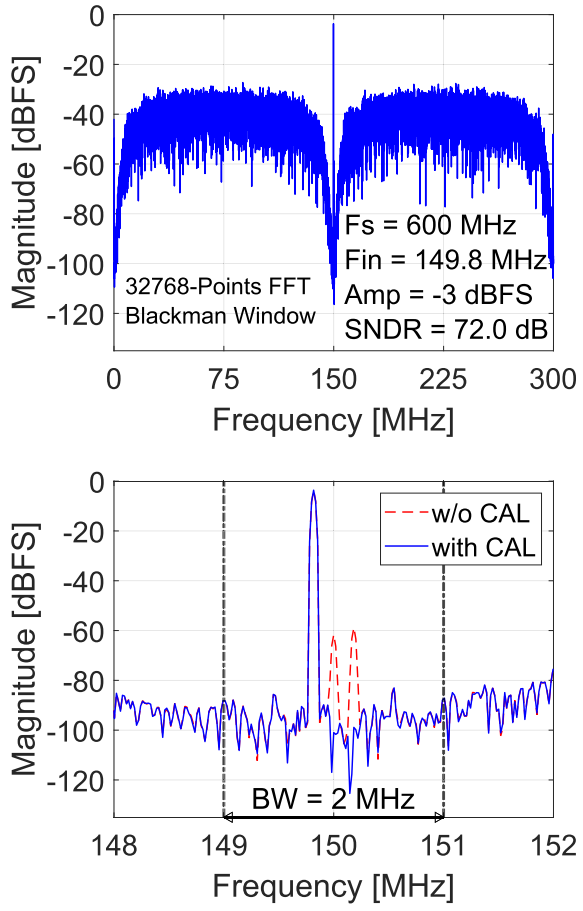

Fig. 18. Measured output spectrum at 150-MHz IF with 149.8-MHz input.

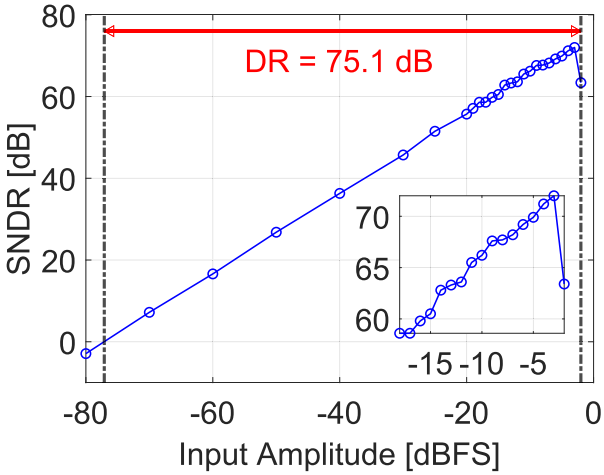

Fig. 19. Measured SNDR versus input amplitude at 150-MHz IF.

0.123 mm^2. The die is mounted in a QFN40 package for measurement. Fig. 16 demonstrates the measurement setup for the single-tone test and the two-tone test, respectively. The maximal rms jitter of the clock source SMA 100A is 36 fs within the IF tuning range. In the single-tone test, the single-ended input signal is converted to differential through an RF-transformer-based balun on the print circuit board (PCB). In the two-tone test, the input tones are first combined through the power splitter/combiner before being converted to differential. The foreground calibration is performed off-chip after capturing the output bit stream from the oscilloscope. For

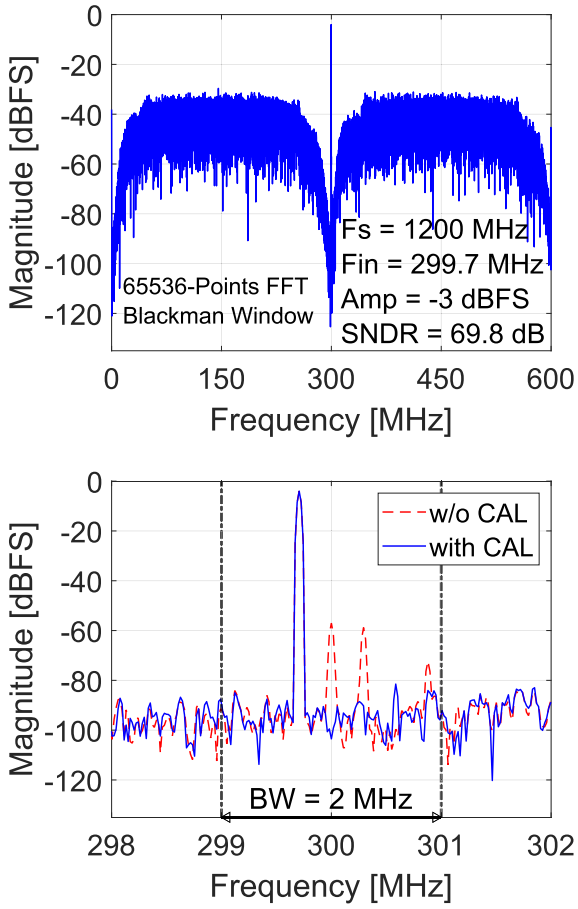

Fig. 20. Measured output spectrum at 300-MHz IF with 299.7-MHz input.

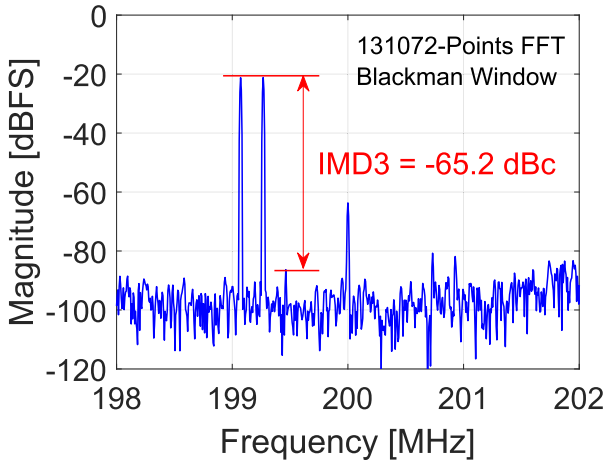

Fig. 21. Measured output spectrum at 200-MHz IF with a two-tone test.

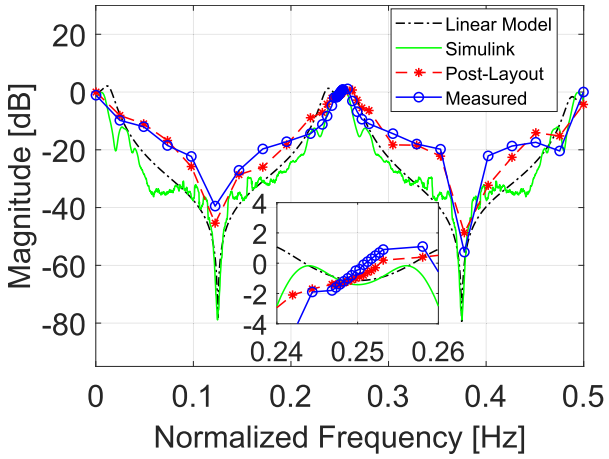

Fig. 22. Measurement STF curve versus the calculation or simulation STF curves in different design phases.

each IF, the calibration coefficients are pregenerated with a test sinewave input to estimate and correct the (offset, gain, and time-skew) mismatch. For a fixed IF, the calibration scheme is insensitive to the input frequency.

The prototype operates under a 1-V supply, and the full scale is defined by a 2-V (peak-to-peak) sinusoid differentially. It achieves a wide IF tuning range from 125 to 600 MHz; while the corresponding power dissipation is between 0.384 (at the minimum operation frequency) and 0.898 mW (at the maximum operation frequency). Fig. 17 shows the power breakdown of the prototype at 150- and 550-MHz IF. The OTAs dissipate constant power within the IF tuning range, while the power consumption of the quantizer and the clock generator is proportional to the operation frequency. As a potential improvement, the power consumption of the clock generator could be lowered with circuits of [18] if a well-balanced differential master clock source is available.

When the prototype is operating at 150-MHz IF, the measured peak SNDR is 72.0 dB and the maximal DR is 75.1 dB over a fixed 2-MHz bandwidth. Fig. 18 shows the measured output spectrum with a 149.8-MHz input. Fig. 19 shows the measured SNDR versus the input amplitude at 150-MHz IF. Referring to Fig. 18, the image tone and the dc component are effectively calibrated, which are mainly caused by path mismatch (including component mismatch) and timing skew. The measured output spectrum at 300-MHz IF is shown in Fig. 20. The peak SNDR at 300-MHz IF is 69.8 dB, with a similar noise floor and a similar NTF shape to the case at 150-MHz IF.

Despite the SNDR degradation at excessively high IF, the modulator's stability is guaranteed up to the clock frequency limit (3 GHz) of the signal generator in the measurement. The partially time-interleaved BP DSM proves to be robust against clock nonidealities over the wide operation frequency span. The measured performance specifications over the entire IF tuning range are summarized in Table I. A peak SNDR over 65 dB is achieved up to 400-MHz IF, and a peak SNDR over 60 dB is achieved up to 550-MHz IF. As the operation frequency further increases to 600 MHz, the clock rising/falling time is almost constant with the fixed driving capacity, thereby equivalently resulting in a smaller duty cycle for each path. As a consequence, the overshrinking duty cycle will severely degrade the bandpass characteristics of the N-path filter (see [4, Fig. 11]). Then, the NTF notches at high IF become shallower than that at low IF. With the rising noise floor and the deteriorate bandpass filtering, the peak SNDR at 600-MHz IF decreases to only 50.9 dB.

Recall that the NTF notches would shift to the low-frequency side, due to the parasitic capacitance at the IF output nodes of the N-path filters; the last two rows in Table I list the

TABLE I
PERFORMANCE SUMMARY OF THE BP DSM

IF/Fclk [MHz]	**125**	**150**	**175**	**200**	**250**	**300**	**350**	**400**	**450**	**500**	**550**	**600**
Bandwidth [MHz]	2	2	2	2	2	2	2	2	2	2	2	2
Peak SNDR [dB]	69.0	72.0	71.8	71.7	70.6	69.8	67.6	65.7	62.8	61.6	60.2	50.9
Power [mW]	0.384	0.420	0.445	0.473	0.524	0.579	0.631	0.685	0.737	0.791	0.844	0.898
[1]**FoM_W [fJ/conv.]**	41.7	32.3	35.0	37.6	47.3	57.3	80.5	108.7	163.3	201.3	252.3	783.4
[2]**FoM_S [dB]**	166.2	168.8	168.3	168.0	166.4	165.2	162.6	160.4	157.1	155.6	153.9	144.4
[3]**Optimal IF [MHz]**	125.0	149.5	174.5	199.5	249.3	299.2	349.6	399.4	448.8	500.0	550.0	600.0
[3]**Corresp. SNDR [dB]**	69.0	72.5	72.5	73.5	72.7	71.5	68.8	67.0	63.3	61.6	60.2	50.9

[1]$\text{FoM}_\text{W} = \text{Power}/(2 \times \text{Bandwidth} \times 2^{\text{ENOB}})$, where $\text{ENOB} = (\text{SNDR} - 1.76)/6.02$.

[2]$\text{FoM}_\text{S} = \text{SNDR} + 10\log_{10}(\text{Bandwidth}/\text{Power})$.

[3]The IF to achieve best performance and the corresponding peak SNDR.

TABLE II
COMPARISON WITH STATE-OF-THE-ART BP DSMS

	This Work		**ISSCC'21 [19]**	**JSSC'20 [3]**	**SSCL'20 [20]**	**JSSC'16 [21]**	**JSSC'16 [22]**	**JSSC'13 [23]**	**JSSC'13 [24]**
Architecture	**TI CT-DSM with NPF**		TINS-SAR with NPF	CT-DSM with NPF	OTAless CT-DSM	Active-RC CT-DSM	Active-RC CT-DSM	Gm-LC CT-DSM	Gm-LC CT-DSM
Process [nm]	**65**		40	65	65	65	65	65	40
Area [mm^2]	**0.123**		0.19	0.032	0.18	0.25	0.03	0.55	0.4
Supply [V]	**1**		1.2	1	0.9	1.2/1.7/2.5	1.4	1	-
Sampling Freq. (Range) [MHz]	**600 (500-2400)**	**800 (500-2400)**	450	700 (400-800)	208	800	1040	100	3200
Center Freq. (Range) [MHz]	**150 (125-600)**	**199.5 (125-600)**	56	175 (100-200)	52	200 (180-220)	260	25	800 (700-800)
BW [MHz]	**2**	**2**	3.5	2	4.3	25	20	4	20
Peak SNDR [dB]	**72.0**	**73.5**	78.7	60.5	59.5	69	56	55	70
DR [dB]	**75.1**	**76.3**	79.8	63.2	-	70	57	57.5	-
Power [mW]	[1]**0.420**	[1]**0.473**	5.04	[2]0.15	0.36	35	13.1	13	20
FoM_W [fJ/conv.]	**32.3**	**30.6**	90.1	43.3	53	270	635	3500	190
FoM_S [dB]	**168.8**	**169.8**	167.1	161.7	160	157	144.2	139.9	160

[1]The power dissipation of the foreground calibration is not included.

[2]The power dissipation of the clock generator is not included.

highest SNDR that the prototype can achieve with the optimal IF. After compensating the minor passband shifting, the peak SNDR is 73.5 dB and the peak DR is 76.3 dB at 199.5-MHz IF.

A two-tone test is conducted to evaluate the prototype's linearity when digitizing multiple in-band subchannels. Fig. 21 shows the measured output spectrum at 200-MHz IF with a two-tone test. The two input tones are at the frequency of 199.07 and 199.27 MHz, respectively. The corresponding third-order intermodulation distortion (IMD3) is -65.2 dBc.

To check the performance of channel-selectivity, the measurement STF curve is plotted in Fig. 22 and compared to the calculation and simulation results over the normalized Nyquist band. A calculated STF is derived with the linear model of the BP DSM. The Simulink model uses a single-bit quantizer, while the postlayout simulation result is plotted to demonstrate the effects of nonidealities in the design. Referring to Fig. 22, there are the three passbands at the multiples of the clock frequency and two notches to reject undesired components. The measured STF curve deviates from the ideal curve, which mainly results from two factors. First, the linear model assumes a constant quantizer gain for the loop filter, while the single-bit quantizer gain is input-dependent and varies in a certain range. Second, the nonidealities would shift or reshape the STF, such as path mismatch, reduced duty cycle, parasitic capacitance, and ON-resistance of the switches. Nevertheless, the measured STF curve delivers a maximum 1.7-dB ripple (flatter with a high IF) in the centered narrow passband, and provides moderate out-of-band attenuation.

Table II compares the prototype's performance with some prior BP DSMs. The performance metrics of this work are divided into two columns. The first column summarizes the measurement results given a nominal IF (a quarter of the sampling frequency), while the second column represents the potentially optimal performance that can be achieved with a fine-tuned IF. The total power consumption takes into account the analog blocks (OTAs and comparators), the digital blocks (latches), and the clocking (clock generator and drivers). The IF tuning range is significantly expanded compared with [3], thanks to the partially time-interleaved implementation. Besides, the sixth-order loop filter improves the peak SNDR and DR with more aggressive noise-shaping. Moreover, the high power-efficiency is well conserved by reducing the digital blocks and pruning the clock tree. The proposed BP DSM achieves the widest tuning range and the best figure-of-merits (FoM) in Table II, thus proving its superior flexibility and efficiency in direct IF digitization.

VI. Conclusion

This work presents a sixth-order partially time-interleaved BP DSM for narrow-band IF digitization. The resonators in the loop filter are based on passive N-path filters, which features efficient and high-Q bandpass characteristics. A prototype is fabricated in a 65-nm GP CMOS technology to validate the design conception. With the proposed partially time-interleaved implementation, the prototype achieves a wide IF tuning range between 125 and 600 MHz. It achieves a peak SNDR of 72.0 dB and a peak DR of 75.1 dB at 150-MHz IF. Operating under a 1-V supply, the overall power consumption is effectively controlled to less than 1 mW within the entire tuning range. These experimental results show that the proposed BP DSM architecture is highly flexible and efficient for sub-GHz IF digitization. It can indeed realize direct RF digitization, for example, in the 433–434-MHz ISM band. If the BP DSM is designed in a more advanced CMOS technology, it has the potential to perform direct digitization in higher RF bands. A unified analysis procedure on such LPTV systems is developed as a supplement, aiming for a design-oriented optimization on the coefficients.

Appendix A
Transfer Function Derivation of the BP DSM

As is discussed in Section III, the proposed BP DSM is partially time-interleaved with shared input resistors and isolated capacitors. Bandpass filtering over the complete waveform is performed through the orderly combination of the four paths. Each path occupies a quarter of the period, such that the input is equivalently divided into segments of duration $(1/4)T_s$. Then, it is reasonable to split them and consider a single path in the analysis, since the other paths are the duplicates with different delays. In the derivation, we attempt to relate the input samples $V_{\text{in}}[(i/4)T_s]$ $(i = 1, 2, 3, \ldots)$ to the output signal sampled by the quantizer. After deriving the transfer function $H(z)$ for one path, we can substitute z (sample period T_s for a single path) with z^4 (equivalent sample period $(1/4)T_s$ for the modulator) to count for the contribution of the other

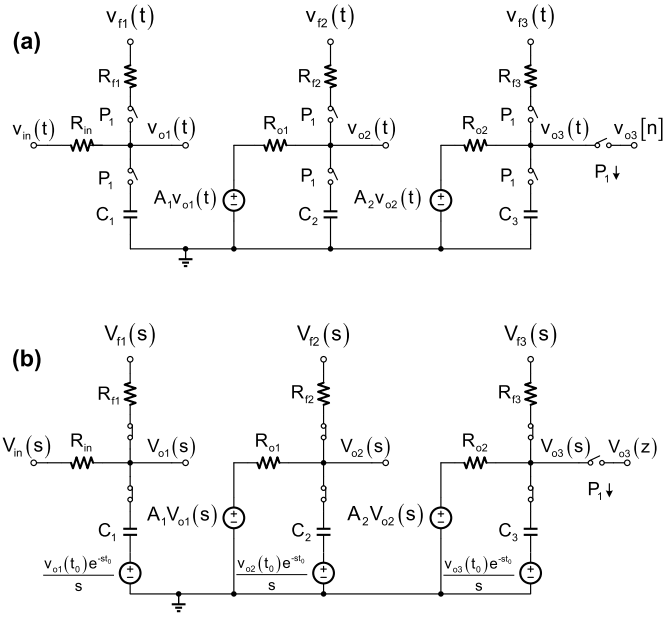

Fig. 23. Small-signal model of the first path of the proposed BP DSM in (a) time-domain and (b) s-domain.

three paths. Without loss of generality, the first path is analyzed here. Fig. 23 shows the small-signal model of the first path, respectively, in time-domain and s-domain.

As is consistent with Fig. 8, the denotation is recapped here to simplify the expressions in the following analysis. The equivalent input resistance of each stage is given by

$$\begin{aligned} R_{\text{eq1}} &= R_{\text{in}} || R_{f1} \\ R_{\text{eq2}} &= R_{o1} || R_{f2} \\ R_{\text{eq3}} &= R_{o2} || R_{f3}. \end{aligned} \tag{7}$$

Then, the voltage dividing ratio of each stage is denoted by

$$\begin{aligned} D_{\text{in}} &= \frac{R_{\text{eq1}}}{R_{\text{in}}}, \quad D_{f1} = \frac{R_{\text{eq1}}}{R_{f1}} \\ D_{o1} &= \frac{R_{\text{eq2}}}{R_{o1}}, \quad D_{f2} = \frac{R_{\text{eq2}}}{R_{f2}} \\ D_{o2} &= \frac{R_{\text{eq3}}}{R_{o2}}, \quad D_{f3} = \frac{R_{\text{eq3}}}{R_{f3}}. \end{aligned} \tag{8}$$

The angular cut-off frequency and the attenuation coefficient of each stage are, respectively, given by

$$\begin{aligned} \omega_1 &= \frac{1}{R_{\text{eq1}} C_1}, \quad \beta_1 = \exp\left(\frac{1}{4}\omega_1 T_s\right) \\ \omega_2 &= \frac{1}{R_{\text{eq2}} C_2}, \quad \beta_2 = \exp\left(\frac{1}{4}\omega_2 T_s\right) \\ \omega_3 &= \frac{1}{R_{\text{eq3}} C_3}, \quad \beta_3 = \exp\left(\frac{1}{4}\omega_3 T_s\right). \end{aligned} \tag{9}$$

Considering the time interval $t_0 \le t \le t_0 + \tau$, where $t_0 = nT_s$ $(n = 0, 1, 2, \ldots)$ and $\tau = T_s/4$, the complete output waveform of the each stage is evaluated to derive the equivalent z-domain transfer function. Since the system is linear over time, superposition applies to all the voltage nodes in both time-domain and s-domain. Then, the output voltage

of each stage in s-domain is given by

$$\begin{aligned}V_{o1}(s) &= V_{\text{in}}(s)\cdot\frac{D_{\text{in}}\omega_1}{s+\omega_1}\\ &\quad+V_{f1}(s)\cdot\frac{D_{f1}\omega_1}{s+\omega_1}\\ &\quad+\frac{v_{o1}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_1}\end{aligned}\tag{10}$$

$$\begin{aligned}V_{o2}(s) &= V_{\text{in}}(s)\cdot\frac{D_{\text{in}}\omega_1}{s+\omega_1}\cdot\frac{A_1D_{o1}\omega_2}{s+\omega_2}\\ &\quad+V_{f1}(s)\cdot\frac{D_{f1}\omega_1}{s+\omega_1}\cdot\frac{A_1D_{o1}\omega_2}{s+\omega_2}\\ &\quad+V_{f2}(s)\cdot\frac{D_{f2}\omega_2}{s+\omega_2}\\ &\quad+\frac{v_{o1}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_1}\cdot\frac{A_1D_{o1}\omega_2}{s+\omega_2}\\ &\quad+\frac{v_{o2}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_2}\end{aligned}\tag{11}$$

$$\begin{aligned}V_{o3}(s) &= V_{\text{in}}(s)\cdot\frac{D_{\text{in}}\omega_1}{s+\omega_1}\cdot\frac{A_1D_{o1}\omega_2}{s+\omega_2}\cdot\frac{A_2D_{o2}\omega_3}{s+\omega_3}\\ &\quad+V_{f1}(s)\cdot\frac{D_{f1}\omega_1}{s+\omega_1}\cdot\frac{A_1D_{o1}\omega_2}{s+\omega_2}\cdot\frac{A_2D_{o2}\omega_3}{s+\omega_3}\\ &\quad+V_{f2}(s)\cdot\frac{D_{f2}\omega_2}{s+\omega_2}\cdot\frac{A_2D_{o2}\omega_3}{s+\omega_3}\\ &\quad+V_{f3}(s)\cdot\frac{D_{f3}\omega_3}{s+\omega_3}\\ &\quad+\frac{v_{o1}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_1}\cdot\frac{A_1D_{o1}\omega_2}{s+\omega_2}\cdot\frac{A_2D_{o2}\omega_3}{s+\omega_3}\\ &\quad+\frac{v_{o2}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_2}\cdot\frac{A_2D_{o2}\omega_3}{s+\omega_3}\\ &\quad+\frac{v_{o3}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_3}\end{aligned}\tag{12}$$

where the initial voltage of each capacitor is composed of

$$\begin{aligned}v_{o1}(t_0) &= v_{o1,in}(t_0)+v_{o1,f1}(t_0)\\ v_{o2}(t_0) &= v_{o2,in}(t_0)+v_{o2,f1}(t_0)+v_{o2,f2}(t_0)\\ v_{o3}(t_0) &= v_{o3,in}(t_0)+v_{o3,f1}(t_0)+v_{o3,f2}(t_0)+v_{o3,f3}(t_0).\end{aligned}\tag{13}$$

Let us consider the transfer function from $v_{f1}(t)$ to $v_{o3}(t)$ for example, then all the irrelevant terms are removed and the output voltage of each stage is reduced to

$$\begin{aligned}V_{o1,f1}(s) &= V_{f1}(s)\cdot\frac{D_{f1}\omega_1}{s+\omega_1}\\ &\quad+\frac{v_{o1,f1}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_1}\end{aligned}\tag{14}$$

$$\begin{aligned}V_{o2,f1}(s) &= V_{f1}(s)\cdot\frac{D_{f1}\omega_1}{s+\omega_1}\cdot\frac{A_1D_{o1}\omega_2}{s+\omega_2}+\\ &\quad+\frac{v_{o1,f1}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_1}\cdot\frac{A_1D_{o1}\omega_2}{s+\omega_2}\\ &\quad+\frac{v_{o2,f1}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_2}\end{aligned}\tag{15}$$

$$\begin{aligned}V_{o3,f1}(s) &= V_{f1}(s)\cdot\frac{D_{f1}\omega_1}{s+\omega_1}\cdot\frac{A_1D_{o1}\omega_2}{s+\omega_2}\cdot\frac{A_2D_{o2}\omega_3}{s+\omega_3}\\ &\quad+\frac{v_{o1,f1}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_1}\frac{A_1D_{o1}\omega_2}{s+\omega_2}\frac{A_2D_{o2}\omega_3}{s+\omega_3}\\ &\quad+\frac{v_{o2,f1}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_2}\cdot\frac{A_2D_{o2}\omega_3}{s+\omega_3}\\ &\quad+\frac{v_{o3,f1}(t_0)}{s}\cdot e^{-st_0}\cdot\frac{s}{s+\omega_3}.\end{aligned}\tag{16}$$

Assuming an impulsive signal at $t=0$ convolved with the NRZ DAC pulse shape, the applied input in time-domain and s-domain is given by

$$\begin{aligned}v_{f1}(t) &= u(t)-u(t-\tau)\\ V_{f1}(s) &= \frac{1}{s}\left(1-e^{-s\tau}\right)\end{aligned}\tag{17}$$

where $u(t)$ is the unit step function. Plug in the expression of $V_{f1}(s)$ and apply the inverse Laplace transform to the output voltage, the transient response in time-domain is given by

$$\begin{aligned}v_{o1,f1}(t) &= v_{o1,f1}(t_0)e^{-\omega_1(t-t_0)}\\ &\quad+D_{f1}\left(1-e^{-\omega_1 t}\right)\cdot[u(t)-u(t-\tau)]\end{aligned}\tag{18}$$

$$\begin{aligned}v_{o2,f1}(t) &= v_{o2,f1}(t_0)e^{-\omega_2(t-t_0)}\\ &\quad+A_1D_{o1}\omega_2v_{o1,f1}(t_0)\cdot\left[\frac{e^{-\omega_1(t-t_0)}}{\omega_2-\omega_1}+\frac{e^{-\omega_2(t-t_0)}}{\omega_1-\omega_2}\right]\\ &\quad+D_{f1}A_1D_{o1}\omega_1\omega_2\\ &\quad\cdot\left[\frac{1-e^{-\omega_1 t}}{\omega_1(\omega_2-\omega_1)}+\frac{1-e^{-\omega_2 t}}{\omega_2(\omega_1-\omega_2)}\right]\\ &\quad\cdot[u(t)-u(t-\tau)]\end{aligned}\tag{19}$$

$$\begin{aligned}v_{o3,f1}(t) &= v_{o3,f1}(t_0)e^{-\omega_3(t-t_0)}\\ &\quad+A_2D_{o2}\omega_3v_{o2,f1}(t_0)\cdot\left[\frac{e^{-\omega_2(t-t_0)}}{\omega_3-\omega_2}+\frac{e^{-\omega_3(t-t_0)}}{\omega_2-\omega_3}\right]\\ &\quad+A_1D_{o1}A_2D_{o2}\omega_2\omega_3v_{o1,f1}(t_0)\\ &\quad\cdot\left[\frac{e^{-\omega_1(t-t_0)}}{(\omega_2-\omega_1)(\omega_3-\omega_1)}\right.\\ &\qquad\left.+\frac{e^{-\omega_2(t-t_0)}}{(\omega_1-\omega_2)(\omega_3-\omega_2)}+\frac{e^{-\omega_3(t-t_0)}}{(\omega_1-\omega_3)(\omega_2-\omega_3)}\right]\\ &\quad+D_{f1}A_1D_{o1}A_2D_{o2}\omega_1\omega_2\omega_3\\ &\quad\cdot\left[\frac{1-e^{-\omega_1 t}}{\omega_1(\omega_2-\omega_1)(\omega_3-\omega_1)}\right.\\ &\qquad+\frac{1-e^{-\omega_2 t}}{\omega_2(\omega_1-\omega_2)(\omega_3-\omega_2)}\\ &\qquad\left.+\frac{1-e^{-\omega_3 t}}{\omega_3(\omega_1-\omega_3)(\omega_2-\omega_3)}\right]\\ &\quad\cdot[u(t)-u(t-\tau)].\end{aligned}\tag{20}$$

Note that these equations are valid only in the interval $t_0\le t\le t_0+\tau$, and the last term of each expression is zero beyond the first period. Assuming the voltage is perfectly hold in the time interval $t_0+\tau<t\le t_0+T_s$, then we have

$$\begin{aligned}v_{o1,f1}((n+1)T_s) &= v_{o1,f1}(nT_s+\tau)\\ v_{o2,f1}((n+1)T_s) &= v_{o2,f1}(nT_s+\tau)\\ v_{o3,f1}((n+1)T_s) &= v_{o3,f1}(nT_s+\tau).\end{aligned}\tag{21}$$

Substitute the time variables with $t_0=nT_s$ and $t=nT_s+\tau$, then the voltages hold by the capacitors at the end of the nth period ($n=1,2,\ldots$) are related by

$$v_{o1,f1}((n+1)T_s)=\beta_1v_{o1,f1}(nT_s)\tag{22}$$

$$v_{o2,f1}((n+1)T_s) = \beta_2 v_{o2,f1}(nT_s) + A_1 D_{o1}\omega_2 \cdot \left(\frac{\beta_1}{\omega_2-\omega_1}+\frac{\beta_2}{\omega_1-\omega_2}\right) \cdot v_{o1,f1}(nT_s) \tag{23}$$

$$v_{o3,f1}((n+1)T_s) = \beta_3 v_{o3,f1}(nT_s) + A_2 D_{o2}\omega_3 \cdot \left(\frac{\beta_2}{\omega_3-\omega_2}+\frac{\beta_3}{\omega_2-\omega_3}\right) \cdot v_{o2,f1}(nT_s) + A_1 D_{o1} A_2 D_{o2}\omega_2\omega_3 \cdot \left[\frac{\beta_1}{(\omega_2-\omega_1)(\omega_3-\omega_1)} + \frac{\beta_2}{(\omega_1-\omega_2)(\omega_3-\omega_2)} + \frac{\beta_3}{(\omega_1-\omega_3)(\omega_2-\omega_3)}\right] \cdot v_{o1,f1}(nT_s) \tag{24}$$

with the initial condition

$$v_{o1,f1}(T_s) = D_{f1}(1-\beta_1) \tag{25}$$

$$v_{o2,f1}(T_s) = D_{f1}A_1 D_{o1}\omega_1\omega_2 \cdot \left[\frac{1-\beta_1}{\omega_1(\omega_2-\omega_1)}+\frac{1-\beta_2}{\omega_2(\omega_1-\omega_2)}\right] \tag{26}$$

$$v_{o3,f1}(T_s) = D_{f1}A_1 D_{o1}A_2 D_{o2}\omega_1\omega_2\omega_3 \cdot \left[\frac{1-\beta_1}{\omega_1(\omega_2-\omega_1)(\omega_3-\omega_1)} + \frac{1-\beta_2}{\omega_2(\omega_1-\omega_2)(\omega_3-\omega_2)} + \frac{1-\beta_3}{\omega_3(\omega_1-\omega_3)(\omega_2-\omega_3)}\right]. \tag{27}$$

When the output voltages are sampled at $t = nT_s$ $(n = 1, 2, \ldots)$, apply z-transform to the sampled sequences $v_{o1,f1}(nT_s)$, $v_{o2,f1}(nT_s)$ and $v_{o3,f1}(nT_s)$. Then, we have

$$V_{o1,f1}(z) = \frac{1}{z-\beta_1} \cdot v_{o1,f1}(T_s) \tag{28}$$

$$V_{o2,f1}(z) = \frac{1}{z-\beta_2} \cdot A_1 D_{o1}\omega_2 \cdot \left(\frac{\beta_1}{\omega_2-\omega_1}+\frac{\beta_2}{\omega_1-\omega_2}\right) \cdot V_{o1,f1}(z) + \frac{1}{z-\beta_2} \cdot v_{o2,f1}(T_s) \tag{29}$$

$$V_{o3,f1}(z) = \frac{1}{z-\beta_3} \cdot A_2 D_{o2}\omega_3 \cdot \left(\frac{\beta_2}{\omega_3-\omega_2}+\frac{\beta_3}{\omega_2-\omega_3}\right) \cdot V_{o2,f1}(z) + \frac{1}{z-\beta_3} \cdot A_1 D_{o1}A_2 D_{o2}\omega_2\omega_3 \cdot \left[\frac{\beta_1}{(\omega_2-\omega_1)(\omega_3-\omega_1)} + \frac{\beta_2}{(\omega_1-\omega_2)(\omega_3-\omega_2)} + \frac{\beta_3}{(\omega_1-\omega_3)(\omega_2-\omega_3)}\right] \cdot V_{o1,f1}(z) + \frac{1}{z-\beta_3} \cdot v_{o3,f1}(T_s). \tag{30}$$

Because there are four time-interleaved paths, the equivalent sampling period of the modulator is a quarter of the period T_s. Therefore, z is replaced with z^4 to count for the contribution of the other three paths. Provided that $R_{eq1}C_1 \gg \tau$, $R_{eq2}C_2 \gg \tau$, and $R_{eq3}C_3 \gg \tau$, the expressions are approximated (with Taylor series) to

$$V_{o1,f1}(z) \approx (\omega_1\tau) \cdot \frac{1}{z^4-\beta_1} \cdot D_{f1} \tag{31}$$

$$V_{o2,f1}(z) \approx (\omega_1\tau)(\omega_2\tau) \cdot \left(\frac{1}{z^4-\beta_2}\frac{1}{z^4-\beta_1} \cdot D_{f1}A_1 D_{o1} + \frac{1}{z^4-\beta_2} \cdot \frac{1}{2} D_{f1}A_1 D_{o1}\right) \tag{32}$$

$$V_{o3,f1}(z) \approx (\omega_1\tau)(\omega_2\tau)(\omega_3\tau) \cdot \left(\frac{1}{z^4-\beta_3}\frac{1}{z^4-\beta_2}\frac{1}{z^4-\beta_1} \cdot D_{f1}A_1 D_{o1}A_2 D_{o2} + \frac{1}{z^4-\beta_3}\frac{1}{z^4-\beta_2} \cdot \frac{1}{2} D_{f1}A_1 D_{o1}A_2 D_{o2} + \frac{1}{z^4-\beta_3}\frac{1}{z^4-\beta_1} \cdot \frac{1}{2} D_{f1}A_1 D_{o1}A_2 D_{o2} + \frac{1}{z^4-\beta_3} \cdot \frac{1}{6} D_{f1}A_1 D_{o1}A_2 D_{o2}\right). \tag{33}$$

Following the same procedure, the transfer function from $v_{f2}(t)$ to $v_{o3}(t)$ is derived as:

$$V_{o3,f2}(z) \approx (\omega_2\tau)(\omega_3\tau) \cdot \left(\frac{1}{z^4-\beta_3}\frac{1}{z^4-\beta_2} \cdot D_{f2}A_2 D_{o2} + \frac{1}{z^4-\beta_3} \cdot \frac{1}{2} D_{f2}A_2 D_{o2}\right) \tag{34}$$

and the transfer function from $v_{f3}(t)$ to $v_{o3}(t)$ is derived as

$$V_{o3,f3}(z) \approx (\omega_3\tau) \cdot \frac{1}{z^4-\beta_3} \cdot D_{f3} \tag{35}$$

with an NRZ DAC pulse shape.

Similarly, an impulsive signal at $t = 0$ is applied to the input of the modulator to evaluate the response. The integration over time should be normalized to the signal fed to the feedback path such that

$$v_{\text{in}}(t) = \tau \cdot \delta(t)$$
$$V_{\text{in}}(s) = \tau. \tag{36}$$

Then, the transfer function from $v_{\text{in}}(t)$ to $v_{o3}(t)$ is derived as

$$V_{o3,in}(z) \approx (\omega_1\tau)(\omega_2\tau)(\omega_3\tau) \cdot \left(\frac{1}{z^4-\beta_3}\frac{1}{z^4-\beta_2}\frac{1}{z^4-\beta_1} \cdot D_{\text{in}}A_1 D_{o1}A_2 D_{o2} + \frac{1}{z^4-\beta_3}\frac{1}{z^4-\beta_2} \cdot D_{\text{in}}A_1 D_{o1}A_2 D_{o2} + \frac{1}{z^4-\beta_3}\frac{1}{z^4-\beta_1} \cdot \frac{1}{2} D_{\text{in}}A_1 D_{o1}A_2 D_{o2} + \frac{1}{z^4-\beta_3} \cdot \frac{1}{2} D_{\text{in}}A_1 D_{o1}A_2 D_{o2}\right). \tag{37}$$

APPENDIX B
CALIBRATION BASED ON LMS ALGORITHM

The foreground calibration employed in the proposed partially time-interleaved BP DSM is illustrated in this appendix.

The calibration is based on an LMS algorithm which is performed in digital domain. Due to the time-interleaved implementation, the feedback DAC in each path is switched on for a quarter of the period and switched off for the rest. Similar to the return-to-zero DAC, the linearity of the modulator does not suffer from ISI caused by the asymmetric rising and falling edges. Since the in-band gain of the first OTA is designed to be about 40 dB, it is reasonable to assume that the system nonidealities are dominant by the input stage.

Considering the mismatch among the four paths, the transfer function of each path at the input stage is rewritten as

$$H_{\mathrm{NPF1},i}(z) = \alpha_{1,i} \cdot \frac{z^{-1}}{1-\beta_{1,i}z^{-1}}, (i = 1, 2, 3, 4) \tag{38}$$

with a sampling period T_s. $H_{\mathrm{NPF1},i}(z)$, $\alpha_{1,i}$ and $\beta_{1,i}$, respectively, represent the transfer function, gain, and attenuation coefficient of the path i. It is noted that the input resistors and the OTAs are shared by the four paths. Then, we should take into account the mismatch of the capacitors $C_{1,i}$ and the feedback resistors $R_{f1,i}$, together with the timing skew $\tau_{1,i}$ in different paths. Therewith, the coefficients $\alpha_{1,i}$ and $\beta_{1,i}$ are, respectively, rewritten as

$$\alpha_{1,i} = \tau_{1,i} \cdot \frac{1}{R_{\mathrm{eq1},i}C_{1,i}} \tag{39}$$

$$\beta_{1,i} = \exp\left[-\tau_{1,i} \cdot \frac{1}{R_{\mathrm{eq1},i}C_{1,i}}\right] \tag{40}$$

where $R_{\mathrm{eq1},i}(= R_{\mathrm{in}}||R_{f1,i})$ denotes the equivalent resistance and $C_{1,i}$ denotes the capacitance in path i. Recall that the RC-constant should be designed to be much larger than $T_s/4$ for a bandpass characteristic, $\alpha_{1,i}$ is approximated to 0 and $\beta_{1,i}$ is approximated to 1. The timing skew manifests as the charging (and discharging) time deviation from the nominal $\tau(= T_s/4)$. When the components mismatch ($\Delta R_{f1,i}$ and $\Delta C_{1,i}$) and the timing skew ($\Delta\tau_{1,i}$) occur, the relative deviation of $\alpha_{1,i}$ and $\beta_{1,i}$ could be derived as (Taylor expansion with first order approximation)

$$\frac{\Delta\alpha_{1,i}}{\alpha_1} \approx \frac{\Delta\tau_{1,i}}{\tau} - \frac{\Delta R_{\mathrm{eq1},i}\Delta C_{1,i}}{R_{\mathrm{eq1}}C_1} \tag{41}$$

$$\frac{\Delta\beta_{1,i}}{\beta_1} \approx -\left(\frac{\Delta\tau_{1,i}}{\tau} - \frac{\Delta R_{\mathrm{eq1},i}\Delta C_{1,i}}{R_{\mathrm{eq1}}C_1}\right) \cdot \alpha_1 \tag{42}$$

where α_1, β_1, R_{eq1}, C_1, and τ are the respective nominal values. It is observed that the mismatch effects on $\beta_{1,i}$ are heavily attenuated by the coefficient α_1. Hence, the major concern is to calibrate the gain mismatch among the paths.

After discussing the effects of mismatch in the proposed BP DSM, we move on to develop the calibration algorithm. Fig. 24 shows the digital bit-streams in the calibration scheme. After fitting the weights of the nonideality terms, the calibrated digital output V_{Dcal} is generated with the contaminated output bit-stream V_{Dout}. The digital output V_{Dout} is the orderly combination of the four time-interleaved sequences V_{D1}, V_{D2}, V_{D3}, V_{D4}. V_{Doff1}, and V_{Doff2} are the predicted idle tones at f_s with 90∘ phase shift, which introduce necessary degrees of freedom in the estimation. Then, the contaminated digital output could

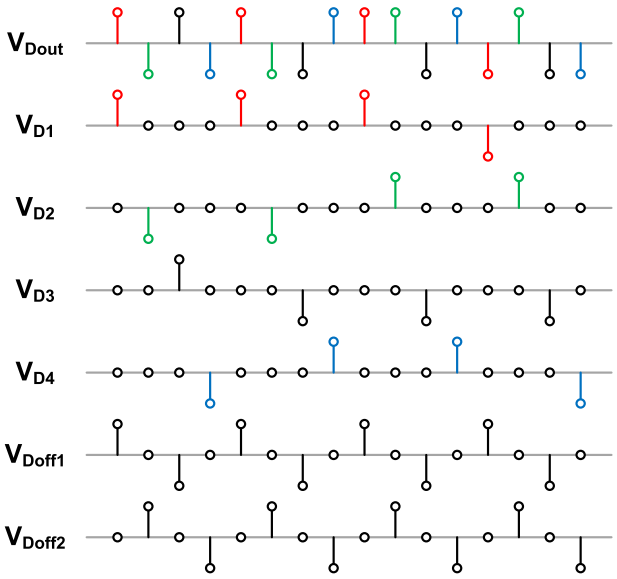

Fig. 24. Digital bit-streams in the calibration scheme.

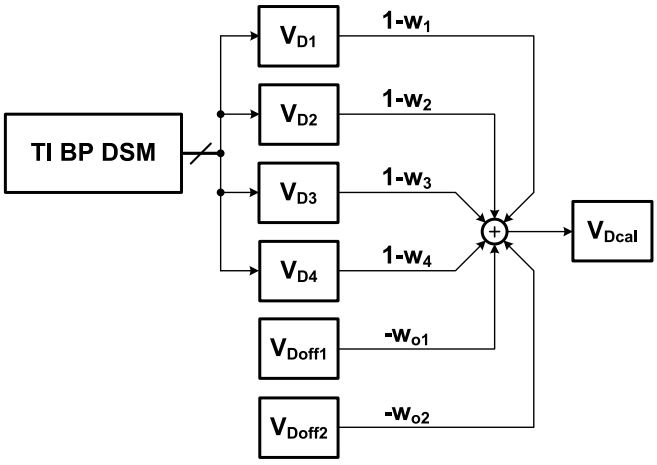

Fig. 25. Block diagram of the digital calibration. The values of these weights (w_i and w_{oi}) are estimated in the foreground as in (47).

be represented by

$$V_{\mathrm{Dout}}[n] = V_{\mathrm{in}}[n] + \sum_{i=1}^{4} w_i V_{\mathrm{D}i}[n] + \sum_{i=1}^{2} w_{oi} V_{\mathrm{Doff}i}[n] + e[n]. \tag{43}$$

The digital output $V_{\mathrm{Dout}}[n]$ is first bandpass-filtered by $B[m]$ to remove the shaped quantization noise $e[n]$. Then, the filtered bit-stream contains the input tones and the nonideal components caused by mismatch. The input $V_{\mathrm{in}}[n]$ is recovered from the peak in-band tone. The nonideal components are expected to be

$$\Delta V_{\mathrm{Dout}}[n] = (V_{\mathrm{Dout}} * B)[n] - (V_{\mathrm{in}} * B)[n] \tag{44}$$

where the symbol $*$ indicates the convolution operation. Therefore, the estimation of the weights w_i and w_{oi} based on the LMS algorithm is translated into minimizing

$$\sum_{n=1}^{N}\left(\Delta V_{\mathrm{Dout}}[n] - \sum_{i=1}^{4} w_i V_{\mathrm{D}i}[n] - \sum_{i=1}^{2} w_{oi} V_{\mathrm{Doff}i}[n]\right)^2 \tag{45}$$

where N is the length of $V_{\text{Dout}}[n]$. With the denotation of weight(s) w and error pattern(s), V_{Derr} in matrix form

$$w = \begin{bmatrix} w_1 & w_2 & w_3 & w_4 & w_{o1} & w_{o2} \end{bmatrix}^T$$
$$V_{\text{Derr}} = \begin{bmatrix} V_{\text{D1}} & V_{\text{D2}} & V_{\text{D3}} & V_{\text{D4}} & V_{\text{Doff1}} & V_{\text{Doff2}} \end{bmatrix} \quad (46)$$

the estimation of w is given by the solution of

$$V_{\text{Derr}}\hat{w} = \Delta V_{\text{Dout}} \quad (47)$$

in the LMS sense. The digital calibration diagram is depicted in Fig. 25. As the four-phase clock generator will cause different clock skews for different IF, $\hat{w}$ in (47) need to be reestimated when the IF changes. Last, if needed, one can remove the tones at dc and Nyquist frequency with a modified digital algorithm by changing the bandpass filter in (44) to a comb filter and adding more correction terms.

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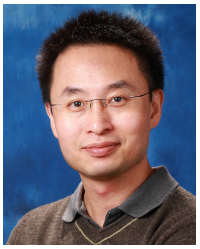
Wei Jin (Member, IEEE) received the B.S. degree in electrical engineering from Zhejiang University (ZJU), Hangzhou, China, in 2016, the M.Sc. degree in mixed-signal microelectronics from Eindhoven University of Technology (TU/e), Eindhoven, The Netherlands, in 2017, and the Ph.D. degree in electronic engineering from The Chinese University of Hong Kong (CUHK), Hong Kong, in 2024.

His research work focuses on power-efficient wideband delta-sigma modulators for wireless communication.



Kong-Pang Pun (Senior Member, IEEE) received the B.Eng. and M.Phil. degrees in electronic engineering from The Chinese University of Hong Kong (CUHK), Hong Kong, in 1995 and 1997, respectively, and the Ph.D. degree in electrical and computer engineering from the Instituto Superior Técnico, Technical University of Lisbon, Lisbon, Portugal, in 2001.

In 2001, he joined the Department of Electronic Engineering, CUHK, as a Faculty Member, where he is currently a Professor. His current research focuses on high power-efficiency circuits for data converters, particularly delta-sigma modulators, as well as circuits for wearable biomedical devices and optical interfaces.

Dr. Pun served as the Chairperson for the IEEE Hong Kong Joint Chapter of the Electron Devices Society and the Solid-State Circuits Society in 2008 and 2009. He was the General Co-Chair and the Technical Program Co-Chair for the IEEE International Conference on Electron Devices and Solid-State Circuits in 2008 and 2016, respectively, and a member of the International Technical Committee of the IEEE International Solid-State Circuits Conference from 2008 to 2012. He has contributed as a Guest Editor of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS 2015 special issue on "Next-Generation Delta-Sigma Converters" and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS 2009 special issue on "Circuits and Systems Solution for Nanoscale CMOS Design Challenges."