A Phased-Array Transceiver With 2-Dimension Continuously Auto Link-Tracking Operation and Time Division Modulator

Xun Luo, *Senior Member, IEEE*, Bingzheng Yang, *Member, IEEE*, Zhixian Deng, *Member, IEEE*, Wen Chen, *Graduate Student Member, IEEE*, Yiyang Shu, *Member, IEEE*, and Jie Zhou, *Member, IEEE*

***Abstract*— This work presents an eight-element 23–40 GHz continuously auto link-tracking phased-array transceiver (TRX) with a time division modulator in a conventional 40-nm CMOS technology. Such a TRX array can support fast auto-beam-steering in both receiver (RX) and transmitter (TX) arrays. The link-tracking loop is introduced to generate the phase and amplitude control codes of the RX array, which can automatically steer the RX beam to the unknown target direction to establish the RX link. After the RX link is located, the link-tracking loop provides a phase control code to steer the TX beam toward the target. Meanwhile, the time division modulator consists of four digital power amplifiers (DPAs), a quadrature signal generator, and a sign-map circuit. The time division modulator can not only tune the LO power for RX gain flatness improvement but also provide a baseband-to-RF direct conversion in TX mode. The measured link-tracking time and peak TX system efficiency are 7 μs and 25.3%, respectively, while the proposed TRX array can support 4.8 Gb/s 64-QAM and 8 Gb/s 16-QAM transmission.**

***Index Terms*— Digital power amplifier (DPA), link-tracking, millimeter-wave (mm-wave), phased-array, time-division modulator, transceiver (TRX), wideband.**

I. Introduction

THE increasing demands on high-data-rate and low-latency wireless communication drive the development of integrated millimeter-wave (mm-wave) phased-array transceiver (TRX), especially for the 5G-NR FR2 application. Recently, various phased-array TRX operated at 24/28 GHz [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], 37/39 GHz [15], [16], [17], [18], [19], [20] bands, and 28/39 GHz [21], [22], [23] bands for 5G mm-wave operations are reported. However, the research on the wideband phased-array TRX that can fully cover the 24/28/37/39 GHz bands is limited. The wideband TRX array is expected to support multi-standard with practical multi-functions. Besides, a large-scale array with high array gain is often used in mm-wave phased-array wireless systems to overcome the relatively larger path loss, which results in a narrow beamwidth and makes the transmission/reception (T/R) link hard to alignment. In general, establishing stable T/R links requires a complex phase-shifting algorithm and power-hungered digital processor. However, in specific high-speed systems (e.g., drone and vehicle), the communication targets are moving quickly and randomly, which results in rapid-changing T/R links. The establishing of stable T/R links is even more complex in such applications. Therefore, the array systems that can support fast beam-tracking are dramatically demanded.

Conventional self-steering arrays perform an auto beam-tracking operation based on coupled-oscillator [24], [25] architectures. However, the phase-shifting range of the coupled-oscillator array is limited. Recent studies on the self-steering array introduce autonomous spatial filter (ASF) based on an all-passive negative feedback network [26], [27], [28], which can achieve auto beam-tracking without any limitation of phase-shifting range. Meanwhile, such an ASF-based array enhances or reduces the strongest signal received from the array. Nonetheless, the phased-array receivers (RXs) based on ASF can only support 1-D antenna array [26], [27], or 2-D antenna array with specific layout [28]. Recently, a hybrid-beamforming with minimum mean-square error (mmse) beam adaptation technique has been proposed for carrier aggregation and multi-stream [21]. The baseband signals are sampled and fed to a digital logic circuit to generate the control codes of programmable-gain amplifiers (PGAs). Then, the beam and null tracking are achieved. Furthermore, the aforementioned techniques for self-steering array are only implemented on the RX, which limits the application in multi-function wireless systems. Therefore, the design of a TRX array that can support arbitrary 2-D auto T/R link-tracking still remains a great challenge.

Except for the link-tracking for communication with high-speed targets, other concerns for the mm-wave phased-array TRX application include the relatively larger power consumption. Meanwhile, the free-space path loss is increased with higher operation frequency, the wireless systems require the multi-element TRX array to improve the link-budget for high-data transmission. The power consumption is multiplied with the increasing of TRX channels. Since the transmitter (TX)

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The authors are with the Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China (UESTC), Shenzhen 518110, China, and also with the Center for Advanced Semiconductor and Integrated Micro-System, UESTC, Chengdu 611731, China (e-mail: xun-luo@ieee.org).

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provides enough output power to establish a wireless link, the power consumption of the TRX array is most contributed by integrated TXs. However, the increasing operation frequency leads to the power efficiency degeneration of the transistor due to process limits, which results in higher power consumption of mm-wave TXs compared to sub-6-GHz designs. Therefore, the increasing power consumption of mm-wave phased-array TRX is a critical issue. Digital TX provides improved system power efficiency by introducing a direct digital-to-RF modulation function [29], [30], [31], [32], [33]. Nonetheless, the design of phased-array TRX with direct digital-to-RF modulated TX suffers from concerns that the LO frequencies for RX and TX are different. The LO frequency is equal to the RF frequency in the digital TX architecture, while high-performance RX generally utilizes heterodyne architecture with different LO and RF frequencies to avoid the LO leakage, flick noise, and even-order distortion from interfering with the weak receiving signal [34]. Therefore, different LO frequencies are required for the digital TX and heterodyne RX, which makes the design of high-performance and high-efficiency phased-array TRX with a great challenge.

This article is an extension of the author's previous work [35] with an in-depth analysis of the operation of continuous auto link-tracking with time division modulation, which presents a 23–40 GHz phased-array TRX in a conventional 40-nm CMOS technology. The proposed phased-array TRX features two advantages to address the aforementioned issues as follows.

1) A link-tracking loop is utilized in each TRX channel, which generates the control codes for auto-beam-steering in each RX and TX, respectively. Therefore, the proposed phased array TRX can support auto T/R link-tracking with an arbitrary 2-D array antenna.
2) A time division modulator driven by an ON-chip wideband fast-locking phase lock loop (PLL) is used to control the gain of the LO signal in RX mode and generate modulated RF signal in TX mode, respectively.

Thus, the high-efficiency digital TX and high-performance RX can be integrated into the phased-array TRX, simultaneously. Based on the aforementioned mechanisms, the proposed phased-array TRX is designed and implemented in a conventional 40-nm CMOS technology for verification, while the measured results exhibit state-of-the-art performance. The article is organized as follows. The prototypes with principle and theoretical analysis of the link-tracking and time division modulation operation are discussed in Section II, while Section III presents the circuit implementation. In Section IV, the proposed phased-array TRX is fabricated, measured, and compared with the state-of-the-arts. The conclusion is summarized in Section V.

II. Principle and Operation

A. Architecture

Fig. 1 shows the architecture of the proposed phased-array TRX, which consists of eight TX/RX channels, a one-time division modulator, and a fast-locking PLL. Each pair of TX and RX shares the same antenna interface by a switch, while

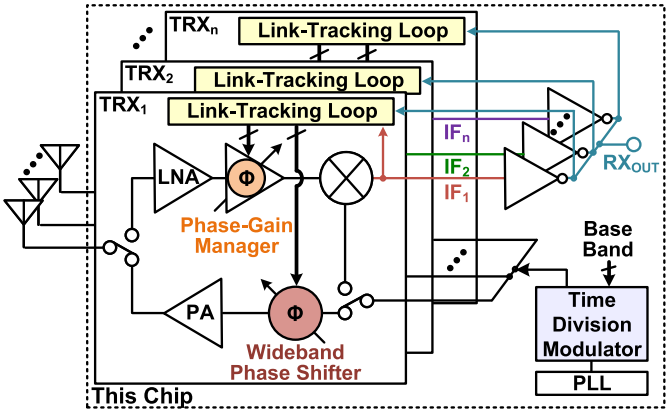

Fig. 1. Architecture of the proposed phased-array TRX.

each channel consists of a link-tracking loop for automatical beam-steering of the phased-array TRX. In the RX, a wideband low noise amplifier (LNA) is used to provide low NF, while a phase-gain manager [36] is utilized for phase and gain tuning. An inverter is introduced for IF amplifying before n-element RXs are combined as a single output RX_{OUT}. Here, the IF signal of each RX (i.e., $IF_m, m = 1, 2, \ldots, n$) and the RX_{OUT} are injected into the link-tracking loop for phase difference (PD) and amplitude detection. The IF signal is used for a link-tracking loop since the relatively low operation frequency reduces the circuit complexity and improves the detection accuracy. Then, the link-tracking loop generates control codes to tune the phase and amplitude of the phase-gain manager. In the TX, a wideband power amplifier (PA) with high output power and efficiency is utilized, while the phase shifting in TX is performed by a vector-sum [37] based wideband phase shifter. Meanwhile, a time division modulator connected with fast-locking PLL is utilized to generate the LO signal for RX and modulated RF signal for TX, and a dividing network loaded with switches is employed for the power distribution of n-element TRX. To clarify the aforementioned principles and guide the implementation of the proposed phased-array TRX, the rest of this section provides the detailed operation and principle of the continuous auto link-tracking and time division modulator.

B. Phased-Array TRX With Continuously Auto Link-Tracking

Fig. 2 shows a simplified model of a phased-array TRX with shared antenna interfaces. For a signal from a certain angle of incidence, due to the various distances from the antennas to the signal source (i.e., communication target), the signal arrives at each antenna element of the RX array with a PD. Then, for the RX array, the phase-shifter in each element provides phase-shifting $-\varphi_m$, $m = 1, 2, \ldots, n$ to compensate the PD, hence combines the signal from each RX in-phase at the single output interface RX_{OUT}. For the TX array steering to the same target direction, the phase-shifter is set to duplicate the PD of the RX array at the shared antenna interface. Then, the required phase-shifting at each phase shifter is equal to φ_m, $m = 1, 2, \ldots, n$. Therefore, to steer the beam T/R link to the same target direction, the phase-shifting of each TX element (i.e., φ_{TXm}) equals to the minus of φ_{RXm}.

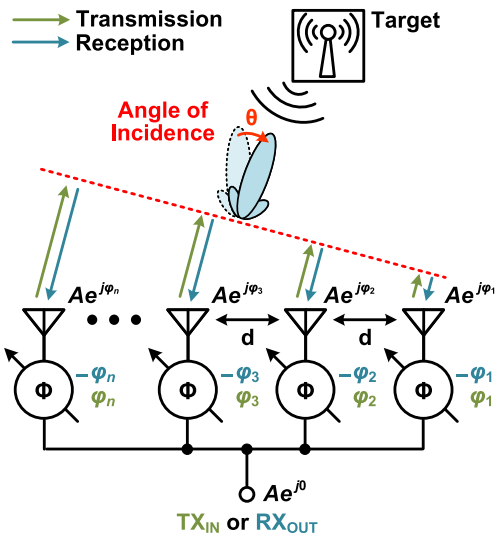

Fig. 2. Concept of a phased-array TRX with shared antenna interface.

Based on the basic principle of the aforementioned T/R beam steering, a three-step T/R link tracking procedure is proposed. As shown in Fig. 3(a), the phase setting in each TRX is identical in the initial state. Once the RX array receives a signal from a target direction, the RX array generates IF signals (i.e., $\mathrm{IF}_m, m = 1, 2, \ldots, n$) with different phases in each RX element. Note that the generated IF signals in each RX channel contain different phase information, which is significant for link tracking. Thus, a mixer for each RX channel is necessary. Besides, compared to the received RX signals, the down-converted IF signals are easier to process in the link tracking loop. Assuming the gain and receiving power in all RXs are equal, then the amplitude of the IF signal in the RX array is identical (i.e., A_{IF}). Thus, the IF signal in each RX element is expressed as

$$\mathrm{IF}_m = A_{\mathrm{IF}} e^{j\varphi m}. \tag{1}$$

Then, those IF signals are combined as a single output $\mathrm{RX_{OUT}}$. An inverter is utilized before combining the IF signals, assuming the gain of the ideal inverter is 1, the $\mathrm{RX_{OUT}}$ is calculated as

$$\mathrm{RX_{OUT}} = \sum_{m=1}^{n} A_{\mathrm{IF}} e^{j\varphi m} e^{j\pi} = -nA_{\mathrm{IF}} \sum_{m=1}^{n} e^{j\varphi m}. \tag{2}$$

Equation (2) suggests that the phase of $\mathrm{RX_{OUT}}$ is equal to the inverse of combined IF signals. As mentioned above, the goal of RX link-tracking is to compensate for the PD between each RX. Thus, the $\mathrm{RX_{OUT}}$ is used as a common reference for all RX elements, while the phase tracking target of each RX is defined by the inverse of $\mathrm{RX_{OUT}}$. As shown in Fig. 3(b), in RX link-tracking procedure, each RX detects the PD between IF signal and $\mathrm{RX_{OUT}}$, then the phase shifter provides phase-shifting φ_{RXm} to compensate the PD. Therefore, identical IF signals are obtained in all RX elements, while the RX beam is steered to the target direction to establish the RX link. By repeating the aforementioned two procedures, the RX array can track the movement target continuously. In the TX array, all TX elements share a single input $\mathrm{TX_{IN}}$. In the initial state,

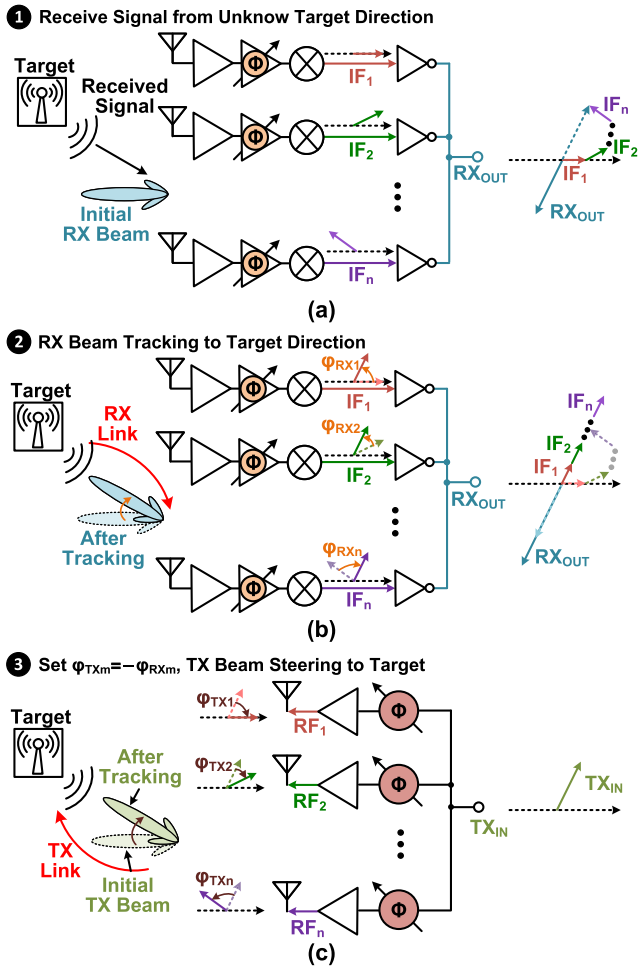

Fig. 3. Concept of the proposed three-step T/R link-tracking procedure. (a) Initial state. (b) RX link-tracking. (c) TX link tracking.

the phase setting of each TX is identical, resulting in an initial TX beam perpendicular to the antenna array. To steer the TX beam toward the target direction for establishing TX link, the phase-shifting of each TX element (i.e., φ_{TXm}) equals to $-\varphi_{\mathrm{RXm}}$, as shown in Fig. 3(c).

In specific practical applications, the communication target moves quickly and randomly, while the rapid-changing received power causes the saturation of the RX element. Meanwhile, the amplitude difference between each RX element causes the degeneration of array gain and sidelobe suppression [16]. Therefore, an auto gain-control (AGC) function is also required in the proposed link-tracking loop to equalize the conversion gain of each RX element. Besides, to provide a continuous tracking operation, the gain and phase codes are updated in real-time. Fig. 4(a) shows the proposed link-tracking loop with auto RX phase/gain control and TX phase control. In the RX mode, the amplitude detector reads the IF signal and generates a related analog voltage V_{AD}. The V_{AD} is compared with a reference voltage V_{AR} and obtains an amplitude error (AE) code. The amplitude target of the IF signal is depended on V_{AR}, while V_{AR} is assigned to avoid the saturation of the RX element. The gain-control code is automatically adjusted according to the AE code. Meanwhile, a detector calculates the PD between IF and $\mathrm{RX_{OUT}}$ signals.

Since the inverters are used for combining the eight-element IF signals to RX_{OUT}, the PD of each element is 180° as the RX beam steering to the target direction. Therefore, the detected PD is compared with 180°, and the phase error (PE) code is obtained according to the comparison result. Besides, the PE code drives all the IF signals close to the reversed resultant RF signal. Although the direction of the resultant RF signal might be changed, each IF signal is still more approximate to the reversed resultant RF signal after each phase change. Note that the locking condition is all IF signals feature the same phase, which means the final phase of the resultant signal is not concerned. Therefore, the locking condition is properly achieved using the proposed auto link-tracking algorithm.

Fig. 4(b) exhibits an example of the proposed continuous tracking procedure. The phase of the tracking target is defined as the reverse of RX_{OUT}, while the amplitude of the tracking target is depended on V_{AR}. The phase-shifting of the IF signal in the initial state is higher than the tracking target, while the amplitude is smaller than the target. Thus, the phase-shifting is decreased with increased gain. Since the phase-shifting function in the proposed TRX array is achieved based on vector-sum, the phase control code provides 90° phase-shifting in each quadrant. Therefore, a quadrant change operation is executed, once the phase-shifting of the IF signal reaches the edge of each quadrant. Each quadrant change results in a 90° phase-shifting, which features a tracking-speed improvement once the IF signal is two quadrants away from the target. In this example, the phase and amplitude are smaller than the target after the quadrant change. Thus, the gain and phase-shifting are increased before the IF signal is allocated close to the tracking target for accomplishing the RX link-tracking. The phase-shifting in RX (i.e., $-\varphi_{RX}$) is calculated for TX link-tracking procedure. The TRX link-tracking is accomplished by setting the TX phase-shifting φ_{TX} equal to $-\varphi_{RX}$.

As shown in Fig. 4, to obtain a constant phase detected voltage during link-tracking, the input signals for the link-tracking loop are continuous-wave (CW) signals. Besides, the current proposed link-tracking loop is aimed at automatically searching the signal with the largest power. Compared to the conventional RF phase-shifting phased-array system, the control codes for phase/gain manager are automatically generated in the RX. Note that the link-tracking loop is only operating on the phase and amplitude code generation. Therefore, similar to the RF phase-shifting phased arrays, the co-channel blocker cannot be canceled, while the null cannot be steering directly. To cancel the co-channel blocker and steer null, additional efforts on phase/amplitude code are required in the digital domain.

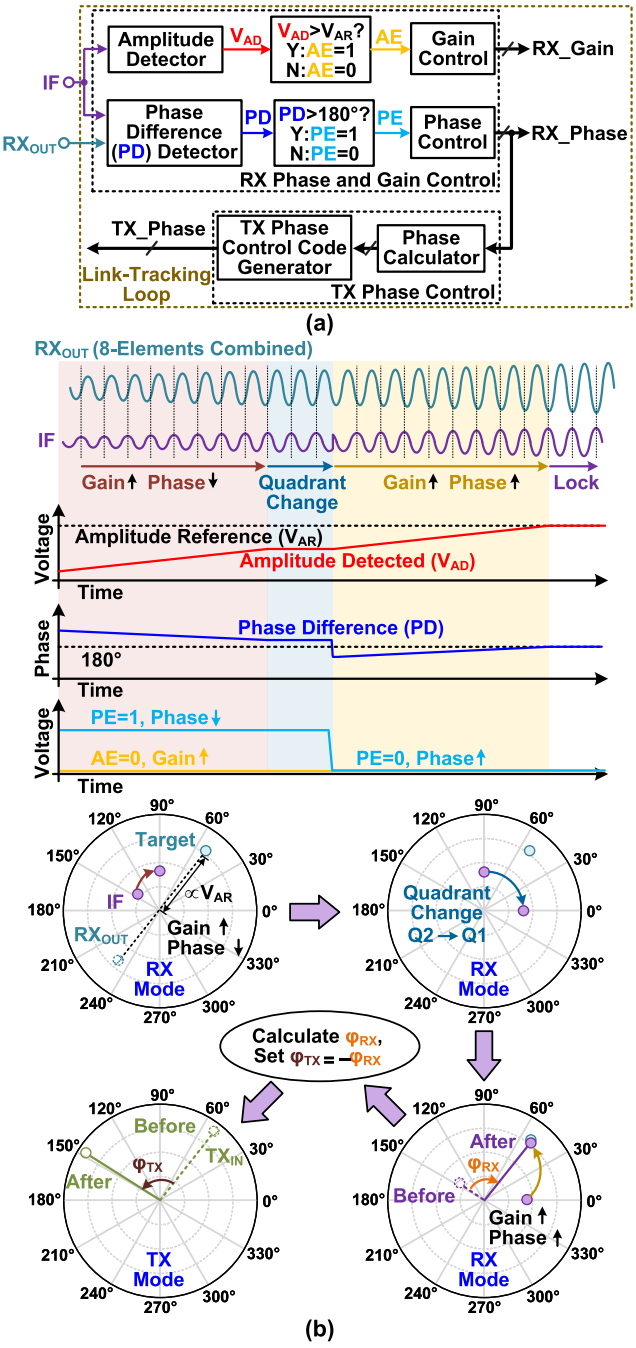

Fig. 4. (a) Block diagram of the proposed link-tracking loop. (b) Example of continuously tracking procedure.

C. Time Division Modulation

Conventional heterodyne TX requires a power-hungered digital-to-analog converter (DAC), a high-linear mixer, and a driver chain to generate a high-speed modulated RF signal with enough power level to drive the PA. The system efficiency and integration level are not easy to improve in such a TX architecture. Meanwhile, a major challenge for wideband RX design is that the power of the LO source varies in different frequencies, this ripple of in-band LO power significantly affects the conversion gain flatness. By introducing a variable gain LO driver to compensate for the power variation, the gain flatness of RX is improved. Therefore, to address the aforementioned design challenge for high-efficiency TX and wideband RX with improved gain flatness, the time division modulation is introduced. The basic concept of time division modulation is to reconfigure the function of the time division modulator in RX- and TX-modes. Such a time-division modulator can generate a signal with programmable power and phase based on the control codes, while the carrier frequency is depended on the output signal of PLL. As shown in Fig. 5(a), the

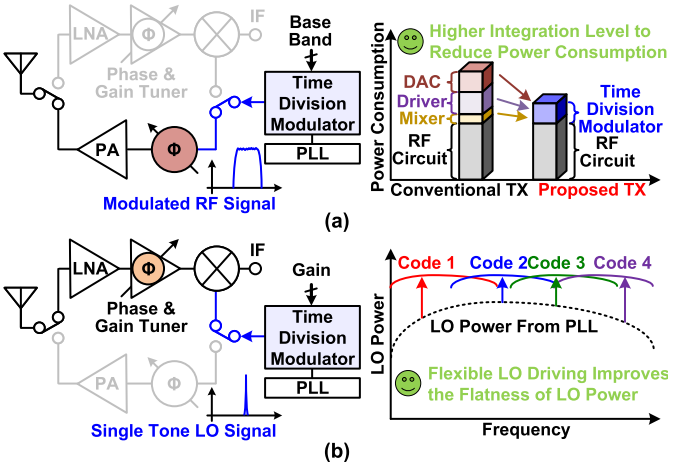

Fig. 5. Concept of the time division modulation TRX. (a) TX mode. (b) RX mode.

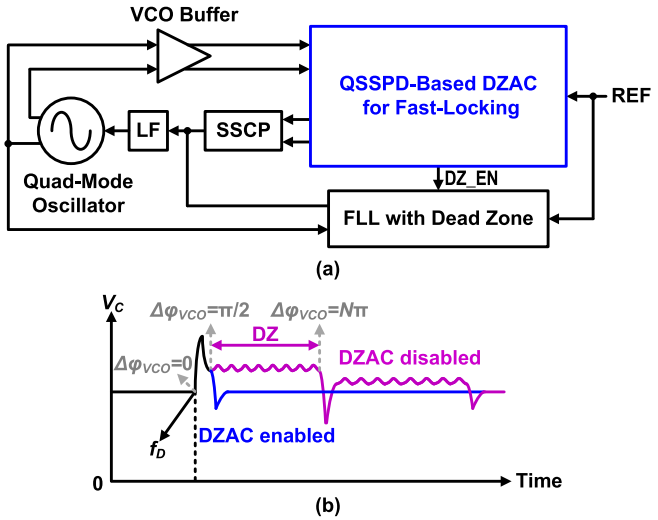

Fig. 6. (a) Block diagram of the proposed fast-locking PLL. (b) Locking behavior of the proposed fast-locking PLL.

baseband signal is injected into the time division modulator for amplitude and phase control in TX mode, while the time division modulator directly converts the baseband signal into the modulated RF signal. Thus, by integrating the multiple functions of DAC, driver, and mixer, the proposed TDM increases the integration level and reduces the overall power consumption. In RX mode, the time division modulator is a LO driver with single-tone signal output, the gain control code is utilized to adjust the output power of the time division modulator, as shown in Fig. 5(b). Therefore, the gain of the time division modulator can be flexibly tuned to compensate for the LO power variation in different frequencies, which improves the flatness of LO power within a wideband. Note that the proposed TX is a direct-conversion scheme, while the RX is configured in a heterodyne architecture. Thus, the required LO frequencies are different in the proposed TX and RX under the same RF frequency. To support a low-latency wireless link with fast T/R switching, the PLL is designed with the capability of fast-locking.

Fig. 6(a) shows the block diagram of the proposed wideband fast-locking sub-sampling PLL (SSPLL) with quadrature sub-sampling phase detector (QSSPD)-based dead-zone automatic controller (DZAC) [40]. Such PLL consists of two feedback loops, i.e., a sub-sampling loop (SSL) and a frequency-locked loop (FLL). The SSL is used for close-in phase lock to achieve low in-band phase noise, while the FLL is introduced to ensure correct frequency locking. Note that a QSSPD-based DZAC is implemented to achieve fast switching between the two loops. Here, the FLL is instantly switched on as the PE exceeds the phase-detecting range of SSPD. During the locking state, only the SSL is active, while the FLL is disabled without any jitter degradation. When the PLL loses lock due to a disturbance, the output of DZAC (i.e., DZ_EN) is used to enable or disable the DZ.

Meanwhile, once the fast-locking SSPLL is pushed out of the lock by a disturbance, the FLL engages the relocking process once PE exceeds $\pi/2$ referring to the integrated voltage-controlled oscillator (VCO). Due to the disturbance, there is an error voltage $\Delta V_C(t)$ on the VCO control voltage. The changed $\Delta V_C(t)$ leads to a phase variation (i.e., the integral of $2\pi K_{\mathrm{VCO}}\Delta V_C(t)$). Note that the PE reaches a magnitude of $\pi/2$ after a lock-reacquisition time T calculated from

$$\left|\int_0^T 2\pi K_{\mathrm{VCO}}\Delta V_C(t)dt\right| = \frac{\pi}{2}. \tag{3}$$

However, for the DZAC disabled, the time for allocating the FLL is

$$\left|\int_0^{T'} 2\pi K_{\mathrm{VCO}}\Delta V_C(t)dt\right| = N\pi \tag{4}$$

where N is the division ratio and the value of DZ is π. Fig. 6(b) shows an example of locking behavior. Once $\Delta\phi_{\mathrm{VCO}}$ is larger than $\pi/2$, the FLL is switched on immediately (i.e., the blue line). For comparison, the violet line exhibits the case for disabled DZAC, where the FLL remains inactive until the PE exceeds the DZ (i.e., $N\pi$) with a long locking time. Therefore, (3) and (4) reveal that by using QSSPD-based DZAC, the long locking time caused by the dead zone of FLL is eliminated.

III. Implementation

A. Phased-Array TRX

Fig. 7 exhibits the block diagram of the proposed eight-element phased-array TRX. In the proposed RX, the noise-canceling LNA and phase-gain manager [36] are utilized in each RX element. The noise-canceling LNA reduces the NF within the wide operation frequency range, while the phase-gain manager can not only provide adjustable phase shifting and gain but also achieve a dual-mode image-rejection function [7]. In the proposed TX, a three-stage PA is connected with a vector-sum-based wideband phase shifter. Meanwhile, a link-tracking loop is used to control the TRX element for auto-beam-steering in both RX and TX, respectively. As shown in Fig. 8(a), the 14-bit phase-gain manager consists of two 7-bit RFVGAs, four mixers, four pairs of 5-bit

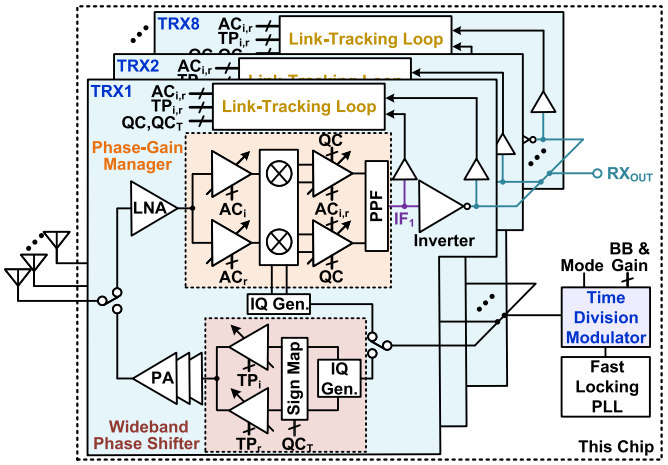

Fig. 7. Block diagram of the proposed eight-element phased-array TRX.

IFVGAs with 2-bit sign-control, and four differential amplifiers. By adjusting the quadrant control code (i.e., QC) and the overall gain of i- and r-paths (i.e., $A_{i1}A_{i2}$ and $A_{r1}A_{r2}$), the phase-gain manager can generate an output signal with arbitrary phase-shifting and gain [22], as shown in Fig. 8(b). Here, the gain A_{PG} of phase-gain manager is

$$A_{\mathrm{PG}} = \sqrt{A_{r1}^2 A_{r2}^2 + A_{i1}^2 A_{i2}^2} \tag{5}$$

while the phase-shifting P_{PG} is

$$P_{\mathrm{PG}} = \tan^{-1}\left(\frac{A_{i1}A_{i2}}{A_{r1}A_{r2}}\right). \tag{6}$$

Note that the gain of i- and r-paths are adjusted by amplitude control codes of AC_i and AC_r. As depicted in Fig. 8(b), the gain control of i- and r-paths are split into the combination of amplitude control A and phase control P expressed as follows:

$$\begin{cases} \mathrm{ac}_i = A + P \\ \mathrm{ac}_r = A - P. \end{cases} \tag{7}$$

Here, the polarity of A is depended on the sign control code QC, while the absolute value of A is larger than that of P (i.e., $|A| > |P|$). Therefore, by combining the phase and amplitude control codes generated by the link-tracking loop, the phase-shifting and gain of the proposed RX can be flexibly adjusted.

As shown in Fig. 9, the wideband IQ generator is introduced to drive the following vector-sum phase shifter in each TX [22], [37]. The schematic of the 2 × 9-bit phase shifter is shown in Fig. 9, which is composed of two quadrature vector modulated VGAs with current-DACs. It combines the amplitude-modulated quadrature signals in the current domain to synthesize the desired phase-shifting of signal $\mathrm{PS}_{\mathrm{out}}$. The output quadrant is controlled by the sign-bit $\mathrm{EN_I}$ and $\mathrm{EN_Q}$. $\mathrm{LO_{IP}}$ and $\mathrm{LO_{IN}}$, $\mathrm{LO_{QP}}$ and $\mathrm{LO_{QN}}$ are input differential LO signals. The binary codes PI[7:0] and PQ[7:0] are used to control the output current for the I and Q paths, respectively. Following the phase shifter, a two-stage PA is proposed, as shown in Fig. 10. For higher output power, the cascode structure with 2VDD supply (i.e., 2.2 V) is adopted for the driver and output stage of the PA. The driver stage

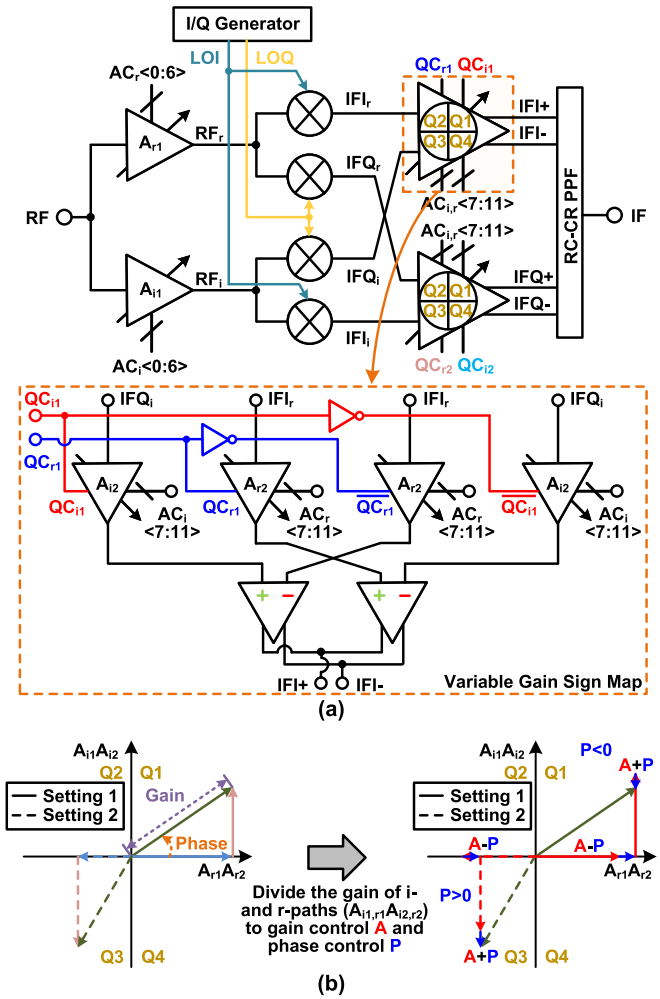

Fig. 8. (a) Schematic of the proposed phase-gain manager in RX. (b) Phase and gain control function of the proposed phase-gain manager.

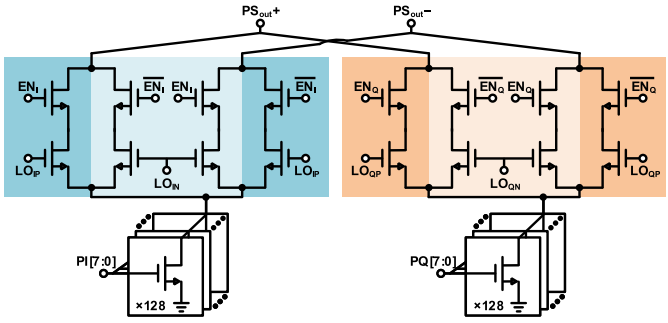

Fig. 9. Schematic of the 2 × 9-bit vector-sum phase shifter.

uses the transistors with the size of 90 μm/40 nm to save dc power consumption with improved efficiency. The last output stage adopts the 300 μm/40 nm transistor for linear output power. The input, interstage, and output matching use transformer-based networks for wideband and low-loss operation. The simulated saturated output power (P_{sat}) and drain efficiency (DE) of the PA are shown in Fig. 10, which exhibits the peak P_{sat} of 17.5 dBm and DE of 33.6%.

A single pole double throw (SPDT) switch is used in this work for TX and RX switching, as shown in Fig. 11, which

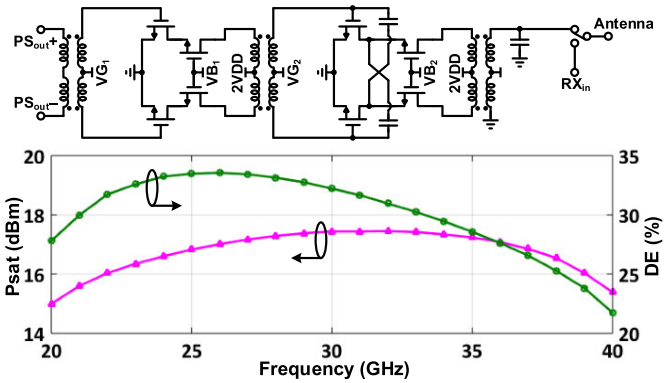

Fig. 10. Schematic and simulated P_{sat} and DE of the PA.

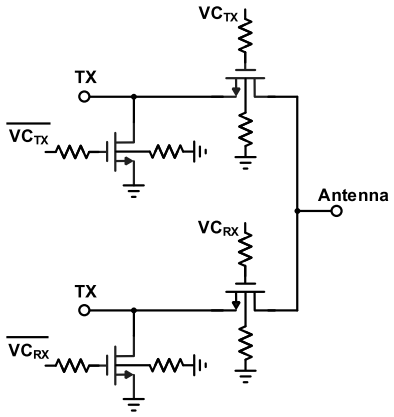

Fig. 11. Schematic of the SPDT switch.

features a minimum loss of 1.1 dB with typical 20.3 dB TX/RX isolation in 20–43 GHz frequency range.

B. Link-Tracking Loop

Based on the principle and operation of the continuously auto T/R link-tracking function, a link-tracking loop is designed and implemented. The block diagram of the proposed TRX with a link-tracking loop is shown in Fig. 12. The reference voltages for amplitude and PD comparisons (i.e., V_{AR} and V_{PR}) are provided by an OFF-chip reference voltage generator. Such reference voltages determine the tracking target. As mentioned in Section II, the amplitude target is allocated to achieve improved system linearity, while the target of PD between IF and RX_{OUT} is 180°. In the RX link-tracking loop, the PD between IF signal and RX_{OUT} is detected by a phase-difference detector. A triple-state comparator generates PE code PE based on the PD, i.e., PE = 1 for PD > V_{PR} and PE = 0 once PD < V_{PR}, respectively. Meanwhile, the amplitude detector transfers the power of the IF signal into a voltage V_{AD}. The V_{AD} is compared with V_{AR} in the triple-state comparator to generate the AE code (i.e., AE). Then, the phase- and amplitude-controllers driven by a clock update the RX phase- and gain-control codes based on the PE and AE, respectively. Finally, the amplitude and phase-control codes are combined to tune the phase and gain of the phase-gain manager in each RX element. Here, once the amplitude and phase of the IF signal are allocated close to the tracking target,

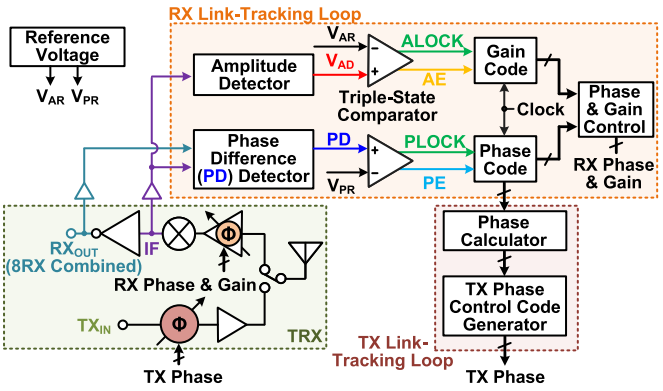

Fig. 12. Configuration of the proposed link-tracking loop in each TRX element.

the triple-state comparator for amplitude and PD comparison can generate A_{LOCK} and P_{LOCK} signals to lock gain- and phase-control codes, respectively. The TX link-tracking loop consists of a phase calculator and a phase control code generator. After the RX link-tracking is completed as the TRX operates in TX mode, the phase calculator reads out the RX phase control code to calculate the related phase setting. The calculated phase setting is transmitted to the TX phase control code generator, where the TX phase control code is generated based on the RX phase-setting. Therefore, by repeating the aforementioned procedures, the continuous T/R link-tracking is completed. Note that the proposed link tracking loop is aimed at the direction of the beam pattern. For the co-channel blocker cancellation and null tracking, the triple-state comparators can be replaced by ADCs and digital processors. The phase and amplitude of IF signals can be converted into digital codes by the ADCs, and then be processed in the processor to generate the required gain and phase control codes for a phase-gain manager.

The key circuit to increase the tracking accuracy is the PD detector, which is shown in Fig. 13(a). Compared with the conventional PD detector using AND gate, the proposed circuit based on edge detection provides a simple method for 360° PD detection. Note that a detailed discussion of the PD detector is shown in the Appendix. Two input signals (i.e., IF and RX_{OUT}) are transferred to the square-wave by buffer chain, then the edge-to-pulse circuit generates a pulse in each rising edge of a square-wave signal. The pulse trigger is designed using two series of connected transmission gates. The upper and lower transmission gates are connected to VDD and GND, respectively, while the inter-connection point of the two transmission gates is the output port. The upper and lower transmission gates driven by the pulses shift the output voltage to VDD and GND, respectively, hence the duty cycle of the output signal is related to the delay of pulses. Finally, an integrator is tapped at the output port to transfer the duty cycle of the output signal into a voltage (i.e., PD). Therefore, the PD between two input signals is transferred to the voltage of PD. Fig. 13(b) shows the output response of the proposed PD detector, which is close to the ideal linear response. Meanwhile, the reference voltage V_{PR} equals the output voltage with 180° PD. The phase detector works under

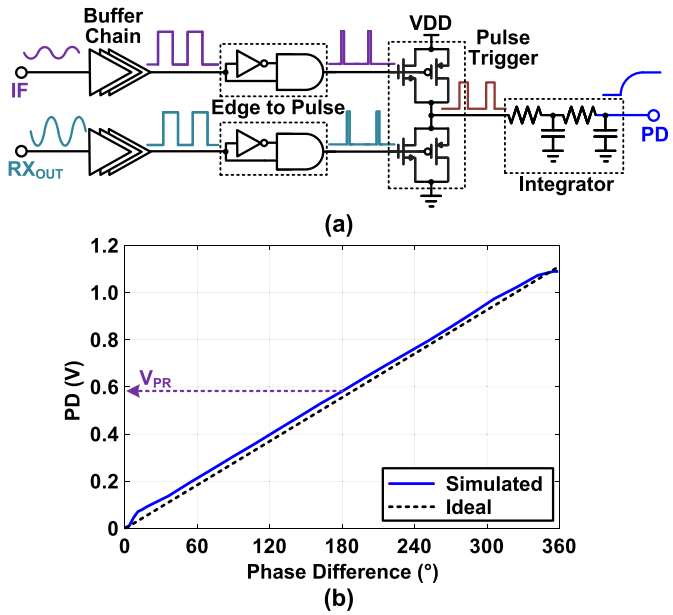

Fig. 13. (a) Schematic of the proposed PD detector. (b) Simulated output response of the proposed PD detector.

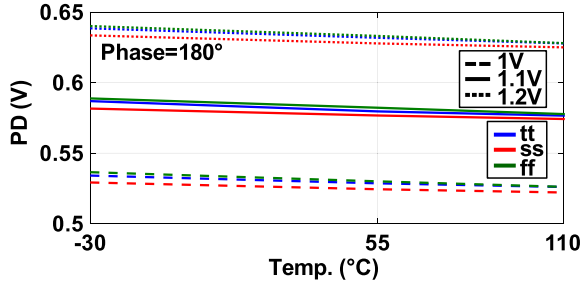

Fig. 14. Simulated PD of the proposed PD detector under PVT variations (PD = 180°).

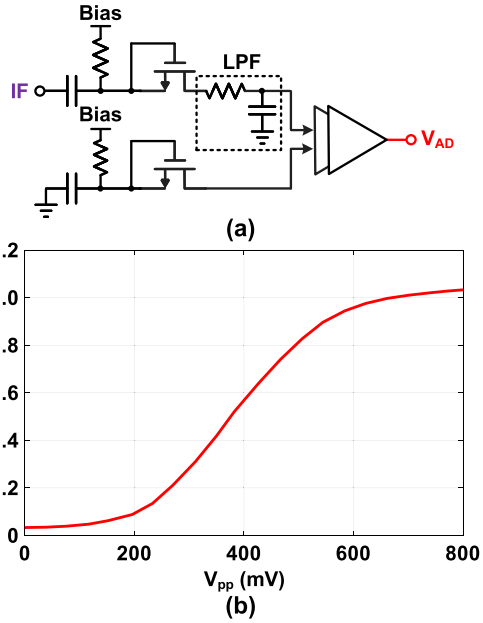

Fig. 15. (a) Schematic of the proposed amplitude detector. (b) Simulated output response of the proposed amplitude detector.

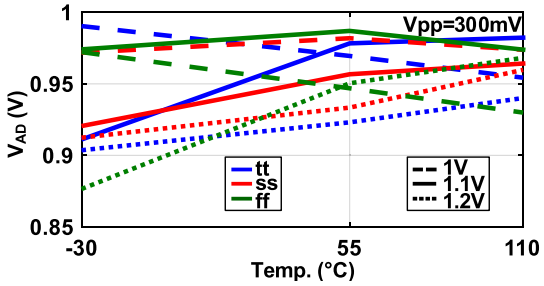

Fig. 16. Simulated V_{AD} of proposed amplitude detector under PVT variations (V_{pp} = 300 mV).

the CW input signals. The modulated RX input is not suitable for phase detection. The simulated output response of the PD detector under various PVT conditions is shown in Fig. 14. The maximum voltage variation is 118 mV. The variations, including process, temperature, and voltages (PVT), can be calibrated by manually setting the reference voltage V_{PR}.

The amplitude detector is required in the link-tracking loop for the AGC function. Fig. 15(a) exhibits the schematic of the proposed amplitude detector based on the concept of self-mixing [38]. The input IF signal is self-mixed to generate dc voltage and second-order harmonic as mixing product, while the second-order harmonic is suppressed by the lowpass filter (LPF) following with the detector. Thus, the power of the input signal is transferred into a dc voltage. A differential amplifier is utilized to amplify the relatively weak dc voltage. The simulated output voltage V_{AD} versus the peak-to-peak voltage (i.e., V_{pp}) of IF signal is shown in Fig. 15(b). Note that the proposed amplitude detector is designed to provide a near-linear response to the input signal voltage within a wide input voltage range. The simulated V_{AD} of the proposed amplitude detector under variable PVT conditions is depicted in Fig. 16. Here, V_{pp} = 300 mV. The maximum detected voltage variation is 113.9 mV. Besides, similar to PD, the PVT variation of V_{AD} can be calibrated by the externally supplied reference voltage V_{AR}.

After phase and amplitude detection, two comparators are utilized in the link-tracking loop to generate phase and AE codes as mentioned in Section II. Meanwhile, to improve the system stability during the tracking procedure, the comparator is expected to generate a lock signal after the phase and amplitude of the IF signal tracked to the specified target. Fig. 17(a) shows the schematic of the proposed triple-state comparator, which consists of two open-loop differential amplifiers and an XOR gate. The input voltages of the comparator are the detected voltage (i.e., V_{AD} and PD) and reference voltage (i.e., V_{AR} and V_{PR}). The input reference voltage is divided by a resistor network to generate the second reference voltage (i.e., V_{ARD} and V_{PRD}). Then, two reference voltages and the detected voltage are injected into two open-loop differential amplifiers for comparison, while the outputs of differential amplifiers are injected to the XOR gate to allocate the lock signals (i.e., A_{LOCK} and P_{LOCK}). Fig. 17(b) exhibits the output response of the triple-state comparator versus the detected voltage. Three cases are concluded as follows: 1) once the detected voltage (V_{AD} for example) is lower than V_{ARD}, the AE = 0 and A_{LOCK} = 0; 2) once the

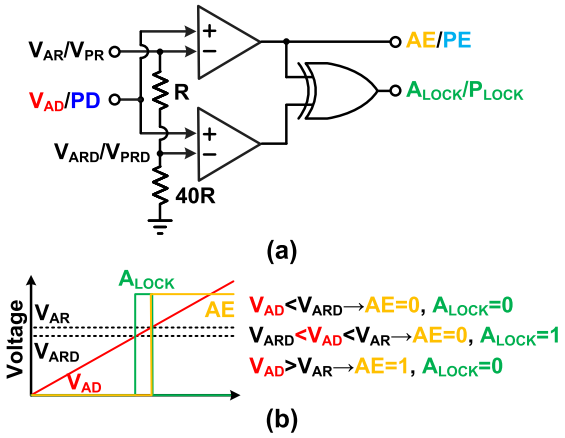

Fig. 17. (a) Schematic of the proposed triple-state comparator. (b) Output of triple-state comparator (amplitude comparator is utilized as an example).

$V_{ARD} < V_{AD} < V_{AR}$, the tracking procedure is accomplished and the $A_{LOCK} = 1$ is generated to lock the controller of the link-tracking loop; and 3) for $V_{AD} > V_{AR}$, the AE = 1 and $A_{LOCK} = 0$.

In the proposed link-tracking loop, V_{PR} and V_{AR} are typically set as 0.55 and 0.95 V, respectively. Then, V_{PRD} and V_{ARD} are calculated as $0.55 \times 40.41 = 0.536$ V and $0.95 \times 40.41 = 0.927$ V, respectively. The ratio between phase and voltage is depended on the proposed PD detector, which is 360°/1.1 V = 0.33°/mV@(V_{PR} = 0.55 V). The ratio between amplitude and voltage is determined by the proposed amplitude detector, which is 1 mV/mV@(V_{AR} = 0.95 V). Thus, the largest phase and amplitude mismatches after locking are (550–536) × 0.33° = 4.62° and (950–927) × 1 mV = 23 mV, respectively. Note that the AE mainly introduces the power error of the synthesized beam. Then, the beam accuracy, i.e., tracking accuracy, can be estimated from PE by the following equation:

$$\theta = \sin^{-1}\left(\frac{\phi}{180^\circ}\right) \tag{8}$$

where θ is beam accuracy and ϕ is PE. Then, the tracking accuracy is 1.47°.

Based on the principle in Fig. 8(b), the amplitude control codes (i.e., $AC_{i,r}$) of the phase-gain manager are generated using the amplitude control code (i.e., RXA) and phase control code (i.e., RXP). The schematic of RX phase- and gain-controllers is shown in Fig. 18(a), which includes two counters and two adder-subtractors. The counters driven by an external clock (i.e., CLK) generate the RXA and RXP based on AE and PE, respectively. The output code of the counter is plus 1 for each clock cycle as the AE or PE equaling to 0, while the output code of the counter is −1 as the AE or PE setting to 1. Therefore, the tracking speed is depended on the frequency of the CLK signal. When A_{LOCK} (or P_{LOCK}) equals to 1, the counter for RXA (or RXP) is disabled to maintain the state. The adder-subtractor combines the RXA and RXP to generate $AC_{i,r}$ = RXA ± RXP, while the polarity is depended on the sign control code SC (e.g., AC_r = RXA + RXP and AC_i = RXA − RXP for SC = 1, AC_r = RXA − RXP and AC_i = RXA + RXP for SC = 0). As mentioned in Section II, once the phase of the IF signal reaches the edge of each quadrant, the quadrant-change operation is performed to provide a 360° auto phase-control in four quadrants. The block diagram and changing conditions of the auto quadrant-change circuit are shown in Fig. 18(b). The $AC_i = 0$ or $AC_r = 0$ means that the IF signal reaches the edge of each quadrant and requires quadrant change, while the value of PE determines the direction of quadrant changing (i.e., quadrant increased for PE = 0, quadrant reduced for PE = 1). Note that before the quadrant change is executed, the changing condition stands for eight clock-cycle to avoid the misjudgement caused by signal fluctuation. The sign control code of the adder-subtractor is depended on the quadrant setting. Here, SC = 1 for quadrant 2 (Q2) and quadrant 4 (Q4), while SC = 0 in quadrant 1 (Q1) and quadrant 3 (Q3), respectively. The amplitude control codes $AC_{i,r}$ and quadrant control codes $QC_{1,2}$ of each RX are transmitted to the OFF-chip micro-control unit (MCU) for phase calculation. Then, the phase control codes of each TX channel are generated using a lookup table of the RX phase setting. Thus, the link-tracking loop with automatical phase, gain, and quadrant control is implemented. Fig. 19 exhibits the simulated output waveform of two RX elements during a tracking procedure, a 10 MHz clock is utilized to drive the link-tracking loop. In the original state, the input signals of two RXs are assigned with a 120° PD, while the original gain settings of two RXs are different. Thus, the phase and amplitude of IF signals are different in the original setting. After the tracking procedure is completed, the phase and amplitude of IF signals are equal. Therefore, the proposed link-tracking loop can provide an automatic phase- and gain-control function.

The tracking time t_{tr} is depended on the counter times N and clock frequency f_{clk}, i.e., $t_{tr} = N/f_{clk}$. For the possible longest case, the initial phase of the IF signal is about 90° PD compared to the phase of the resultant RF signal, as shown in Fig. 20. Then, the phase change is about 180°. Assuming the initial phase of IF signal is 180° (i.e., AC_r[11:0] = 111111111111, AC_i[11:0] = 000000000000, $QC_1 = 0$, $QC_2 = 1$). Then, the phase changes from 180° to 90° (i.e., AC_r[11:0] = 000000000000, AC_i[11:0] = 111111111111, $QC_1 = 0$, $QC_2 = 1$). Next, the quadrant changes ($QC_1 = 0$, $QC_2 = 0$). Finally, the phase changes from 0° to 90° (i.e., AC_r[11:0]=111111111111, AC_i[11:0] = 000000000000, $QC_1 = 0$, $QC_2 = 1$). Note that the code AC_r and AC_i are separated into two parts in the proposed work, i.e., $AC_{i,r}$[0:6] for RF-LNA and $AC_{i,r}$[7:11] for IF-VGA. Then, the bits of the counter for phase and amplitude, as shown in Fig. 18, are designed as 7 bits. Under the possible longest case, the counter changes from 0000000 to 1111111 in the first phase tune, and then changes from 1111111 to 0000000 in the second phase tune, i.e., the counter change time N is $2^8 = 256$. Then, the longest tracking time under a clock frequency of 10 MHz can be calculated as 256/10 MHz = 25.6 μs. Note that the amplitude and phase are calibrated, simultaneously. Thus, whatever the initial amplitude of the IF signal is, the amplitude (7-bit) can be calibrated under 2^8 times code change. Meanwhile, the largest clock frequency is limited by the longest settle time of the three circuits, i.e., PD detector,

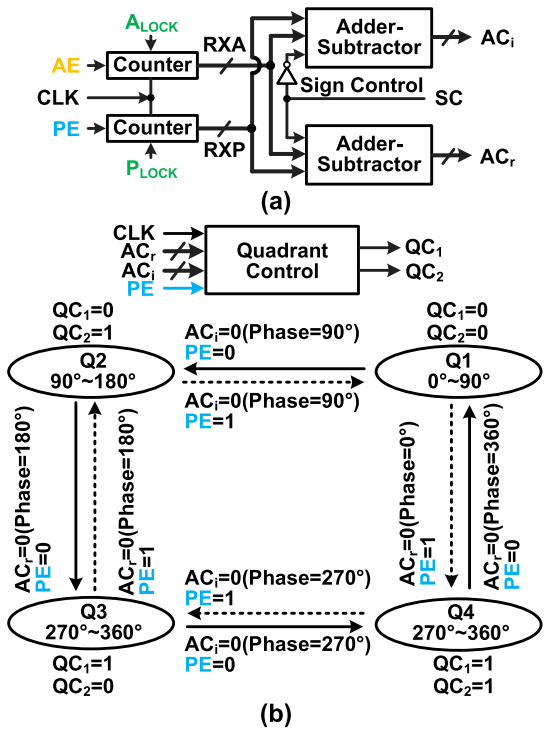

Fig. 18. (a) Block diagram of the proposed RX phase- and gain-controllers. (b) Block diagram and changing conditions of the auto quadrant change circuit.

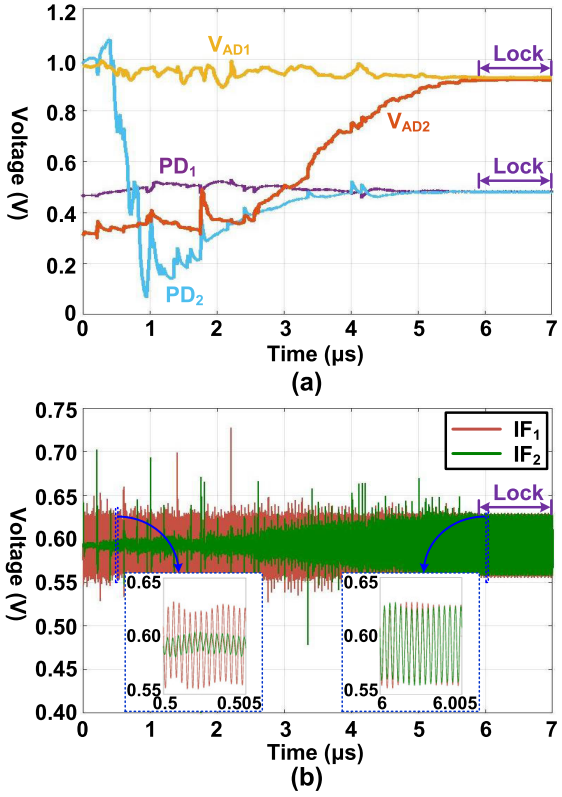

Fig. 19. (a) Simulated V_{AD} and PD of two link-tracking loops. (b) Simulated IF signals of two RX elements.

amplitude detector, and triple-state comparator. Due to the LPF (R and C) circuits existing in the two detectors, the settling time of the detector is longer than the comparator.

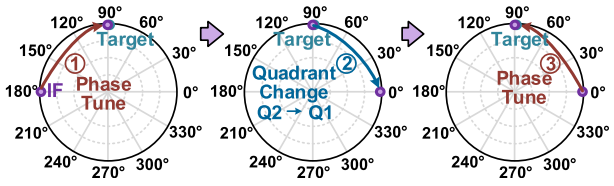

Fig. 20. Possible longest case for the link tracking loop.

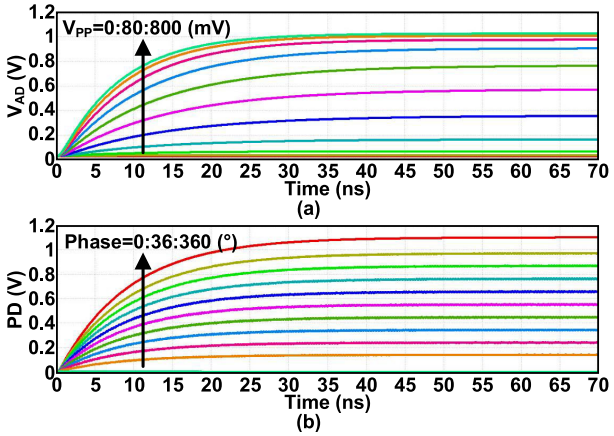

Fig. 21. Simulated voltages of (a) amplitude detector and (b) PD detector.

The simulated voltage transients of the amplitude detector and PD are shown in Fig. 21. It is notable that the settle times are 50 and 40 ns, respectively. Then, the fastest clock frequency is 20 MHz.

C. Time Division Modulator and Fast-Locking PLL

Based on the principle and operation of time division modulation mentioned in Section II, the time division modulator generates the single-tone LO signal in RX mode and modulated RF signal in TX mode, respectively. The schematic of the proposed time division modulator is shown in Fig. 22. The main part of the time division modulator consists of a sign-map circuit, an in-phase/quadrature (I/Q) generator, four digital PA (DPA) arrays [39], and an output transformer. The LO signal from PLL is transmitted to the I/Q generator with quadrature LO signal outputs (i.e., $LO_{0°}$, $LO_{90°}$, $LO_{180°}$, and $LO_{270°}$). As shown in Fig. 22(a), the sign-map circuit determines the polarity of output quadrature LO signal (i.e., LOI+, LOQ+, LOI−, and LOQ−) according to the sign-control code. Then, each LO is transmitted to a DPA array, while the output amplitude of DPA is depended on the number of ON-state unit cells. The ON-state unit cells of DPAs with LOI+ and LOI− are controlled by baseband signal BBI<0:7>, while the on-state unit cells of DPAs with LOQ+ and LOQ− are depended on BBQ<0:7>. By combining the quadrature outputs of four DPAs, the proposed time division modulator can provide a signal with programmable phase and amplitude. Therefore, the time division modulator is configured as a radio frequency DAC (RFDAC) with a direct digital-to-RF modulation function, while the output of the time division modulator is a modulated RF signal. For RX mode shown in Fig. 22(b), the sign map circuit is disabled, while all the DPA arrays are controlled by an identical gain control code

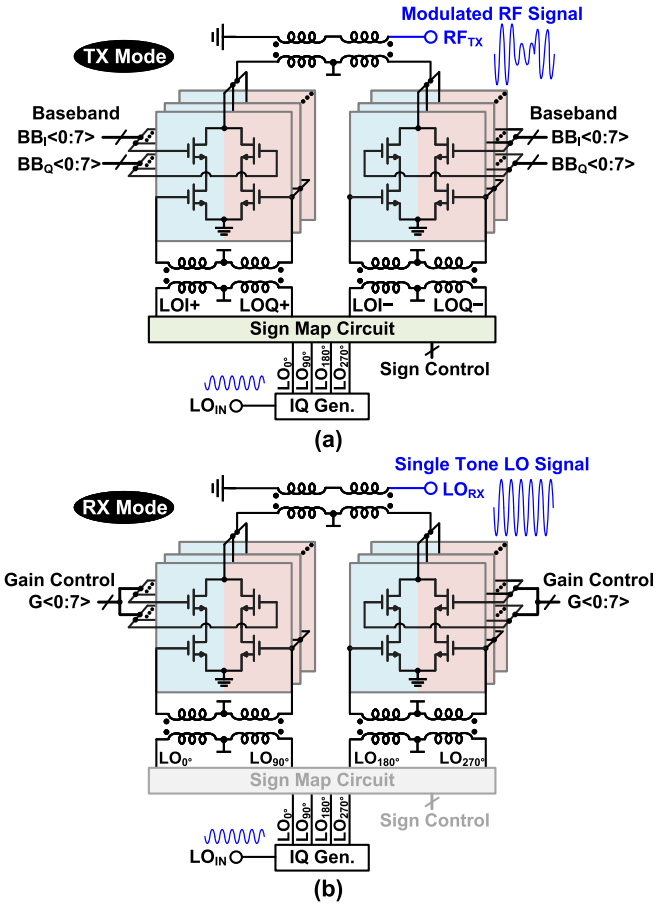

Fig. 22. Schematic and configuration of the proposed time division modulator in (a) TX mode and (b) RX mode.

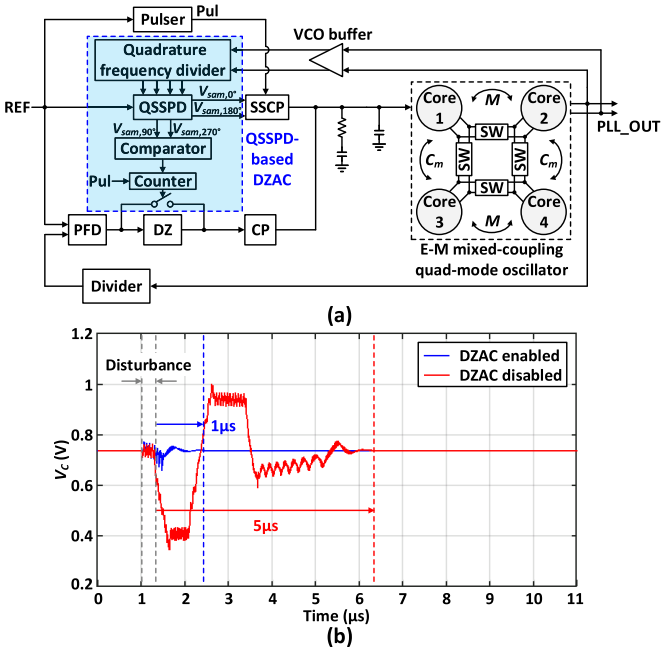

Fig. 23. (a) Schematic of the proposed fast-locking PLL. (b) Simulated locking time of proposed fast-locking PLL with or without enabling DZAC.

G<0:7> to generate a single-tone LO signal with programmable amplitude. Thus, the time division modulator acts as a variable gain LO driver, where good LO

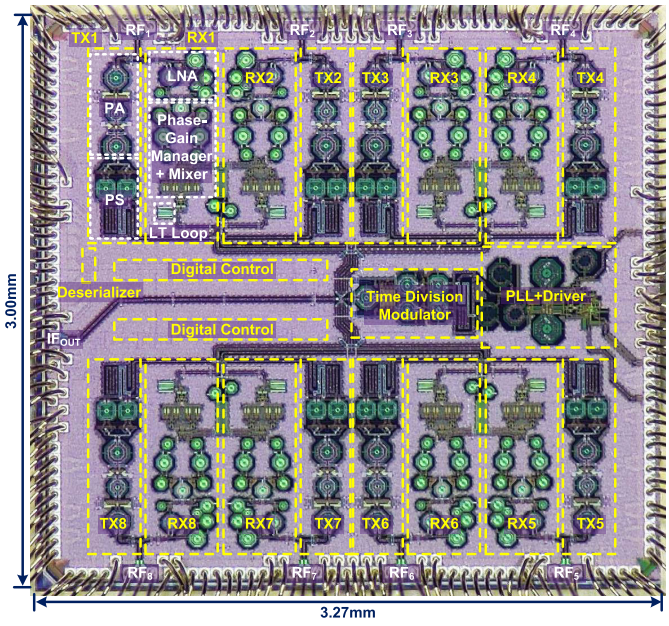

Fig. 24. Chip micrograph of the fabricated eight-element phased-array TRX.

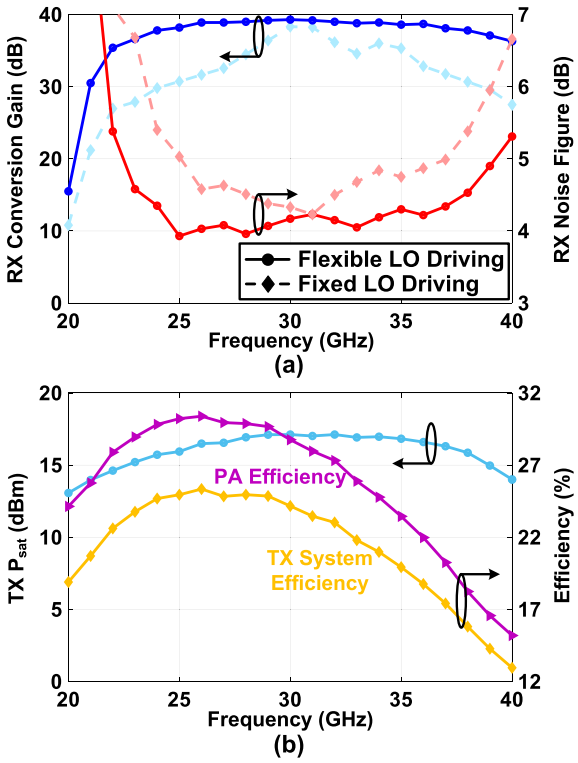

Fig. 25. (a) Measured gain and NF of the RX with or without flexible LO driving. (b) Measured P_{sat}, PA efficiency, and system efficiency of the TX.

power flatness can be achieved within the wide frequency range.

Fig. 23(a) depicts the schematic of the proposed wideband fast-locking SSPLL [40]. In order to fully verify the performance of the proposed SSPLL architecture in wideband mm-wave operation, a quad-mode oscillator is integrated into the SSPLL. The quadrature frequency divider is used to generate the IQ signals over the wide operation frequency

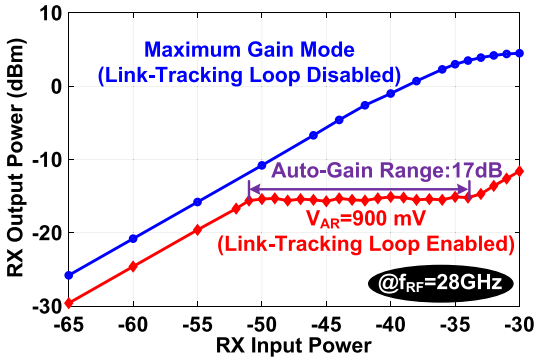

Fig. 26. Measured RX output power versus input power with or without link-tracking loop.

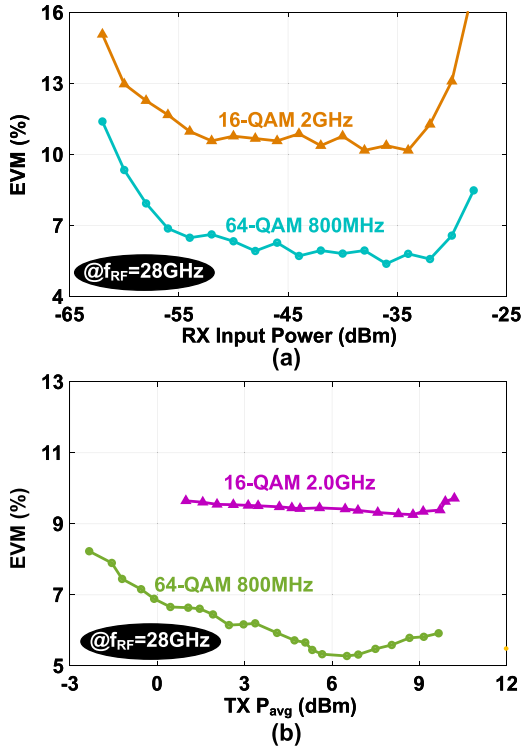

Fig. 27. (a) Measured EVM of the RX under various input power. (b) Measured EVM of the TX under various average output power (P_{avg}).

range. A disturbance is injected into the loop to observe the locking operation of the fast-locking SSPLL at 28 GHz. Fig. 23(b) shows the simulated transient of VCO control voltage in fast-locking SSPLL under a disturbance at 1 μs. The simulated locking time of the fast-locking SSPLL with disabled DZAC is 5 μs. Under the same disturbance, the fast-locking SSPLL with enabled DZAC recovers to a steady state within 1 μs, while the simulated locking time is improved by more than 5$\times$ with the enabled DZAC.

IV. Measured Results

Based on the aforementioned structures, the proposed phased-array TRX is implemented and fabricated using a conventional 40-nm CMOS technology. The chip micrograph is shown in Fig. 24, where the chip occupies an area of 3.00 $\times$ 3.27 mm. Here, two RXs close to each other are

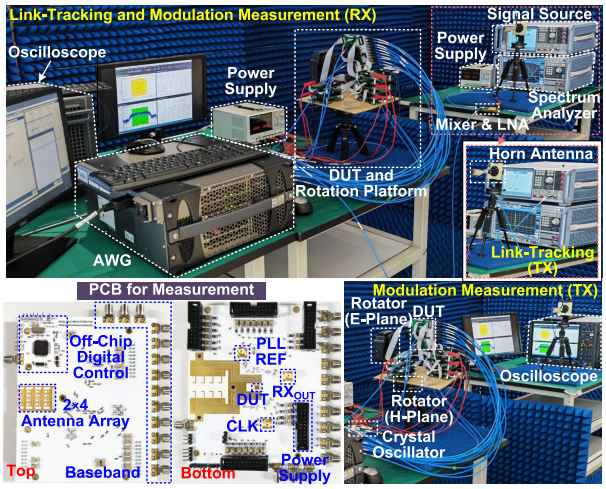

Fig. 28. Test circuit board of the proposed eight-element phased-array TRX and the over-the-air measurement set-up.

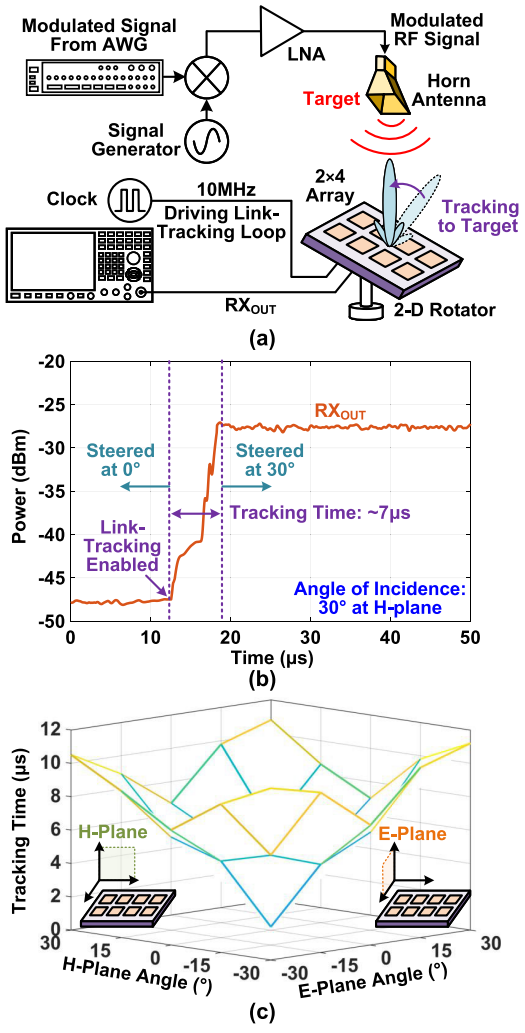

Fig. 29. (a) Measurement set-up for link-tracking time. (b) Measured output power of RX_{OUT} after the link-tracking loop is enabled. (c) Measured link-tracking time under various incidence angles.

shared with a single I/Q generator for compact size. The fabricated chip consumes 86 mW in the PLL and LO driver, 209 mW in the time division modulator (under maximum

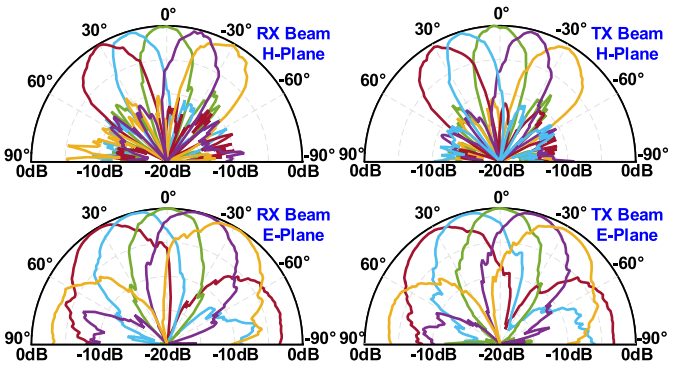

Fig. 30. Measured beam pattern after tracking.

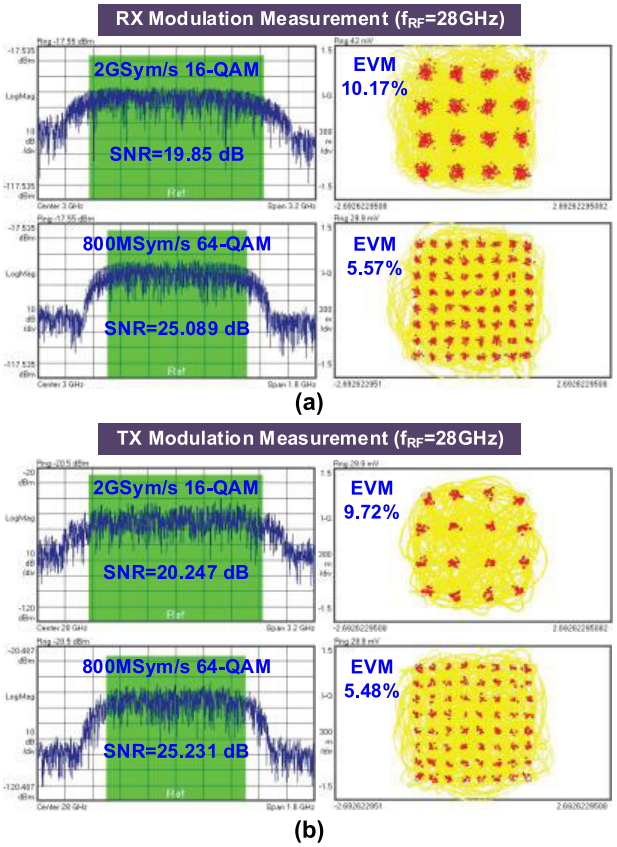

Fig. 31. Measured output spectrum and constellation diagrams of the proposed phased-array TRX at $f_{RF} = 28$ GHz. (a) RX and (b) TX.

output power), 75 mW in each RX element (including the link-tracking loop), and 179 mW (at P_{sat}) in each TX element. The measured results of single element TRX are shown in Fig. 25. Fig. 25(a) exhibits that by using the time division modulator to provide a flexible LO driving ability, the flatness of gain and noise figure (NF) is improved. The maximum gain of each RX is 39 dB at 30 GHz with a 3-dB bandwidth of 23–40 GHz, while the minimal NF is 3.9 dB at 25 GHz. The NF is lower than 5.3 dB within the operation frequency range of 23–40 GHz. As shown in Fig. 25(b), the P_{sat} of each TX is 14.0–17.1 dBm at 23–40 GHz, while the peak PA efficiency and TX system efficiency are 30.4% and 25.3%, respectively. As exhibited in Fig. 26, under the maximum

f_{RF}	24GHz				
Angle	-30°	-15°	0°	15°	30°
64-QAM 4.8 Gb/s EVM (RX)	7.19%	6.94%	6.70%	6.89%	7.48%
64-QAM 4.8 Gb/s EVM (TX)	6.64%	6.53%	6.47%	6.58%	6.61%
f_{RF}	28GHz				
Angle	-30°	-15°	0°	15°	30°
64-QAM 4.8 Gb/s EVM (RX)	6.09%	5.62%	5.57%	5.81%	6.07%
64-QAM 4.8 Gb/s EVM (TX)	5.89%	5.77%	5.48%	5.54%	5.70%
f_{RF}	39GHz				
Angle	-30°	-15°	0°	15°	30°
64-QAM 4.8 Gb/s EVM (RX)	7.64%	7.33%	6.44%	6.98%	7.46%
64-QAM 4.8 Gb/s EVM (TX)	6.74%	6.65%	6.48%	6.60%	6.79%

Fig. 32. Measured constellation diagrams of the proposed phased-array TRX.

gain mode (i.e., the link-tracking loop is disabled), the input 1-dB compression point ($IP_{1\ dB}$) of the RX is −32 dBm at 28 GHz. By setting the reference voltage $V_{AR} = 900$ mV, the RX controlled by the link-tracking loop provides an auto-gain range of 17 dB. Fig. 27(a) describes that the RX achieves EVM of 5.6%–7.3% from −52 to −30 dBm input power (i.e., P_{in}) under 800 MHz symbol rate 64-QAM signal input, and 10.2%–11.9% EVM from −54 to −32 dBm P_{in} with a 2 GHz symbol rate 16-QAM modulation signal. Meanwhile, as exhibited in Fig. 27(b), the TX obtains 5.3%–7.2% EVM from −2.5 to 9.6 dBm average output power (P_{avg}) under 800 MHz symbol rate, 64-QAM modulation and 9.2%–9.7% EVM from 0.5 to 10.2 dBm P_{avg} under 2 GHz symbol rate 16-QAM modulation. Therefore, the proposed TRX provides a high operating power range to support a high data rate, which is attractive for multiple applications with various T/R power levels.

To evaluate the over-the-air performance of the proposed phased-array TRX, the test circuit board and measurement setup are shown in Fig. 28. A 2 × 4 wideband slot antenna array [41] operating from 21 to 45 GHz is utilized for over-the-air measurement, while the digital control code for TX

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART TRX ARRAYS

Ref.	**This Work**	ISSCC 2022$^{\diamond}$ [23]	JSSC 2022 [22]	JSSC 2020 [16]	ISSCC 2018 [1]
Technology	**40-nm CMOS**	28-nm SOI CMOS	65-nm CMOS	65-nm CMOS	28-nm CMOS
Architecture	**Link-Tracking TRX Array with Time Division Modulator**	Heterodyne TRX Array	Heterodyne Full-Duplex TRX Array	Phase and Gain Self-Calibrated TRX Array	Heterodyne TRX Array
TRX Beam Steering	**Auto Beam-Control By Using On-Chip Link-Tracking Loop**	Off-Chip Digital Control	Off-Chip Digital Control	Off-Chip Digital Control with On-Chip Calibration	Off-Chip Digital Control
Integration Level	**Full RX with Mixer and IF Circuit + Full TX with Direct BB-RF Modulation + PLL**	Full TRX with Mixer + PLL	Full TRX with Mixer and Baseband Processing	Full TRX with Mixer and IF Circuit	Full TRX with Mixer and IF Circuit + PLL
Frequency (GHz)	**23–40**	26–28 / 39	28 / 37	39	26.5–29.5
RX Conv. Gain (dB)	**39**	N/A	44 / 37	3	34
RX NF (dB)	**3.9–5.3**	4.3–6.4 / 5.3–6.8	7.9 / 8.8	7.7	4.4–4.7
RX IP_{1dB} (dBm)	$-$**32***	N/A	-29 / -22	-22	N/A
RX Modulation EVM Data Rate	**16-QAM, 10.17% 8 Gb/s 64-QAM, 5.57% 4.8 Gb/s**	64-QAM, 4.97% 4.264 Gb/s^{+}	64-QAM, 4.02% 1.5 Gb/s	64-QAM, 3.09% 2.4 Gb/s (TX-to-RX)	64-QAM, 1.58% 2.4 Gb/s
TX P_{sat} (dBm)	**17.1**	16.1	15.5 / 15.6	15.5	$>$14
PA Efficiency (%)	**30.4**	N/A	21 / 21.5	25.5	$>$20
Peak TX SE$^{\#}$ (%)	**25.3**	N/A	N/A	N/A	N/A
TX Modulation EVM (%) Data Rate (Gb/s)	**16-QAM, 9.72% 8 Gb/s 64-QAM, 5.48% 4.8 Gb/s**	64-QAM, 4.41% 0.077 Gb/s^{+}	64-QAM, 4.12% 1.5 Gb/s	64-QAM, 3.09% 2.4 Gb/s (TX-to-RX)	64-QAM, 1.12% 2.4 Gb/s
P_{dc}/Elements (mW)	**290**	307.33	267.5	500	164
Area (mm^2)	**9.81 (8 TRXs)**	25.08 (16 TRXs)	12.65 (8 TRXs)	12 (4 TRXs)	27.76 (24 TRXs)

$^{\#}$: System efficiency including all baseband to RF circuits. *: Maximum gain mode. $^{\diamond}$: Beamformer chip. $^{+}$: With ADC and DAC.

link-tracking is generated by a digital control circuit. The baseband signal and gain control code of the time division modulator are provided by an arbitrary waveform generator (AWG). Meanwhile, the CLK signal to drive the link-tracking loop is fed by a signal generator, while the reference signal for PLL is provided by a stand-along crystal oscillator module. For the 2-m wireless communication measurement, a 2-D rotation platform is used to change the angle of incidence of the TRX array, while the communication target is a fixed horn antenna. Fig. 29(a) shows the test setup of link-tracking time. The link-tracking loop is disabled in the original setting (i.e., the beam steered to 0°), then rotating the phased-array to achieve an angle of 30° from the horn antenna. By using a 10 MHz clock to trigger the link-tracking loop, the proposed phased-array steers the beam automatically to the target. Fig. 29(b) exhibits that the power of RX_{OUT} increased rapidly after the tracking loop is enabled, while the tracking time is about 7 μs in this case. As shown in Fig. 29(c), the tracking time is varied with the incidence angle, which maintains lower than 11 μs under various incidence angles. Once the link-tracking is completed, the beam pattern is measured after disabling the link-tracking loop. Fig. 30 depicts that the proposed phased-array TRX

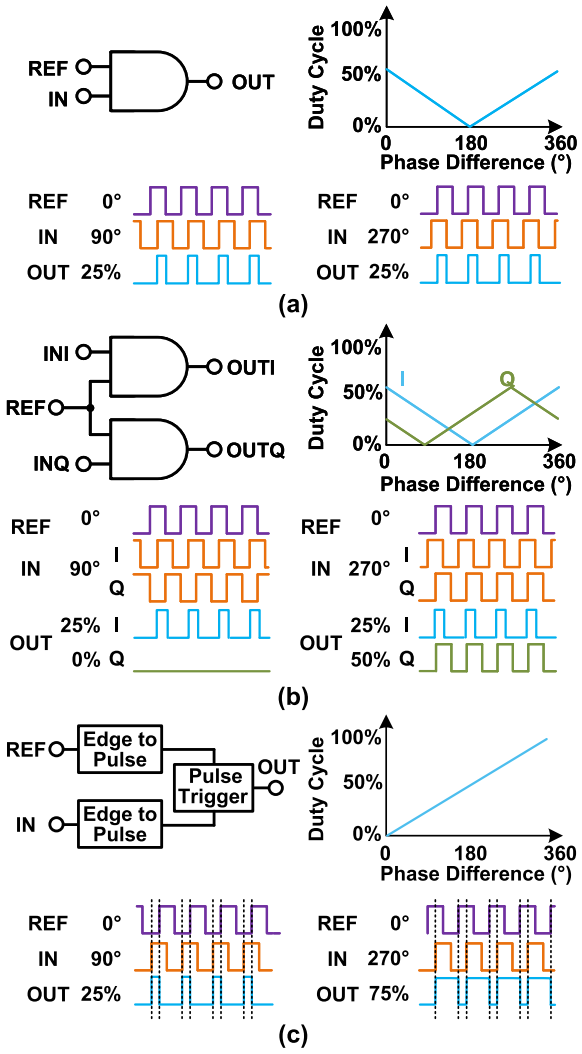

Fig. 33. PD detector. (a) AND gate. (b) I/Q signal as input of AND gate. (c) Proposed PD detector based on edge detection.

provides good auto-beamforming operation. The sidelobe suppressions for RX beam H- and E-planes are 5.1 and 2.6 dB, respectively. Besides, the sidelobe suppressions for TX beam H- and E-planes are 7.6 and 2.6 dB, respectively. Note that each slot antenna implemented on the PCB for the DUT test is the omnidirectional antenna, while the antenna linked to the instrument is the directional horn antenna. As exhibited in Fig. 31, the phased-array TRX can support 8.0 Gb/s, 16-QAM and 4.8 Gb/s, 64-QAM modulation signals transmission. Note that the modulation signals are transmitted after link-tracking. Besides, if the direction is not changed, the link-tracking does not need to be re-constructed. Fig. 32 reveals that the proposed phased-array TRX can transfer the high data-rate at 24, 28, and 39 GHz, simultaneously. Besides, the EVM shows little variation with different incidence angles.

The performance summary of the proposed phased-array TRX and the comparison with state-of-the-arts are shown in Table I. The proposed work is the first TRX array with ON-chip auto link-tracking. It demonstrates the merits of a wide operation frequency range with low RX NF, high TX efficiency, and high data-rate transmission covering the $n257$/$n258$/$n260$/$n261$ bands for the 5G-NR FR2 standard.

V. Conclusion

This article presents an eight-element phased-array TRX operating at 23–40 GHz. A link-tracking loop is introduced in each TRX channel, which can generate the gain and phase control codes for the RX to track the target signal from unknown directions. Based on the phase setting of each RX, the link-tracking loop provides a phase control code for each TX to steer the beam of the TX array to the target. Meanwhile, a time division modulator connected with a fast-locking PLL is integrated. Such a time division modulator can not only provide a flexible LO driving ability for gain flatness improvement of RX but also generate the modulated RF signal based on digital baseband directly to improve the TX system efficiency. Then, the proposed eight-element phased array TRX using a conventional 40-nm process is fabricated and measured for verification. With the state-of-the-art performance, the proposed phased-array TRX is attractive for wideband mm-wave wireless applications, including the 5G-NR FR2.

Appendix

An AND gate used in straightforward through of PD detection can convert the PD between two square wave signals (i.e., reference signal REF and input signal IN) to the duty cycle of the output signal. As shown in Fig. 33(a), the PD detector based on AND gate suffers from a critical issue, where the phase detection range is limited within 180°. Meanwhile, one duty cycle is referred to as two-PD detection results (e.g., the duty cycle of the output signal is 25% for the PD of 90° and 270°). Such an issue can be avoided by using I/Q signals as the input of the AND gate, as shown in Fig. 33(b). However, it requires a bulky I/Q signals generator, while an additional phase-difference recover circuit is needed to convert the I/Q output to a single detection result. In this work, a phase-difference detector based on edge detection is proposed, as shown in Fig. 33(c). The edge-to-pulse circuits are used to transfer the rising edge of the input signal and reference signal to a pulse. Then, the pulse signals drive a pulse trigger. Such a trigger counts the delay between two input pulses and generates an output signal with a duty cycle related to the delay. Therefore, the PD between two signals is referred to as the duty cycle of the output signal linearly.

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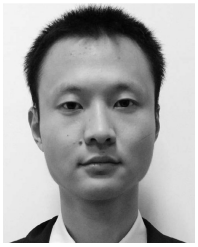
Xun Luo (Senior Member, IEEE) received the B.E. and Ph.D. degrees in electronic engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2005 and 2011, respectively.

From 2010 to 2013, he was the Project Manager with Huawei Technologies Company Ltd., Shenzhen, China, guiding research and development projects of multi-band microwave/millimeter-wave (mm-wave)-integrated systems for backhaul and wireless communication. Before joining UESTC, he was an Assistant Professor with the Department of Microelectronics, Delft University of Technology, Delft, The Netherlands. Since 2015, he has been a Full Professor with UESTC, where he has been appointed as the Executive Director of the Center for Integrated Circuits. Since 2020, he has founded and been the Head of the Center for Advanced Semiconductor and Integrated Micro-System (ASIS), UESTC. He has authored or coauthored more than 160 IEEE journals and conference papers. He holds 56 patents. His research interests include RF/microwave/mm-wave-integrated circuits, multiple-resonance terahertz (THz) modules, multi-band backhaul/wireless systems, reconfigurable passive circuits, artificial intelligence synthesis, array antennas, smart radar, and system in package.

Dr. Luo serves as a Technical Program Committee Member for multiple IEEE conferences, including the IEEE International Solid-State Circuits Conference (ISSCC), the IEEE International Microwave Symposium (IMS), the IEEE Custom Integrated Circuits Conference (CICC), and the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. He is also an IEEE Microwave Theory and Techniques (MTT)-Society Technical Committee Member of MTT-4 on Microwave Passive Components and Transmission Line Structures, MTT-5 on Filters, and MTT-23 on Wireless Communications. He was bestowed by China as the China Overseas Chinese Contribution Award in 2016 and was selected by the IEEE MTT-Society for the IEEE Outstanding Young Engineer Award in 2022. He was with the Center for ASIS and was a recipient of the UESTC Outstanding Team for Teaching and Education Award in 2021 and the UESTC Excellent Team for Postgraduate Supervision Award in 2021. He also won the UESTC Distinguished Innovation and Teaching Award in 2018 and the UESTC Outstanding Undergraduate Teaching Promotion Award in 2016. His Research Group BEAM X-Laboratory received multiple best paper awards and design competition awards, including the IEEE RFIC Best Student Paper Award in 2021, the IEEE RFIT Best Student Paper Award in 2016 and 2019, the IEEE IWS Best Student Paper Award in 2015 and 2018, the IEEE IMS Student Design Competition Award in 2017, 2018, 2019, and 2023, the IEEE IMS Sixty-Second Presentation Competition Award in 2019, and Multiple Best Paper Award Finalists from the IEEE conferences. He was the TPC Co-Chair of the IEEE IWS in 2024, 2023, and 2018, and the IEEE RFIT in 2019. He is the Vice-Chair of the IEEE MTT-Society Chengdu Chapter. He was a Track Editor of IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS from 2018 to 2021. He serves as an Associate Editor or Guest Editor for IEEE OPEN JOURNAL OF THE SOLID-STATE CIRCUITS SOCIETY, *IET Microwaves, Antennas and Propagation*, and *IEEE Microwave Magazine*.



Bingzheng Yang (Member, IEEE) received the B.E. degree in microelectronics and the Ph.D. degree in microelectronics and solid-state electronics from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2016 and 2022, respectively.

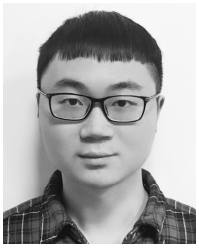
Since 2022, he has been a Faculty Member at UESTC. His research interests include microwave and millimeter-wave power amplifiers, transmitters, and array systems.

Dr. Yang was a recipient of the 2021–2022 IEEE Solid-State Circuits (SSC)-Society Predoctoral Achievement Award, the 2021 IEEE Microwave Theory and Techniques (MTT)-Society Graduate Fellowship Award, and the 2021 Chinese Institute of Electronics Integrated Circuit Scholarship Award.

Zhixian Deng (Member, IEEE) received the B.E. degree in microelectronics science and engineering and the Ph.D. degree in electronic science and technology from the University of Electronic Science and Technology of China, Chengdu, China, in 2019 and 2023, respectively.

His research interests include the reconfigurable microwave/millimeter-wave transceiver and passive components, especially integrated circuits.

Dr. Deng was a recipient of the 2022 IEEE Microwave Theory and Techniques (MTT)-Society Graduate Fellowship Award, the 2022–2023 IEEE Solid-State Circuits (SSC)-Society Predoctoral Achievement Award, and the IEEE International Microwave Symposium (IMS) Student Design Competition Award from 2017 to 2019.



Wen Chen (Graduate Student Member, IEEE) received the B.E. degree in microelectronics from the University of Electronic Science and Technology of China, Chengdu, China, in 2019, where he is currently pursuing the Ph.D. degree in electronic science and technology.

His research interests include the wideband microwave/millimeter-wave frequency synthesizer, oscillator, and circulator.

Mr. Chen was a recipient of the 2023 IEEE Microwave Theory and Techniques (MTT)-Society Graduate Fellowship Award, the IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Best Student Paper Award in 2021, and the China National Scholarship in 2016 and 2017.

Yiyang Shu (Member, IEEE) received the B.E. and Ph.D. degrees in microelectronics from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2016 and 2021, respectively.

Since 2021, he has been a Faculty Member at UESTC. His research interests include the integrated wideband microwave/millimeter-wave/terahertz oscillator and frequency synthesizer.

Dr. Shu was a recipient/co-recipient of the IEEE International Symposium on Radio Frequency Integration Technology (RFIT) Student Design Competition Award in 2016, the IEEE International Microwave Symposium (IMS) Student Design Competition Award in 2018, the IEEE International Wireless Symposium (IWS) Best Student Paper Award in 2018, the 2020–2021 IEEE Solid-State Circuits (SSC)-Society Predoctoral Achievement Award, the 2020 IEEE Microwave Theory and Techniques (MTT)-Society Graduate Fellowship Award, the 2020 Chinese Institute of Electronics Integrated Circuit Scholarship Award, and the IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Best Student Paper Award in 2021.

Jie Zhou (Member, IEEE) received the B.E. degree in microelectronics and the Ph.D. degree in microelectronics and solid-state electronics from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2016 and 2021, respectively.

Before joining UESTC, he was a joint Post-Doctoral Fellow at the University of Macau, Macau, China, and UESTC. Since 2023, he has been a Faculty Member at UESTC. His research interests include reconfigurable transmitter, receiver, and phased array.

Dr. Zhou was a recipient of the 2017 IEEE Microwave Theory and Techniques (MTT)-Society Undergraduate/Pregraduate Scholarship Award.