A Phase-Modulation Phase-Shifting Phased-Array Transmitter With Phase Self-Calibration and Deep PBOs Efficiency Enhancement

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***Abstract*— In this article, a digital phase-modulation (PM) phase-shifting (PS) phased-array transmitter is proposed. Both PM and PS are implemented in a PS modulator. Meanwhile, a self-calibration loop is introduced in the PS modulator for improved phase linearity and minimized phase error. The phase control voltages for the PS modulator are generated from the self-calibration loop based on the output signals and reference signals. To reduce the calibration time, a capacitor-array-based state store memory is introduced in the self-calibration loop. Efficiency at 2.5-/6-/12-dB power back-off (PBO) is enhanced by class-G Doherty switched-capacitor power amplifier (SCPA). As a verification of the concept, a 2.1–2.9-GHz four-element phased-array transmitter is designed and fabricated in a conventional 40-nm CMOS technology. The transmitter features a 10-bit fast-locking phase self-calibration with measured 0.4° rms phase error and 0.2-dB rms power error. The measured peak saturated output power of each element is 26.95 dBm at 2.4 GHz. Besides, the measured system efficiency at 0-/2.5-/6-/12-dB PBO is 37.25%/34.24%/30.12%/21.23%. For 20-MHz 64-QAM/15-MHz 256-QAM modulation signal, it exhibits EVM of 4.65%/2.84%, average output power of 19.91/16.59 dBm, and average system efficiency of 24.12%/19.21% at 2.4 GHz. By connecting monopole antenna units with a gain of 4.21 dBi, the measured peak effective isotropic radiated power (EIRP) of phased-array transmitter is 42.05 dBm.**

***Index Terms*— Efficiency enhancement, phase self-calibration, phased-array transmitter, phase-shifting (PS) modulator, switched-capacitor power amplifier (SCPA).**

I. Introduction

INCREASING demands on high-precision detecting and high-data capacity accelerate developments of phased-array systems [1], [2]. The detecting accuracy increases with enhanced directivity of beams, which necessitates a large array size [3], [4], [5], [6]. Thus, the system efficiency of each element is significant to decrease the whole power consumption of the phased-array system. Besides, to support a high-data transmission within a limited bandwidth, high-order modulation is required [7], [8], [9]. Then, the average efficiency for modulated signals with high peak-to-average power ratio (PAPR) is critical [10], [11], [12], [13], [14]. Therefore, efficiencies under both the peak and back-off power are important for the phased-array systems.

Radio frequency (RF) [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25] and local oscillator (LO) [26], [27], [28], [29], [30] phase-shifting (PS) architectures are widely utilized in phased-array systems due to the potentiality on high system efficiency. As shown in Fig. 1(a), in an RF PS phased-array transmitter, phase shifters are placed between mixers and power amplifiers. The RF signals are the same before phase shifters. Thus, mixers can be shared in the RF PS phased-array system. With reduced blocks, system efficiency is improved [31], [32], [33], [34], [35]. However, the nonideality of phase shifters, such as gain variation and implicit nonlinearity, cannot be ignored. In an LO PS phased-array transmitter, phase shifters are added in the LO signal path, as shown in Fig. 1(b). Due to the constant envelope

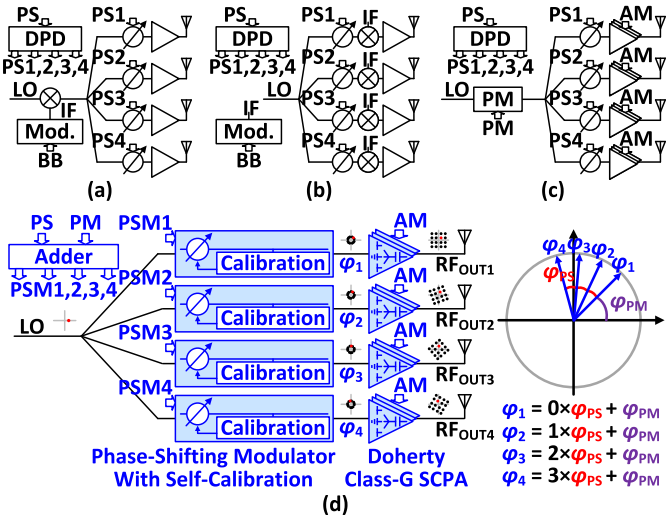

Fig. 1. Simplified architecture of (a) RF PS phased-array transmitter, (b) LO PS phased-array transmitter, (c) PM PS phased-array transmitter, and (d) proposed PM PS phased-array transmitter with phase self-calibration and efficiency enhancement.

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of LO signals, the deterioration from phase shifters can be decreased [36], [37], [38], [39]. Nevertheless, extra LO buffers and independent mixers are required in each element. Besides, both in RF and LO PS phased-array transmitters, an extra modulator to generate the modulated IF signal from baseband is necessary. In general, additional digital predistortion (DPD) techniques for both phase calibration and signal modulation in such phased-array transmitters are also needed.

To obtain enhanced system performance, phase-modulation (PM) PS digital polar phased-array transmitter is introduced, as shown in Fig. 1(c) [40]. As for a digital polar transmitter architecture, IF modulators and mixers are not required. Phase modulator and digital power amplifier are used for signal modulation. Therefore, system efficiency of a phased-array transmitter can be improved with a digital power amplifier. Meanwhile, the phase shifter is inserted between the phase modulator and digital power amplifier. Due to the constant envelope of PM signals, the influence of nonideality introduced by phase shifters can be decreased. By the aforementioned mechanisms, signals with direct-modulation and beam-steering are achieved, simultaneously. However, the nonlinearity of these circuits, i.e., AM–AM, AM–PM in digital power amplifier, phase versus code in phase modulator and phase shifter, limits the application. Additional DPD technique with lookup table (LUT) is required to solve the nonlinearity issues. Besides, the DPD technique is susceptible from the process, voltage, and temperature (PVT). With the variation of PVT, the LUT changes. Thus, in practical application, the digital modulation polar phased-array transmitter requires complex control systems. Meanwhile, in the reported digital phased-array transmitters [40], [41], [42], [43], [44], only peak efficiency is considered. The average system efficiency is relatively low, especially for modulated signals with high PAPR. Nowadays, digital power amplifiers with deep power back-off (PBO) efficiency enhancement are widely introduced to improve the average system efficiency [45], [46], [47], [48], [49]. However, the design of phased-array transmitter with high phase resolution, high output power, and high average system efficiency still remains great challenges.

To generate high-efficiency modulated signals with beam-steering characteristic, a digital PM PS phased-array transmitter with fast-locking phase self-calibration and PBO efficiency enhancement is presented in this article, as shown in Fig. 1(d) [50]. A PS modulator is utilized to integrate functions of PM and PS, which can minimize the complexity of the phased-array systems. Besides, a phase self-calibration loop is introduced to improve the phase linearity of PS modulator. Output signals are compared with a reference signal to obtain the control voltages based on the calibration loop. A state memory is introduced to speed up the calibration for high data rates. A digital switched-capacitor power amplifier (SCPA) is introduced to achieve amplitude modulation. Class-G and Doherty operations are employed in the SCPA implementation, which can improve the system efficiency at deep PBO peaks. To demonstrate the concept mentioned above, a PM PS phased-array transmitter in a conventional 40-nm CMOS technology is designed and fabricated. The measured 1-dB fractional bandwidth (FBW) is from 2.1 to 2.9 GHz. It achieves a peak saturated output power of 26.95 dBm at 2.4 GHz, while the corresponding system efficiency is 37.25%. Besides, the fabricated phased-array transmitter exhibits 34.24%/30.12%/21.23% system efficiency at 2.5-/6-/12-dB PBO peaks. A 10-bit phase self-calibration with 0.4°/0.2-dB rms phase/power error is achieved to support the high-resolution beam steering characteristics.

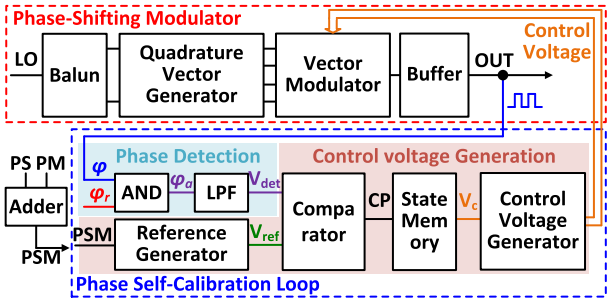


Fig. 2. Block diagram of PS modulator with phase self-calibration loop.

This article is organized as follows. In Section II, the operation of phase self-calibration is analyzed. The detailed architecture and circuit implementation are described in Section III. Section IV discusses the experimental results and performance comparison with the state-of-the-arts. Finally, Section V is the conclusion.

II. Topology and Operation

In a PM PS phased-array transmitter architecture, as shown in Fig. 1(c), only three components (i.e., phase modulator, phase shifter, and digital power amplifier) are utilized [40]. The output signals from a single element are expressed as

$$S_{\mathrm{PM}} = G_{\mathrm{PS}}(\varphi_{\mathrm{PS}}(t))G_{\mathrm{DPA}}(A(t))\cos(\omega_0 t + \varphi_{\mathrm{PM}}(t)+\varphi_{\mathrm{PS}}(t)) \tag{1}$$

where $\varphi_{\mathrm{PS}}(t)$ and $G_{\mathrm{PS}}(\varphi_{\mathrm{PS}}(t))$ are phase shift and $\varphi_{\mathrm{PS}}(t)$-dependent gain determined by the phase shifter, respectively. $\varphi_{\mathrm{PM}}(t)$ is PM determined by a phase modulator and $G_{\mathrm{DPA}}(A(t))$ is amplitude-dependent gain determined by the digital power amplifier, respectively. Note that, both phase modulator and phase shifter are working on phase characteristics in the phased-array transmitter. Thus, a PS modulator is utilized to replace the phase modulator and phase shifter in the phased-array transmitter. Then, the output signals can be simplified as

$$S_{\mathrm{PM}} = G_{\mathrm{PSM}}(\varphi_{\mathrm{PSM}}(t))G_{\mathrm{DPA}}(A(t))\cos(\omega_0 t + +\varphi_{\mathrm{PSM}}(t)) \tag{2}$$

where $\varphi_{\mathrm{PSM}}(t)$ and $G_{\mathrm{PSM}}(\varphi_{\mathrm{PSM}}(t))$ are PS modulation and $\varphi_{\mathrm{PSM}}(t)$-dependent gain determined by the PS modulator, respectively. The PS signal is converted to rail-to-rail signal before driving DPA. Hence, the $\varphi_{\mathrm{PSM}}(t)$-dependent amplitude variation have a slight effect on the output signals, i.e., S_{PM} is approximated as

$$S_{\mathrm{PM}} = G_{\mathrm{PSM}}G_{\mathrm{DPA}}(A(t))\cos(\omega_0 t + +\varphi_{\mathrm{PSM}}(t)). \tag{3}$$

It is notable that only two circuits-dependent variables [i.e., $G_{\mathrm{DPA}}(A(t))$ and $\varphi_{\mathrm{PSM}}(t)$] exists in S_{PM}. In the proposed PM

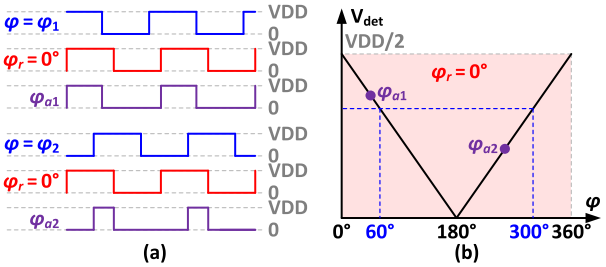


Fig. 3. (a) Waveform of output signals with one reference. (b) Corresponding ratio curve between output phase ϕ and detected voltage V_{det}.

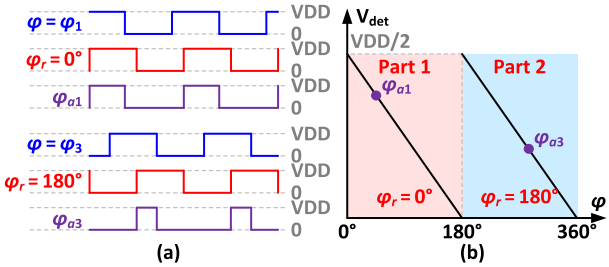


Fig. 4. (a) Waveform of output signals with two differential references. (b) Corresponding ratio curve between output phase ϕ and detected voltage V_{det}.

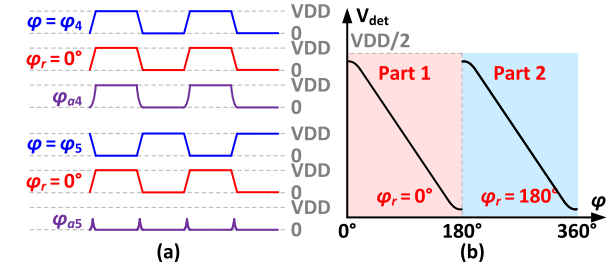


Fig. 5. (a) Waveform of output signals considering nonideality. (b) Corresponding ratio curve between output phase ϕ and detected voltage V_{det}.

PS phased-array transmitter, shown in Fig. 1(d), the digital SCPA is utilized for power amplifier implementation. No DPD calibration is required for $G_{\text{DPA}}(A(t))$, due to the merits of good linearity in SCPA. As for $\varphi_{\text{PSM}}(t)$, the vector-sum topology is used to achieve high resolution. The phase is generated by synthesizing the quadrature vectors with various weights. Phase selection technique (i.e., phase DPD) is required to minimize PM and PS errors [51]. However, the calibrated results are sensitive to temperature, process, and frequency variations. To address this issue, phase self-calibration techniques are proposed. The control code (PSM) for the PS modulator is obtained by adding the control codes for PM and PS directly. Thus, both PS and PM can be calibrated, when phase calibration is carried out. Then, no extra DPD techniques are required in the proposed phased-array transmitter.

A. Phase Detection

The PS modulator with a feedback loop is shown in Fig. 2. The output signal of the PS modulator (i.e., φ) is detected and fed back to the loop. Assuming the output signal with phase ϕ is expressed as

$$x(t) = \begin{cases} \text{VDD}, & \dfrac{-\phi}{2\pi}T + nT < t \le \dfrac{\pi-\phi}{2\pi}T + nT \\ 0, & \dfrac{\pi-\phi}{2\pi}T + nT < t \le \dfrac{2\pi-\phi}{2\pi}T + nT \end{cases} \tag{4}$$

where T is the period of output signals. Then, to detect the phase of the output signals, a reference signal with 0° phase (i.e., φ_r) is introduced. The reference signals are expressed as

$$x_r(t) = \begin{cases} \text{VDD}, & nT < t \le \dfrac{T}{2} + nT \\ 0, & \dfrac{T}{2} + nT < t \le T + nT. \end{cases} \tag{5}$$

The output signal φ is compared and multiplied with the reference signal φ_r. As shown in Fig. 3(a), the duty cycle of the generated signal (i.e., φ_a) changes as the output phase varying, which is calculated as

$$x_g(t)|_{\phi\in(0,\pi]} = \begin{cases} \text{VDD}, & nT < t \le \dfrac{\pi-\phi}{2\pi}T + nT \\ 0, & \dfrac{\pi-\phi}{2\pi}T + nT < t \le T + nT \end{cases} \tag{6}$$

$$x_g(t)|_{\phi\in(\pi,2\pi]} = \begin{cases} \text{VDD}, & \dfrac{2\pi-\phi}{2\pi}T + nT < t \le \dfrac{T}{2} + nT \\ 0, & \dfrac{T}{2} + nT < t \le \dfrac{4\pi-\phi}{2\pi}T + nT. \end{cases} \tag{7}$$

Therefore, the phase of the output signal can be represented by the duty cycle of the generated signal. To further quantize the phase, the Fourier transform is utilized for analysis. The dc component of the generated signal is expressed as

$$a_0 = \frac{1}{T}\int_0^T x_g(t)dt = \left|\frac{\pi-\phi}{2\pi}\right|\text{VDD}. \tag{8}$$

It is notable that the dc component of the generated signal is linear with the output phase ϕ. Thus, the phase of the output signal can be obtained by detecting the dc component. Besides, the dc component a_0 is insusceptible to frequency. Thus, the phase detection can be achieved within a wideband. A low bandpass filter (LPF) is utilized to convert the generated signal into dc voltage V_{det}. The relationship curve between dc voltage V_{det} and output phase ϕ is shown in Fig. 3(b). Due to the periodicity of signals, there are two same dc voltages in the 360° phase range. For example, the dc voltage for the output signal with $\phi = 60°$ is the same as that for the output signal with $\phi = 300°$. In this case, it is not able to confirm the accurate phase from the dc voltages based on circuits directly.

To address this issue, two reference signals with 0° and 180° are introduced. By two reference signals, the relationship between dc voltage V_{det} and output phase ϕ are modified as Fig. 4. The output signals are divided into two parts, i.e., the output phase of 0°–180° and 180°–360°. Then, the output phase ϕ is uniquely identified by the dc voltage V_{det}.

In practice, there is nonideality of square wave, such as raise and fall times, as shown in Fig. 5. A nonlinear ratio curve between dc voltage V_{det} and output phase ϕ exists, when output

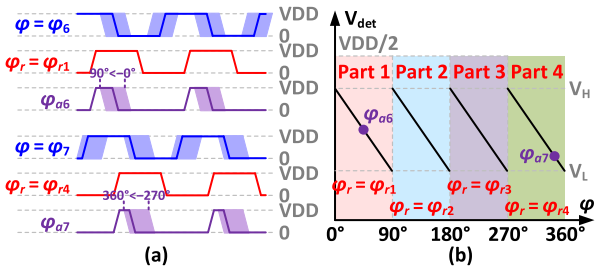


Fig. 6. (a) Waveform of output signals with four quadrature references. (b) Corresponding ratio curve between output phase ϕ and detected voltage V_{det}.

phase ϕ is around 0° and 180°. Meanwhile, the output phases are not easy to calibrate, once the ratio curve is nonlinearity. To obtain a linear ratio curve between dc voltage and output phase, a constant phase delay is introduced in the reference signals. As aforementioned analysis, the phase delay should be larger than the raise time. Besides, to cover 360° phase range, four signals with 90° phase difference are utilized for the reference signals. The ratio curve between dc voltage V_{det} and output phase ϕ is divided into four parts, as shown in Fig. 6. Then, a linear ratio curve is obtained in each part. Besides, the highest and lowest voltages are V_H and V_L. Note that, each part corresponds to each quadrant of the vector-sum PS modulator. The reference signals are changed with quadrant selection.

B. Phase Calibration

The output phase of the PS modulator is converted into voltage using the phase detection circuits. Then, to achieve phase calibration, the control voltages for PS modulator are generated based on the detected phase. The control voltage generation module is developed, which is composed of a reference generator, a voltage comparator, and a control voltage generator. A reference voltage is generated by the reference generator, which is compared with the detected voltage to allocate the control voltage of PS modulator. Since the required phase is represented by the reference voltage, the phase is calibrated, once the detected voltage is equal to a reference voltage.

The flowchart of the phase self-calibration mechanism is shown in Fig. 7. The phase calibration procedure is summarized as follows: 1) the required PS ϕ_{PS} and PM ϕ_{PM} are summed to obtain the demanded phase ϕ_i of PS modulator; 2) convert the ideal phase ϕ_i into voltages V_{ref} by the reference generator; 3) detect the output phase of PS modulator and convert it into voltage V_{det}; 4) compare the detected voltage V_{det} with the reference voltage V_{ref}; 5) determine the control voltage V_c based on the compared results; 6) generate the phase control voltages $V_{\text{I,Q}}$ based on the control voltage and quadrant information; and 7) update the output phase of the PS modulator by the phase control voltages. Note that there is a feedback and locking mechanism from steps 3) to 7). Therefore, the output phase is automatically calibrated by the calibration loop. An example of voltage transients in one phase calibration period is shown in Fig. 8. Note that the calibration time is depended on the settle time of control voltage.

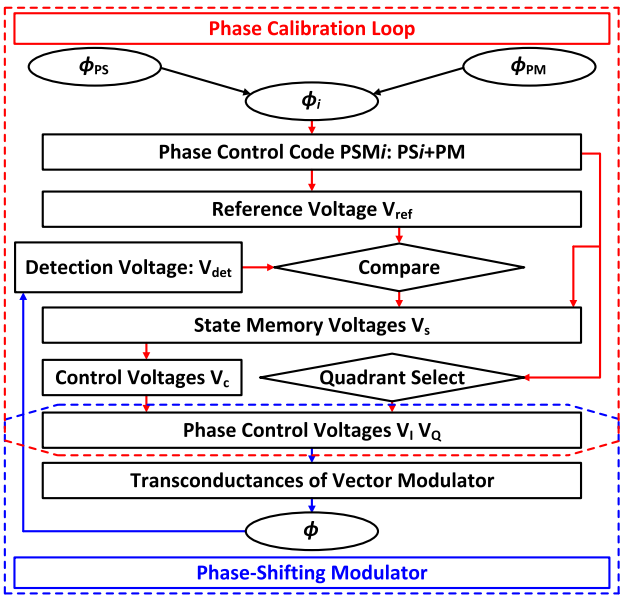


Fig. 7. Flowchart of the phase self-calibration mechanism.

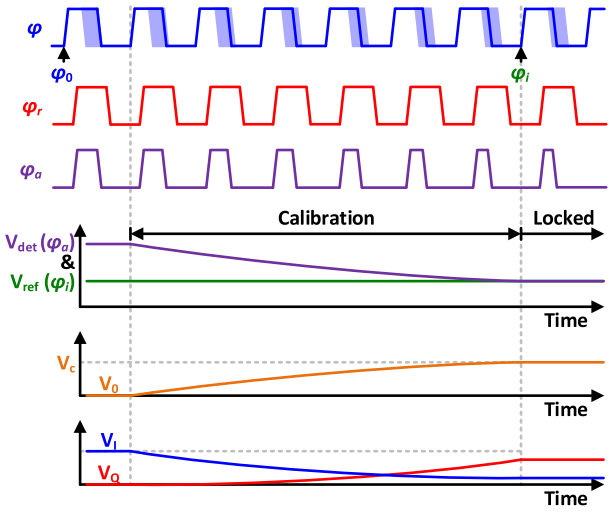


Fig. 8. Example of voltage transients in one phase calibration period.

C. Fast Calibration

In the proposed phase self-calibration loop, the control voltage is obtained by charging or discharging a capacitor. Thus, the calibration time for one phase is limited by the charge and discharge time of capacitors. Besides, the memory effect exists in the capacitor. The voltage changes from the voltage state of the former phase calibration. Therefore, the calibration time is long, when the phase jump is large between two adjacent phase states. A long calibration time leads to a limited bandwidth of the modulation signal.

To improve the speed of calibration, the state memory is introduced. Such state memory can pre-store the voltages for different phase states, which is controlled by the phase codes. Besides, the control voltages for two-phase states with slight phase difference are similar. Then, the phase calibration can start from the closest stored voltage state (V_s) instead of the former state. In this way, the charge and discharge time of the

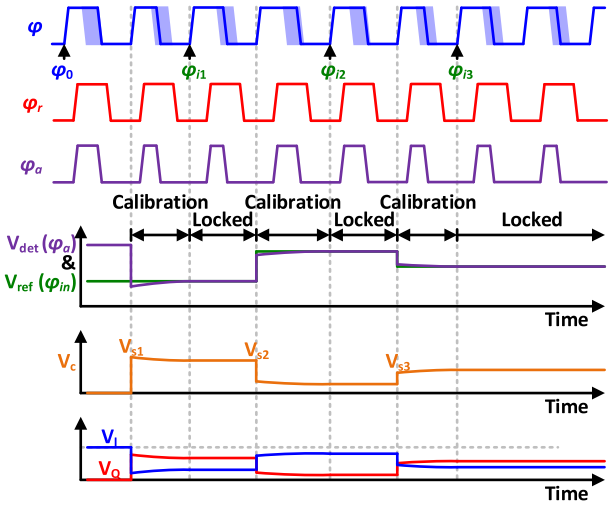


Fig. 9. Example of voltage transients with state memory in three-phase calibration periods.

capacitor are reduced. The fast calibration procedure speeds up the settle time of calibration significantly. An example of voltage transients with state memory in three-phase calibration periods is shown in Fig. 9. The phase is jumped at the begin of the calibration. Then, the small deviation is quickly calibrated by the calibration loop.

III. Circuit Implementation

A. Architecture

Based on the principle investigated in Section II, a PM PS phased-array transmitter with phase self-calibration and deep PBOs efficiency enhancement is designed in a conventional 40-nm CMOS technology. The simplified block diagram of the proposed phased-array transmitter is shown in Fig. 10. The chip employs a 2 × 2 array topology. Three active power dividers are utilized to divide the signals into four elements. Each element combines a PS modulator and a digital SCPA. The input LO signal is reconstructed with a controllable phase and amplitude for beam steering and modulation, simultaneously. The LO signals are interpolated by the PS modulator to produce quadrature PM signals (PM_n) with controllable PSs. The control codes for PS modulator (PSM_n), including PM and PS information, are pre-added and sent to the circuits by an on-chip deserializer. The amplitude information (AM) is restored by the digital SCPA. Besides, Doherty and class-G operations are adopted in the SCPA to improve deep PBO efficiency. AM and PM signals are synchronized by adjusting the clocks (CLK_A and CLK_P) to decrease the delay mismatch.

B. Phase-Shifting Modulator

To support the wideband and high-resolution phase operations for the phased-array transmitter, the PS modulator, including active balun, quadrature signals generator, and vector modulator, is introduced. The LO signal is converted into differential signals (LO+, LO−) by the active balun, as shown in Fig. 11(a). In this work, the passive balun is not chosen due to its large circuit size with relatively large insertion loss. The common-source common-gate topology is utilized in the active balun implementation. The in-phase signals are provided by the common-gate transistor (M_1), while the out-of-phase signals are achieved by the common-source stage (M_2). Meanwhile, transistors M_3, M_4, M_5, and bias voltage VG are optimized for an improved wideband balance characteristic. Then, the differential signals are converted into quadrature signals ($LO_{I\pm}$, $LO_{Q\pm}$) by a tunable poly-phase filter (PPF) within a wideband. A two-stage topology for PPF design is employed considering the trade-off between bandwidth and insertion loss. Besides, to further improve the bandwidth of PPF, a switched-capacitor array is introduced. With the increasing operation frequency, the capacitance of switched-capacitor array is deceased. The optimized values are shown in the inset table. Fig. 11(b) shows the rms phase and amplitude errors of generated quadrature signals. With the reconfigurable mechanism, the phase and amplitude errors are less than 1.5° and 0.27 dB over 1.5–3.5 GHz, respectively.

The vector modulator, shown in Fig. 12(a), is implemented by the Gilbert-type cells with voltage-controlled current source. Note that the control voltages ($V_{I\pm}$, $V_{Q\pm}$) are generated from the phase self-calibration loop. Besides, the analog mechanism instead of the digital mechanism is utilized in the current source for easy calibration and high accuracy. To avoid additional switch circuits in signal paths, four pairs of Gilbert-type cells are used for a 360° PS range. Meanwhile, the Gilbert-type cells with two turned-on and two turned-off achieve quadrant selection. The detailed operation states of the PS modulator are listed in Fig. 12(a). With the increasing of control voltage, the transconductance of core MOSFETs in the Gilbert-type cells become larger. The output phase are changed, when the control voltage in one quadrature path increases and the other quadrature path decreases. Then, the output signals are converted into rail-to-rail signals by the buffer chain to drive the switch-cells in the next digital SCPA. To show the original characteristic of the PS modulator, the post-simulated phase response versus control voltage V_c is shown in Fig. 12(b). Note that, the control voltages for I and Q paths are complementary, i.e., $V_{I+}(V_{I-})+V_{Q+}(V_{I-}) = 1.1$ V. For example, $V_{Q+} = V_c$ and $V_{I+} = 1.1 - V_c$ in quadrant 1. A nonlinearity characteristic between phase and voltage is exhibited. Therefore, the phase calibration is necessary.

C. Phase Self-Calibration Loop

The target of the phase self-calibration loop is to linear the relationship between output phase φ and control code PSM of the PS modulator. To achieve the phase self-calibration, the control voltages for the PS modulator are generated from the phase self-calibration loop. As mentioned in Section II, the phase self-calibration mechanism is composed of three parts, i.e., phase detection, reference comparison, and control voltage generation. Fig. 13(a) shows the circuit implementation of the phase detection. The AND gate circuit and two-stage RC low-pass filter are utilized. The rail-to-rail square-wave signals from output and reference terminals are multiplied by the AND gate circuits. The duty cycle of the obtained signals is linear with the phase of output signals. Besides, the dc component of the obtained signals is filtered by the low-pass filter. Fig. 13(b)

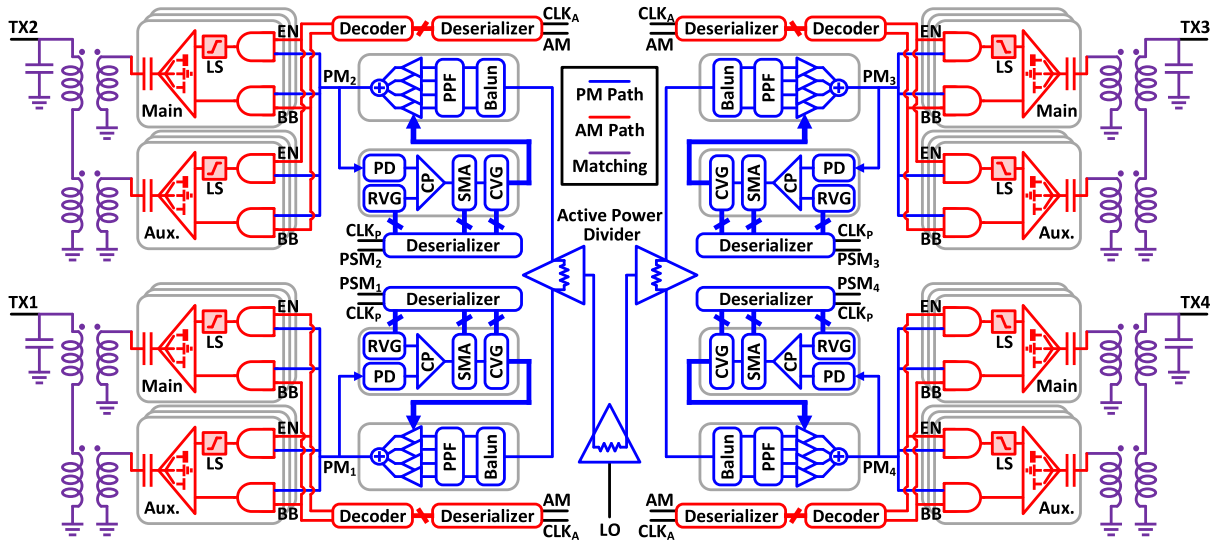


Fig. 10. Simplified block diagram of the proposed PM PS phased-array transmitter (PPF: poly-phase filter, PD: phase detector, RVG: reference voltage generator, CP: comparator, SMA: state memory array, CVG: control voltage generator, and LS: level shifter).

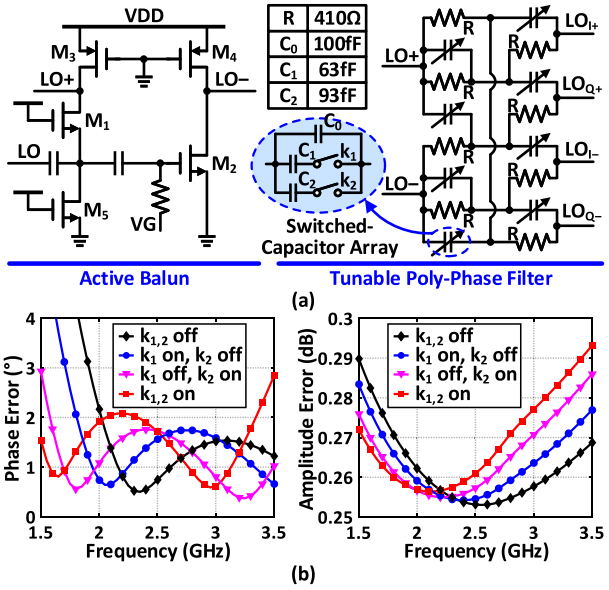


Fig. 11. (a) Schematic of the quadrature signals generator. (b) Simulated rms phase and amplitude errors of quadrature signals.

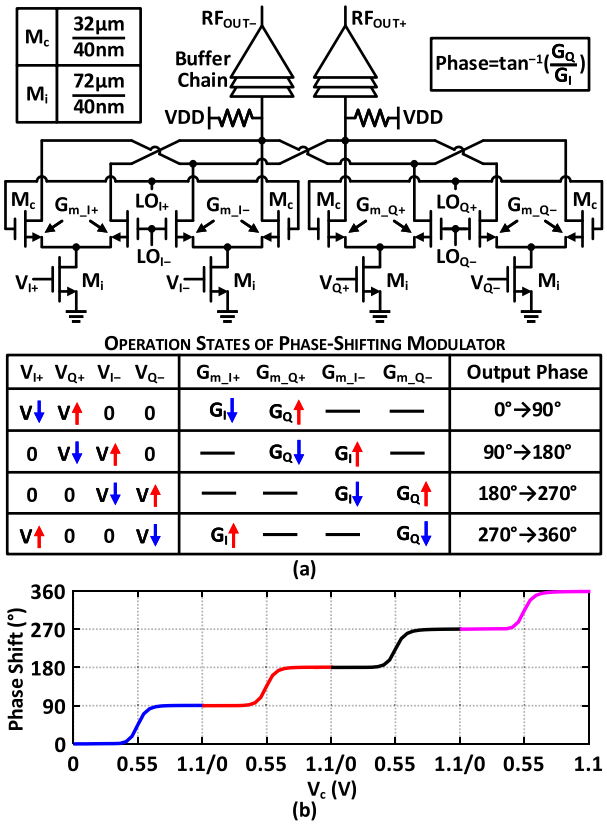


Fig. 12. (a) Schematic and operation of the vector modulator. (b) Simulated phase response of the PS modulator.

illustrates the simulated dc voltage versus output phase under different PVT. It is notable that a linear ratio curve between dc voltage and output phase is obtained under different PVT. Assuming the maximal and minimal values of the detected voltages are V_H and V_L, respectively. Then, the relationship between detected voltage V_{det} and output phase ϕ can be expressed as

$$V_{\text{det}} = -\frac{\phi}{90^\circ}(V_H - V_L) + V_H. \tag{9}$$

Note that, the circuit to generate the reference signals is a replicate of the PS modulator with fixed phase, as shown in Fig. 14(a). Thus, the phase variations introduced by PVT for reference signals φ_r and detected signals φ are the same. Then, the relative phase relationship between reference signals and detected signals is constant. Besides, the quadrant change is achieved by allocating the voltages according to the phase control code (PSMi[9:8]). The detailed operation states are shown in Fig. 14(b).

Due to the linear ratio curve between phase and detection voltage, the reference voltages should be linear with the control codes. Then, the resistor-based voltage-dividing circuit is utilized for reference voltage generation. The schematic of

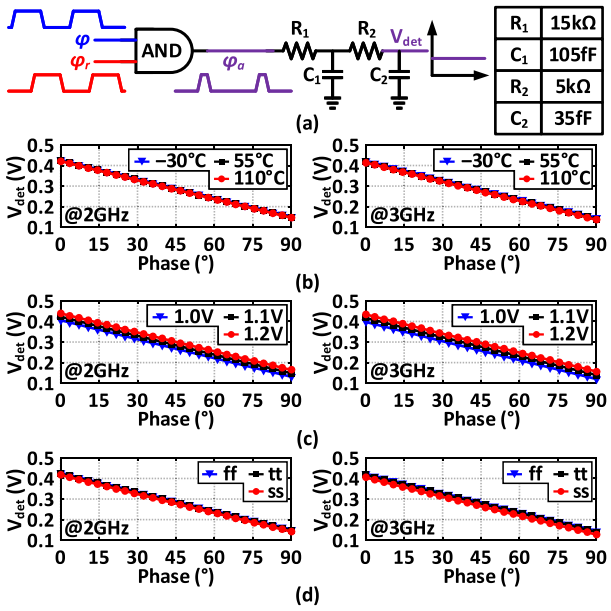


Fig. 13. (a) Schematic of the phase detector. Simulated dc voltages versus output phase under (b) different temperatures, (c) voltages, and (d) process.

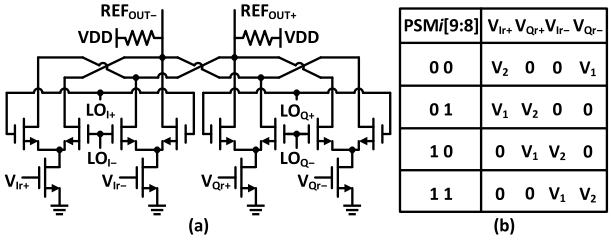


Fig. 14. (a) Schematic and (b) operation states of the quadrature reference signals generator.

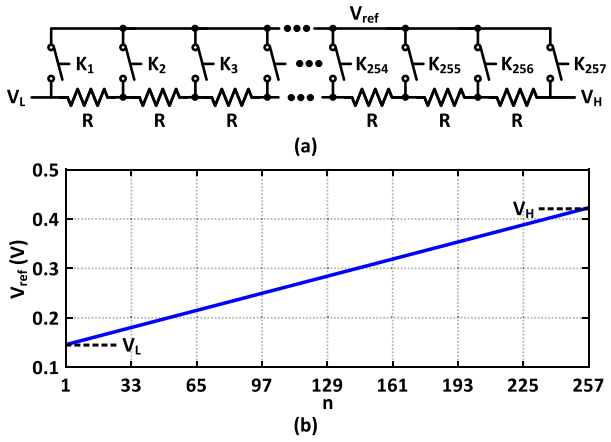


Fig. 15. (a) Schematic of the reference voltages generator. (b) Simulated reference voltages versus the phase control codes.

the reference voltage generator is shown in Fig. 15(a). The identical resistors are connected in series and the switches are connected at the terminals of the resistors to select the desired voltage output. Each switch is determined by the phase control codes. To achieve a 10-bit phase calibration resolution, an 8-bit reference voltage generator is introduced, which includes 2^8 resistors and 2^8+1 switches. When the n^{th} switch is turned on ($K_n = 1$), the reference voltage V_{ref} is

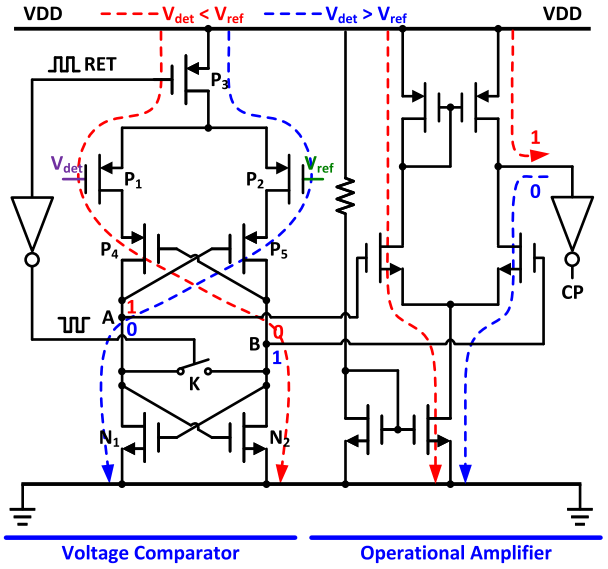


Fig. 16. Schematic of the comparator circuit.

expressed as

$$V_{\text{ref}}|_n = V_L + \frac{n-1}{256}(V_H - V_L), \quad 1 \le n \le 257. \tag{10}$$

Fig. 15(b) illustrates the simulated reference voltages versus the phase control codes. Besides, each resistor in the reference voltage generator is implemented by the polycrystalline silicon resistor with identical width and length. Since the same resistors are used, the reference voltage V_{ref} is depended on the selected switch. The actual resistance value of the resistors has a slight influence on the reference voltages. Note that, the maximal and minimal values of the detected voltages, i.e., V_H and V_L, are used for the reference voltages. Then, the voltage in the reference voltage generator aligns with the voltage variation introduced by the PVT in the phase detector.

A comparator is introduced to compare the detection voltages and reference voltages [52]. The target of the comparator is to achieve $V_{\text{det}} = V_{\text{ref}}$, when phase self-calibration loop is locking. Then, by calculating (9) and (10), the relationship between phase ϕ and code n can be expressed as

$$\phi = \left(1 - \frac{n-1}{256}\right) \times 90°. \tag{11}$$

It means the output phase is only determined by the control code n, when (9) and (10) are satisfied. The phase shift is not susceptible to PVT variations.

The detailed schematic of the comparator is shown in Fig. 16. The comparator consists of a voltage comparator and an operational amplifier. A PMOS differential pair with a digital-controlled switch source and cross-coupled transistor pairs construct the voltage comparator. A control signal RET is introduced to initialize the voltage comparator. When RET is VDD, the current source P_3 of the differential pair is switched off. Then, the current charging path is cut off. Besides, the switch K in the cross-coupled transistor pairs is turned on. Thus, the voltages between nodes A and B are the same, the comparator circuit is initialized. The voltages can be compared under RET = 0. When the detection voltages V_{det} and

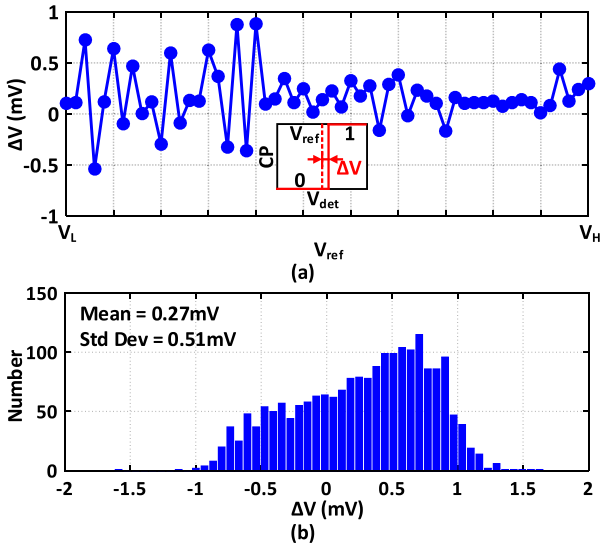


Fig. 17. (a) Simulated offset voltage of the comparator circuit. (b) 2000 point Monte-Carlo offset-voltage simulation.

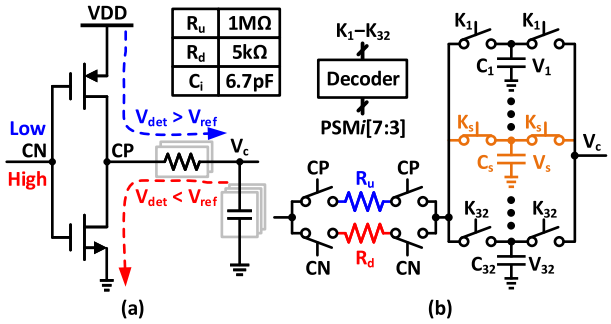


Fig. 18. (a) Control voltage generation. (b) Schematic of the capacitor-based state memory array.

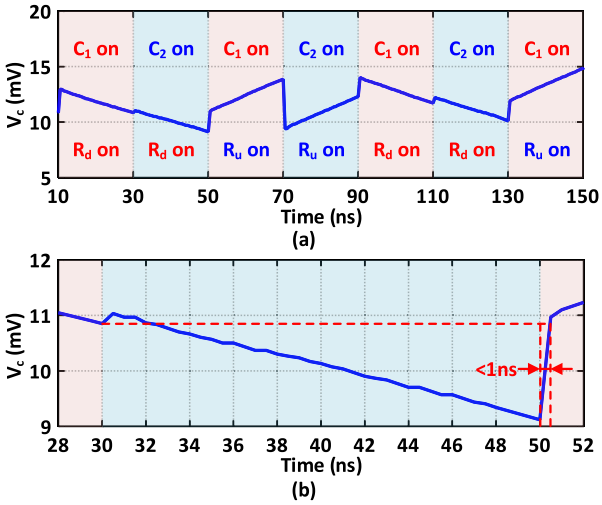


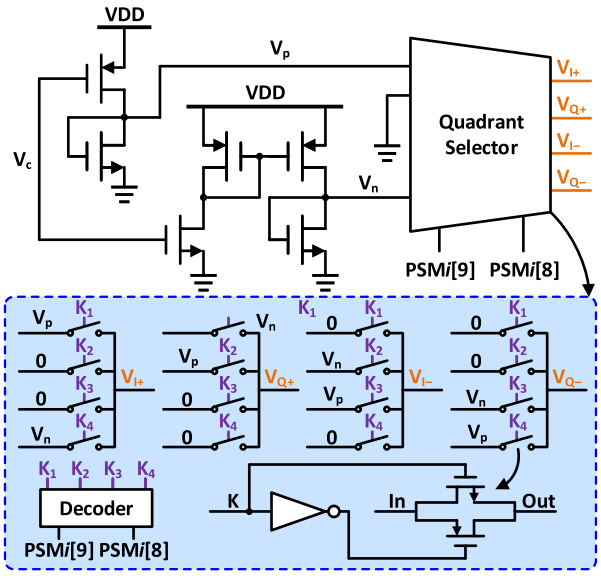
Fig. 19. Simulated transient voltage under (a) seven and (b) one switch times.

reference voltages V_{ref} are different, the drain–source currents between P_1 and P_2 in the differential pair are nonidentical. Thus, the charge time at nodes A and B are different. When V_{det} is smaller than V_{ref}, node A is charged to VDD faster than node B. Then, N_2 is switched on and node B is discharged to GND. Besides, the cross-coupled transistor pairs are locked and a stable comparison result is obtained. When V_{det} is larger than V_{ref}, node B will be charged to VDD faster than node A. Then, N_1 is switched on and node A is discharged to GND. The cross-coupled transistor pairs are locked and a contrary comparison result is obtained. To improve the drive capability, the operational amplifier is introduced after the voltage comparator.

The simulated offset voltages ΔV versus various reference voltages are shown in Fig. 17(a). Note that, the offset voltage is defined as the voltage difference between input voltage V_{det} and reference voltage V_{ref} when the comparison results CP is turned. The offset voltages versus various reference voltages are less than 1 mV. Besides, to show the robustness of the voltage comparator, the Monte-Carlo simulation with 2000 point is performed. The simulated result is shown in Fig. 17(b). Note that, the reference voltage is set as 275 mV, i.e., about $(V_H + V_L)/2$ in a typical case. The average and standard deviation values are 0.27 and 0.51 mV, respectively. The ideal calibration condition is $V_{\text{det}} = V_{\text{ref}}$. Thus, the offset voltage brings a phase calibration error. The voltage range of the detected voltage is about $1.1V/4 = 275$ mV. Besides, the corresponding phase range is 90°. Therefore, the phase error introduced by the offset voltage can be estimated as 90°/275 mV = 0.33°/mV, i.e., 1-mV offset voltage error introduces 0.33° phase error.

The control voltages for PS modulator are generated based on the compared results. It is achieved by an RC charging circuit, as shown in Fig. 18(a). When V_{det} is larger than V_{ref}, the compared result is high. Then, the capacitor is charged and the control voltage V_c increases. When V_{det} is smaller than V_{ref}, the compared result is low. The capacitor is discharged and the control voltage V_c decreases. Two resistors (i.e., R_u and R_d) are utilized to adjust the charge/discharge speed. The optimized values of R_u and R_d are 1 MΩ and 5 kΩ, respectively. Besides, a switched capacitor array, shown in Fig. 18(b), is introduced to store the control voltages for various phase states. The switch for each capacitor is controlled by the phase control codes directly. Meanwhile, the value of each capacitor is chosen as 6.7 pF and 32 capacitors are utilized in the switched capacitor array. Fig. 19 illustrates the simulated transient voltage. It is notable that the switch time between two voltages is less than 1 ns.

The phase calibration loop is based on the feedback principle. Thus, the calibration time is determined by the locking time of the feedback loop, i.e., the settle time of control voltage V_c. To reduce the locking time of the loop, the capacitor-based state memory array is introduced to pre-store the required control voltages. Then, the phase self-calibration loop operates in two cases, i.e., initialization case and amplifying case. In the initialization case, each capacitor in the state memory array is charged and stores the different calibrated states. In the amplifying case, the stored voltages is re-charged to maintain the calibrated states. Thus, the PS modulator requires only one relatively long (μs-level) initialization time and does not need to be recalibrated for each phase calibration. Besides, the calibration time is equal to the switching time



$V_{det} > V_{ref}$: V_c ↑ $V_{det} < V_{ref}$: V_c ↓

PSM*i*[9]	PSM*i*[8]	K_1	K_2	K_3	K_4	V_{I+}	V_{Q+}	V_{I-}	V_{Q-}
0	0	1	0	0	0	V_p↓↑	V_n↑↓	0	0
0	1	0	1	0	0	0	V_p↓↑	V_n↑↓	0
1	0	0	0	1	0	0	0	V_p↓↑	V_n↑↓
1	1	0	0	0	1	V_n↑↓	0	0	V_p↓↑

Fig. 20. Schematic of the control voltage generator.

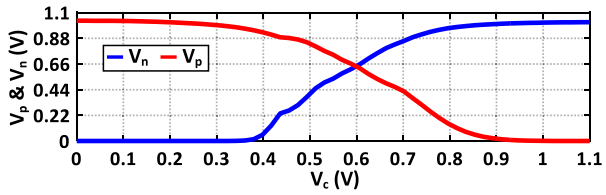


Fig. 21. Simulated result of the control voltage generator.

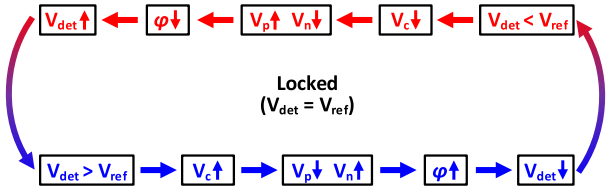


Fig. 22. Phase calibration procedure.

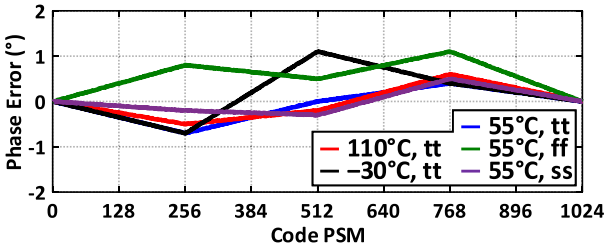


Fig. 23. Simulated phase error of the PS modulator under various corners and temperatures.

of the state memory array, i.e., less than 1 ns. 2^5 capacitors are used in the state memory array. Thus, 7-bit PS with fast-locking is achieved to support high data rates. To improve the phase resolution for beam-steering, the additional 3-bit PS is achieved by further charging/discharging the stored voltages. Then, the longest calibration time can be estimated as 400 (mV)/32/2 × 10 (ns/mV) = 62.5 ns, where 400 mV is the range of V_c and 10 ns/mV is the charging/discharging speed of the capacitor.

For the proposed PS modulator, the control voltage V_c needs to be converted into voltages V_p and V_n. An inverse-proportional circuit is utilized to generate the voltage V_p, while a direct-proportional circuit is used to generate the voltage V_n. The inverse-proportional circuit consists of a PMOS and a NMOS, as shown in Fig. 20. The control voltage V_c is fed to the gate of PMOS, then the drain voltage (V_p) decreases with the increasing of V_c. The direct-proportional circuit is composed of two cascaded inverse-proportional circuits. Thus, the drain voltage (V_n) increases with the increasing of V_c. The simulated V_p and V_n versus V_c are shown in Fig. 21. Then, the voltages V_p and V_n are converted into $V_{I\pm}$ and $V_{Q\pm}$ by a quadrature selector. The control voltages $V_{I\pm}$ and $V_{Q\pm}$ are connected to the current source of vector modulator in the PS modulator. The voltages V_p, V_n and 0 are selected based on the highest two bits of phase control codes.

From the perspective of circuits and signal, the whole phase calibration procedure can be summarized in Fig. 22. When the output phase is smaller than the desire phase, the detected voltage V_{det} is larger than the reference voltage V_{ref}. Then, the compared result charges the capacitor to obtain an increased control voltage V_c. An increased V_c induces a decreased V_p and increased V_n, which leads to a larger output phase to approach the desire phase. On the contrary, when the output phase is larger than the desire phase, the detected voltage V_{det} is smaller than the reference voltage V_{ref}. Then, a decreased control voltage V_c induces a smaller output phase to approach the desire phase. The circuits are locked as detected voltage V_{det} is equal to reference voltage V_{ref}. Meanwhile, the output phase is the same as the desire phase. The simulated relationship between phase error and code of the PS modulator with phase self-calibration loop under various corners and temperatures are shown in Fig. 23. From the simulation, corners and temperatures exhibit little influence on the quadrature signals generation.

D. Class-G Voltage-Mode Doherty SCPA

To enhance the system efficiency of the phased-array transmitter under modulation signals with high PAPR, the SCPA with PBO efficiency enhancement is proposed. With combination of Doherty and class-G operations, efficiency enhancement at 0-/2.5-/6-/12-dB PBOs is achieved [53]. Fig. 24 depicts the schematic of the proposed class-G voltage-mode Doherty SCPA, which consists of main sub-PAs, auxiliary sub-PAs, and a 4-to-1 transformer. Each sub-PA is composed of 6-bit unary-weight MSB cells and 2-bit binary-weighted LSB cells. Besides, each unit cell is implemented by the cascode inverter, which can support three operation modes, i.e., high power (2VDD) mode, low power (VDD)

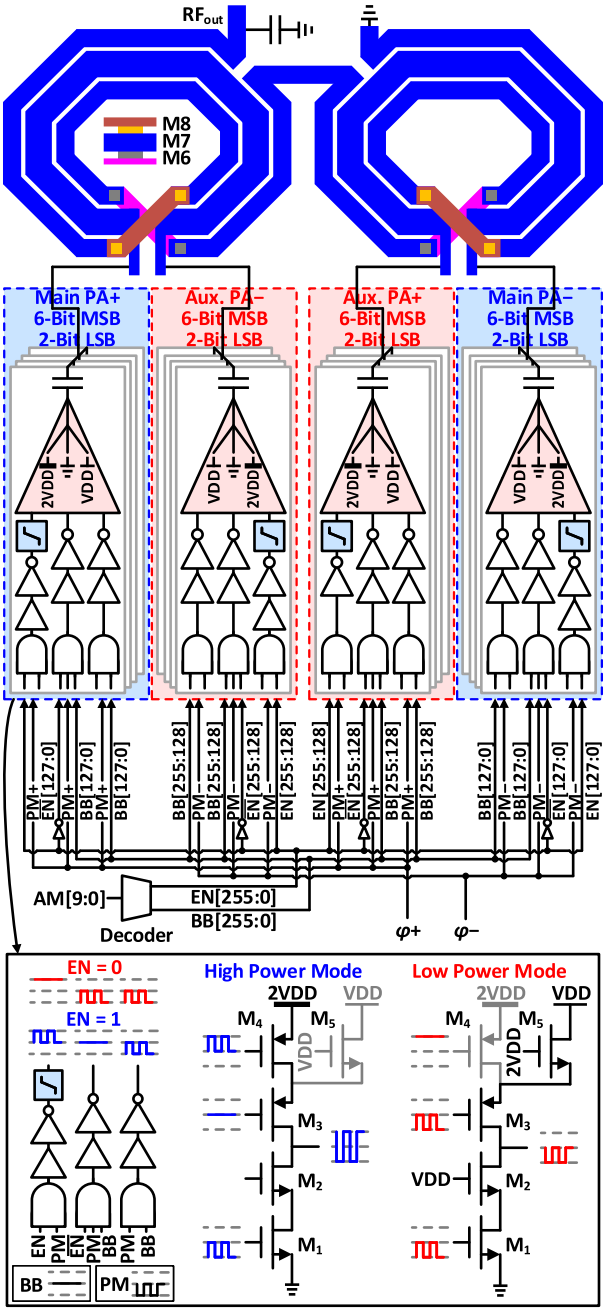


Fig. 24. Schematic of the proposed class-G voltage-mode Doherty SCPA.

mode, and off (GND) mode. Note that, the dimensions of PMOS (M_3 and M_4) and NMOS (M_1, M_2, and M_5) are 108/40 and 54 μm/40 nm, respectively. The ac-coupled capacitor C_{ac} is optimized as 330 fF for each MSB unit cell. Meanwhile, the ac-coupled capacitors for 2-bit LSB unit cells are 165 and 82.5 fF, respectively. The mode selection is achieved by the control signal EN. When EN = 1, the unit cell is working on high power mode. The transistor M_5 is turned off. M_4 is switching from 2VDD to VDD, while M_1 is switching from VDD to GND. Once EN = 0, the unit cell is working on low power mode. The transistor M_4 is turned off. M_3 and M_1 are switching from VDD to GND. The 4-to-1 transformer is implemented by the top three thick metals.

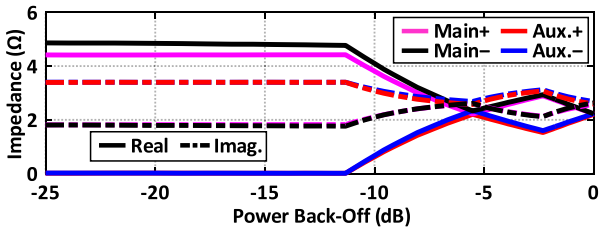
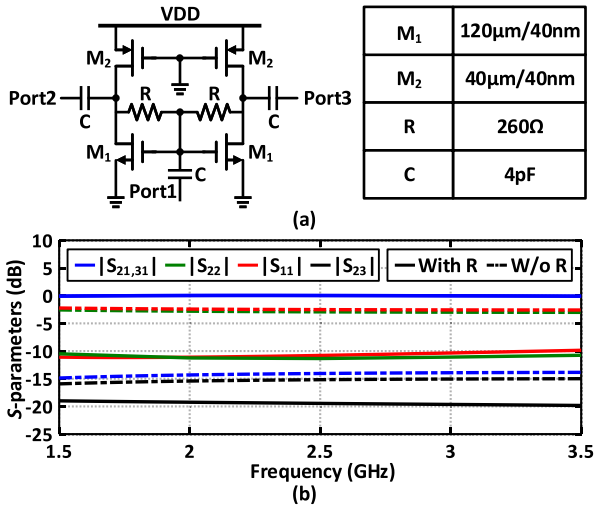


Fig. 25. Simulated load impedances at the four terminals (Main+/− and Aux.+/−) of the output combiner.



M_1	120μm/40nm
M_2	40μm/40nm
R	260Ω
C	4pF

Fig. 26. (a) Schematic of the active power divider. (b) Simulated S-parameter.

The EM-simulated inductances of primary and secondary inductors (i.e., L_p and L_s) are 260 and 800 pH, respectively. Besides, the typical quality factors Q_p and Q_s are 14.8 and 14.9, respectively. The simulated power loss of the 4-to-1 transformer is less than 1.4 dB from 2.1 to 2.9 GHz. Fig. 25 exhibits the simulated load impedances at the four terminals (Main+/− and Aux.+/−) of the 4-to-1 transformer at 2.4 GHz. The simulated real part of the passive load impedance is boosted by the Doherty techniques.

E. Active Power Divider

To improve the isolation among different transmitter channels, active power dividers with low size are introduced [54]. Fig. 26(a) depicts the schematic of the proposed active power divider. Two common-source amplifiers are utilized to divide the input signal into two paths. Besides, two resistors R are connected between two output terminals. Three capacitors are introduced in the input and output terminals for the dc block. The optimized values of the active power dividers are shown in the inset table. The resistor in the proposed active power amplifier has three functions: 1) offer the proper quiescent point, i.e., bias voltage for M_1; 2) enhance the isolation between Port 2 and 3; and 3) improve the impedance matching for input and output ports. The simulated S-parameter with and without R is shown in Fig. 26(b). The insertion gain, excluding 3-dB dividing power, is better than 2.9 dB from 1.5 to 3.5 GHz, while the in-band isolation is higher than 19 dB with resistors.

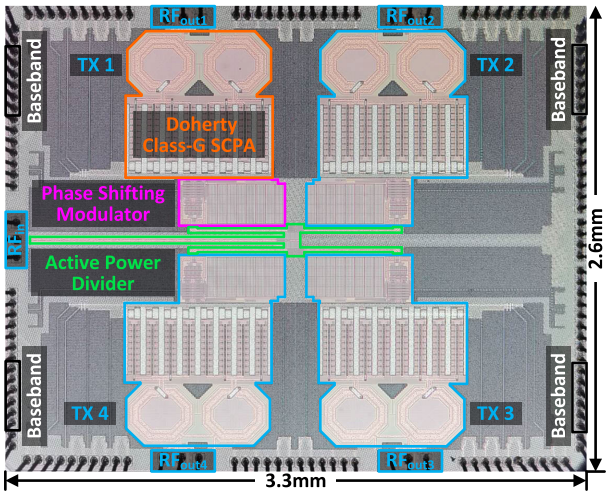


Fig. 27. Die micrograph of the proposed phased-array transmitter.

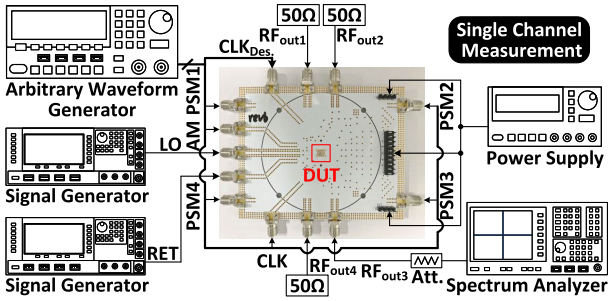


Fig. 28. Measurement setup for single-channel characterizations.

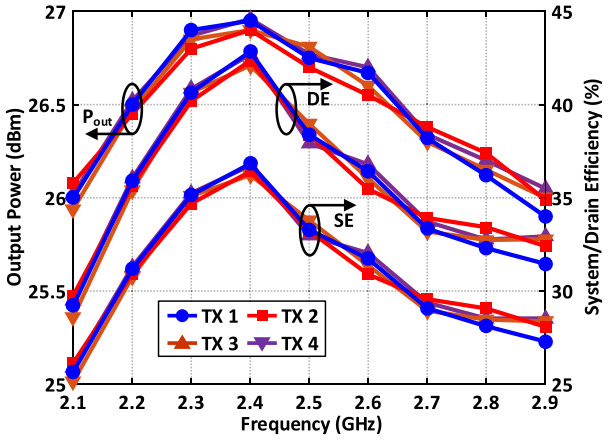


Fig. 29. Measured output power and efficiency among four channels.

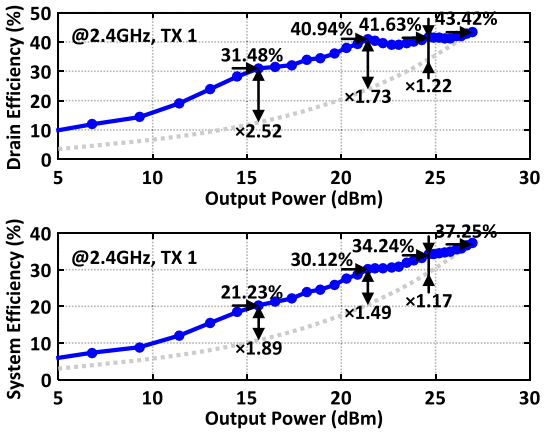


Fig. 30. Measured drain and system efficiencies versus output power.

IV. Fabrication and Measurement

Based on the mechanisms mentioned above, a PM PS phased-array transmitter with phase self-calibration and deep PBOs efficiency enhancement is implemented and fabricated in a conventional 40-nm CMOS technology. The chip microphotograph is shown in Fig. 27. The total chip size is 3.3 × 2.6 mm^2 including all pads. Meanwhile, to support a high output power and class-G operation, the supply voltage is 1.1/2.2 V.

Fig. 28 shows the measurement setup for each single transmitter channel. The chip is mounted on a printed circuit board (PCB) without any off-chip matching networks. All pads, including input and output GSG pads, are wire-bonding on the PCB. Besides, the RF, baseband, and clock signals are fed into the chip by the SMA connectors. A signal generator and a spectrum analyzer are utilized to measure the output power, power linearity, and output phases of the proposed phased-array transmitter. The reset signal RET for the self-calibration loop is provided by a signal generator, while the baseband signals are offered by an arbitrary waveform generator. The amplitude (C_{AM}) and phase codes ($C_{\mathrm{PSM}n}$) are synchronized with CLK. Each channel is measured with other three channels connecting to 50-Ω load. All the losses, including path, wire-bonding, and connector loss, are calibrated out.

The measured output powers among four transmitter channels of the proposed phased-array transmitter are illustrated in Fig. 29. The fabricated phased-array transmitter delivers a peak output power of 26.95 dBm at 2.4 GHz. Besides, the 1-dB operation bandwidth is from 2.1 to 2.9 GHz, while the corresponding FBW is 32%. The output power variation is less than 0.15 dB among four channels. For continuous waveform (CW) measurement at 2.4 GHz, the power consumption of SCPA, PS modulator with self-calibration loop, and active power divider at saturation power are 4 × 1262.1, 4 × 62.6, and 3 × 7.1 mW, respectively. The power consumptions of digital circuits, drivers, and buffers are also included in the corresponding parts. All the power consumptions are considered in the calculation of system efficiency. The peak system efficiency is 37.25% at 2.4 GHz, while the corresponding drain efficiency is 43.42%. To investigate the efficiency performance at PBO, the drain and system efficiencies versus output power are depicted in Fig. 30. The phased-array transmitter achieves drain efficiency of 43.42%, 41.63%, 40.94%, and 31.48% for 0-, 2.5-, 6-, and 12-dB PBO peaks at 2.4 GHz, while the corresponding system efficiency is 37.25%, 34.24%, 30.12%, and 21.23%, respectively. 1.22×, 1.73×, and 2.52× drain efficiency improvements are achieved at 2.5-, 6-, and 12-dB PBO peaks, respectively, compared to conventional class-B power amplifier. Meanwhile, the corresponding improvements of system efficiency are 1.17×, 1.49×, and 1.89×, respectively.

The 10-bit output phase response after self-calibration is measured as shown in Fig. 31(a). The relatively phase shifts

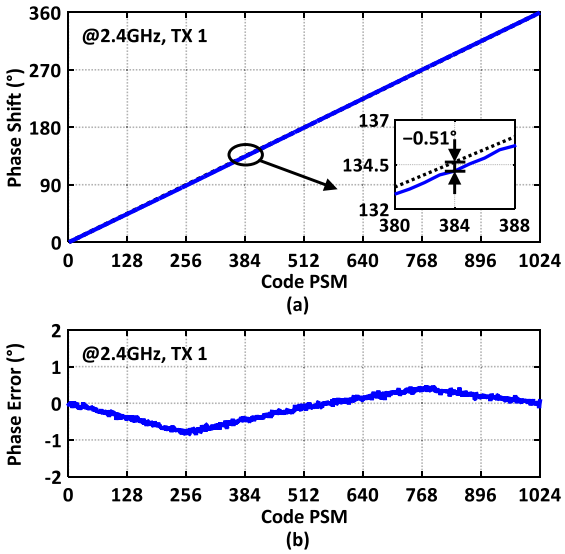


Fig. 31. (a) Measured phase shift with phase self-calibration at 2.4 GHz. (b) Measured phase error.

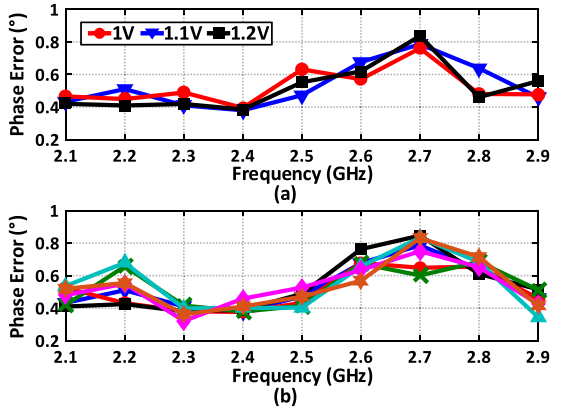


Fig. 32. RMS phase errors versus (a) different supply voltages and (b) chip samples.

are obtained by subtracting the measured phase shifts from 0 state phase shift. With the phase self-calibration, the phase response shows a linear characteristic, which is close to the ideal value. Besides, the phase errors for each phase state are calculated as depicted in Fig. 31(b). A maximum 0.87° phase error is achieved for 1024 phase states. To investigate the influence of supply voltage and process on rms phase errors, different supply voltages and chip samples are measured. As shown in Fig. 32, there is a small discrepancy of phase errors among different voltages and chip samples, which means a negligible influence of voltage and process on the phase self-calibration. Note that, the phase errors are mainly caused from the phase mismatch of the quadrature signals generated by the tunable PPF. Fig. 33 illustrates the measured output powers versus phase control codes. Due to the PM PS architecture, the amplitude variation of PS modulator has a negligible influence on the output power of the phased-array transmitter. The output power variation versus phase shift is less than ±0.4 dB at 2.4 GHz. Then, the rms output phase and power errors are calculated at 2.4 GHz, which are 0.4° and 0.2 dB, respectively.

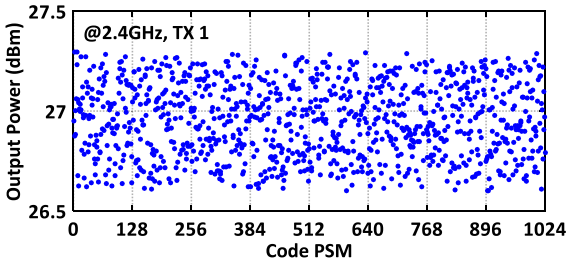


Fig. 33. Measured output power versus phase control code C_{PSM}.

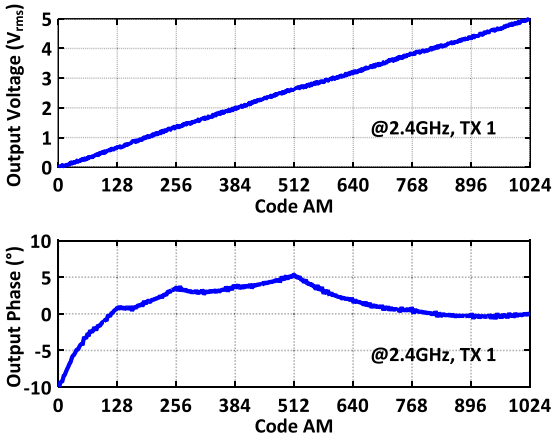


Fig. 34. Measured AM/AM and AM/PM distortions.

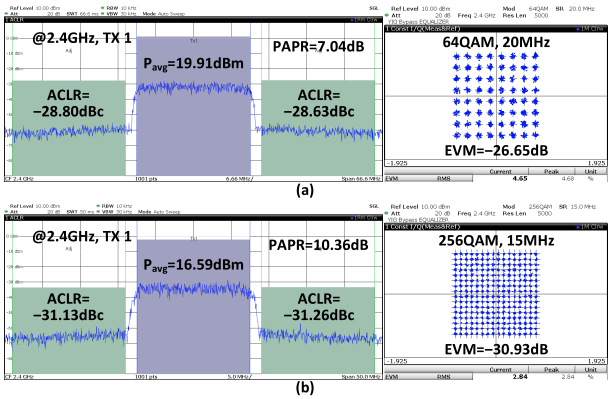


Fig. 35. (a) Measured 64-QAM constellation and spectrum with 20-MHz modulation bandwidths at 2.4 GHz. (b) Measured 256-QAM constellation and spectrum with 15-MHz modulation bandwidths at 2.4 GHz.

Fig. 34 shows the measured AM/AM and AM/PM distortions of the phased-array transmitter by swinging the amplitude codes AM. Since the unit cells in SCPA are operated from different power supplies individually, the amplitude glitch at code 512 is that of a single unit cell. Besides, the proposed SCPA features a 10-bit amplitude resolution. Thus, little amplitude discontinuity at 6-dB PBO is achieved. Due to the similar operation with SCPA [53], the phased-array transmitter shows a linear AM/AM distortion. In addition, the corresponding AM/PM distortion is less than 10°.

Fig. 35 shows the measured spectrum and constellation at 2.4 GHz. The proposed transmitter exhibits EVM of −26.65 dB for 64-QAM signals with modulation bandwidths of 20 MHz at a data rate of 120 Mb/s, P_{avg} of 19.91 dBm,

TABLE I
COMPARISONS WITH THE STATE-OF-THE-ART PHASED-ARRAY TRANSMITTERS

Ref.		This work		ISSCC 2019 [41]	JSSC 2021 [40]	RFIC 2020 [43]	JSSC 2019 [42]	JSSC 2020 [2]
Architecture		Doherty class-G SCPA with self-calibration phase-shifting modulator		SCPA with multi-phase phase-shifting	Digital modulated polar TX with PM phase-shifting	Direct digital beamforming with FIR H-bridge CSDAC	True-time-delay digital beamformer	True-time-delay digital beamformer
Frequency (GHz)		2.1–2.9*	1.9–3.3$^{\Delta}$	1.45–2.15$^{\Delta}$	3–7$^{\Delta}$	6	1	9.1–10.6*
Normalized Bandwidth (%)		32*	53.8$^{\Delta}$	38.9$^{\Delta}$	80$^{\Delta}$	N/A	N/A	15.2
Elements		4		4	4	8	16	4
Phase Resolution (°)		0.35		0.7	0.35	N/A	0.35	5.625
Calibration		On-chip self-calibration		Off-line calibration	Digital pre-distortion	Digital calibration	N/A	N/A
RMS Phase Error (°)		0.4		0.32	0.3–1.6	N/A	N/A	3.1
RMS Pout Error (dB)		0.2		0.15	0.2	N/A	N/A	1.08
Peak Pout (dBm)		26.95		24.4	21.8	4.7	N/A	10.2
On-Chip PA		Yes		Yes	Yes	No	No	Yes
System Efficiency (%)	0dB PBO	37.25		24.2	38.2	N/A	N/A	19.3
	2.5dB PBO	34.24		N/A	N/A	N/A	N/A	N/A
	6dB PBO	30.12		N/A	N/A	N/A	N/A	N/A
	12dB PBO	21.23		N/A	N/A	N/A	N/A	N/A
Modulation		20MHz 64-QAM	15MHz 256-QAM	15MHz 64-QAM	40MHz 64-QAM	24MHz 16-QAM	5MHz 512-QAM	N/A
Average SE (%)		24.12	19.21	14	N/A	N/A	N/A	N/A
EVM (%)		4.65@2.4GHz	2.84@2.4GHz	3.7@1.75GHz	5.76@5GHz	3.3@6GHz	0.89@1GHz	N/A
Supply Voltage (V)		1.1/2.2		1.4/2.8	1.1/1.2	1	N/A	1.2
Technology		40nm CMOS		65nm CMOS	40nm CMOS	28nm CMOS	40nm CMOS	65nm CMOS
Chip Area (mm×mm)		3.3×2.6		2×2.5	4.3×2	1.5×1.1	2.2×2	4×2.65$^{\#}$

*1-dB output power bandwidth; $^{\Delta}$3-dB output power bandwidth; $^{\#}$TRX

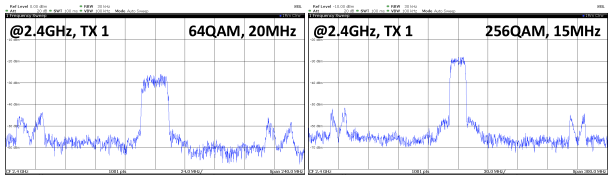


Fig. 36. Measured out-of-band spectrum of 20-MHz 64-QAM and 15-MHz 256-QAM signals.

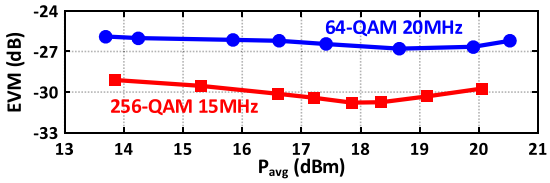


Fig. 37. Measured EVM of modulation signals versus P_{avg}.

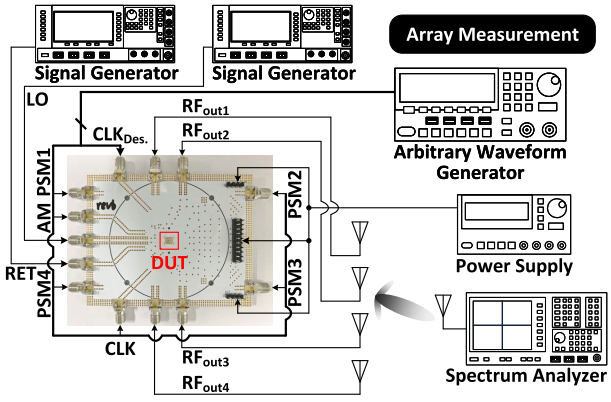


Fig. 38. Measurement setup for array characterizations.

adjacent channel leakage ratio (ACLR) ≤ -28.63 dBc, and a baseband sampling frequency of 100 MHz at 2.4 GHz. In addition, the proposed transmitter exhibits EVM of -30.93 dB for 256-QAM signals with modulation bandwidths of 15 MHz

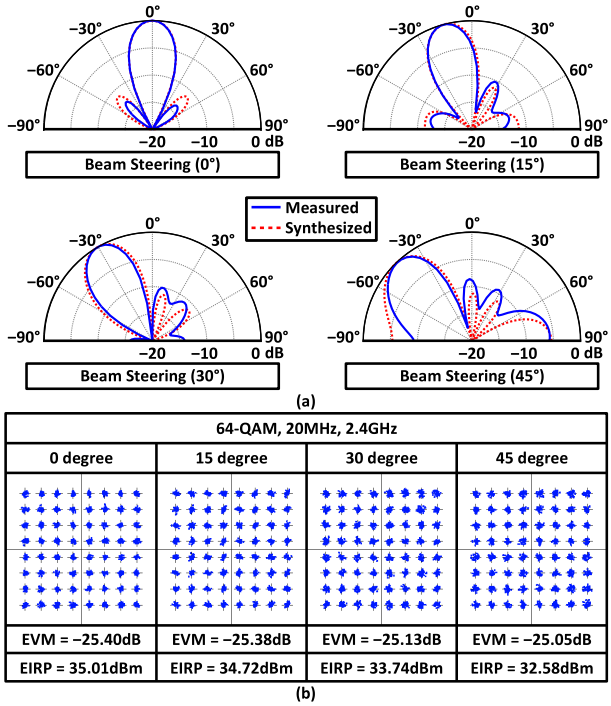


Fig. 39. (a) Measured four-element radiation patterns at 2.4 GHz with 0°, 15°, 30°, and 45° beam steering. (b) Measured constellations and EIRP of 64-QAM signals with bandwidths of 20 MHz from 3-m distance at 2.4 GHz.

at a data rate of 120 Mb/s, P_{avg} of 16.59 dBm, ACLR ≤ -31.13 dBc, and a baseband sampling frequency of 100 MHz at 2.4 GHz. The out-of-band spectrum of 20-MHz 64-QAM and 15-MHz 256-QAM signals are shown in Fig. 36. The spectrum image is mainly caused by the digitized and time-sampled interpolations of the signal envelope. The measured EVM of modulation signals versus average output power P_{avg} is shown in Fig. 37. The EVM of 64- and 256-QAM signals could be further improved at proper PBO levels.

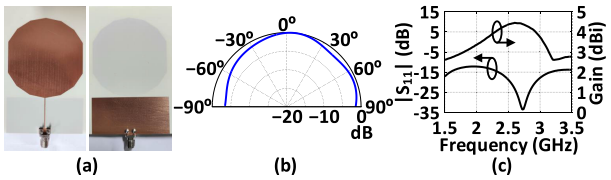


Fig. 40. (a) Photograph of the monopole antenna. (b) Measured radiation pattern. (c) Measured return loss and gain of the monopole antenna.

To further validate the array level performance of the proposed phased-array transmitter, measurements with antennas are carried out with the measurement setup in Fig. 38. The monopole antenna arrays are utilized as the transmitting antenna, which features an antenna gain of 4.21 dBi at 2.4 GHz. The detailed discussion of the antenna is shown in the Appendix. As the definition of effective isotropic radiated power (EIRP) in [3], the measured EIRP is 42.05 dBm at 2.4 GHz. Under a half wavelength ($\lambda/2$) spacing between two adjacent antennas at 2.4 GHz, the radiated beam patterns with 0°, 15°, 30°, and 45° steering are measured. Normalized to the peak power, the measured beam patterns are depicted in Fig. 39(a). Meanwhile, Fig. 39(b) illustrates the measured constellations of 64-QAM signals with a bandwidth of 20 MHz from a 3-m transmission distance. The phased-array transmitter exhibits EVM of −25.40, −25.38, −25.13, and −25.05 dB and EIRP of 35.01, 34.72, 33.74, and 32.58 dBm under 0°, 15°, 30°, and 45° beam steering, respectively.

Table I summarizes and compares performances with the state-of-the-art phased-array transmitters. It is notable that the proposed phased-array transmitter exhibits a competitive phase and power errors with phase self-calibration, the highest output power, and efficiency enhancement at deep PBOs, which is a promising candidate for modern wireless systems.

V. Conclusion

In this article, a PM PS phased-array transmitter with phase self-calibration and deep PBOs efficiency enhancement is proposed. To obtain high-resolution PS and PM characteristics, a PS modulator with a phase self-calibration loop is introduced. Besides, the fast locking technique is presented to lower the calibration time. Then, to improve the average system efficiency under modulation, the class-G and Doherty operations are employed in the SCPA implementation. Based on a conventional 40-nm COMS technology, the proposed phased-array transmitter is implemented with rms power and phase errors of 0.2 dB and 0.4° at 2.4 GHz. Meanwhile, the phased-array transmitter delivers 37.25%, 34.24%, 30.12%, and 21.23% system efficiency at 0-, 2.5-, 6-, and 12-dB PBOs. With the accurate phase response, low phase/power errors, and high system efficiency, the proposed phased-array transmitter is attractive in high data-rate wireless communication and high-resolution detection radar systems.

Appendix

The monopole antenna, shown in Fig. 40(a), is utilized for measurement. The measured normalized radiation pattern of the antenna at 2.4 GHz is shown in Fig. 40(b). Besides, the measured antenna gain and return loss are shown in Fig. 40(c). The antenna features a better than 2.5-dBi antenna gain from 1.5 to 3.5 GHz. Meanwhile, the measured return loss is better than −12 dB.

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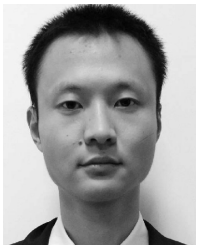

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