Design of a Low-Power, High-Data-Rate, and Crystal-Less All-Digital IR-UWB Transmitter for High-Density Neural Implants

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***Abstract*— This article presents an all-digital, crystal-less impulse radio ultra-wideband (IR-UWB) transmitter for the high-density neural implants with several thousand channels. A six-order hybrid modulation scheme combining the differential 16-pulse-position modulation (D16PPM), pulsewidth modulation (PWM), and differential bi-phase shift keying (DBPSK) is proposed to achieve a high data rate and guarantee the transcutaneous data transmission. A detailed theoretical analysis of the signal-to-noise ratio (SNR) and symbol error rate (SER) relationship is included, along with the analysis of removing the crystal. The proposed transmitter uses a 42-stage bi-phase ring oscillator (RO) to provide all the edges to combine. A highly symmetrical pulse generator and a pulse shaper (PS) with an edge detector (ED) chain are designed, respectively, to realize the proposed modulation scheme efficiently. The transmitter achieves a data rate of 1.8 Gbps with a power consumption of only 4.09 mW. Thus, a power efficiency of 2.3 pJ/bit is achieved. In an ex vivo test, a transcutaneous transmission range of 20 cm was measured with 18-mm pork tissue applied.**

***Index Terms*— Brain–machine interfaces (BMIs), crystal-less, digital transmitter, hybrid modulation, impulse radio ultra-wideband (IR-UWB), neural implants.**

I. Introduction

NEURAL implants enable neural signal acquisition from the inner brain, offering new possibilities for interacting between man-made devices and the neural system. Since there are billions of neurons in the human–brain, more sensing channels are needed for higher spatial resolution. Recently, a batch of thousand-channel high-density electrodes have been reported in the literature [1], [2], [3], [4]. The data throughput of the neural implants increases proportionally to the number of channels to Gbps level. For instance, a neural implant with 3000 sensing channels, a sampling rate of 30 kSps per channel, and a 16-bit quantization generates a total data throughput of 1.44 Gbps. Such a large data throughput becomes a key challenge in transferring the acquired neural data to the outside body, across the skull and skin [5], [6]. Lossy compression technologies, such as ON-chip spike sorting, spike-driven data compression, and compressed sensing, have been proposed to reduce the data load by 6×–10× [7], [8], [9], [10]. However, the additional power required for data compression may exceed the power saved by the wireless data link [5]. In addition, since there is not yet a consensus on the specifications of the compressed neural data [11], the lossless raw data are still preferred in current scientific research. A high-data-rate wireless telemetry module that can transmit all the raw acquired neural data is strongly demanded by the high-density neural implants.

Various wireless technologies have been explored for the implantable scenarios, such as custom Medical Implant Communication System (MICS) or Industrial Scientific Medical (ISM) band transmission [12], [13], [14], [15], inductive coupling transmission [16], [17], [18], [19], ultrasonic communication [20], [21], [22], optical communication [23], [24], [25], human body communication (HBC) [26], [27], [28], [29], [30] and impulse radio ultra-wideband (IR-UWB) [31], [32], [33], [34], [35], [36], [37]. Most of these solutions achieve a data rate from several Mbps to ∼300 Mbps, while IR-UWB outperforming them by achieving the highest data rate of more than 1 Gbps. This performance is due to its >500 MHz available bandwidth, allowing Gbps throughput with a relatively low complexity and low-power consumption design. Therefore, IR-UWB is a promising option to meet the requirements of high-density neural implants.

Nevertheless, there are still several challenges remaining to be addressed. One of the key design challenges is that the transmit power spectral density (PSD) is limited to −41.3 dBm/MHz to comply with the Federal Communication Commission (FCC) UWB regulation. For a UWB transmitter operating with an exact bandwidth of 500 MHz, the maximum TX power is limited to −14.3 dBm. For IR-UWB, the TX power is equal to the pulse repetition frequency (PRF)

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multiplied by the energy per pulse. While the PRF should typically be higher to boost the data rate, an escalation of PRF in turn reduces the energy per pulse, which consequently weakens the ability to cope with the additional path loss due to the biological tissue. Thus, a contradiction arises between the high-data-rate demand and the practicality of transcutaneous data transmission. Two methods have been proposed to alleviate this contradiction. One is to further increase the bandwidth. Kim and Rabaey [38] introduced triple-channel UWB with a total bandwidth of 1 GHz. Geng et al. [39], Ko and Gharpurey [40], and Lee et al. [41], [42] introduced frequency hopping technology, achieving a total bandwidth of more than 2 GHz, respectively. With a larger bandwidth, the total TX power can be larger to guarantee the energy per pulse. The other way to balance the data rate and the transcutaneous transmission is to increase the modulation order. Lee et al. [43] proposed digitalized multi-pulse-position modulation (D-MPPM). With a sync pulse and a data pulse with 32 possible positions in one symbol, the modulation order increased to 2.5. Lee et al. [41], [42] further added one more data pulse in a symbol and introduced extended multi-pulse-position modulation (E-MPPM), resulting in a modulation order of 3. However, the sync pulse in E-MPPM still reduced the modulation order by 1/3. With 50% more pulses and nearly halved pulse positions of ∼50 ps, the modulation order of E-MPPM increased by only 0.5 compared with D-MPPM. Song et al. [34], [35] improved the modulation order to 7 by introducing a 4PAM–8PSK–4PPM hybrid modulation, achieving a data rate of 1.66 Gbps with 2-cm transcutaneous transmission range. Compared with a standalone modulation scheme, the adoption of hybrid modulation reduces the requirement of the signal-to-noise ratio (SNR) [35]. But the hybrid modulation in [34] and [35] requires an initiative reduction of the TX pulse amplitude due to the use of PAM, resulting in a reduction of the transmission range.

Considering the power consumption, the high-frequency carrier generation is usually power-hungry for the conventional upconversion architecture [33], [34], [35], [38], [39], [40]. Alternatively, IR-UWB transmitters can adopt an all-digital edge-combine technique to replace the high-frequency carrier and save power [32], [42], [43], [44], [45], [46]. The edge-combine architecture typically uses a delay line to generate the edges, and a digital combine logic to construct the edges into UWB pulses. However, the modulation order of the digital edge-combine transmitters is usually limited to 2–3 due to the lack of phase modulation [41], [42], [43]. In addition, the delay of the delay cells in the delay line varies with the process corners. Switched capacitors are widely used to calibrate the delay cells [32], [41], [42], [43], which is especially complicated as an extra high-speed oscilloscope is usually needed to quantify the ∼100-ps delay of each stage.

The third challenge is the small form-factor challenge. For an IR-UWB transmitter, there are usually three parts of external components that increase the volume of the system: the external matching network, the antenna, and the crystal oscillator. Prior UWB works have proposed matching-network-free [32], [41], [43] or ON-chip-matching [34], [35] transmitters and even ON-chip antenna [33], [47]. Notably, some of these works manage to achieve a data rate of ∼1 Gbps. However, the data rate of the existing crystal-less UWB transmitters is usually limited to ∼Mbps [48], [49], [50]. This limitation is primarily due to the need for precise timing in high-speed transmitters.

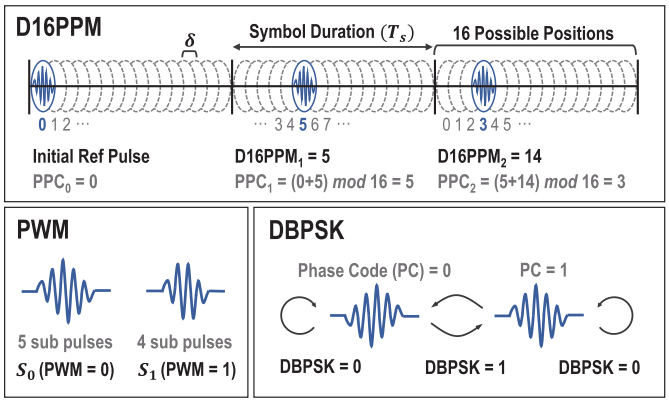

Fig. 1. Diagram of the D16PPM–PWM–DBPSK hybrid modulation scheme. A total modulation order of 6 is achieved.

This article proposed an IR-UWB transmitter for high-density neural implants, as a possible solution to previous challenges [36]. A hybrid modulation scheme combining the differential 16-pulse-position modulation (D16PPM), pulsewidth modulation (PWM), and differential bi-phase shift keying (DBPSK) is proposed to balance the data rate and transcutaneous data transmission. A total modulation order of 6 is achieved. This six-order modulation scheme is realized by an all-digital transmitter, with a ring oscillator (RO) providing all the edges to combine. The calibration of the RO frequency also calibrates all the delay cells, which is much easier than the switched capacitor method. The proposed modulation scheme and the transmitter are also optimized for crystal-less working scenarios. The transmitter features a data rate of 1.8 Gbps with a power consumption of only 4.09 mW. Thus, an energy efficiency of 2.3 pJ/bit is achieved. A transcutaneous transmission range of 20 cm is measured with 18-mm pork tissue applied.

The rest of this article is organized as follows. Section II introduces the proposed hybrid modulation scheme, including theoretical analysis among the SNR, symbol-error rate (SER), and the link budget, along with the impact of removing the crystal. The architecture of the transmitter and the detailed circuit implementation are introduced in Section III. Section IV explains the experimental results, including an ex vivo transcutaneous transmitting test, while Section V concludes the entire work.

II. Hybrid Modulation Scheme

A. D16PPM–PWM–DBPSK Modulation

The diagram of the proposed D16PPM–PWM–DBPSK hybrid modulation scheme is illustrated in Fig. 1. The D16PPM modulates the data as the pulse-position difference of adjacent pulses. There are 16 possible positions in every symbol. The pulse-position code (PPC) of one symbol can be expressed as

$$\mathrm{PPC}_i \equiv \mathrm{D16PPM}_i + \mathrm{PPC}_{i-1} \pmod{16}. \quad (1)$$

In addition, the PWM modulates the data into a varying number of sub sinusoidal pulses in the TX wave. In the proposed design, there are five and four sub sinusoidal pulses with the PWM code of 0 and 1, respectively, denoting the signal model as S_0 and S_1. DBPSK further modulates the data with a 0° or 180° phase shift of adjacent pulses for code 0 or 1, respectively. As shown in Fig. 1, the two optional phases for a UWB TX wave are denoted as phase code (PC) 0 or 1. The 180° phase shift of a signal can be expressed by multiplying a parameter $p_i \in \{-1, 1\}$. Thus, the TX signal can be expressed as

$$S(t) = \sum_{i=0}^{\infty} p_i \cdot S_{\mathrm{PWM}}(t - i \cdot T_s - \delta \cdot \mathrm{PPC}_i) \tag{2}$$

where T_s is the symbol duration. δ is the D16PPM time step.

D16PPM features a modulation order of 4. Together with PWM and DBPSK, the hybrid modulation scheme achieves a total modulation order of 6.

To decrease the symbol duration and to increase the PRF, the time step of the D16PPM pulse positions (δ) can be rendered shorter than the pulsewidth, as indicated in Fig. 1. In the proposed design, the time step of the D16PPM is half a sinusoidal period. Given that a pair of adjacent rising and falling edges in the edge-combine circuit corresponds exactly to half a sinusoidal period, this design allows the generation of pulses and the regulation of pulse positions to be performed by a single module. Compared with the previous two-step approach [41], [42], [43], which uses a stand-alone digital-to-time converter (DTC) to delay the trigger signal, followed with a stand-alone pulse generator to generate the pulses, a better efficiency can be expected for the proposed design. In addition, both the PWM and DBPSK in the hybrid modulation scheme are also suitable for digital edge-combine transmitters. This is because the pulsewidth variation in PWM equates to an integer multiple of sub-pulses. For DBPSK, a phase difference of 180° can be simply created with an inverter, or a bi-phase RO in this work.

In this work, the PRF is designed as 300 MHz, enabling a T_s of 3.33 ns. The data rate is specified at 1.8 Gbps. Every symbol duration is divided equally into 28 time slots, with each time slot corresponding to half a sinusoidal period. Thus, the time step of D16PPM (δ) is 119 ps. The time step of PWM is 238 ps. The carrier frequency of the TX signal is established at 4.2 GHz.

B. SNR and Link Budget Analysis

In assessing the viability of a new modulation scheme, a crucial step is to provide a theoretical analysis of the SNR and SER relationship, followed with a link budget analysis. This analysis is vital to determine whether this new approach is suitable for the intended working scenario, and to identify the requested performance of the circuits involved.

Fig. 2 illustrates the logical diagram of a pair of modulator and demodulator for SNR analysis. For the modulator, the clock source first generates the system clock. The DTC delays the clock according to the D16PPM codes and generates the trigger signal for the Pulse Gen (PG). The PG then produces

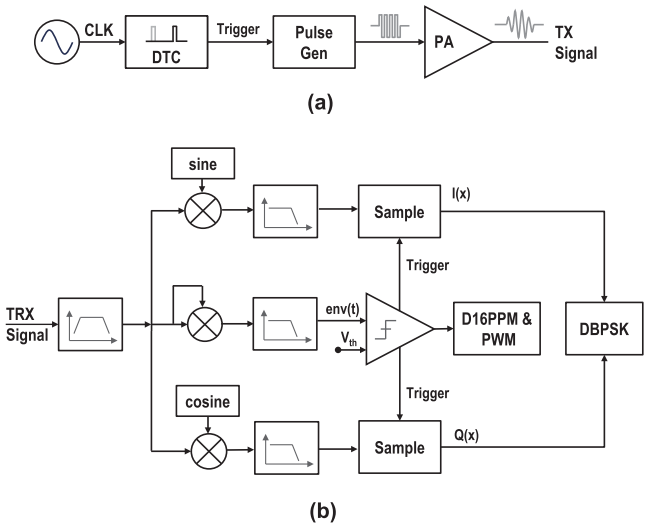

Fig. 2. (a) Logical diagram of a modulator for the proposed hybrid modulation scheme. (b) Diagram of a non-optimal demodulator for the D16PPM–PWM–DBPSK modulation scheme. The SNR analysis is based on the modulator and demodulator in this figure.

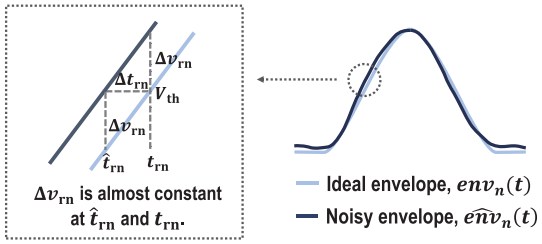

Fig. 3. Effect of the envelope noise on the trigger time of the ED, taking the rising edge as an example. The noise value (Δv_{rn}) is considered to be constant in a very short duration.

pulses, based on the DBPSK codes and PWM codes. Finally, the pulse amplifier (PA) completes the TX process by shaping and amplifying the pulses and generating the final TX signal.

For the demodulator, an optimal demodulator with the maximum likelihood strategy features the ideal best performance on the additive white Gaussian noise (AWGN) channel. However, for the proposed hybrid modulation scheme, the extremely high hardware complexity of the optimal demodulator makes it not a good solution for practical scenarios. Alternatively, non-coherent receivers with an asynchronous edge detector (ED) are widely adopted for PPM-based UWB systems [41], [42], [43]. Fig. 2(b) illustrates a suitable demodulator for the proposed modulation scheme. The non-coherent self-mixing branch extracts the signal envelope (env(t)) and detects the rising and falling edges of the envelope for D16PPM and PWM demodulation. The coherent I/Q branches are implemented for DBPSK demodulation. The sampling events of the coherent branches are triggered by the ED in the self-mixing branch. Thus, the phase of received signal can be synchronized in every symbol.

Although the relationship between the SNR and SER of the asynchronous edge-detecting systems has been widely discussed, the existing analyses primarily focus on situations with no overlap between adjacent pulse positions [51], [52], [53]. For the modulation scheme with an overlap, it is necessary to first derive the probability density function (pdf)

of the ED trigger time deviation. Fig. 3 illustrates the effect of the envelope noise (Δv_{rn}) to the ED trigger time, taking the rising edge as an example. The subscript n denotes the symbol index, and r denotes the rising edge. V_{th} is the threshold voltage of the ED. t_{rn} and $\hat{t}_{rn}$ are the ideal trigger time and the actual trigger time, respectively. Since the low-pass filter (LPF) in the non-coherent branch features a cut-frequency of ~1.6 GHz for the proposed modulation, with a typical time deviation (Δt_{rn}) of only tens of microseconds, the noise value (Δv_{rn}) can be considered to be constant at t_{rn} and $\hat{t}_{rn}$. In addition, the pdf of a squared signal with the original amplitude A and noise variance σ^2 can be expressed by the non-central chi-square distribution [52], [54] as

$$p_1(x, A, \sigma) = \frac{1}{2\sigma^2}\left(\frac{x}{A^2}\right)^{-\frac{1}{4}} \exp\left(-\frac{x + A^2}{2\sigma^2}\right) I_{-\frac{1}{2}}\left(\frac{A\sqrt{x}}{\sigma^2}\right) \tag{3}$$

where $I_n(x)$ is the modified Bessel function of the first kind with an order of n. Thus, the pdf of Δv_{rn} is

$$p_2(\Delta v_{rn}) = p_1(V_{\text{th}} + \Delta v_{rn}, \sqrt{V_{\text{th}}}, \sigma). \tag{4}$$

Since $\Delta v_{rn} = V_{\text{th}} - \text{env}_n(\hat{t}_{rn})$, the pdf of $\hat{t}_{rn}$ is given as

$$p_3(\hat{t}_{rn}) = p_2(V_{\text{th}} - \text{env}_n(\hat{t}_{rn})) \cdot \left|\frac{\mathrm{d}\hat{t}_{rn}}{\mathrm{d}\Delta v_{rn}}\right|. \tag{5}$$

Thus, the pdf of Δt_{rn} is

$$p_4(\Delta t_{rn}) = p_3(\Delta t_{rn} + t_{rn}). \tag{6}$$

The above derivation only considered the thermal noise at the input of the receiver, while for the transmitter, the timing noise of the equivalent DTC affects the TX signal quality the most. If the variance of the DTC timing jitter is σ_t^2, the final expression of the pdf of Δt_{rn} is

$$p_n(\Delta t_{rn}) = \int_{-\infty}^{\infty} p_4(\Delta t_{rn} - x) \cdot p_t(x, \sigma_t^2)\mathrm{d}x \tag{7}$$

where $p_t(x, \sigma_t^2)$ is the pdf of the Gaussian distribution with 0 mean and σ_t^2 variance. The expression of the pdf of the falling edge trigger time deviation (Δt_{fn}) is the same as (7).

For any Δt_{rn} value in symbol n, D16PPM is demodulated correctly only if the rising edge trigger time deviation of symbol $n-1$ meets the following condition:

$$\left|\Delta t_{rn} - \Delta t_{r(n-1)}\right| < 0.5 \cdot \delta \tag{8}$$

where δ is the time step of D16PPM in (2).

For DBPSK, the possibility of demodulating a DBPSK code correctly is

$$P_{\text{DBPSK}}(\psi_1 < \psi < \psi_2 \mid \Delta\theta_n) = F_{\Delta\theta_n}(\psi_2) - F_{\Delta\theta_n}(\psi_1) + 1 \tag{9}$$

where $\Delta\theta_n$ is the input phase shift of adjacent UWB pulses. ψ is the demodulated phase shift. ψ_1 and ψ_2 are the boundaries

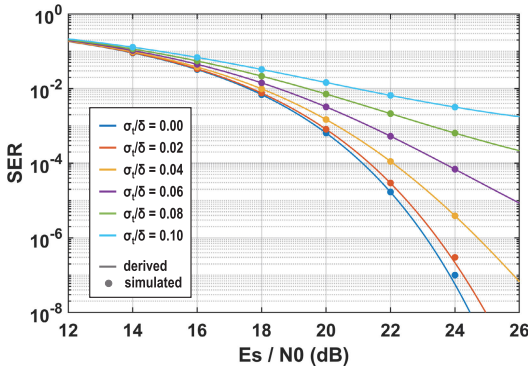

Fig. 4. Derived and simulated SER versus E_S/N_0 curves of the proposed hybrid modulation scheme with the demodulator in Fig. 2. σ_t/δ is the standard deviation of the DTC jitter in comparison to the D16PPM time step.

for code decisions. $F_{\Delta\theta_n}(\varphi)$ can be expressed as

$$F_{\Delta\theta_n}(\varphi) = \frac{\sin(\Delta\theta_n - \varphi)}{4\pi} \times \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{\exp\left\{-\frac{E_s}{N_0}[1 - \cos(\Delta\theta_n - \varphi) \cdot \cos t]\right\}}{1 - \cos(\Delta\theta_n - \varphi) \cdot \cos t}\mathrm{d}t. \tag{10}$$

Ideally, when the DBPSK code is 0, $\Delta\theta_n$ is 0. When the DBPSK code is 1, $\Delta\theta_n$ is π. However, for the proposed modulation scheme, the synchronization of an adjacent I/Q data is realized by the ED in the non-coherent branch. Thus, Δt_{tn} and $\Delta t_{t(n-1)}$ introduce a synchronization error to $\Delta\theta_n$

$$\Delta\hat{\theta}_n = \Delta\theta_n + \frac{\Delta t_{rn} - \Delta t_{r(n-1)}}{\delta} \cdot \pi. \tag{11}$$

As a result, for any Δt_{rn}, the possibility of a correct D16PPM and DBPSK demodulation is

$$P_1(\Delta t_{rn}) = \int_{-\frac{\delta}{2}+\Delta t_{rn}}^{\frac{\delta}{2}+\Delta t_{rn}} P_{\text{DBPSK}}(-\pi/2 < \psi < \pi/2 \mid \Delta\hat{\theta}_n) \cdot p_n(\Delta t_{r(n-1)}) \cdot \mathrm{d}\Delta t_{r(n-1)}. \tag{12}$$

Similar to D16PPM, the possibility of a correct PWM demodulation with any Δt_{rn} is

$$P_2(\Delta t_{rn}) = 0.5 \cdot (P_{\text{PWM=0}} + P_{\text{PWM=1}}) = 0.5 \cdot \left[\int_{\Delta t_{fn} < \delta + \Delta t_{rn}} p_n(\Delta t_{fn}) \cdot \mathrm{d}\Delta t_{fn} + \int_{\Delta t_{fn} > -\delta + \Delta t_{rn}} p_n(\Delta t_{fn}) \cdot \mathrm{d}\Delta t_{fn}\right]. \tag{13}$$

The final expression of the SER is given as

$$\text{SER} = 1 - \int P_1(\Delta t_{rn}) \cdot P_2(\Delta t_{rn}) \cdot p_n(\Delta t_{rn}) \cdot \mathrm{d}\Delta t_{rn}. \tag{14}$$

Fig. 4 illustrates the derived SER versus E_S/N_0 curves, as well as several simulated results, with different DTC jitter values (σ_t) in comparison to the D16PPM time step (δ). Although some approximations are used during the above derivation process, the derived results are consistent well with the simulation results.

For a time step of 119 ps, a DTC jitter of 0.06 least significant bit (LSB) (7.14 ps) is reasonable to achieve. Thus,

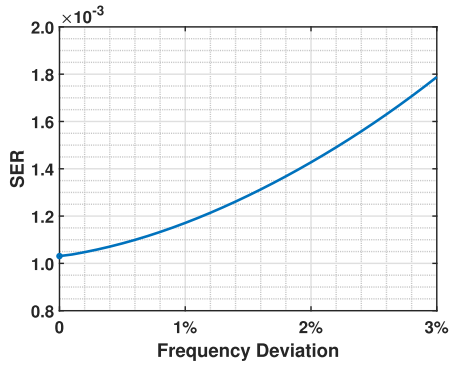

Fig. 5. Impact of the frequency deviation to the SER. This result is derived with an SNR of 21.3 dB and a DTC jitter of 7.14 ps.

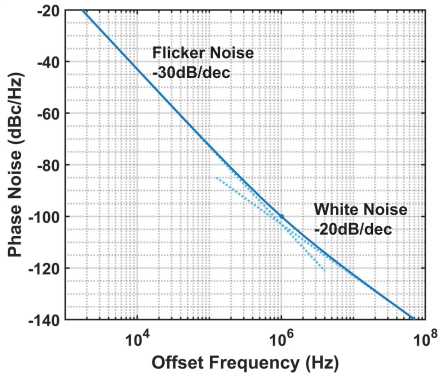

Fig. 6. Ideal DSB phase noise spectrum of a free-running 300-MHz CMOS oscillator. The corner frequency of this spectrum is set at 1 MHz, where the phase noise is −100 dBc/Hz.

the required SNR for an SER of 10^{-3} is 21.3 dB. The link budget can be calculated as

$$\frac{E_S}{N_0} + \mathrm{NF} + N + \mathrm{IL} = P_{\mathrm{TX}} + G_i - \mathrm{PL} - \mathrm{LM} \tag{15}$$

where NF is the noise figure of the RX. N is the noise power in the targeting bandwidth. IL is the implementation loss. P_{TX} is the TX power. G_i is the antenna gain. PL is the path loss. LM is the link margin. For a targeting bandwidth of ∼1.5 GHz, the noise power N is −82.2 dBm. The TX power of a triangular-shaped UWB signal with the proposed modulation is −11.9 dBm, if it adheres to the −41.3-dBm/MHz spectrum mask. Assuming NF, IL, and G_i are 5 dB, 3 dB, and 7 dBi respectively, the sum of PL and LM is 48 dB. In addition, according to the measurement results in this work and in literature [55], we can estimate a path loss of roughly 40 dB, for a 4.2-GHz UWB signal transmitting through the skull and over a distance of several centimeters. Therefore, it can be concluded that the proposed hybrid modulation scheme is suitable for the targeting high-density neural implants.

C. Impact of Removing the Crystal

According to the above analysis, the performance of the equivalent DTC in the transmitter is crucial for the hybrid modulation scheme. This work aims to implement a crystal-less transmitter to reduce the system volume. The absence of the crystal oscillator and the associated phase-locked loop (PLL) may result in two consequences: frequency deviation of the system clock and degradation of the timing noise.

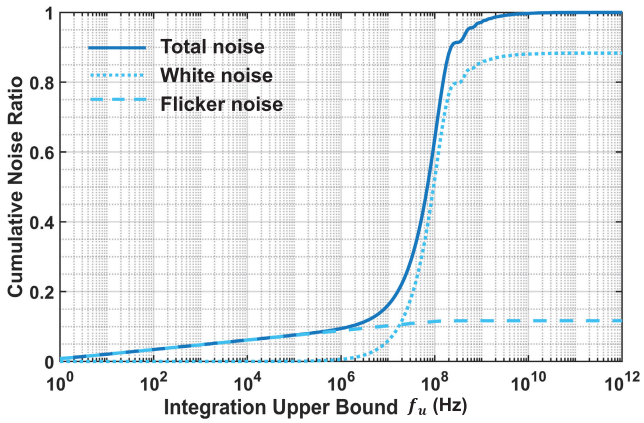

Fig. 7. Cumulative noise ratio $r_n(f_u)$ of the free-running oscillator, with the individual contribution of white noise and flicker noise presented.

The influence of the frequency deviation can be quantified by incorporating this factor to the theoretical analysis discussed in Section II-B. In our implementation, the deviation of the D16PPM time step, the PWM time step, and the carrier frequency correspond directly to the deviation of the oscillator's frequency. Taking these factors into account, the curve for the relationship between the frequency deviation and SER is shown in Fig. 5. This analysis assumes a crystal-less transmitter paired with a receiver with accurate frequency. And the results are based on an SNR of 21.3 dB and a DTC jitter of 7.14 ps. According to Fig. 5, a frequency deviation of 1 MHz, corresponding to 0.3% of the 300-MHz target frequency, results in a 2.7% increase in the SER. This slight increase can be considered bearable. In addition, the simulation results indicate that a calibrated 300-MHz RO may feature a frequency drift of 0.5 MHz/mV, or 1‰/°C. Nevertheless, the supply voltage drift can be compensated by common technologies, including voltage regulators or controlled current sources. Regarding the temperature drift, the internal temperature of the targeting implanted area is relatively stable. It is not likely for a temperature drift of >3 °C. Thus, the frequency deviation of the crystal-less system is acceptable.

As for the timing noise, a free-running oscillator may suffer from a root mean square (rms) jitter of up to tens of picoseconds. However, the proposed modulation scheme primarily uses the position or phase difference of adjacent UWB pulses to encode data. Crucially, it is the timing noise accumulated within a few symbol periods that really degrades the quality of the TX signal. In the following, a theoretical and quantified analysis will be given, based on the logical modulator depicted in Fig. 2(a).

In every TX cycle, the DTC in Fig. 2(a) is triggered by the system clock from the oscillator. Thus, the initial timing noise that actually affects the difference of adjacent pulse positions is the period jitter of the free-running oscillator, which can be quantified as the standard deviation of the oscillation period. And the period jitter can be calculated from the self-referenced phase noise variance accumulated within a symbol period

$$\sigma_{T_s} = \frac{\sqrt{\sigma^2_{\phi\mathrm{osc}}(T_s)}}{2\pi f_c} \tag{16}$$

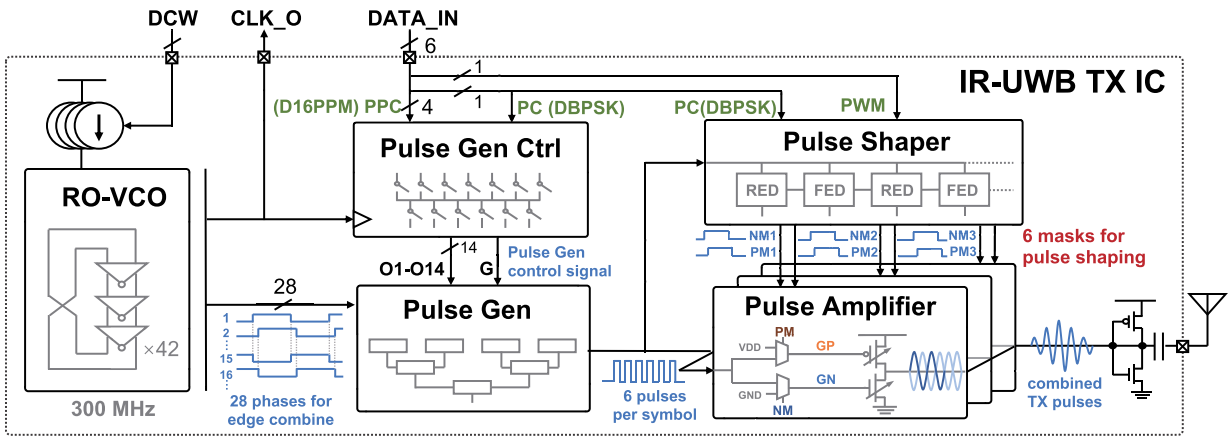

Fig. 8. Diagram of the proposed transmitter for the D16PPM–PWM–DBPSK hybrid modulation scheme.

where σ_{T_s} is the period jitter, $\sigma^2_{\phi\text{osc}}(T)$ is the self-referenced phase noise variance accumulated within time T, and f_c is the oscillation frequency. The phase noise primarily comes from two noise sources: the white noise, which is characterized by its uniform spectral distribution, and the flicker noise, which mainly dominates in the low frequency band. The relationship between the phase noise variance and the noise sources can be expressed as follows [56]:

$$\sigma^2_{\phi\text{osc}}(T_s) = 2 \cdot \int_0^{\infty} \frac{\sin^2(\pi f T)}{\pi^2 f^2} S_n(f)\, df \tag{17}$$

where $S_n(f)$ is the PSD of the stationary noise sources, including the white noise and the flicker noise.

As a specific calculation, we can consider the double-sideband (DSB) phase noise spectrum of a free-running 300-MHz CMOS oscillator shown in Fig. 6. Assume the corner frequency where the white noise and the flicker noise contribute equally is 1 MHz. And let the DSB phase noise at 1 MHz offset is −100 dBc/Hz. Then the calculated period jitter of this free-running oscillator is 2.04 ps. Considering the 7.14-ps jitter limit which was introduced in the previous section, the remaining jitter budget for the DTC is

$$\begin{aligned}\sigma_{(\text{budget})} &= \sqrt{\frac{\sigma^2_{(2\ \text{DTC convertion})} - \sigma^2_{(\text{trigger})}}{2}} \\ &= \sqrt{\frac{2 \times \sigma^2_{(\text{DTC limit})} - \sigma^2_{T_s}}{2}} \\ &= \sqrt{\frac{2 \times 7.14^2 - 2.04^2}{2}} = 6.99\ \text{ps}. \end{aligned} \tag{18}$$

Thus, there is enough budget for the transmitter to achieve the targeting timing performance, even if the oscillator is running free.

In addition, the impact of phase noise with different offset frequencies on the period jitter can also be quantified. First, the cumulative noise ratio, denoted as $r_n(f_u)$, can be defined as follows:

$$r_n(f_u) = \frac{2 \cdot \int_0^{f_u} \frac{\sin^2(\pi f T_s)}{\pi^2 f^2} S_n(f)\, \mathrm{d}f}{\sigma^2_{\phi\text{osc}}(T_s)} \tag{19}$$

where $r_n(f_u)$ denotes the proportion of the phase noise accumulated from zero offset frequency to f_u, in relation to the total phase noise for the period jitter. For the free-running oscillator depicted in Fig. 6, the calculated $r_n(f_u)$ is illustrated in Fig. 7. This figure also highlights the individual contributions of the white noise and flicker noise. As observed from Fig. 7, it is evident that the predominant contributor to the period jitter is the white noise in the frequency range exceeding 1 MHz. Notably, in the frequency band above 100 MHz, the remaining noise still accounts for nearly 40% of the total. Therefore, if a crystal oscillator is implemented, it would necessitate designing a PLL with a bandwidth close to the oscillation frequency, which is challenging, while giving a limited benefit in return.

In conclusion, while the performance of the DTC in the transmitter is critical for the proposed modulation scheme, it is still feasible to eliminate the crystal oscillator. The proposed modulation scheme offers the potential to reduce the system's volume without compromising the needed timing performance.

III. Circuits Implementation

A. Transmitter Architecture and Timing Diagram

The diagram of the proposed digital edge-combine transmitter is shown in Fig. 8. In contrast to the open-loop delay lines commonly adopted in prior work, this study proposes a 42-stage bi-phase RO in the transmitter to generate the edges for combination. The oscillation frequency of the RO is regulated and calibrated by a current digital-to-analog converter (DAC). This current DAC uses a design with folded cascode mirrors and source degeneration resistors to minimize the impact of the noise. Calibrating the RO frequency also directly calibrates the delay cells within the RO, presenting a simpler approach compared with the switched capacitor method typically used for open-loop delay lines.

The RO generates a total of 84 phases. One in every three phases is routed out for edge-combine. In every TX cycle, the PG combines the 28 phases from the RO into six pulses. The position of the six pulses is determined by the Pulse Gen Ctrl (PGC) according to the 4-bit PPC code and the 1-bit PC code. The six output pulses from the PG are fed into three PAs. Each PA consists of an nMOS switch array and a pMOS switch array that are controlled by their gate voltages, GN and GP, respectively. When one of the MOS

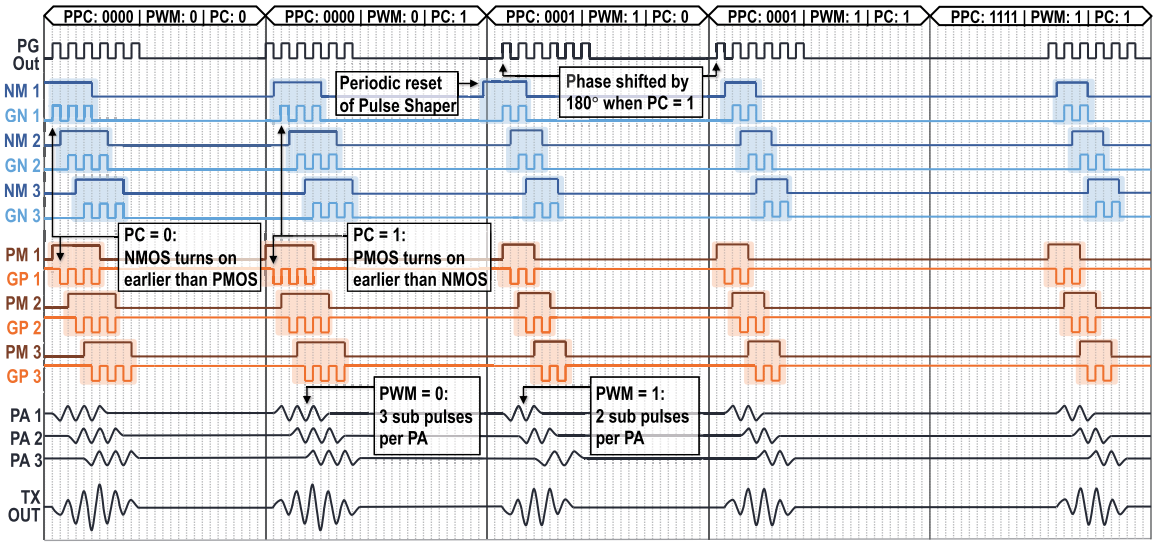

Fig. 9. Timing diagram of the transmitter. The hybrid modulation scheme is realized by the PG, PS, and PAs efficiently.

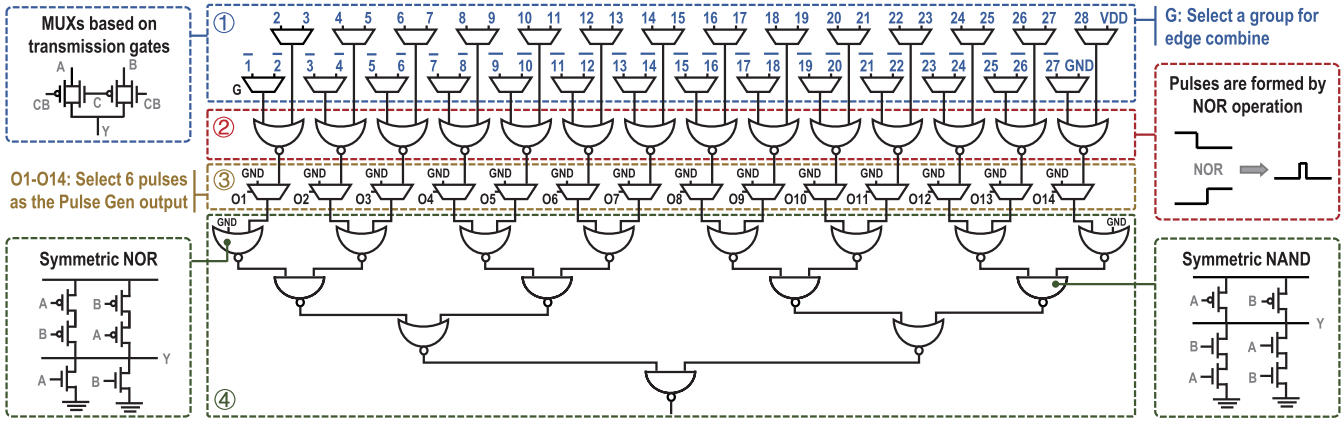

Fig. 10. Diagram of the PG module. The PG is highly symmetrical to realize a precise timing control during the edge combination.

switches is turned on, it pulls up or pulls down the dc voltage at the output to form the TX wave. The driven strength of the switch arrays is also configurable to fine-tune the envelope of the TX pulses. A pair of masks, PM and NM, are used to control which portion of the six pulses from PG reach the gate of the MOS switches. PM and NM are generated from the pulse shaper (PS) according to the six pulses from PG, the PC, and the PWM code. Fig. 9 illustrates the detailed timing diagram. Within the PG, the PC introduces a 180° phase shift of the six output pulses. Subsequently, the PS detects every rising and falling edge of the six pulses to generate the mask signals, PM1-3 and NM1-3, for the three PAs, respectively. The number of the pulses in the mask is decided by the PWM code. The PC determines the sequence of NM and PM, which controls the activation order of the MOS and nMOS in turn. As a result, the three PAs are successively activated, each generating two or three sub pulses with different phases in a single TX cycle. Ultimately, the sum of the three PA outputs is the modulated TX wave.

B. Pulse Gen and Pulse Gen Ctrl

The PG combines the 28 phases into six pulses in every TX cycle. The detailed diagram of the PG is illustrated in Fig. 10. There are four layers of logic gates. In the first

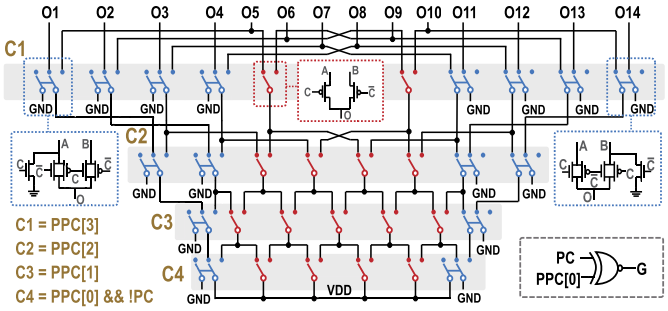

Fig. 11. Diagram of the PGC. An XNOR gate is used to generate the control signal G. The four-layer selection circuit generates the control signals O1–O14.

layer, 28 MUXs select a combination of the 28 RO phases from two options according to the PC and the PPC. This selection mechanism enables the 180° phase shift of the PG output upon changes in the PC, as indicated in Fig. 9. The second layer generates 14 individual pulses with the input RO phases. Typically, XOR gates are widely used to combine two edges into one single pulse. However, conventional XOR gates, comprising multiple NAND gates, suffer from imprecise timing control, since the input-to-output delays across different inputs are usually unequal. The proposed PG generates a pulse by performing NOR operation on a phase and its adjacent

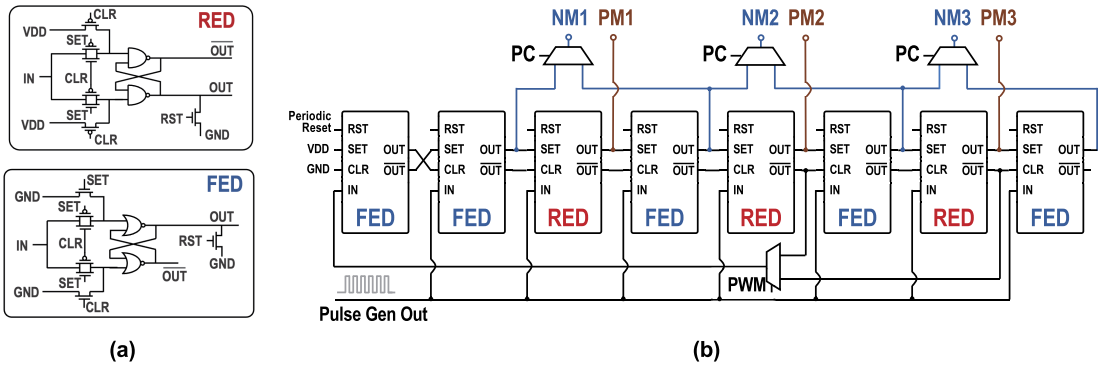

Fig. 12. Design of the PS. (a) FED and the RED. (b) Diagram of the PS with an edge-detector chain of FEDs and REDs.

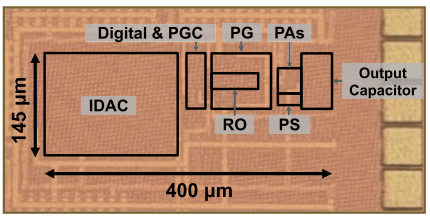

Fig. 13. Microphoto of the chip die.

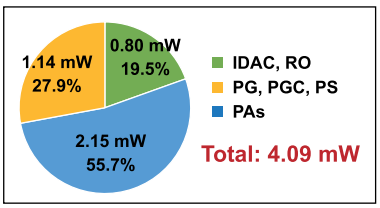

Fig. 14. Measured performance of the free-running RO. (a) DSB phase noise. (b) Timing jitter.

anti-phase. No additional inverter is needed, since the anti-phases of the 28 phases are naturally within the 28 phases. For the third layer, 14 MUXs select six consecutive pulses from the 14 outputs of the second layer, according to the PPC and the PC. The fourth layer combines the six selected pulses using symmetric NOR gates and NAND gates to improve the symmetry of the input-to-output delay across different pathways.

As discussed in Section II-B, the performance of the equivalent DTC in the transmitter is pivotal to the overall system performance. In the proposed transmitter, this equivalent DTC is primarily realized by the PG. To mitigate the non-linearity of the PG, transmission-gate-based MUXs are used in layer 1 and layer 3 to minimize the mismatch, offering an advantage over the traditional inverter-based MUXs. Furthermore, all the logic gates in the PG use transistors that are several times larger than those typical used in standard digital circuits. According to the post-simulation results generated by the Monte Carlo process, the LSB standard deviation of the equivalent DTC due to the local mismatch is only 3.6 ps.

Fig. 11 depicts the architecture of the PGC, which is responsible for generating all the MUX control signals in the PG. An XNOR gate is used to generate the control signal G for the 28 MUXs in the first layer in PG. A four-layer selection circuit with two types of selection cells is designed to generate O1–O14 for the 14 MUXs in the third layer in PG. Separated control signals C1–C4 are applied to each layer. With all the MUXs in the PG as the working load, the PGC consumes a total power of 42 uW, with an input-to-output delay of only 120 ps.

C. Pulse Shaper

The PS detects every rising and falling edge of the six pulses from PG and generates the PM1-3 and NM1-3 mask signals for the PAs. To realize this function, an SR NOR latch-based falling ED (FED) and an SR NAND latch-based rising ED (RED) are designed, respectively, as shown in Fig. 12(a). The behaviors of the FED and RED are controlled by the CLR signal and the SET signal. When CLR is 1 and SET is 0, the outputs flip to 0 at targeting edges. When CLR is 0 and SET is 1, the outputs flip to 1 at targeting edges.

The PS consists of an edge-detector chain incorporating the proposed FEDs and REDs. In every transmit cycle, the former EDs enable the subsequent ED. The outputs of all the EDs first change to 1 with targeting edges. A return path enables the second detection round, causing the outputs to revert to 0 with targeting edges. The masks are generated at the outputs of the EDs. An MUX controlled by the PWM code is used to decide which rising edge detection is fed back to the first ED. This control mechanism adjusts the duration of the PM and NM signals, thereby realizing the PWM control. In addition, three MUXs, under the control of the PC, decide the order of NM and PM, enabling the DBPSK modulation.

IV. Experimental Results

The proposed IR-UWB transmitter was fabricated in 40-nm CMOS technology, occupying a silicon area of 0.058 mm^2. A microphotograph of the die is shown in Fig. 13.

The measured performance of the free-running RO is illustrated in Fig. 14. According to the DSB phase noise spectrum in Fig. 14(a), the RO has a corner frequency of about 1.25 MHz, where the phase noise is −104 dBc/Hz. Thus, the calculated period jitter by (16) and (17) is 1.64 ps. This result matches the directly measured period jitter of 1.71 ps in Fig. 14(b). Regarding the power supply rejection, the measurement results show that a 20-mV drift in the supply voltage of the current DAC results in a 0.12-MHz frequency drift of the RO. This translates to a mere 1.33-ps deviation in the oscillation period. As a result, the precision afforded by

TABLE I
COMPARISON WITH RELATED WORKS

	This Work	ISSCC 22 [34]	JSSC 22 [42]	JSSC 19 [43]	TCAS I 18 [37]	JSSC 16 [38]
Process	**40 nm**	28 nm	65 nm	65 nm	130 nm	65 nm
Frequency Band	**3.1-5 GHz**	6-9 GHz	3.5-6 GHz	3.1-5 GHz	3.5-4.5 GHz	3.1-10.6 GHz
Architecture	**Edge Combine**	Up-Conversion	Edge Combine	Edge Combine	Edge Combine	Up-Conversion
Modulation	**D16PPM + PWM + DBPSK**	4PPM + 8PSK + 4PAM	E-MPPM	D-MPPM	OOK	BPSK
Modulation Order	**6-bit**	7-bit	3-bit	2.5-bit	2-bit	1-bit
Crystal-less TX	**Yes**	No	No	No	No	No
Data Rate	**1.80 Gbps**	1.66 Gbps	1.125 Gbps	0.5 Gbps	1 Gbps	1 Gbps
TX Power Consumption	**4.09 mW**	9.69 mW	9.2 mW	7 mW	5 mW	21.4 mW
TX Energy Efficiency	**2.3 pJ/bit**	5.8 pJ/bit	8.2 pJ/bit	14 pJ/bit	5 pJ/bit	21.4 pJ/bit
Area	**0.058 mm^2**	0.155 mm^2	-	0.27 mm^2 *	0.04 mm^2	1.1 mm^2 *
Max Output Amp.	**140 mV**	120 mV	200 mV	200 mV	50 mV	80 mV
Tissue Type	**18 mm skin/fat**	15 mm skin/fat	No Tissue	No Tissue	-	No Tissue
TX Antenna Gain	**2.6 dBi**	-8.5 dBi **	3 dBi	3 dBi	-	1.5 dBi
RX Antenna Gain	**3.5 dBi**	5 dBi	3 dBi	3 dBi	-	1.5 dBi
Transmission Range	**15 cm (10^{-4} BER) 20 cm (10^{-3} BER)**	2 cm @ 1.66 Gbps (10^{-4} BER) 15 cm @ 1.43 Gbps (10^{-4} BER) ***	2 m (10^{-3} BER)	1 m (10^{-3} BER)	-	1 m (10^{-3} BER)

* Estimated from the chip die photo.
** Attenuation of a human head model included.
*** 4PAM decreased to 2PAM to ensure the transmission range.

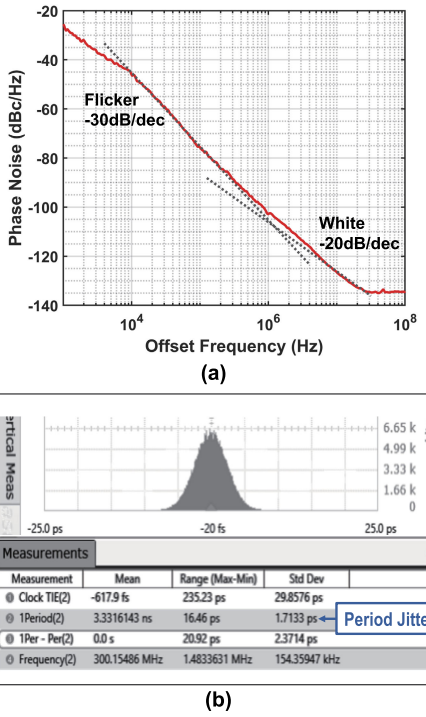

Fig. 15. Measured TX output waveform with different modulation codes.

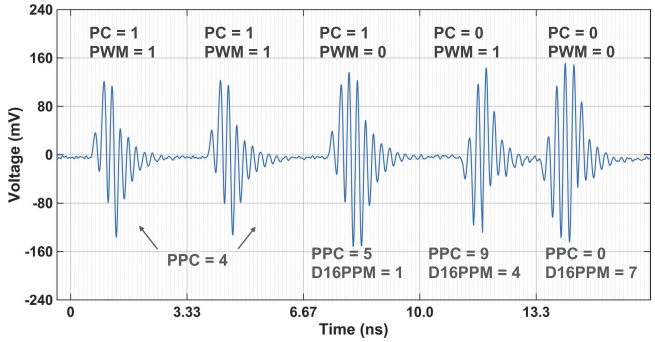

Fig. 16. Measured TX power spectrum.

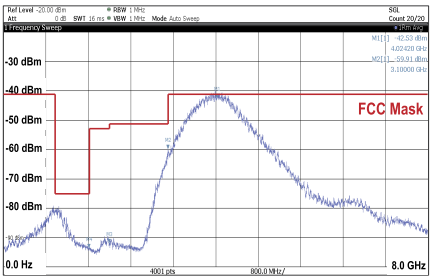

Fig. 17. Power consumption break-down.

the free-running RO is sufficient for the timing requirements of the proposed hybrid modulation scheme.

The TX output waveform, measured by a high-speed oscilloscope, is shown in Fig. 15. The TX pulses with different PPC, PC, and PWM codes are also illustrated. The measured TX power is approximately −12.4 dBm. The TX power spectrum also satisfies the FCC UWB mask (Fig. 16).

The power consumption break-down is illustrated in Fig. 17. The current DAC and the RO consume 0.8 mW. The PAs consume 2.15 mW. The pulse generator and other logic consume 1.14 mW. As a result, the 1.8-Gbps transmitter consumes a total power of only 4.09 mW, realizing an energy efficiency of 2.3 pJ/bit.

To quantify the modulation performance of the transmitter, a demodulation algorithm based on the demodulator in Fig. 2(b) is implemented to the measured TX transient signal. The performance of the equivalent DTC for D16PPM is presented in Fig. 18. The equivalent DTC achieved a maximum differential non-linearity (DNL) of 11.7 ps and a maximum integral non-linearity (INL) of 15.5 ps. For the timing noise, the measured jitter of the DTC is only 5.59 ps, which satisfies the design requirements in Section II-B.

The performance of PWM and DBPSK is illustrated in Fig. 19. For PWM, the standard deviation of the pulsewidth is approximately 10 ps. For DBPSK, ΔIQ, which is the difference of adjacent IQ values, is plotted in the constellation diagram. Since there is a frequency offset of the free-running RO, the ΔIQ points form several full circles on the constellation diagram. There are three circles on the outside. This is due to the cross modulation from the combination of adjacent PWM codes. Nevertheless, the distinction of the ΔIQ points from different DBPSK codes is quite clear. The DBPSK

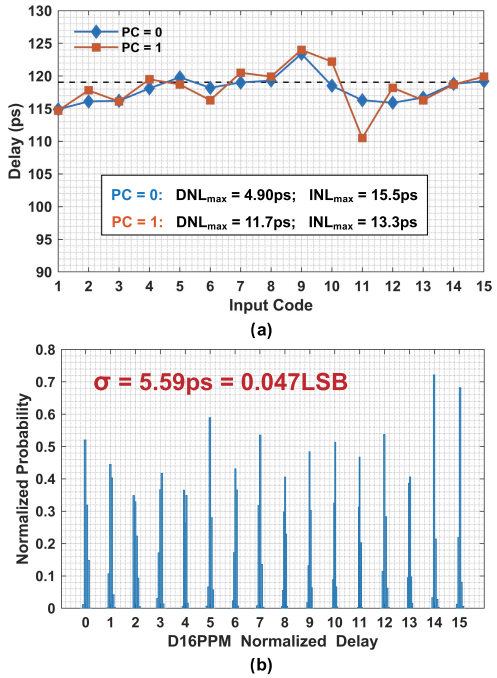

Fig. 18. Measured equivalent DTC performance. (a) Measured linearity results. (b) Output histogram of the DTC with different input codes.

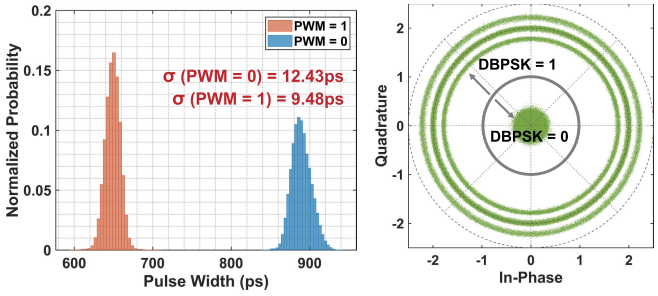

Fig. 19. Measured pulsewidth histogram and DBPSK ΔIQ constellation diagram.

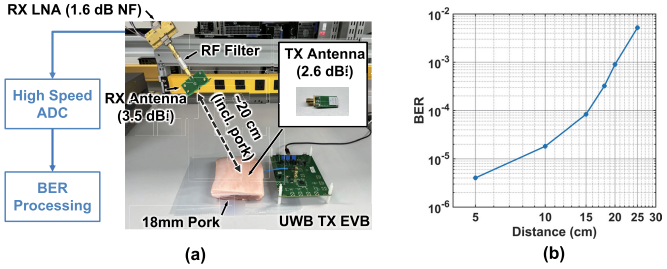

Fig. 20. Ex vivo TRX test. (a) Experimental setup. (b) Measured BER versus distance curve.

code can be given by judging whether the ΔIQ point is located in the circle of radius 1. For the error-vector magnitude (EVM) calculation, one approach is to designate the reference position to the origin point for ΔIQ points with DBPSK = 0. For DBPSK = 1, the reference position is designated to the circle where the delta IQ points would be if there is no frequency deviation. Thus, the calculated EVM is −21.2 dB.

To test the transcutaneous transmission, an ex vivo TRX test was implemented with 18-mm pork tissue applied, as shown in Fig. 20. A small-size 2.6-dBi antenna (NN01-107 from Ignion) was used as the TX antenna. The discrete RX system consisted of a 3.5-dBi antenna, an RF filter (VHF-2700+ from Mini Circuits), a 1.6-dB-NF LNA (QPM1000 from Qorvo), and a high-speed oscilloscope (DSAZ594A from Keysight) operated as an ADC. The received data were decoded by the demodulator shown in Fig. 2. The measured bit error rate (BER) versus the transmission distance is plotted in Fig. 20(b). At a distance of 20 cm, the measured total path loss is about 45 dB, where the BER is approximately 10^{-3}. Consequently, the proposed transmitter is able to give a steady transcutaneous transmission for the targeted high-density neural implants.

Table I shows comparison of the proposed UWB transmitter with related low-power and short-range UWB transmitters in prior arts. A data rate of 1.8 Gbps with a power efficiency of 2.3 pJ/bit is achieved by the proposed transmitter, resulting in highest data rate, lowest power consumption, and best efficiency among the works listed in the table.

V. Conclusion

This article proposed a hybrid modulation scheme combining D16PPM, PWM, and DBPSK to balance the data rate and enable the transcutaneous data transmission for the high-density neural implants. The hybrid modulation scheme achieves a total modulation order of 6. A detailed theoretical analysis on the SNR and SER relationship, as well as the timing noise that affects the modulation, is illustrated in this article. This modulation scheme is realized by a crystal-less all-digital transmitter. An RO provides the phases for edge combine, as a simpler way to calibrate the delay cells, compared with the switched capacitors in conventional open-loop delay lines. The transmitter features a pulse generator to precisely combine the edges and a PS with an ED chain, achieving high efficiency. The transmitter achieves a data rate of 1.8 Gbps with a power consumption of only 4.09 mW. Thus, a power efficiency of 2.3 pJ/bit is achieved. In the ex vivo test, a transcutaneous transmission range of 20 cm was measured with 18-mm pork tissue applied. Consequently, the proposed UWB transmitter proves its high potential for the high-density neural implants.

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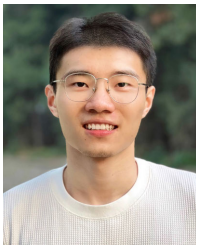

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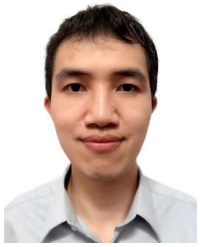

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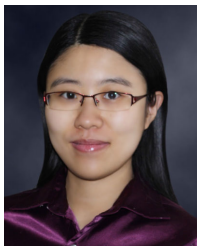

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