Concurrent Body-Coupled Powering and Communication ICs With a Single Electrode

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***Abstract*— Body-coupled powering (BCP) and body-coupled communication (BCC) utilize the human body channel as the wireless transmission medium, which shows less path loss around the body area. However, integrating both BCP and BCC requires multiple electrodes or alternating the uplink and downlink in the time domain, due to signal interferences and backflow between different paths. To address this issue, we propose a base station (BS) IC and a sensor node (SN) IC with BCP and BCC concurrency. At the BS, the adaptive self-interference cancellation (SI-C) structure suppresses the output signals that are coupled at the data receiver, enabling the concurrent uplink data recovery and downlink power delivery. At the SN, the ground domain of the uplink data path is separated from that of the downlink power/data path to suppress leakage between the paths. For regulated power supply in different ground domains, the cross-ground-domain power converter is designed with 89.1% efficiency. The ICs are implemented in a 40-nm 1P8M standard CMOS process, and BCC + BCP concurrent operations are successfully validated.**

***Index Terms*— Body-coupled communication (BCC), body-coupled powering (BCP), power–data co-transfer, power–data concurrency, wireless body-area network (BAN).**

I. Introduction

BODY-AREA network (BAN) empowers the cooperated sensing, recognition, and stimulation of bio-signals distributed around the body area [1]. However, on the one hand, the increasing need for downlink (e.g., for remote control and coordination) and uplink communication (e.g., for multi-site sensing) incurs additional power overhead. On the other hand, the need for miniaturized form factor (e.g., for user comfort) further limits the on-chip energy, demanding wireless power delivery to prolong the battery lifetime. Therefore, to achieve the sustainable operation of the miniaturized BAN nodes distributed around the body, enabling the simultaneous wireless powering and communication is crucial (Fig. 1).

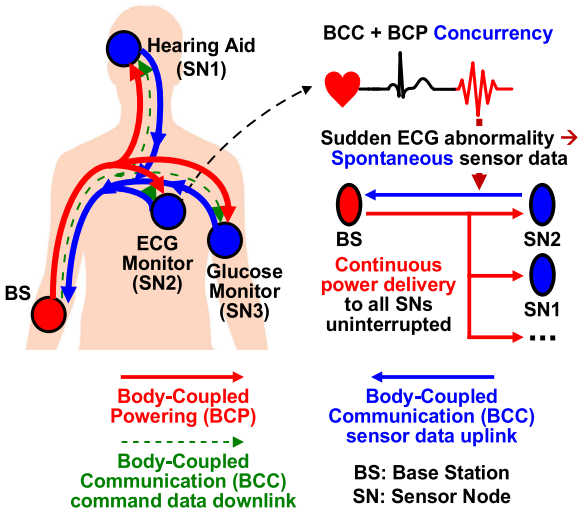

Fig. 1. Motivation for concurrent BCP and BCC.

While the RF-based transmission is a popular wireless solution over the air, it suffers from antenna pattern distortion and the body shadowing effect under non-line-of-sight conditions near the body area [2]. In contrast, by using the body as a forward transmission path and the parasitic capacitance as the return path, the capacitive body-coupled approach is shown to have an advantageous on-body path loss while being insusceptible to the body shadowing effect [3], [4], [5], [6], [7]. In spite of channel variations when coupling condition changes, by leveraging on the advantageous body path loss, the body-coupled communication (BCC) could enable lower energy per bit [8], [9], [10], [11], [12], [13], whereas the body-coupled powering (BCP) could enable higher power efficiency and wider body area power coverage [14], [15], [16], [17], [18], [19].

To achieve a wireless BAN node with power sustainability, the integration of BCP and BCC has been studied, as illustrated in Fig. 2. In [16], [20], and [21], the BCP downlink, BCC downlink, and BCC uplink are incorporated at the base station (BS) and sensor node (SN), but these three paths are enabled in a time-domain multiplexing (TDM) fashion as they share the body channel. Switches dedicated to the path selection are required, where the synchronization

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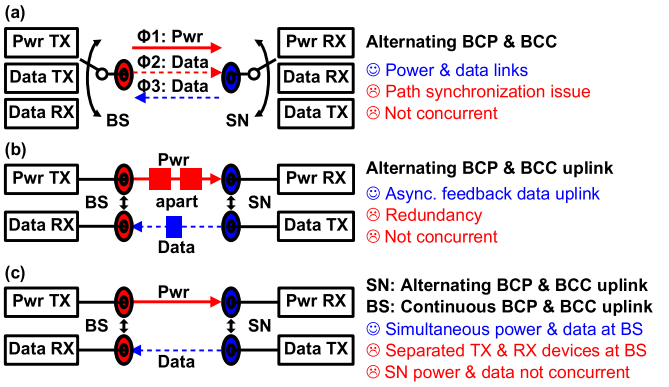


Fig. 2. Conventional BCP and BCC integration. (a) BCP and BCC uplink/downlink alternated. (b) BCP and BCC uplink alternated. (c) BCP and BCC uplink alternated at SN, with continuous BCP and BCC at BS.

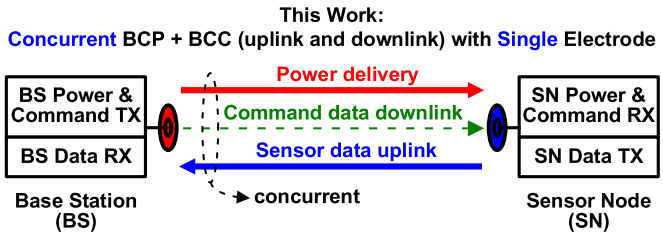
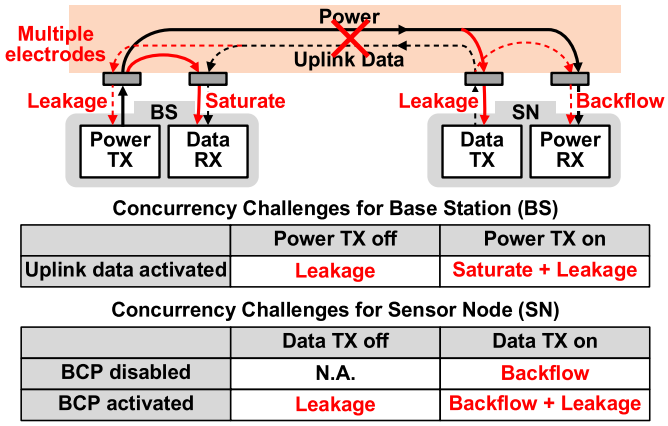


Fig. 3. Proposed system achieving the BCP and BCC (uplink and downlink) concurrency via a single electrode at both BS and SN.

and switch control remain a challenge. In [22], TDM-based power downlink and data uplink are implemented, where path selection switches are avoided by introducing an electrode at the body interface of each path. To alleviate the need for synchronization between paths, the asynchronous data feedback mechanism that relies on the repetitive transmission of a data packet is proposed, causing redundancy and low data rate. The above TDM-based alternation of BCP and BCC paths poses a trade off between power delivery and data connectivity, which, in a multi-node setting, stops power delivery for all nodes when one is communicating and disrupts all communication when one requires power delivery. Moreover, it limits the communication spontaneity, for example, upon a hypoglycemia shock or a sudden abnormality in the biosignals. Lee et al. [23], on the other hand, alternates the power and data path based on the on-chip energy level at the SN. At the BS, the power transmitter and data receiver are separated into two devices to reduce coupling. Kim et al. [24] achieve the simultaneous power delivery and bi-directional communication for an implantable system, by separating the corresponding electrodes away from each other and separating the external power transmitter and data receiver into two devices, which limits the placement and challenges the miniaturization.

Therefore, to address the limitations in the conventional TDM-based BCP and BCC integration, this work proposes a BS IC and an SN IC that achieve the concurrent BCP downlink, BCC downlink, and BCC uplink, while using a single electrode at each device interface which avoids placement constraints and eases miniaturization, as shown in Fig. 3.

The rest of this article is organized as follows. Section II identifies the challenges for achieving the BCP and BCC concurrency, at both BS and SN. Section III then presents the system architecture, providing an overview of the corresponding solutions in this work. Sections IV and V introduce the detailed design of the proposed BS and SN, respectively. Section VI presents the circuit and on-body system-level measurement results, followed by Section VII which concludes this article.



Concurrency Challenges for Base Station (BS)

	Power TX off	Power TX on
Uplink data activated	Leakage	Saturate + Leakage

Concurrency Challenges for Sensor Node (SN)

	Data TX off	Data TX on
BCP disabled	N.A.	Backflow
BCP activated	Leakage	Backflow + Leakage

Fig. 4. Challenges for BCP and BCC concurrency at BS and SN.

II. Challenges for BCP and BCC Concurrency

The challenges for achieving the BCP and BCC concurrency are summarized and illustrated in Fig. 4. Here, two electrodes are shown at each BS/SN to clarify the interrupting signal paths. Note that the challenges discussed below worsen as the two electrodes are placed closer or the TX amplitude gets higher.

At the BS, first, the strong output power signal ($8.4V_{PP}$, for higher power delivery) saturates the data RX. With the body being a good coupling medium, the output power TX signal is coupled at the data RX front end, which is generally larger than the uplink data signal due to closer distance and thus stronger coupling. This saturates the RX front-end amplifier, disrupting the simultaneous uplink data recovery. Furthermore, it is worth noting that the characteristics of such interference signal coupled are subject to changes in the environmental or body-coupling condition. Second, the uplink data signal leaks to the circuit ground through the power TX output path. At power TX output, the parasitic capacitance between the output and circuit ground, or the output switching activity when enabled, forms a relatively low-impedance path to circuit ground (compared with the RX input impedance), degrading the received signal strength of the uplink data.

At the SN, first, the downlink power leaks to the circuit ground through the data TX output path. Similar to the case with power TX, the parasitic capacitance or switching activity at data TX forms a low-impedance path to ground, degrading the power level received at the SN power RX. Second, the uplink data TX output backflows into the power RX. The power RX input impedance is dynamically tracked for maximum power extraction and is comparable or lower than the environmental interface impedance. This causes the data TX signal to flow into the power RX, which not only

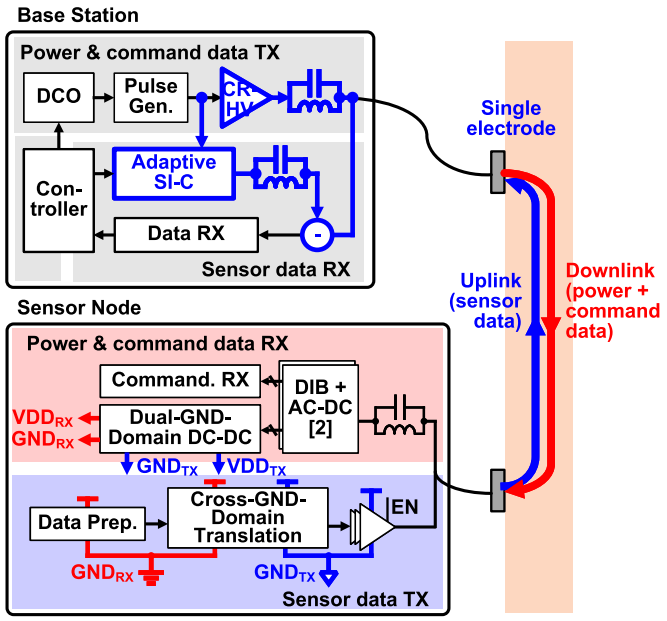


Fig. 5. System architecture.

degrades the output signal strength but also more importantly disrupts the rectifier operation and degrades the power recovery significantly.

III. System Architecture

Fig. 5 shows the proposed BS and SN system architecture [25], to address the challenges identified above. The BS consists of a power and command data TX, a data RX, and the adaptive self-interference cancellation (SI-C) circuit to cancel the interference of the coupled TX signal at the RX front end. The power and command data TX consists of an frequency-shift keying (FSK) baseband controller, a digital-controlled oscillator (DCO) that adopts the constant energy-per-cycle ring oscillator (CERO) structure [26] with open-loop for ample testing flexibility, a pulse generation block for driver switch control, and a charge-replenishing high-voltage (CR-HV) driver for reduced power consumption. The OOK data RX consists of an active low-pass filter, a low-noise amplifier (LNA), an envelope detector, a comparator, and a decoder.

The SN consists of a power RX, a data RX, and a data TX, where the circuit ground of the data TX output drivers (GND_{TX}) is separated from that of the other blocks (GND_{RX}), to avoid current backflow and leakage in between the uplink and downlink paths. The power RX consists of two detuned impedance boosting (DIB) and rectifier circuits [2], [27] for power recovery from the downlink FSK signal, as well as a dual-ground-domain boost power converter, to provide the regulated power supply for both ground domains while maintaining the ground separation. The data RX is passive receiver based, which performs the clock and data recovery for the downlink signal. The data TX consists of an OOK data preparation block in the GND_{RX} domain, the tri-state output drivers in the GND_{TX} domain, and a cross-ground-domain translation block for signal translation while maintaining the ground separation.

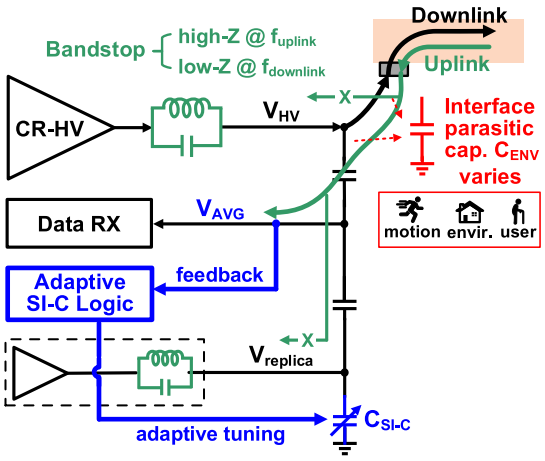


Fig. 6. BS structure for BCP and BCC concurrency.

IV. Base Station Design

This section elaborates on the BS structure that enables the concurrent power/data TX and data RX, including the adaptive SI-C circuits to cancel the HV TX interference at the data RX front end, as well as the band-stop *LC* filters to suppress uplink signal leakage. It also elaborates the CR-HV TX driver design, to reduce the BS power consumption and prolong its battery lifetime.

A. Adaptive Self-Interference Cancellation

To avoid saturating the data RX by the TX output signal ($8.4V_{\text{PP}}$), analog cancellation is performed at the data RX front end, where the TX output signal V_{HV} is canceled with its 180° out-of-phase replica signal V_{replica}, as shown in Fig. 6. However, inherent to the capacitive body-coupling mechanism, the equivalent loading capacitance at the TX output interface C_{ENV} is subject to variations when the electrode or environmental coupling condition changes, causing the actual output signal V_{HV} slew rate to vary. To ensure accurate V_{HV} cancellation in spite of such loading variations, an adaptive SI-C logic is proposed, which adaptively tunes the replica signal loading capacitance $C_{\text{SI-C}}$, such that V_{replica} matches with the actual output V_{HV}.

The adaptive SI-C logic is illustrated in Fig. 7(a). In cases where $C_{\text{SI-C}}$ is larger than C_{ENV}, V_{replica} transitions slower than V_{HV}. At V_{HV} falling edge, this leads to negative peaks observed in the cancellation result V_{AVG}. On the other hand, if $C_{\text{SI-C}}$ is smaller, positive peaks would occur. By using the cancellation result V_{AVG} as the feedback to tune $C_{\text{SI-C}}$ toward the actual C_{ENV}, the adaptive cancellation of V_{HV} could be achieved. Fig. 7(b) shows the circuit implementation of the adaptive SI-C logic. To ensure a consistent interpretation of V_{AVG}, the positive and negative peak detection, or V_{AVG} evaluation, are activated upon V_{HV} falling edge, where switches $S1$ and $S2$ are open, and $S3$ and $S4$ are closed; otherwise, $S1$ and $S2$ are closed and both V_{POS} and V_{NEG} are tied to "low." The upper path performs negative peak detection, where V_{NEG} is pulled to "high" when V_{AVG} amplitude falls below "0" within a hysteresis window and is tied to "low" otherwise. The lower path performs the positive peak detection, which pulls V_{POS}

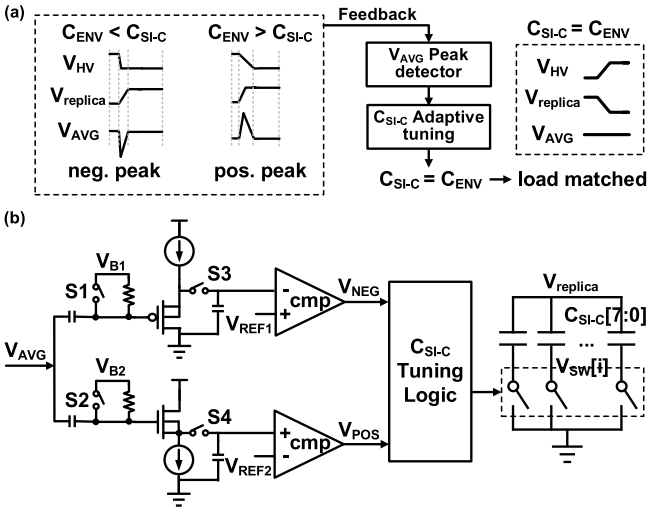


Fig. 7. (a) Adaptive SI-C logic. (b) SI-C logic circuit implementation.

to "high" when a positive peak occurs in V_{AVG}. By extracting the amplitude and polarity of V_{AVG}, the loading capacitor bank C_{SI-C} of replica signal $V_{replica}$ could be tuned by the C_{SI-C} tuning logic, such that the cancellation results stay within the acceptable range. With V_{POS} = "1" and V_{NEG} = "0" which indicates a positive peak in V_{AVG} and thus $C_{SI-C} < C_{ENV}$, the C_{SI-C} control bit will be incremented. When V_{POS} = "0" and V_{NEG} = "1," C_{SI-C} will be decremented.

The C_{SI-C} capacitor bank switch design is worth noting, considering that the $8.4V_{PP}$ (V_{HV} and $V_{replica}$ output swing) across its source and drain. For a standard CMOS-compatible design, the on/off path of the high-voltage (HV) switch consists of four stacked transistors, such that each has a V_{DS} within the nominal level. As Illustrated in Fig. 8, to avoid the additional level shifters or biasing circuits for control signal generation in different voltage domains, M_{P1}–M_{P6} are designed to enable the direct control of the HV switch by a nominal gate control signal V_{CTR}. When V_{CTR} = "0," M_{N1}–M_{N4} are configured to be a high-impedance inverted diode ladder to suppress the current flow from V_{SW} to the ground (i.e., HV switch off), where V_{DS} of each transistor approaches $1/4V_{SW}$. Under the worst case where $V_{SW}[i] = 4V_{DD}$ (10 V theoretically but 8.4 V measured due to the charge pump conduction loss), the drain voltage of M_{N1}–M_{N4} is thus settled at V_{DD}, $2V_{DD}$, $3V_{DD}$, and $4V_{DD}$, respectively, and V_{DS} approaches $1V_{DD}$, within the nominal range. When $V_{CTR} = 1V_{DD}$ for the HV switch on, $M_{P2,4,6}$ is closed, such that V_G of the four stacked transistors is settled around $V_{CTR} = 1V_{DD}$ (2.5 V), and their V_{DS} is settled around 0 V, enabling the current flow from V_{SW} to ground.

The adaptive SI-C achieves the HV TX interference suppression by ~40 dB (as shown in Section VI), avoiding the saturation of the active low-pass filter in the data RX signal chain, which further suppresses such out-of-band interference. Considering the small ON-resistance of the TX driver output and the small equivalent series resistance (ESR) of the inductors/capacitors, the main noise-contributing block introduced in the RX signal chain is the active low-pass filter required for further interference suppression.

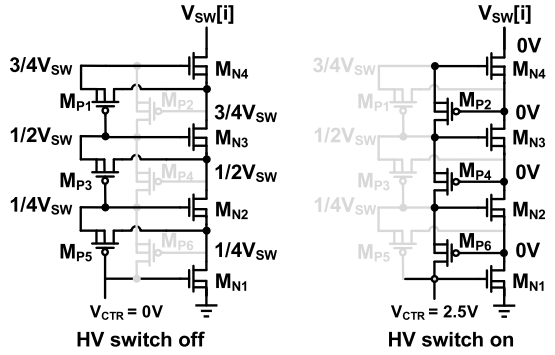


Fig. 8. HV switch schematic and operation.

B. Band-Stop Filter

To avoid the uplink data signal leakage through the CR-HV driver or the replica driver output, a band-stop *LC* filter is introduced at the TX output, as shown in Fig. 6. It resonates near the data uplink frequency (1 MHz) and thus exhibits high impedance to suppress the uplink signal leakage while having a low impedance near the downlink frequency for the normal TX operation. In this work, the bandstop *LC* filter has the values of 47 μH and 560 pF and is implemented off-chip. The Q factor of the bandstop *LC* filter should be designed as high as possible while tolerating the inaccuracies of the carrier frequency generated due to the PVT variations.

C. Charge-Replenishing High-Voltage Driver

For higher power delivery over the optimal BCP frequency span (up to 80 MHz [7]), an HV driving stage is designed at the BS TX. Compared with the implementations in the HV or SOI process [28], standard CMOS-compliant designs use the stacked MOS configurations with corresponding biasing techniques to tackle the overstress and gate–oxide reliability issue [22], [29], [30]. Serneels et al. [29] and Luo and Ker [30] introduced the self-generated and adaptive gate biasing techniques, respectively. However, both biasing techniques consume high static current which increases with the switching speed. Dong et al. [22] introduced a four-stage charge-pump-based gate biasing technique, which removes the need for additional biasing circuits, level shifters, and tapered buffers, reducing the power consumption. However, the limited transition speed in [22] not only limits the driver switching frequency but also leads to increased power loss due to the crowbar current at a higher switching frequency.

To further minimize the power consumption, while achieving the $8.4V_{PP}$ swing and up to 80-MHz frequency in standard CMOS, the CR-HV driver is introduced, as illustrated in Fig. 9. The driver stage consists of stacked transistors. The $4V_{DD}$ supply, intermediate voltage levels ($3V_{DD}$, $2V_{DD}$), and the $4V_{DD}$-to-$3V_{DD}$ control signal swing are all generated on-chip from a four-stage charge pump. During the pull-down stage, the three intermediate nodes (nodes 1–3) fast transition from $4V_{DD}$ to $3V_{DD}$, $2V_{DD}$, and $1V_{DD}$, respectively (enabled by MN1–3 and MP1–3), where charges are transferred from the parasitic capacitors (formed with the chip ground, at nodes 1–3) to C_{CP1}–C_{CP3}. During the pull-up stage, charges stored (on C_{CP1}–C_{CP3}) are then used to assist in biasing

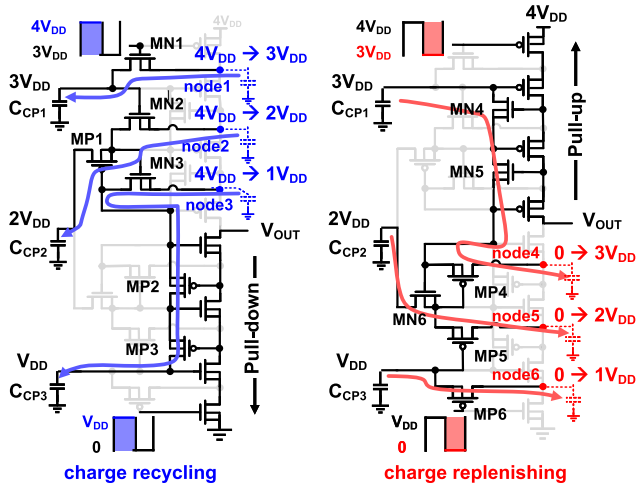


Fig. 9. CR-HV driver.

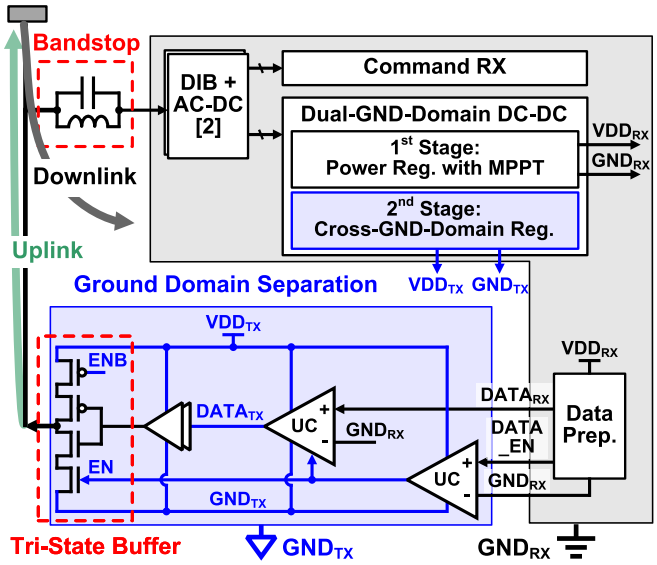


Fig. 10. Leakage and backflow suppression techniques at SN.

nodes 4–6 to transition to higher voltages (corresponding with voltages at C_{CP1}–C_{CP3}). This enables the faster transition of node voltages, and, thus, higher achievable frequency and lower crowbar current. Moreover, by recycling and replenishing charges at the intermediate nodes, power drawn from the supply is reduced.

V. Sensor Node Design

This section elaborates the SN design for uplink and downlink concurrency, including the ground-domain separation structure and techniques for leakage and backflow suppression, the dual-ground-domain dc–dc converter for regulated supply in both ground domains, as well as the downlink power and data co-recovery structure.

A. Sensor Node Leakage and Backflow Suppression

At the SN, both the power receiving path and the data output path exhibit low impedance, causing input signal leakage (through the output) and output signal backflow (to the input). To minimize such inter-path current flow, high impedance should be maintained in between the power RX and data TX paths. However, considering the good coupling characteristics of the human body and the need for miniaturization (i.e., downlink and uplink electrodes should be close), this work separates the circuit grounds of the two paths into GND_{RX} and GND_{TX}, to suppress the inter-path current flow.

The detailed ground-domain separation structure is illustrated in Fig. 10. In the CMOS process, GND_{RX} is the p-substrate, whereas GND_{TX} is implemented in deep n-well. VDD_{RX} and VDD_{TX} are the supply voltage with respect to GND_{RX} and GND_{TX}, respectively. The n-well and deep n-well potentials are connected to the supply voltage of the particular ground domain (i.e., VDD_{TX} for GND_{TX}-domain transistors and VDD_{RX} for GND_{RX}-domain transistors). With the GND_{TX} domain introduced, additional couplings exist between GND_{TX} and the electrode interface, BS ground, as well as GND_{RX}. The coupling between the two ground mains (i.e., GND_{TX} and GND_{RX}) could cause the inter-path signal flow, degrading the downlink/uplink performance when enabled concurrently. Thus, to minimize this coupling, the GND_{TX} domain area in the layout is minimized. Thus, Along the data TX output path, only the driver stage is implemented in the GND_{TX} domain, with the baseband data preparation performed in the GND_{RX} domain. The post-layout simulation shows <0.4 pF coupling. It is worth noting that the potential difference between the GND_{TX} and GND_{RX} is below the nominal range (2.5 V for the thick-oxide devices used), which is attributed to: 1) the relationship between GND_{RX} and GND_{TX} potential through the common signal at uplink/downlink interface and their parasitic coupling and 2) the parasitic diode between p-substrate and deep n-well.

For output signal translation across the ground domains, a comparator operating in the GND_{TX} domain with full input swing is implemented, which takes in the GND_{RX}-domain signal and the GND_{RX} as its inputs, and outputs GND_{TX} or VDD_{TX}. To avoid oscillation and to improve the setting time, the comparator is designed with asymmetrical input transistor pairs for an intentional constant offset, given that the input signal difference is either VDD or 0 (approximately) in this case. Such comparators are, thus, referred to as "unbalanced comparators" and are also used in the cross-ground-domain dc-dc converter control (to be elaborated later). The NMOS transistors are implemented in deep n-well which is connected to the supply in the respective ground domain.

Considering the parasitic coupling between the two ground domains (<0.4 pF), to further prevent the data output from backflowing into the power RX path, a band-stop *LC* filter is designed at the power RX input, which resonates near the data uplink frequency (1 MHz) to exhibit high impedance for the data output signal and low impedance for the input power recovery, as illustrated in Fig. 10. Moreover, to further suppress downlink signal leakage when the data TX is off, a tri-state buffer is introduced at the data TX output stage to exhibit high impedance when off.

B. Dual-Ground-Domain DC–DC Converter

To provide the regulated supply for circuits designed in both GND_{RX} and GND_{TX} domains while minimizing the

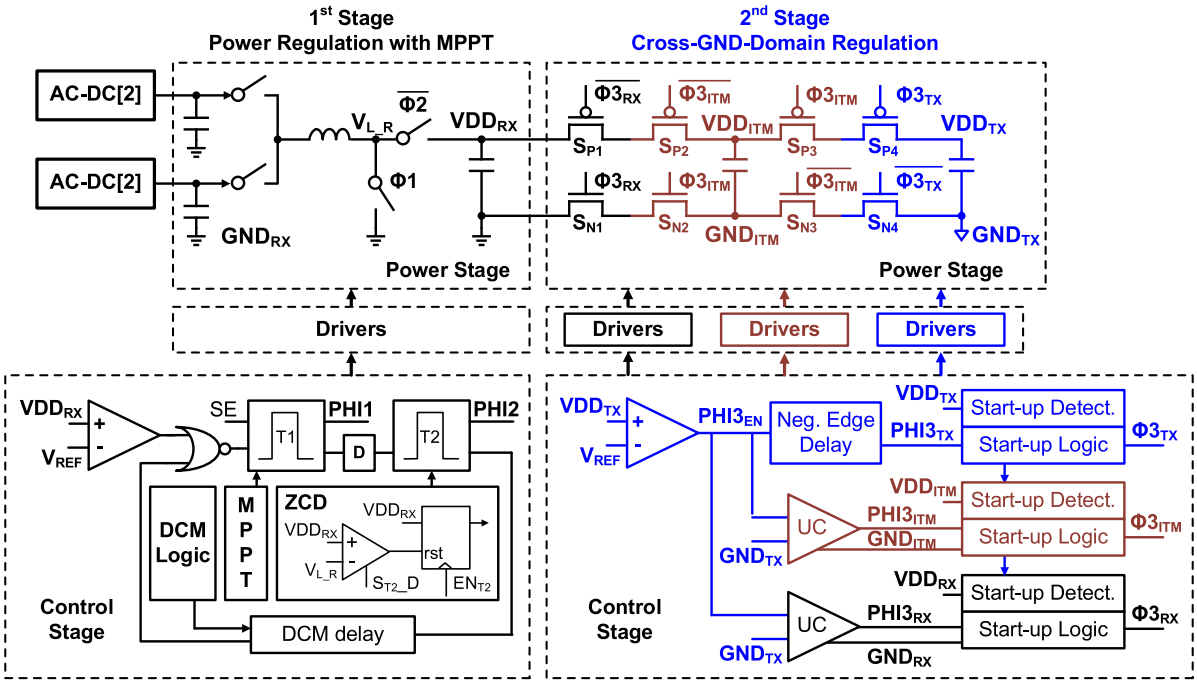


Fig. 11. Dual-ground-domain dc–dc converter.

coupling, the dual-ground-domain dc–dc converter is introduced, as illustrated in Fig. 11. The converter consists of two stages, outputting the regulated VDD_{RX} and VDD_{TX}, respectively.

The first-stage power conversion performs the dual-input boost conversion with the maximum power point tracking (MPPT) [2]. The switched-mode power converter operates in the discontinuous conduction mode (DCM), where the inductor charging time $T1$ is determined by the hill-climbing algorithm-based MPPT [31]. The inductor discharging time $T2$ is determined by zero-current switching (ZCS), where a direct comparison between V_{L_R} and VDD_{RX} is performed to determine the PHI2 duration. To reduce the static power consumption for higher conversion efficiency, the ZCS comparator is power gated depending on the $T1$ completion and zero-current crossing detection. The maximum conversion frequency is dependent on the DCM time, which adapts to the input voltage level [2].

The second-stage conversion performs the cross-ground-domain voltage regulation, converting the regulated VDD_{RX} to the regulated VDD_{TX} (with respect to GND_{TX}) while maintaining the separation. Considering the indeterminate relative potentials between VDD_{RX} and VDD_{TX} in the switched-capacitor-based converter power stage, to ensure the complete GND_{RX}-domain and GND_{TX}-domain switch on/off, an intermediate stage (GND_{ITM}) is introduced. The GND_{ITM} (VDD_{ITM}) connects to GND_{RX} (VDD_{RX}) for charge transfer from VDD_{RX} to the intermediate-stage capacitor. It connects to GND_{TX} (VDD_{TX}) for charge transfer to VDD_{TX}. Switches in different ground domains are controlled by signals that are translated to their corresponding domains, by the unbalanced comparators.

The normal-mode operation is illustrated in Fig. 12(a). When VDD_{TX} falls below the reference voltage, $PHI3_{EN}$ is pulled down, which is then translated to $PHI3_{ITM}$ and $PHI3_{RX}$, opening S_{P1}–S_{P2} and S_{N1}–S_{N2}, while closing S_{P3} and S_{N3}. The negative edge delay is introduced to ensure that $PHI3_{TX}$ is pulled down last, to avoid flow-through current due to switch transition overlapping which would otherwise degrade the ground-domain isolation. When VDD_{TX} increases above the reference voltage, $PHI3_{EN}$ is pulled up, causing $PHI3_{TX}$ to pull up and thus opening S_{P4} and S_{N4}. Upon signal translation to the GND_{ITM} and GND_{RX} domain, $PHI3_{ITM}$ and $PHI3_{RX}$ are then pulled up, opening S_{P3} and S_{N3} while closing S_{P1}–S_{P2} and S_{N1}–S_{N2}.

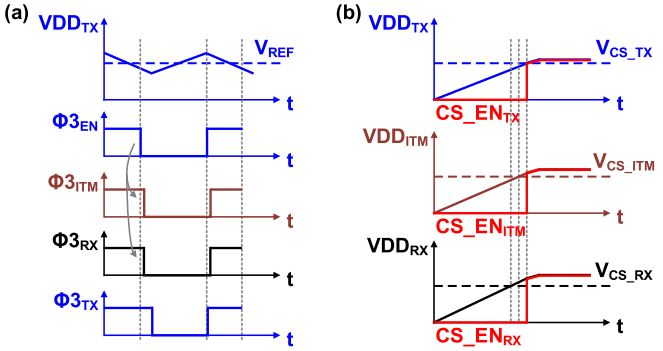


Fig. 12. Transient illustrations of (a) normal-mode operation and (b) cold-start operation.

When VDD_{TX} is below 0.8 V (the pre-defined cold-start threshold), the second-stage conversion enters the cold-start mode, where all second-stage power switches are closed. Therefore, during cold-start, the data TX should be disabled. In each ground domain (GND_{TX}, GND_{ITM}, and GND_{RX}), the startup detector [32] is introduced to monitor VDD, which outputs "0" if VDD is below 0.8 V and tracks VDD otherwise. As illustrated in Fig. 12(b), due to the conduction loss, VDD_{RX} usually rises above the cold-start threshold first, followed

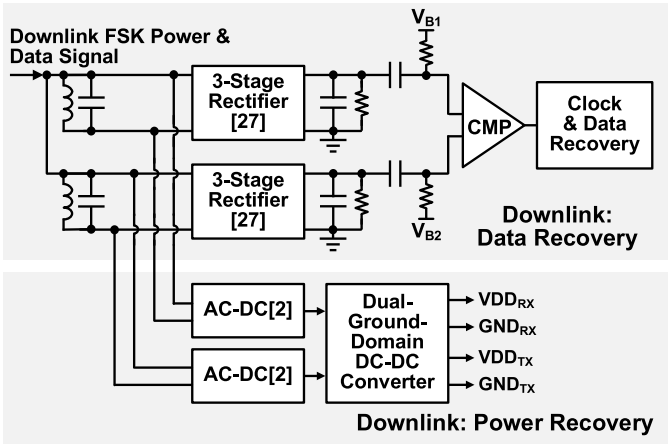


Fig. 13. Command data RX schematic.

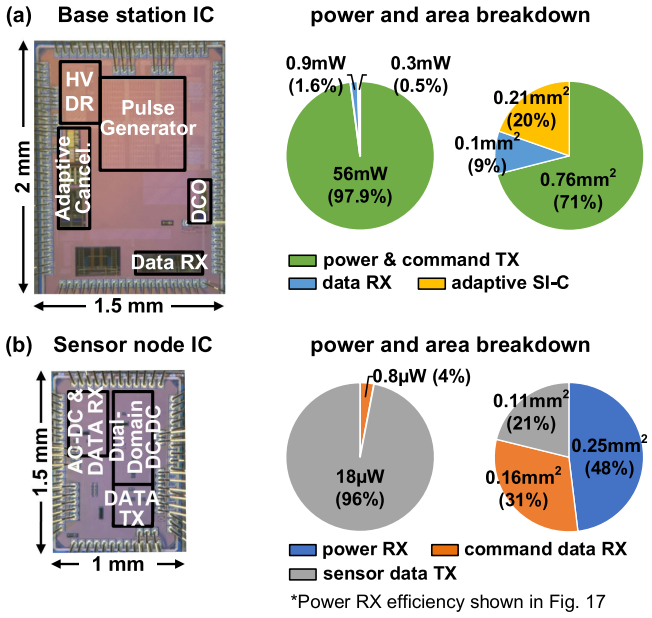


Fig. 14. Micrographs, power and area breakdown of (a) BS and (b) SN ICs.

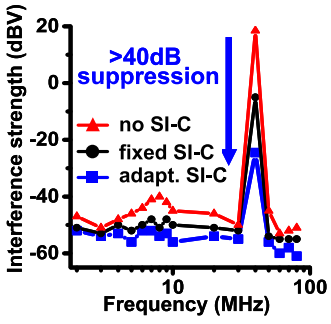


Fig. 15. Measured adaptive self-interference suppression at BS.

by VDD_{ITM} and then VDD_{TX}. Despite that, CS_EN_{RX} and CS_EN_{ITM} are only pulled to VDD_{RX} and VDD_{ITM}, respectively, after CS_EN_{TX} is pulled high when VDD_{TX} rises above 0.8 V, in order to align the mode of operation across all three domains.

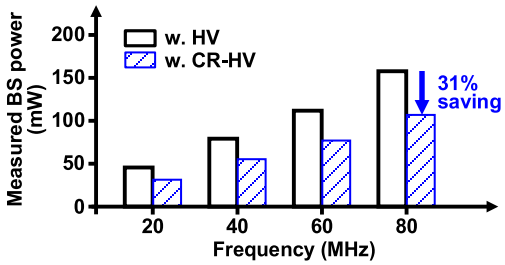


Fig. 16. Measured BS power reduction by the charge-replenishing technique proposed.

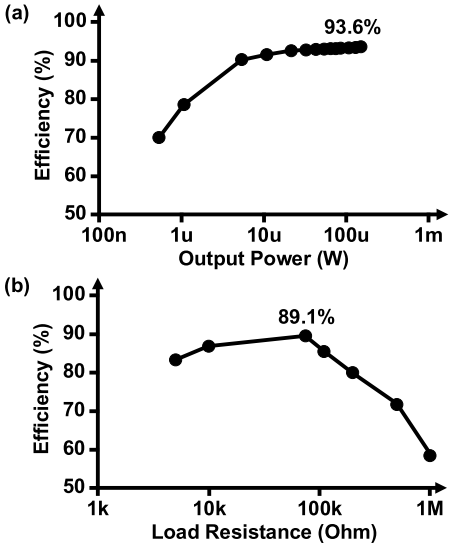


Fig. 17. Measured dc–dc conversion efficiency. (a) First-stage conversion. (b) Second-stage cross-ground-domain conversion.

C. Passive Receiver-Based Command Data RX

The downlink power and data recovery structure is shown in Fig. 13, where the FSK command data receiver is passive receiver based to reduce the active power consumption. The parallel *LC* structure filters and boosts the input signal at each FSK frequency (1.2 μH and 12 pF for 40 MHz and 8.2 μH and 22 pF for 10 MHz in this design, implemented off-chip). The FSK frequencies and their separation are determined by the body-coupled path loss and the receiver's capability to distinguish, within its power budget. The three-stage rectifier down converts the two frequencies, which are then compared for baseband data extraction, as well as the clock and data recovery. Considering that the human body channel loss differs at different transmission frequencies, to overcome errors in decoding, external biases V_{B1} and V_{B2} are introduced to adjust the comparator offset to balance the sensitivity for the two frequencies.

VI. Measurement Results

This section first shows the BS and SN circuit measurements and then presents the on-body system measurement results for uplink and downlink concurrency.

A. Circuit Performance Measurements

Fig. 14 shows the BS and SN chip micrographs, both of which are implemented in the 40-nm 1P8M CMOS process.

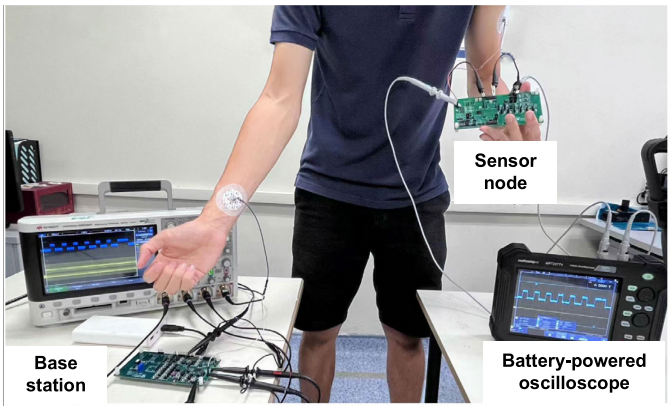


Fig. 18. On-body system measurement setup for system operations.

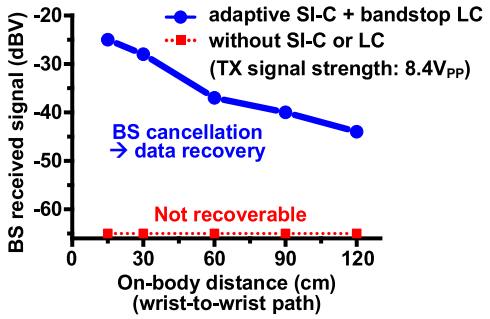


Fig. 19. BS: measured RX signal strength while transmitting power.

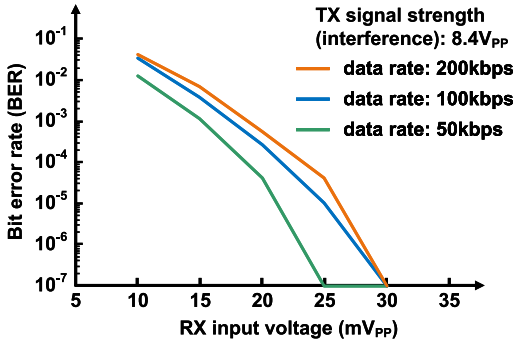


Fig. 20. BS: measured BER against RX input voltage at different rates, when 8.4V_{PP} TX output is enabled concurrently.

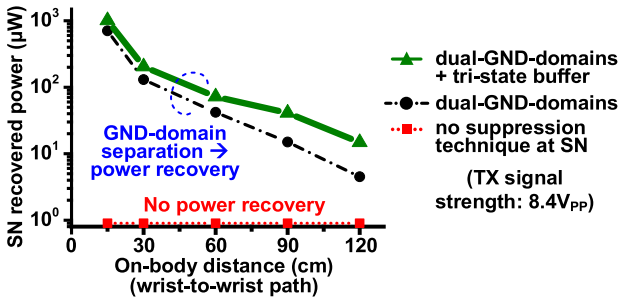


Fig. 21. SN: measured recovered power when SN data TX is off.

At the BS, the adaptive SI-C performance is characterized by measuring the signal strength V_{AVG} at the data RX front end, when the downlink high-voltage signal output is coupled to the data RX via the shared electrode. As shown in Fig. 15, the analog cancellation structure achieves the interference

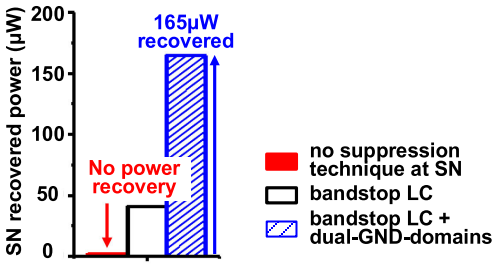


Fig. 22. SN: measured recovered power when SN data TX is on.

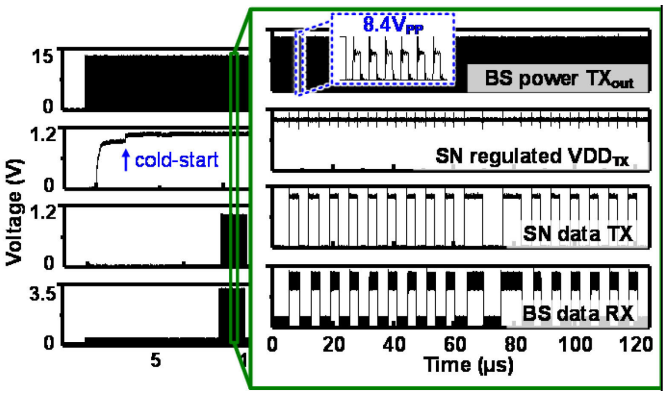


Fig. 23. System: transient measurements of the concurrent downlink (BS → SN) powering and uplink (SN → BS) data transmission.

suppression by around 20 dB. By adapting the replica signal loading capacitance for improved cancellation, the adaptive SI-C further improves the interference suppression to over 40 dB, enabling the concurrent data recovery. Considering the interferer signal at 40 MHz and the uplink RX signal at 1 MHz which could be separated in the frequency domain, the interference suppression achieved is sufficient to avoid saturation in the active low-pass filter (for further out-of-band interference suppression), which is then followed by an amplifier and OOK demodulation circuits for RX data recovery. Nonetheless, due to the limit in the interference suppression, the bit error rate (BER) with concurrent HV output could be degraded by ∼1–2 orders of magnitude, when the RX input voltage is low (e.g., <20 mV_{PP}), compared with the scenario when HV output is disabled.

Fig. 16 shows the measured power consumption of the BS, where the driver outputs an 8.4V_{PP} signal (with no FSK modulated data), at frequencies ranging from 20 to 80 MHz. With the HV driver being the most power-hungry block at BS, the charge-replenishing technique proposed leads to the overall BS power reduction. As the driver frequency increases and thus consumes higher power, the percentage of power reduction increases, reaching 31% at 80 MHz.

At the SN, the dual-ground-domain dc–dc converter efficiency is shown in Fig. 17. The first-stage conversion efficiency is measured to be over 90% at the output power ranging from a few microwatts to over 100 μW and over 70% at the output power of over 500 nW. To ensure the ground domain separation while measuring the second-stage power conversion efficiency, VDD_{RX} is battery powered and different resistors are soldered across the VDD_{TX} and GND_{TX} to adjust the output power. A USB-powered picoscope is

TABLE I
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART BODY AREA POWERING AND COMMUNICATION SYSTEMS

	This Work	JSSC'22 [23]	ASSCC'21 [24]	JSSC'22 [16]	ISSCC'21 [33]	JSSC'14 [34]
Technology	**40nm CMOS**	110nm/180nm CMOS	180nm CMOS	65nm CMOS	180nm BCD	65nm CMOS
Scheme	**BCP + BCC (concurrent & single electrode at BS & SN)**	BCP (2 separate devices) + BCC uplink	BCP + BCC (concurrent at BS & SN)	Quasi-static BCP+ BCC (alternating)	Inductive power + data downlink	RF power + data uplink
Number of electrodes per BS/SN	**1**	2	4 (2 pairs apart)	1 (w. path switches)	1 coil	2 antenna
BS: uplink data recovery & downlink P_{OUT}	**Concurrent (single electrode); Data: 100kbps; P_{OUT}: 30mW (40MHz)**	Concurrent with 2 separate devices; Data: 20.48Mbps; V_{OUT}: $10V_{PP}$	Concurrent with 2 separate devices; Data: 10Mbps; V_{OUT}: $3\text{-}6V_{PP}$	Alternating; Data: 1-20kbps; P_{OUT}: 650µW	Downlink only; P_{OUT}: 128mW	N.A.
SN: downlink P_{RV} & uplink data transfer	**Concurrent (single electrode); Data: 100kbps; P_{RV}: 165µW (30cm), 12.5µW (120cm)**	TDM; Data: 20.48 Mbps; P_{RV}: 50s 5nF capacitor charged to 2.7V	Concurrent with electrodes separated; Data: 10Mbps; P_{RV}: 25µW-568µW	Alternating; Data: 1-20kbps; P_{RV}: 28µW for all body distance	Downlink only; P_{RV}: 110mW	Concurrent with 2 antenna separated; Data: 250kbps; P_{RV}: 231.6µW
Data uplink-downlink	**Uplink: 100kbps (OOK); downlink: 20kbps (FSK)**	Uplink only: 20.48Mbps (direct signaling)	Uplink: 10Mbps; Downlink: 200kbps	Alternating; 1-20kbps	Downlink only; 2.5Mbps (FR-FSK)	Uplink only; 250kbps (OOK)
Transmission Distance	**Full body**	Neural implant	Neural implant	Full body	5-8mm Cochlear implant	0.9m-9m LoS

* BS: Base Station; SN: Sensor Node

used to observe the output voltage (regulated around 1 V). Up to 89.1% conversion efficiency is measured at 75 kΩ, and over 70% efficiency is observed at the loading from around 5–500 kΩ.

B. On-Body System Measurements

The on-body system measurement setup is shown in Fig. 18. It covers three measurement categories: 1) BS; 2) SN; and 3) system measurements. The BS and SN are placed/held separately on two sides of the body, where wet electrodes are used to couple the signal onto and from the body. We ensure that the measurement equipment does not share common ground. For system operation verification (simultaneous downlink power delivery and uplink data communication), measurements are performed at both BS and SN simultaneously, which mandates oscilloscopes on both sides. It should be noted, though, that having equipment attached at both BS and SN sides with wirings could cause additional coupling, which may lead to more optimistic results (i.e., less path loss). Therefore, to minimize the equipment-induced couplings when measuring the BS or SN performance only (e.g., BS: data recovery and SN: power recovery), equipment is only attached to the device under test, whereas the other device (not being measured directly) does not have external equipment attached.

At the BS, the received uplink signal strength is measured when the downlink HV signal is transmitted concurrently. As shown in Fig. 19, measured along the wrist-to-wrist path, by suppressing the leakage and HV interference, the proposed techniques achieve > -45 dBV received signal strength at the RX input, compared with no effective uplink data signal observed otherwise. The measured BER of the uplink data receiver is illustrated in Fig. 20, when the downlink HV output is enabled concurrently (i.e., self-interference: $8.4V_{PP}$). As the RX input voltage increases, the influence of HV interference reduces.

At the SN, to measure the input power leakage suppression (through the low-impedance data TX output path), the uplink data TX is first disabled. As shown in Fig. 21, without the proposed techniques, power recovery is unachievable due to leakage. In contrast, by suppressing the current flow between the two paths, the ground-domain separation achieves around 700 μW at 15-cm on-body distance and 4 μW at 120 cm. This is further improved by the tri-state buffer, achieving around 1 mW at 15 cm and 15 μW at 120 cm.

Fig. 22 shows the measurement results of the concurrent power recovery while transmitting the uplink data. The overall power recovery is the sum of the optimal GND_{RX} domain power extracted and the GND_{TX} domain power consumed by the data TX. Without the proposed techniques, power recovery is insignificant due to leakage and the disruption of rectifier operation caused by backflow. In contrast, the proposed ground-domain separation and band-stop *LC* techniques enable the power recovery of 165 μW at 30-cm apart and 12.5 μW at 120-cm apart.

The transient measurements of the concurrent powering and uplink data transmission at the BS and SN are illustrated in Fig. 23. The downlink power delivery from the BS powers the SN wirelessly and regulates the VDD_{TX}, which then enables the uplink data TX. The data RX at the BS recovers such uplink data concurrently.

The performance comparison with the state-of-the-art body area powering and communication system is summarized in Table I. Overall, this work achieves the concurrent BCP and BCC (uplink and downlink) via a single electrode, which has not been achieved before. Compared with [16] that integrates the BCP and BCC in a TDM-based alternating manner with switches for path selection, this work achieves the BCP and BCC concurrency, which is essential for the sustained BAN powering without disruptions of the data connectivity. Compared with [23] and [24] that separate the power TX and uplink data RX into two devices with multiple electrodes for downlink–uplink concurrency at the BS, this work achieves the concurrency in an integrated device via a single electrode, at both BS and SN. Compared with inductive- [33] or RF-based [34] systems that are constrained

to certain on-body paths (e.g., line-of-sight and alignment), this work uses the body-coupled approach for wireless powering and communication, achieving the full body area coverage.

VII. Conclusion

To conclude, this work proposed the BAN BS and SN ICs that could achieve the concurrent BCP, uplink, and downlink BCC via a single electrode. At the BS, this is enabled by the adaptive SI-C with the band-stop *LC* techniques, which overcome the HV signal saturation and leakage, enabling 100 kb/s concurrent uplink data recovery. At the SN, the uplink and downlink concurrency is enabled by the ground-domain separation, band-stop *LC*, and tri-state buffer techniques, which overcome the leakage and backflow, enabling 12.5-μW power recovery at 120 cm while transmitting the uplink data.

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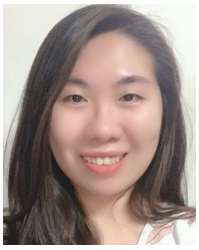

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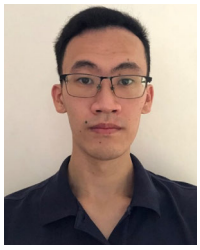

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