A Sub-THz Full-Duplex Phased-Array Transceiver With Self-Interference Cancellation and LO Feedthrough Suppression

Chun Wang, *Graduate Student Member, IEEE*, Ibrahim Abdo, *Member, IEEE*, Chenxin Liu, *Graduate Student Member, IEEE*, Carrel da Gomez, *Graduate Student Member, IEEE*, Jill Mayeda, *Member, IEEE*, Hans Herdian, *Graduate Student Member, IEEE*, Wenqian Wang, *Student Member, IEEE*, Xi Fu, *Member, IEEE*, Dongwon You, *Student Member, IEEE*, Abanob Shehata, *Graduate Student Member, IEEE*, Sunghwan Park, Yun Wang, *Member, IEEE*, Jian Pang, *Member, IEEE*, Hiroyuki Sakai, *Senior Member, IEEE*, Atsushi Shirane, *Member, IEEE*, and Kenichi Okada, *Fellow, IEEE*

***Abstract*— A sub-THz (88–136 GHz) full-duplex (FD) phased-array transceiver (TRX) integrating an RF self-interference (SI) canceller with differential feeding FD antennas is presented in this work. The LO phase generation chain controls differential transmitter outputs for the phased-array operation. The differential feeding FD antenna with differential pairs of chips achieves over 35-dB SI suppression. The SI suppression is improved by 20 dB when the SI canceller is turned on. Without any digital-domain SI cancellation (SIC), a total SI suppression of >60 dB is achieved over a 2-GHz bandwidth. The proposed neutralized mixer with over 20-dB LO feedthrough suppression and wideband RF amplifiers support a large data rate at sub-THz frequencies. This is the world's first demonstrated sub-THz FD phased-array TRX. In the over-the-air (OTA) measurements for FD mode, the proposed FD TRX achieves 6 Gb/s in 8PSK and 4 Gb/s in 16QAM. It also achieves a 112-Gb/s data rate for OTA TX-to-RX.**

***Index Terms*— 6G, full-duplex (FD), LO feedthrough suppression, phased-array transceiver, self-interference (SI) suppression, sub-THz, wideband.**

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Chun Wang, Chenxin Liu, Carrel da Gomez, Jill Mayeda, Hans Herdian, Wenqian Wang, Xi Fu, Dongwon You, Abanob Shehata, Sunghwan Park, Hiroyuki Sakai, Atsushi Shirane, and Kenichi Okada are with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo 152-8550, Japan (e-mail: wangc@ssc.pe.titech.ac.jp).

Ibrahim Abdo was with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo 152-8550, Japan. He is now with NTT Device Technology Laboratories, NTT Corporation, Atsugi, Kanagawa 243-0198, Japan.

Yun Wang was with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo 152-8550, Japan. He is now with the State Key Laboratory of Integrated Chips and Systems, Fudan University, Shanghai 200120, China.

Jian Pang was with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo 152-8550, Japan. He is now with the Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai 200241, China.

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I. Introduction

THE world has been shifting to the fifth-generation (5G) communication network, and many new applications are developing, such as 5G mobile phones, automatic driving cars, virtual reality (VR) terminals, Internet of Things (IoT) devices, ultra-high digital television, and drones in both commercial and the military [1], [2], [3], [4]. Many of these new applications require large data rates, some even requiring over 100 Gb/s [5], [6]. Even though 5G is still being developed, researchers and engineers are already looking ahead to sixth-generation (6G) applications to help remedy many societal shortcomings with speculated applications such as immersive XR, high-fidelity mobile holograms, and digital replicas. These new applications would require even higher data rates than 5G as 6G would be expected to require up to 1 Tb/s [7], [8], [9]. Already, there is an issue with 5G due to the current usable spectrum limitation for communication, and the throughput of present applications is not large enough according to the Shannon rule; thus, this problem will become even more exaggerated for 6G. Therefore, 6G is expected to include communication networks based on the millimeter-wave/sub-THz band, and thus, developing these systems is crucial to future communication networks.

Besides using a wider spectrum for data communication, a full-duplex (FD) technique has also been proposed to increase the throughput for communication [10], [11], [12], [13], [14], [15], [16], [17], [18], [19]. Compared with the existing time-division duplex (TDD) and frequency-division duplex (FDD) systems, FD communication could double the spectral efficiency immediately in the physical layer by transmitting and receiving simultaneously on the same frequency channel. One of the major challenges of FD technology is to suppress wideband modulated self-interference (SI) from a transmitter (TX) to a receiver (RX) front end. Otherwise, a strong SI signal could lead to intermodulation products in the RX chain [20]. An extremely high suppression is usually required within all the antenna-, RF-, and digital-domain cancellations, as shown in Fig. 1 [20], [21], [22], [23], [24], [25]. However, as shown in the theoretical analysis, these cancellations are

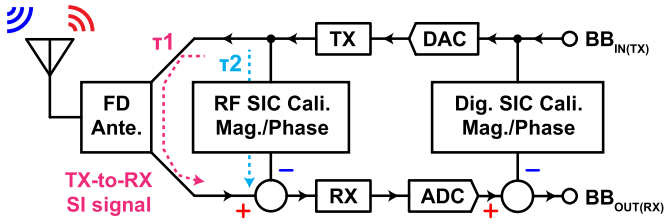


Fig. 1. SI signal and its cancellation in an FD TRX.

difficult. Because the time delay of the SI signal path from the TX output port, through the FD antenna, transmitting to the RX input port (pink dot link) should be the same as the time delay of the SI cancellation (SIC) signal modulated by the calibration circuits (blue dotted line).

To achieve the above requirements of the FD system, numerous topologies have been proposed, such as using an antenna/duplexer [26], [27], [28], [29], [30], [31], [32], [33]; controlling time delay [34], [35], [36], [37], [38], [39], [40], [41], [42]; noise cancellation [43], [44], [45], [46], [47], [48], [49], [50]; and SIC [51], [52], [53], [54], [55], [56], [57], [58]. Unfortunately, all these efforts focus at low frequencies, and their communication bandwidth is narrower than 1 GHz. The main difficulty for higher frequencies is that the SIC signal needs accurate control of magnitude, phase, and time delay; however, inductors, capacitors, and transistor models are not that accurate in millimeter-wave frequencies. Nevertheless, there have been several demonstrated FD systems at millimeter wave. For instance, Dinc et al. [20], [21] integrated a full antenna-, RF-, and digital-domain SIC and were the first works that showed an FD system at 60 GHz. They introduced a polarization-based antenna with a reflective load to increase the SI suppression of the signal radiating from TX to RX. However, this kind of antenna consists of two separated TX and RX patch antennas, which are area-consuming and not convenient to apply to sub-THz. Chi et al. [59], [60] proposed a multi-feeding polarization antenna to combine TX radiating and RX receiving together at 60 GHz. However, these works only considered RF block design, and the passive reconfigurable canceller was limited in a magnitude tuning range. Mondal et al. [61] and Mondal and Paramesh [62] introduced an FDD/FD transceiver based on a transformer-coupled resonator at 28/37 GHz. However, these works do not integrate the antenna and consist of only RF blocks. Furthermore, all the above-introduced works suffer from narrow bandwidth, and the maximum data rate is not large enough to support 6G communication.

In this article, we present a sub-THz FD phased-array transceiver (TRX) integrating an RF SI canceller with differential feeding FD antennas, which, to the best of the authors' knowledge, is the world's first sub-THz FD phased-array TRX. First, an FD differential feeding dual-polarized antenna driven by two TRX chips is used, as explained in Fig. 2. When a single-ended dual-polarized antenna is used, the RX performance suffers from large TX leakage due to the poor isolation caused by the asymmetric antenna structure [see Fig. 2(a)]. This issue could be overcome by switching to a differential FD antenna, but if a single chip is used for feeding the differential TX and RX signals with four feedings, there

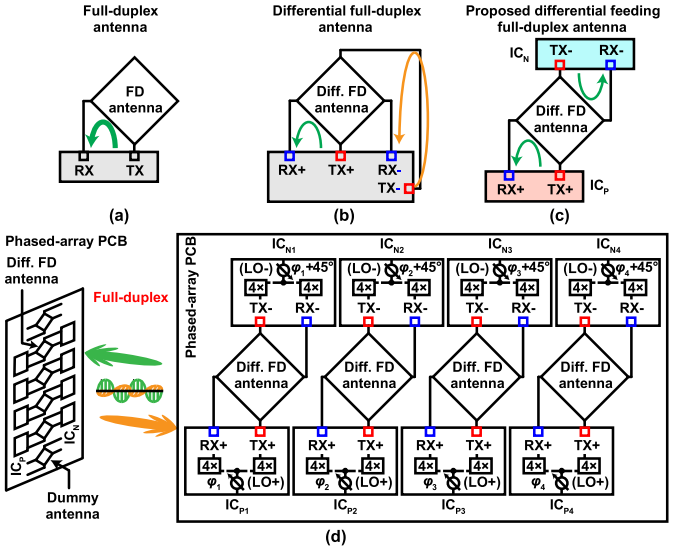


Fig. 2. (a) Single-ended dual-polarized antenna with a large SI signal. (b) Differential feeding dual-polarized antenna with asymmetric TX and RX arrangement. (c) Proposed differential feeding dual-polarized antenna with rotational-symmetric TX and RX arrangement. (d) Proposed sub-THz FD phased-array TRX.

would easily be a magnitude/phase mismatch issue, which would also lead to poor isolation [see Fig. 2(b)]. To solve the signal mismatch, symmetric differential TX and RX signals should be considered. The proposed FD antenna configuration overcomes the above issues by utilizing a rotational-symmetric structure and a pair of chips (IC_P and IC_N) to feed differential signals, as shown in Fig. 2(c). The FD antenna is based on a rotational-symmetric dual-polarized patch antenna. It has four slot coupling angle feedings, whose two parallel TX feedings are orthogonally placed with the other two parallel RX feedings. An on-chip LO generation chain controls the beam steering angle and differential excitations from two separated ICs, as shown in Fig. 2(d). In measurement, the proposed FD antenna could provide high SI on-antenna suppression larger than 35 dB. After adding the RF SI canceller, the total SI suppression could be over 60 dB with a wider 2-GHz bandwidth. The proposed single-ended neutralized mixer achieves 22.6-dB LO feedthrough suppression, which saves the LO chain power and area consumption. The phased-array implementation not only enables beam steering and boosts the antenna gain but also compensates for the large path loss at sub-THz frequencies, making the proposed system much more practical in future 6G communication systems. In OTA measurement, the maximum measured data rate is 6 Gb/s in the FD mode and 112 Gb/s in the TX-to-RX.

This article is organized as follows. Section II describes the design details of the proposed sub-THz FD phased-array transceiver. Section III details the implementation. Section IV presents the measured results. Section V concludes this article.

II. Transceiver Design

Fig. 3 shows the block diagram of the proposed F-band FD phased-array system. The TX integrates two neutralized single-ended mixers, two five-stage RF variable-gain amplifiers (VGAs), and an eight-stage wideband power amplifier (PA). Too large LO leakage causes the gain compression

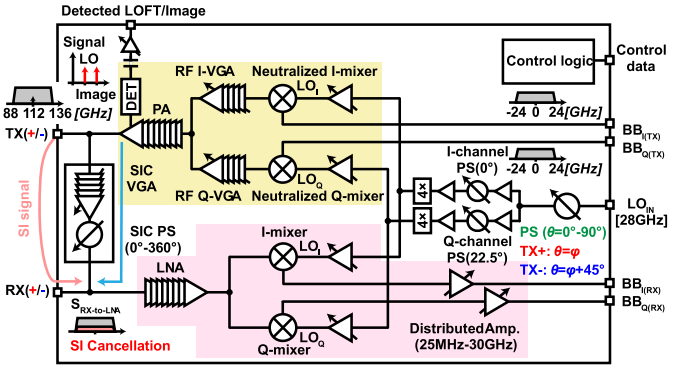


Fig. 3. Block diagram of the proposed Sub-THz TRX.

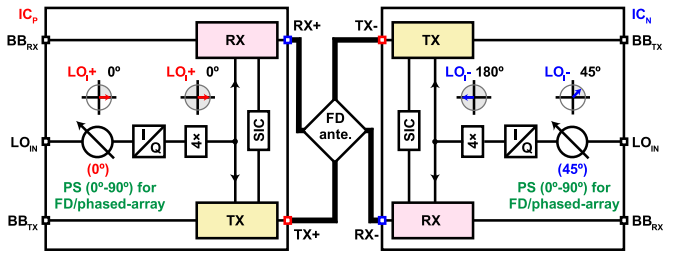


Fig. 4. Beam steering angle and differential feeding signal generation.

in the following RF VGA stage. The proposed neutralized single-ended mixer suppresses LO feedthrough to avoid RF VGA saturation and improves its conversion gain and output power at the 1-dB compression point (OP1dB). Two RF VGAs are connected to the neutralized mixers before I/Q combining to compensate for the I/Q mismatch and improve the isolation between the I/Q channels. A detector is combined with the PA, which checks the LO feedthrough suppression and image rejection. When applying two quadrature single-tone baseband signals with the frequency of ω_{BB} to the TX I/Q inputs, it couples a small portion (around -15 dB) of the PA output to a square-law detector. The detector down-converts the LO leakage to ω_{BB} and the image signal to $2\omega_{BB}$. The circuit design is based on [63] and shifts the frequency to 112 GHz.

The RX includes an eight-stage wideband LNA, two passive single-ended mixers, and two three-stage wideband distributed amplifiers. The wideband distributed amplifier employs a cascode topology [64], whose 3-dB bandwidth is 25 MHz–30 GHz. The LO generation chain comprises three phase shifters (PSs) and two quadruplers [65]. Two switch-type PSs (STPS) with a 22.5° phase difference and two quadruplers generate the 112-GHz LO I/Q signals. An additional 90° range STPS is integrated before two PSs of I/Q channels for the beam steering and differential feeding for IC_P and IC_N. The RF SIC circuit contains a six-stage VGA with a 55-dB gain range and a 360° range STPS with 0.4° phase resolution. The SIC circuit couples a small portion of the PA output, which is magnitude and phase modulated by the SIC VGA and SIC PS, and the calibrated signal is sent to the LNA input for the SIC operation.

A. Beam Steering Angle and Differential Feeding Signal Generation

As shown in Fig. 4, the 90° range STPSs in IC_P and IC_N are used to generate differential signals as well as for realizing

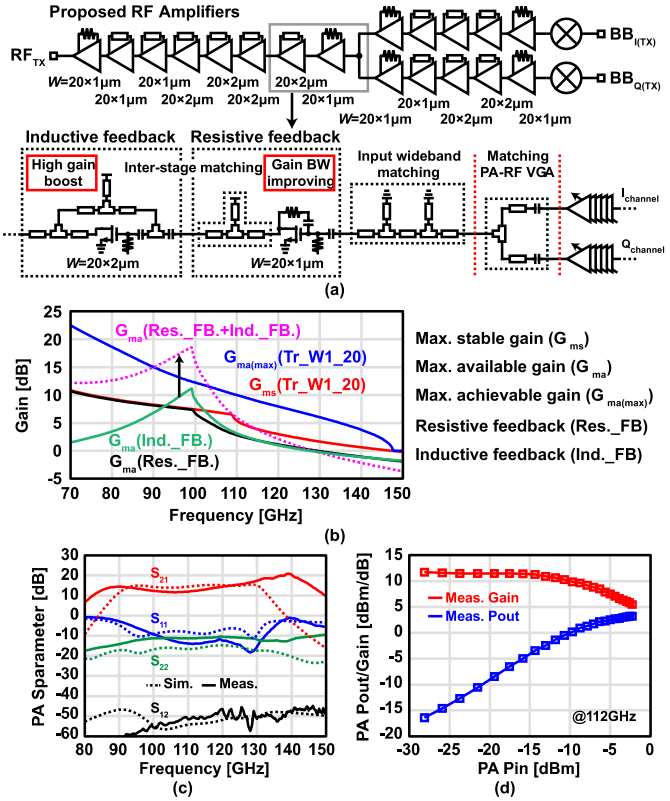


Fig. 5. Proposed wideband RF amplifiers. (a) Circuit design. (b) Maximum available gain analysis. The stand-alone PA TEG (c) simulated and measured S-parameters and (d) measured linearity performance.

phased-array operation. The 90° range is multiplied by the quadrupler, and the 360° range can be obtained, i.e., the differential signal is generated by 45° offset before the quadrupler. The symmetric patch antenna is used for transmitting and receiving differential signals.

B. Wideband RF PA and RF VGA

Wideband amplifiers are essential for supporting large data rate communication. Fig. 5 analyzes the proposed wideband RF amplifiers. For both PA and RF VGAs, a common source topology with resistive feedback at the input and output stages, and a common source topology with inductive feedback at intermediate stages [66], [67], [68] are used. The inductive feedback topology could boost power gain at the millimeter frequency band, which is known as the maximum achievable gain [66]. However, when designing a wideband amplifier, this topology suffers from narrow 3-dB gain–bandwidth characteristics and a small ΔK margin for unconditional stability. As shown in Fig. 5(b), when cascading a common source topology with resistive feedback (black line) and inductive feedback (green line), the combined maximum available gain could be enhanced on a broader frequency range (>0 dB part in the pink line) with the slope decreasing less as frequency increases past the peak power gain point. In Fig. 5(a), the transistor size of 20 μm has a high f_{max} frequency, and it is used in the common source topology with resistive feedback and the common source topology with inductive feedback for boosting gain at the high F-band frequency range. A transistor size of 40 μm is used for boosting at the low

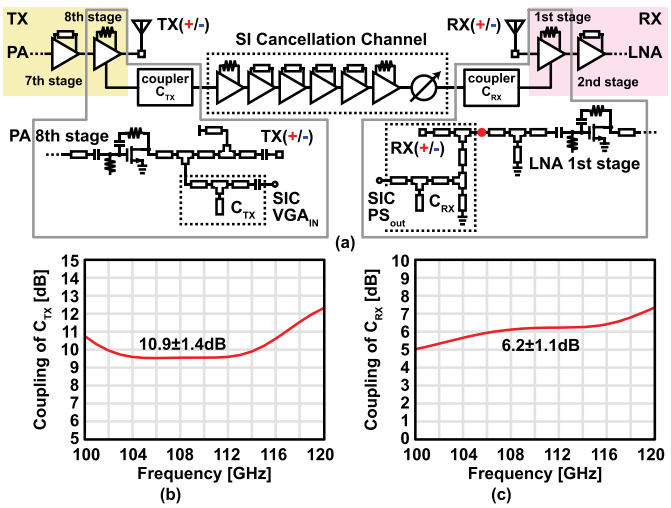


Fig. 6. (a) Design details of the RF SIC channel. The coupling of (b) coupler C_{TX} and (c) coupler C_{RX}.

F-band frequency range. The inter-stage matching circuits are also shown in Fig. 5(a). A stand-alone PA TEG was made to demonstrate the performance. The measured PA gain is higher than 11 dB within the entire F-band [see Fig. 5(c)], and the mismatch between simulation and measurement is likely due to the transistor model inaccuracy over 130 GHz. This is because these two transistors (20 × 1 and 20 × 2 μm) are newly prepared for this design, while the transmission line and capacitors have been used in the W-band and 300-GHz band [65], [69], [70]. Fig. 5(d) shows the proposed RF PA linearity measurement, which achieves a saturated power of 3 dBm at 112 GHz.

C. SIC Channel

Fig. 6(a) shows the design details of the RF SIC channel. Two wideband couplers connect the last stage of PA and the first stage of LNA. Through the coupler C_{TX} [see Fig. 6(b)], a small portion of the TX output signal will be coupled to the SIC channel. After being coupled, the signal magnitude and phase are modulated by the SIC VGA and SIC PS, and the calibrated signal will be coupled to the LNA by the coupler C_{RX} [see Fig. 6(c)] to achieve SIC operation.

1) I/O SIC Channel Port Couplers: The two couplers (C_{TX} and C_{RX}) use open-shunt transmission lines at the output and input matching circuits of the PA and LNA. The transmission lines' lengths are optimized to have a minimal influence on the output and input matching of the PA and LNA. The coupling of the coupler C_{TX} is defined as the power at the PA output port dividing the power at the SIC VGA input port. The coupling of the coupler C_{RX} is defined as the power at the SIC PS output port dividing the power at the red point in Fig. 6(a), which is set before the second short-shunt transmission line at the LNA input. The coupling of the coupler C_{TX} is 10.9 dB, and the coupling of the coupler C_{RX} is 6.2 dB. The 3-dB bandwidth of both couplers is over 20 GHz with a center frequency of 110 GHz.

2) SIC Channel PS: The 360° range STPS details are shown in Fig. 7(a). There is a 5-bit STPS as well as a fine-tuning

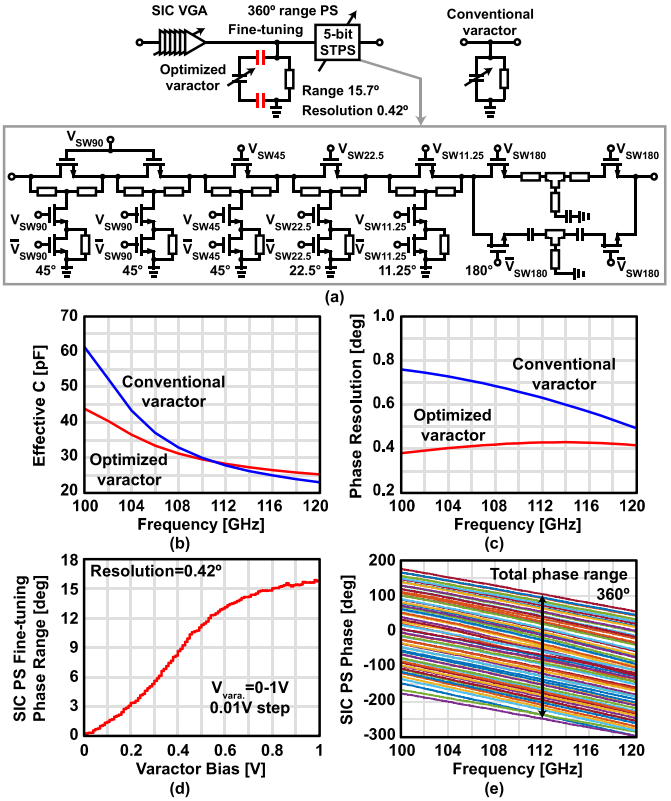


Fig. 7. PS of the SIC channel. (a) Circuit design and optimized varactor topology. (b) Simulated effective capacitance of optimized and conventional varactors. (c) Simulated phase resolution of an LC-based PS by using optimized and conventional varactors. (d) Measured SIC PS fine-tuning stage performance. (e) Measured SIC PS phase range.

stage for resolution improvement. For the 5-bit STPS of the SIC PS, it contains a 90° stage (consisting of two 45° stages), 45°, 22.5°, 11.25°, and 180° stage PS. The fine-tuning stage is connected in series before the 5-bit STPS. The 90° phase change is combined with two 45° STPS for broader bandwidth and better phase linearity. The 180° STPS uses a classical LC–CL network [71], [72]. For the fine-tuning stage, compared with conventional LC-based reflection-type PS topology, the optimized varactor is connected in series with capacitors on both sides, thus decreasing effective varactor capacitance [see Fig. 7(b)]. Therefore, in Fig. 7(c), the phase resolution of an LC-based PS with the optimized varactor has a smaller and more stable wideband phase resolution in simulation when the varactor bias is swept by a 0.01-V step size from 0 to 1 V. Fig. 7(d) shows the measured results of the proposed fine-tuning stage. With the same bias setting in simulation, the fine-tuning stage could cover a 15.7° phase range with a 0.42° phase resolution. It is worth mentioning that the integrated logic controller has a 10-bit digital-to-analog converter, and the bias setting sweep step could be 0.001 V to improve the fine-tuning phase resolution further. The measured total phase range of the SIC PS is shown in Fig. 7(e). The proposed STPS achieves a 360° phase range and 0.42° phase resolution, which is much better than the conventional LC-based PS.

3) SIC Channel VGA: Fig. 8(a) explains the circuit details of the SIC VGA design. It also uses a similar topology as

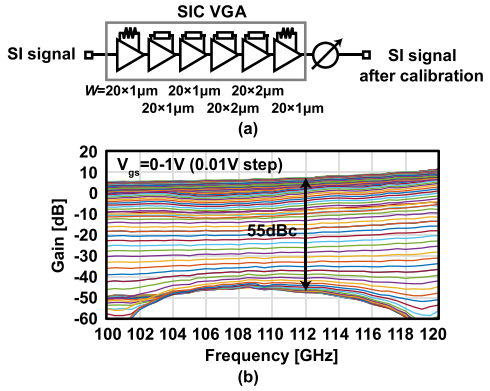


Fig. 8. VGA of the SIC channel. (a) Circuit design. (b) Measured gain tuning range.

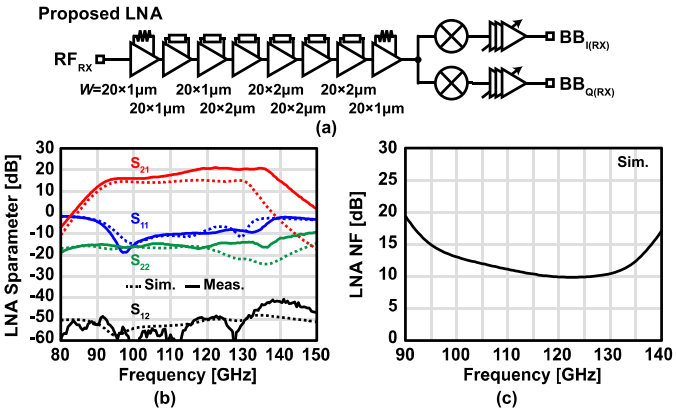


Fig. 9. Wideband LNA. (a) Circuit design. (b) Simulated and measured S-parameters. (c) Simulated NF.

the RF PA and the bias of the transistors is set at the same value. The measured gain range of the SIC VGA is 55 dBc at 112 GHz when the bias sweep step is 0.01 V from 0 to 1 V [see Fig. 8(b)]. Because the integrated logic controller has a 10-bit digital-to-analog converter for bias setting, the gain resolution of the SIC VGA could be improved further if a 0.001-V sweep step is utilized.

D. Wideband RF LNA

The eight-stage RF LNA utilizes the same topology and transistor size as the RF PA, as shown in Fig. 9(a). The difference between them is that the LNA input port matching circuit is optimized for NF and the output port includes an inter-stage matching circuit connected to the RX single-ended mixers and is optimized for conversion gain. Fig. 9(b) shows the measured S-parameters of the LNA. It also maintains a gain higher than 12 dB across the entire F-band. Fig. 9(c) shows the simulated NF, which achieves lower than 15 dB from 95 to 138 GHz.

E. SIC Operation

As we mentioned in the theoretical analysis, the SIC operation should ensure that the SI and SIC signals have the same magnitude and are out-of-phase, which means that the time delay of these signals must also be the same.

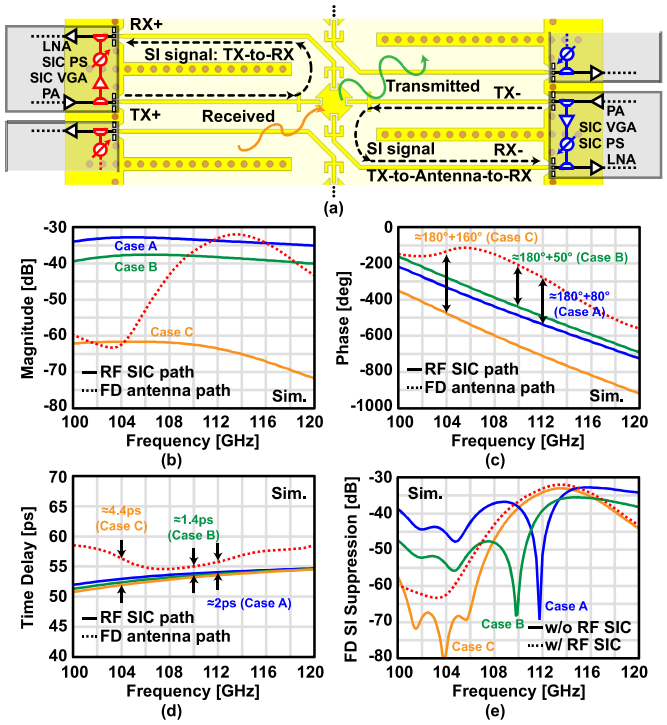


Fig. 10. SI signal calibration in simulation. (a) Diagram for both antenna- and RF-domain SIC. (b) Magnitude, (c) phase, and (d) time delay of the SI and SIC signals with different SIC conditions (Cases A–C). (e) SI suppression when the RF SIC channel is turned on and off with the different SIC conditions (Cases A–C).

In Fig. 10(a), a diagram for the antenna and RF SIC sections is shown, illustrating that the FD antenna's feeding line lengths are optimized. The target SI signal is from the TX to the antenna and, then, the antenna back to the RX. The SI signal passing through the FD antenna path is eliminated at the RX input port by the SI signal passing through the SIC circuit path. Fig. 10(b)–(e) shows the SIC operation based on previously introduced couplers, RF PA, SIC PS, SIC VGA, RF LNA, and the FD antenna. There are several conditions of the SIC channel (Cases A–C) to achieve different frequencies for maximum SIC improvement. The time delay between SI and SIC signals shown in Fig. 10(d) could be compensated by shifting the phase of the SIC PS. Fig. 10(e) shows several simulated SI suppression at the RX input port with the different SIC conditions. When frequencies move away from the desired frequencies, the SIC performance degrades due to the magnitude and phase mismatch increasing between SI and SIC signals. Different SIC conditions are adopted to shift the desired frequencies at 112 GHz (Case A), 110 GHz (Case B), and 104 GHz (Case C).

F. Neutralized Mixer for LO Feedthrough Suppression

In this design, a single-ended mixer is used although it suffers from LO feedthrough due to the significant coupling at these frequencies due to the gate-to-drain capacitance C_{gd}, and as a result, the LO feedthrough saturates the following RF VGA. One way to relieve this would be to use a differential mixer to suppress the LO feedthrough, but it requires a balun and additional buffers to generate differential LO signals, which is area- and power-consuming in the sub-THz region.

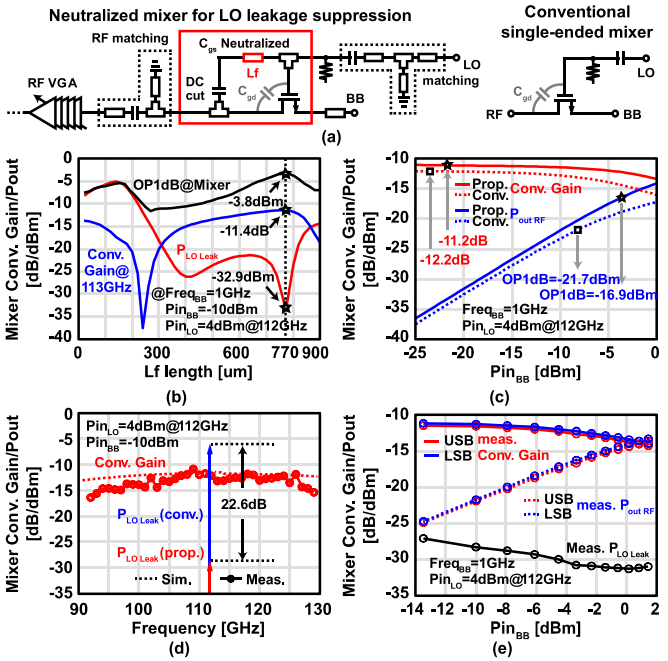


Fig. 11. Proposed neutralized mixer. (a) Circuit design. (b) Simulated LO leakage, conversion gain, and OP1dB by sweeping neutralized transmission line length. (c) Simulated conversion gain and OP1dB of neutralized mixer and conventional single-ended mixer. (d) Measured conversion gain and LO feedthrough suppression. (e) Measured linearity performance.

Thus, a neutralized single-ended mixer is utilized for suppressing LO feedthrough in this work, and the circuit details are shown in Fig. 11(a) [73]. It saves power consumption and chip area compared with the differential mixer. The neutralization is done by connecting a transmission line (length is Lf) between the gate and drain nodes. The transmission line resonates with the gate-to-drain capacitance C_{gd}, which mitigates the LO leakage. To illustrate the design process of the proposed mixer, Fig. 11(b) shows the simulation results of the neutralized mixer LO leakage, conversion gain, and OP1dB with sweeping the transmission line length (Lf). When the transmission line (Lf) resonates with the parasitic capacitor (C_{gd}), the neutralized mixer has the lowest LO leakage, maximum conversion, and highest OP1dB. Compared with a conventional single-ended mixer, when each mixer's ports have comparable return loss (<-10 dB), the proposed neutralized mixer improves conversion gain by around 1 dB and OP1dB by around 4.8 dBm in simulation [see Fig. 11(c)]. The simulation results show that this topology suppresses the LO feedthrough to avoid RF VGA saturation, and the mixer linearity and conversion gain are also improved. Fig. 11(d) and (e) shows the measurement results. When input signal power is -10 dBm, the measured LO feedthrough is 22.6 dB suppressed compared with a conventional single-ended mixer, and the measured proposed mixer conversion gain is -14 dB on average. The measured linearity performance is shown in Fig. 11(e), which is consistent with the simulation results in Fig. 11(c). The LO leakage power level changing with the input signal power is mainly due to large-signal matching and conversion gain compression of the transistor.

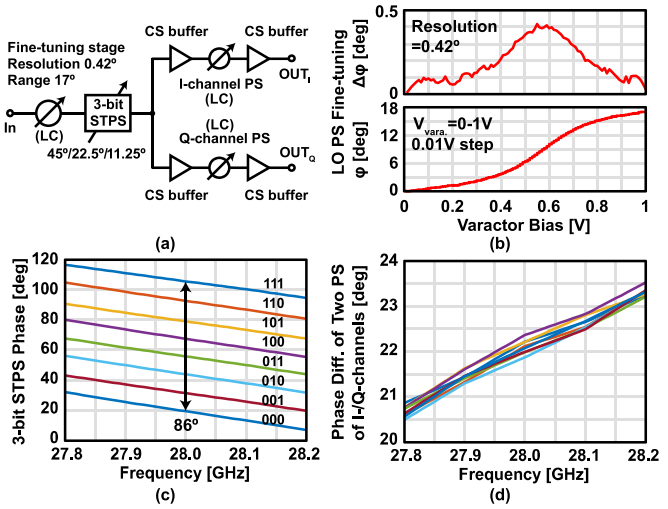


Fig. 12. LO distribution chain and PS of the I/Q channels. (a) Block diagram. (b) Measured fine-tuning stage performance. (c) Measured 3-bit STPS results. (d) Measured phase difference between the two PSs of the I/Q channels.

G. LO Distribution Chain and PSs of the I/Q Channels

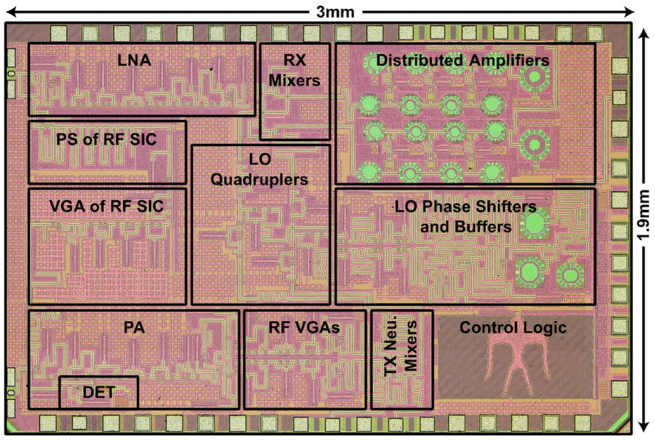
Fig. 12(a) shows the block diagram of the LO distribution chain and PSs of the I/Q channels. First, a 28-GHz LO goes through a 90° range PS. This PS architecture is similar to that of the SIC PS presented earlier, where it includes a fine-tuning stage with an optimized varactor [see Fig. 7(a)] and a 3-bit STPS (45°/22.5°/11.25°). After the first PS, the LO is split into I and Q. To compensate for the splitter insertion loss and increase isolation between the I/Q channels, each channel includes a single-stage common source buffer after the splitter. The same optimized varactor topology is also adopted into the PSs of the I/Q channels. The phase difference between the two PSs is 22.5° and could be finely compensated by tuning the varactor bias. After the two PSs, each channel includes a single-stage common source buffer to enhance the isolation between the PS and the quadrupler. Fig. 12(b) shows the measured fine-tuning stage phase range and resolution of the LO chain. It could cover a total of 17° with 0.4° phase resolution when varactor bias is set a 0.01-V sweep step from 0 to 1 V. Fig. 12(c) shows the measurement results of the 3-bit STPS. The phase range is 86°, which is a little larger than expected one. While combined with the fine-tuning stage, an accurate phase change between 0° to 90° still could be obtained. Fig. 12(d) shows the I/Q phase difference when changing the 3-bit STPS. The measured phase difference is close to 22.5°, and thus, their varactor bias could compensate for the small variation.

III. Board Implementation

The proposed sub-THz FD phased-array chip is fabricated in a 65-nm CMOS process. The total chip area is 5.7 mm^2. Area and power breakdown are also summarized in Fig. 13.

A. FD PCB

The sub-THz FD TRX phased-array PCB consists of parts A–C, as shown in Fig. 14(a). Part B includes the ICs and differential feeding FD antenna array. The differential feeding



	TX	RX	LO	SIC	DET
Area(mm²)	0.93	1.23	0.96	0.39	0.05
P_{DC}(mW)	199	121	198	59	23

Fig. 13. Die micrograph of the proposed sub-THz FD TRX.

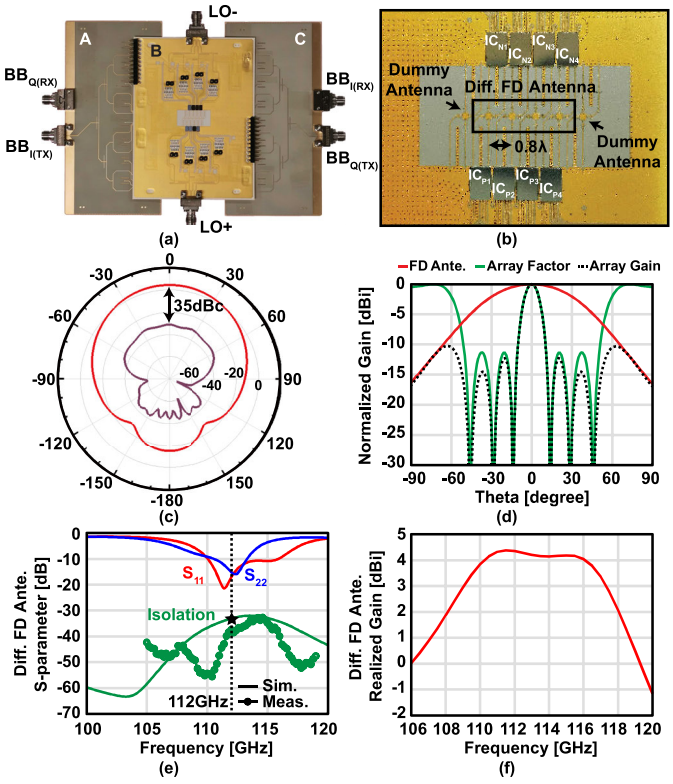


Fig. 14. Performance of the proposed differential-feeding FD antenna. (a) FD PCB implementation photo. (b) Photograph of FD antennas. (c) Simulated cross-radiation results. (d) Expected array gain. (e) Simulated and measured FD antenna S-parameter. (f) Simulated FD antenna realized gain in the frequency domain.

FD antenna is based on the dual-polarized patch antenna. However, the material for the sub-THz FD antenna should be carefully chosen to avoid high loss. Thus, a liquid crystal polymer (LCP) is used to fabricate PCB B in this work due to its small permittivity ($\varepsilon_r = 3.2$) and low-loss tangent coefficient ($\delta = 0.005$) [74]. The LCP layer thickness is chosen as 50 μm, and the PCB surface gold thickness is 18 μm. Parts A and C are dividers and combiners for $BB_{I/Q(TX/RX)}$, respectively. These parts use four layers of metal with a

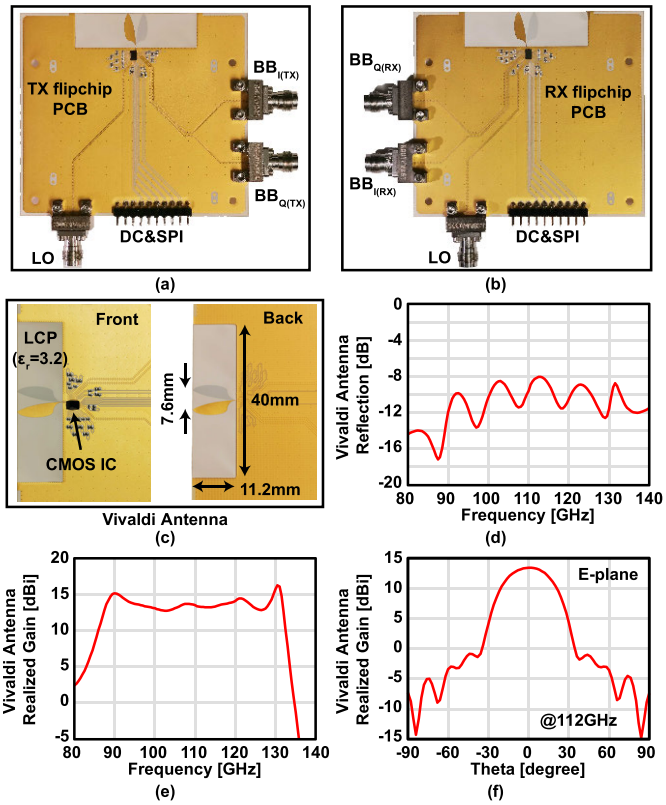


Fig. 15. Vivaldi antenna performance for OTA TX-to-RX measurement. (a) TX and (b) RX PCB. (c) Design details, (d) simulated reflection, (e) realized gain in the frequency domain, and (f) E-plane radiation pattern of the Vivaldi antenna.

Megtron-6 material because the signal frequency is lower than 30 GHz. The signal divider and combiner are designed on both the top and bottom layers of the four-layer Megtron-6 PCB. The dielectric thickness of L1-to-L2 and L3-to-L4 is 100 μm, and the middle dielectric thickness is 750 μm. The surface gold thickness of Megron-6 PCB is 43 μm. The connection between parts A-to-B and part B-to-C adopts the Hirose Electric BM46 multi-RF compatible board-to-board connectors.

Fig. 14(b) illustrates the details of the antenna array. Differential feeding FD antennas are arranged in line with a 0.8λ pitch at 112 GHz and driven by four pairs of chips. Two dummy FD antennas are placed on both sides of the antenna array to decrease radiation pattern mismatch. Fig. 14(c) shows a 35-dBc cross-polarization of the differential feeding FD antenna in simulation, and the expected four-element radiation pattern is simulated in Fig. 14(d). The coupling between the adjacent elements causes a slight degradation in the gain of each element, and hence, the array gain is several decibels lower than the ideal theoretical value. Fig. 14(e) shows the simulated reflection and isolation of the differential feeding FD antenna, and the measured isolation is also consistent with the simulation result. For radiation characteristics in the frequency domain, the 3-dB bandwidth is from 107.5 to 118.5 GHz [see Fig. 14(f)].

B. OTA TX-to-RX PCBs

We also made PCBs to demonstrate the OTA TX-to-RX performance of the proposed system. An on-PCB Vivaldi antenna

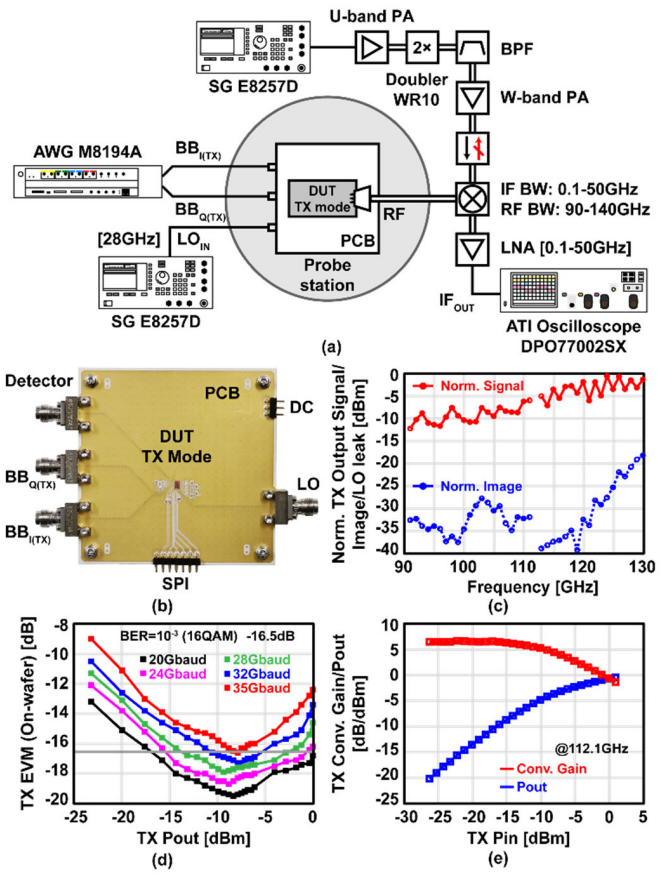


Fig. 16. TX on-wafer measurement results. (a) Setup. (b) TX wire bonding PCB. (c) I/Q mismatch calibration. (d) Measured EVM and data rate. (e) Measured linearity performance.

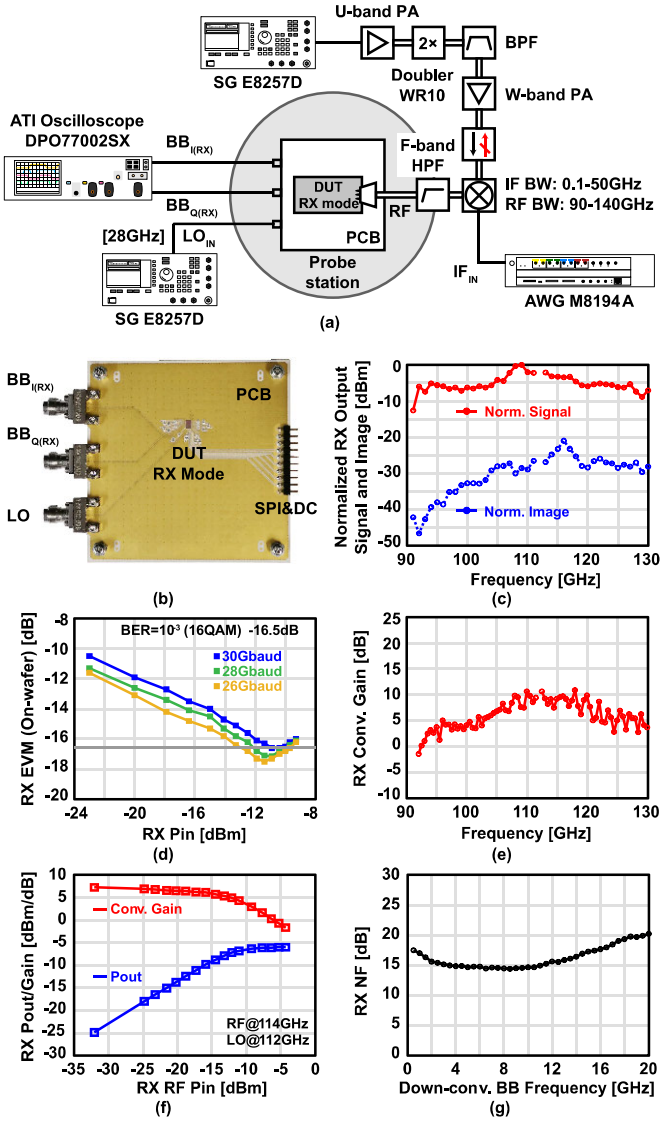


Fig. 17. RX on-wafer measurement results. (a) Setup. (b) RX wire bonding PCB. (c) I/Q mismatch calibration. (d) Measured EVM and data rate. (e) Measured RX conversion gain. (f) RX linearity measurement. (g) RX single-sideband NF.

is used to radiate and receive the modulated signal. The Vivaldi antenna was chosen due to its endfire radiation pattern and wide bandwidth characteristics. Fig. 15(a) and (b) shows the OTA TX-to-RX PCB photographs. Fig. 15(c) explains the design detail of the Vivaldi antenna. The length and width of the Vivaldi are 11.2 and 7.6 mm, respectively. The PCB GND is 20 mm away from the Vivaldi antenna aperture boundary to decrease reflection as much as possible. The chip RF output used gold bumps to connect with the PCB Vivaldi antenna [65]. The simulated reflection of the Vivaldi antenna is shown in Fig. 15(d). The matching degradation, leading to reflection, was caused by the PCB design rules. The simulated bandwidth of the Vivaldi antenna in the E-plane covers the frequency from 86 to 132 GHz with more than 10-dBi realized gain, as shown in Fig. 15(e). The E-plane radiation pattern of the Vivaldi antenna is shown in Fig. 15(f) at 112 GHz.

IV. Measurement

A. On-Wafer TX and RX Measurements

First, the on-chip TX and RX measurements are shown where the TX/RX PCBs were placed on a probe station. All the chip's VDD, GND, IF, and LO pads were connected to the PCB by wire bonding, and the RF was probed with a Formfactor commercial waveguide probe [see Figs. 16(a) and 17(a)].

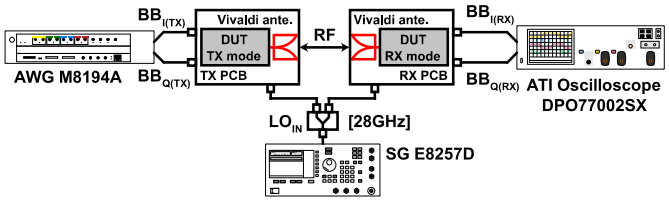
Fig. 16 shows the measured TX performance. The BB I/Q signals are generated by the Keysight arbitrary waveform generator (AWG) M8194A (120 GS/s), and a roll-off factor of 0.35 with the root-raised-cosine filter was used for TX EVM measurement. The LO was generated by an external Keysight signal generator (E8257D) at 28 GHz. An SAGE single-ended mixer with custom design was connected to the TX RF output through an F-band probe for the external down-conversion. The mixer's RF frequency range was 90–140 GHz, and the IF frequency range was 0.1–50 GHz. The LO of the external mixer was set at 88 GHz (44 GHz × 2), and a bandpass filter only selected the second harmonic of the doubler. The down-converted signal was amplified by a B&Z wideband LNA and observed using the Tektronix DPO77002SX oscilloscope (200 GS/s). Fig. 16(b) shows the TX photograph. The TX I/Q mismatch was calibrated before the EVM measurement by changing the gain of RF VGA and the phase between two PSs of the I/Q channels in the

LO chain [75]. Fig. 16(c) shows the normalized desired and image signal power at the TX output. After calibration, the image signal kept a low power level for the desired signal. The measured EVM results are shown in Fig. 16(d). The maximum data rate for on-wafer TX was 140 Gb/s in 16QAM (EVM is −16.7 dB and $\alpha = 0.35$ with the root-raised-cosine filter). Fig. 16(e) shows the linearity measurement results of the TX. A VDI Power Meter (PM5) replaced the external down-conversion part for this measurement. According to the measured results, the input power of the 1-dB point of the PA was −12 dBm in Fig. 5(d), and the OP1dB of the neutralized mixer was −17.2 dBm (LSB) and −17.5 dBm (USB) in Fig. 11(e); thus, the neutralized mixer was compressed earlier than the PA in the TX chain. The measured TX saturated power was around 0 dBm. However, the RF PA was not saturated, and the output power may be limited due to the output power of the on-chip neutralized mixer, according to the simulation.

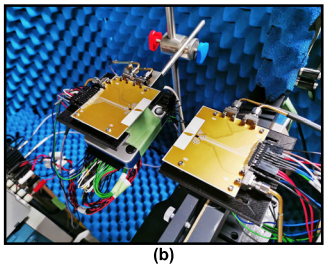
The measured RX on-wafer results are shown in Fig. 17. For this measurement, the external customer-designed SAGE single-ended mixer generated the RX input signal. The LO of the external mixer was kept at the same frequency of 28 GHz, and an additional high-pass filter was added between the external mixer output port and the F-band waveguide probe to suppress undesired spurs. The Keysight AWG M8194 provided an IF signal from 0.1 to 45 GHz to the external mixer. The RX PCB down-conversion BB signals were connected to the Tektronix DPO77002SX oscilloscope for demodulation. The RX test setup is shown in Fig. 17(a), and the RX PCB photograph is shown in Fig. 17(b). Similar to the TX on-wafer measurement, the I/Q mismatch was calibrated first. The RX I/Q mismatch was calibrated by changing the gain of two distributed amplifiers and the phase between two PSs of the I/Q channels in the LO chain [75]. Fig. 17(c) shows the normalized desired signal and the image signal power level. The image signal was also suppressed at a low level. The measured EVM results are shown in Fig. 17(d). The maximum data rate for on-wafer RX is 120 Gb/s in 16QAM (EVM is −16.6 dB and $\alpha = 0.35$ with the root-raised-cosine filter). Fig. 17(e) shows the measured RX conversion gain, which shows a value of around 5 dB. Fig. 17(f) shows the linearity measurement results of the RX. An SAGE D-band quadrupler replaced the external up-conversion part as the RX input signal. Using Keysight PNA-X (N5247B), the folded single-sideband NF of the RX is shown in Fig. 17(g).

B. OTA TX-to-RX Measurement

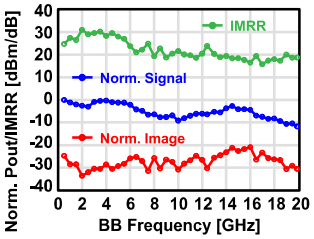
Next, Fig. 18 shows the details of the OTA TX-to-RX measurement. TX and RX PCB shared the same LO signal (28 GHz) by a power splitter and a signal generator (E8257D). The TX input BB ports were connected to the Keysight AWG for I/Q signals excitation, and the RX output BB ports were connected to the Tektronix DPO77002SX oscilloscope for demodulation [see Fig. 18(a)]. The measurement photograph is shown in Fig. 18(b). The TRX image response rejection radio (IMRR) was calibrated by the same I/Q mismatch calibration method of the on-wafer TX and RX measurement. The IMRR was almost larger than 20 dB from 92 to 132 GHz.



(a)



(b)



(c)

Link distance	5cm		2cm	
Modulation	QPSK	16QAM	QPSK	16QAM
TX-to-RX data rate	32Gb/s	64Gb/s	56Gb/s	112Gb/s
Constellation	TX-to-RX EVM = -16.5dB	TX-to-RX EVM = -16.5dB	TX-to-RX EVM = -16.6dB	TX-to-RX EVM = -16.6dB

(d)

Fig. 18. OTA TX-to-RX measurement. (a) Setup and (b) photograph. (c) I/Q mismatch calibration. (d) Measured EVM and constellation.

Fig. 18(d) summarizes the OTA EVM measurement results using a roll-off factor of 0.25 with the root-raised-cosine filter. When the baseband signal is 28 Gbaud, the maximum data rate is 112 Gb/s in 16QAM (EVM is −16.6 dB). Corresponding to the on-wafer TX and on-wafer RX measurements, when a 28-Gbaud baseband signal was used, their minimum achieved EVM were −17.9 and −17.1 dB, respectively. As for EVM limitation factors, the measured IMRR was frequency-dependent, and it would be the limitation factor to achieve lower than −20 dB EVM when using a large baud rate signal.

C. OTA FD Measurement

For the FD phased-array PCB, a beam pattern measurement was performed, as shown in Fig. 19. It was performed in an anechoic chamber to avoid the reflection from nearby instruments or metals influencing the beam patterns. The measurement setup is shown in Fig. 19(a). The AWG generated I/Q BB signals at 1 GHz. The signals were then down-converted by the external mixer to 23 and 25 GHz, which were observed by the oscilloscope. Fig. 19(b) shows the photograph of this measurement. The background calibrations for the I/Q mismatch within a chip and the mismatch between two separate chips were done before beam pattern measurement. The I/Q mismatch calibration was the same as that of on-wafer TX. The leakage signal from the differential signals of TX+ and TX− to the RX chain was observed for detecting the mismatch between TX+ and TX−. For a double check, an external down-conversion for measuring the mismatch between TX+ and TX− was used. In the measurement, the phase difference between the TX+ and TX− could be calibrated within

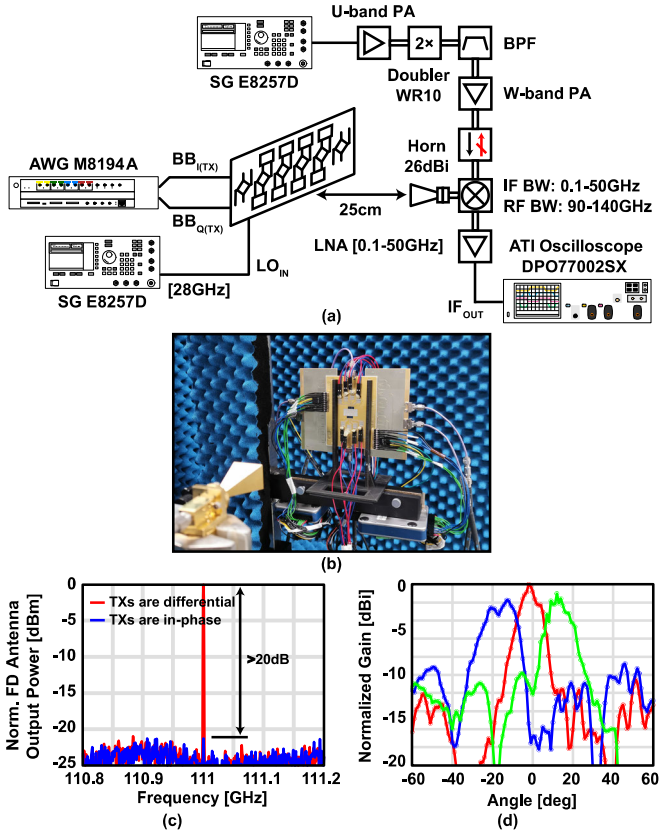
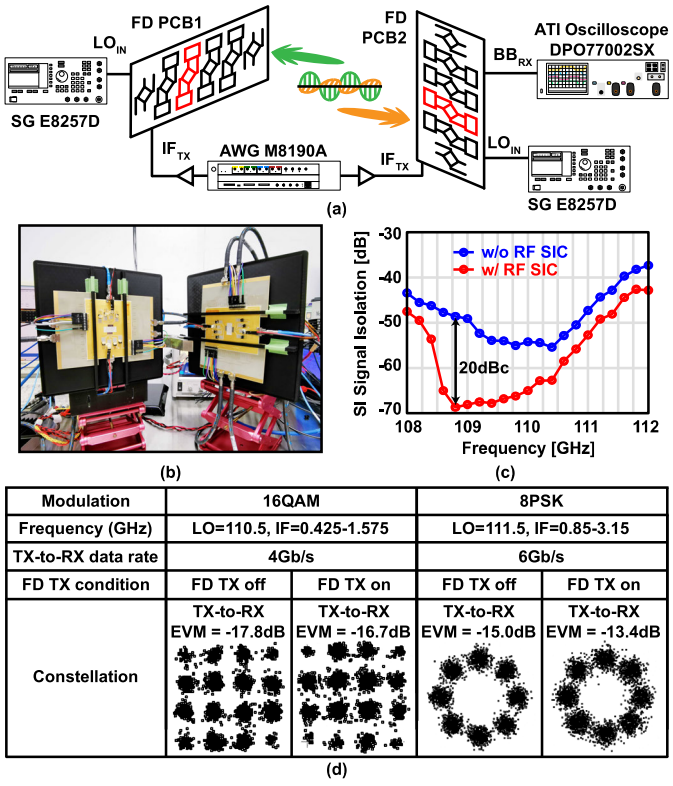


Fig. 19. Beam pattern measurement for proposed FD TRX. (a) Setup and (b) photograph. (c) Normalized FD antenna output power when connected TXs of IC_P and IC_N are differential and in-phase states after calibration. (d) Measured beam pattern for $-13°$, $0°$, and $+13°$ main-beam direction.



Modulation	16QAM		8PSK	
Frequency (GHz)	LO=110.5, IF=0.425-1.575		LO=111.5, IF=0.85-3.15	
TX-to-RX data rate	4Gb/s		6Gb/s	
FD TX condition	FD TX off	FD TX on	FD TX off	FD TX on
Constellation	TX-to-RX EVM = -17.8dB	TX-to-RX EVM = -16.7dB	TX-to-RX EVM = -15.0dB	TX-to-RX EVM = -13.4dB

(d)

Fig. 20. FD OTA measurement. (a) Setup and (b) photograph. (c) SI suppression when the RF SIC circuit is turned on and off. (d) Measured EVM and constellation.

$180° \pm 1.7°$ by adjusting magnitude and phase calibration. The $180°$ offset between two TXs could be controlled by the $45°$ stage of the $90°$ range STPS in the LO chain, and the phase calibration was for realizing the fine phase calibration to make the signal of TXs be in phase first. The FD antenna requires differential feeding signals, and the output power reaches the minimum when the feeding signals are in phase. By changing the gain of RF PA and the phase of $90°$ range STPS in the LO chain, the magnitude and phase mismatch between two TXs of IC_P and IC_N could be calibrated. In measurement, the phase resolution of the fine-tuning stage was $0.42°$ and became $1.7°$ after the quadrupler multiplication. In Fig. 19(c), after calibrating the mismatch between two chips, the FD antenna output power difference was over 20 dB for in-phase and differential states between the TX+ and TX−. The beam pattern was measured for $-13°$, $0°$, and $+13°$ main-beam direction. The array antennas were placed in 0.8λ pitch, so PSs were configured with $+90°$ phase steps for each adjacent IC in case of the $13°$ direction.

A single-path FD link was evaluated over 1.5 cm using a 1-Gbaud 16QAM signal in Fig. 20. As shown in Fig. 20(a), using two FD TRXs (PCB1 and PCB2), PCB1 was configured as TX for generating the target modulated signal ($\alpha = 0.15$ with the root-raised-cosine filter), and PCB2 was configured as FD RX. To test the functionality of the SIC circuit, PCB2 also transmitted a dummy modulated signal with the same bandwidth and frequency range so that the dummy transmitting spectrum completely overlapped with the received signal spectrum. For the SIC measurement, only one element in each PCB was turned on, and heterodyne architecture was chosen to observe SIC performance easily. The LO and IF frequencies were shifted according to the SIC conditions and baud rates. In the measurement, the SI signal passing the FD antenna (TX-to-Antenna-to-RX) was dominant rather than the SI signal from the TX-to-RX port. Similar to the simulation results in Fig. 10(e), the measurement results show that the SIC circuit is able to improve the SI signal suppression as the SI signal isolation decreased by 20 dB when FD PCB2 turned on its RF SIC circuit. The measured TX-to-RX EVM was -17.8 dB in 16QAM without the dummy transmitting signal, and the EVM became -16.7 dB after the dummy transmitting signal was turned on. The EVM degradation was only 1.1 dB, thanks to the proposed architecture. 8PSK also evaluated it, and the maximum date rate was 6 Gb/s. The measured EVMs were -15.0 and -13.4 dB before and after the dummy TX signal was turned on, respectively.

The SIC calibration was done before the SIC EVM measurement. It was not very stable due to the temperature drift, and background calibration should be applied in a real use case [78]. For supporting a larger die-to-die process variation, the calibration range for SIC should be wider even though this might cause a larger layout area and higher power consumption. The present SIC circuit focuses on canceling the SI signal from the same antenna transmitter. A careful antenna design is required to minimize the antenna-to-antenna coupling for supporting the FD operation.

TABLE I
COMPARISON WITH STATE-OF-THE-ART FD AND SUB-THz TRANSCEIVERS

	Full-duplxing					Sub-THz TRX/TX		
	This work	JSSC 2016 [20]	JSSC 2018 [60]	ISSCC 2018 [34]	JSSC 2020 [62]	ISSCC 2022 [76]	ISSCC 2022 [77]	ISSCC 2018 [70]
Technology	65nm CMOS	45nm SOI CMOS	45nm SOI CMOS	40nm LP CMOS	65nm CMOS	130nm SiGe BiCMOS	22nm FinFET	65nm CMOS
RF freq. [GHz]	88-136	57-66	60-75	1.6-1.9	28/37	130-164	140‡	70-105
Modulation	16QAM	BPSK	16QAM	64QAM	64QAM	64QAM	16QAM	16QAM
Integration	Transceiver	Transceiver	RF blocks	Transceiver	RF blocks	Sep. TX+RX	TX	TRX
Antenna	Single antenna	Two separated antennas	Single antenna	N/A##	N/A##	N/A††	N/A††	N/A††
Structure	Phased-array	Single-element	Single-element	Single-element	Single-element	Phased-array	Single-element	Single-element channel comb.
Full-duplex mode data rate [Gb/s]	6	1	4	0.48†	1.5/1.5†	N/A††	N/A††	N/A††
OTA TX-to-RX data rate [Gb/s]	112	5	N/A*	N/A*	1.5/1.5†	30	160	60+60
SI suppression [dB]	>60@ 108.5-110.5GHz	>70@59GHz	>60@63-65GHz, 65-66GHz, 71.7-72.3GHz	>65@ 1.73-1.81GHz	>75@ 27.2-27.5GHz	N/A††	N/A††	N/A††
P_{DC} [W]	TX: 0.20 RX: 0.12	TX: 0.21 RX: 0.11	TX: 0.30** RX: 0.11	TRX: 0.12	TX: 0.12 RX: 0.04	TX: 0.26 RX: 0.2	TX: 0.17	TX: 0.12 RX: 0.16
Chip area [mm²]	5.7	4.42	7.29#	4	1.05	TX: 4.46 RX: 4.46	TX: 4	6

* No half-duplex measurement. ** Calculated by TX P_{sat} and PAE_{max}. # RF blocks + on-chip antenna. ‡ Center frequency.
Without antenna integration. † No OTA measurement. †† No full-duplex mode and SIC.

V. CONCLUSION

This work presented the first reported sub-THz FD phased-array TRX and was implemented in a 65-nm CMOS process. To achieve FD operation, a differential feeding FD antenna and an SIC circuit are implemented. In measurement, without any digital-domain SIC, the SI signal achieves over 60-dB suppression with a wider 2-GHz bandwidth. Measurements show that when the SIC is turned on, the SI suppression is improved by 20 dB. In addition, the EVM only degraded by 1.1 dB when turning on the TX mode of the receiving side of the FD TRX (1 Gbaud in 16QAM). The on-wafer TX and RX also achieve a maximum of 140- and 120-Gb/s data rate, respectively. Table I shows a comparison of this work to other state-of-the-art works. It shows that this is the first FD phased-array TRX over 100 GHz with the highest data rate by achieving 6 Gb/s in 8PSK. The SIC is fairly competitive to the other state-of-the-art, lower frequency FD works, especially when taking into account that we are operating almost at twice the frequency. In addition, the table shows that this work's 112-Gb/s TX-to-RX data rate is one of the fastest among sub-THz phased-array TRX. Thus, this work paves the way for future sub-THz communication systems that require high data rates by demonstrating a sub-THz FD TRX system.

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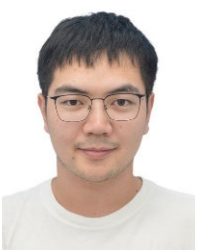
Chun Wang (Graduate Student Member, IEEE) received the B.E. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2015, and the M.E. degree from Zhejiang University, Hangzhou, China, in 2018. He is currently pursuing the Ph.D. degree in electrical and electronic engineering with the Tokyo Institute of Technology, Tokyo, Japan, focusing on millimeter-wave front end and system design.

His research interests include CMOS RF/sub-THz/THz transceivers, phased-array transceivers, device modeling, and wireless communication systems.

Ibrahim Abdo (Member, IEEE) received the B.Sc. degree in electronics engineering from Princess Sumaya University for Technology (PSUT), Amman, Jordan, in 2014, and the M.E. degree in physical electronics and the Ph.D. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2017 and 2021, respectively.

He is currently a Researcher with NTT Device Technology Laboratories, NTT Corporation, Atsugi, Japan, where he is engaged in the research and development of monolithic microwave integrated circuits (MMICs) for ultra-high-speed wireless communications. His research interests include high-data-rate millimeter-wave/sub-terahertz wireless transceiver circuit design and phased-array implementation.

Dr. Abdo was a recipient of the Japanese Government (MEXT) Scholarship, the IEEE SSCS Predoctoral Achievement Award from 2021 to 2022, and the Seiichi Tejima Doctoral Dissertation Award. He serves as a reviewer for IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) and IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (TMTT).



Chenxin Liu (Graduate Student Member, IEEE) received the B.E. degree from the Nanjing University of Science and Technology, Nanjing, China, in 2019, and the M.E. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2021, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering.

His research interests include millimeter-wave wireless communication system designs.

Carrel da Gomez (Graduate Student Member, IEEE) received the B.Sc. degree in electrical engineering from the Institut Teknologi Bandung, Bandung, Indonesia, in 2017, and the M.Eng. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2020, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering.

His research interests include CMOS millimeter-wave and sub-terahertz integrated circuits for wireless communication and radar.

Mr. da Gomez was a recipient of the Japanese Government (MEXT) Scholarship in 2018.

Jill Mayeda (Member, IEEE) received the B.Sc. degree in applied and computational mathematical sciences from the University of Washington, Seattle, WA, USA, in 2014, and the Ph.D. degree in electrical engineering from Texas Tech University, Lubbock, TX, USA, in 2022.

She has spent seven years in the industry working at Noise Figure Research from 2015 to 2022. She is currently a Post-Doctoral Researcher with the Tokyo Institute of Technology, Tokyo, Japan, with a research focus on CMOS satellite communication transceivers. Her research interests include mm-wave PA design using CMOS, HBT, and III–V technologies, and CMOS mm-wave transceiver designs.

Dr. Mayeda received the Best Ph.D. Student Award from Texas Tech University in 2022.

Hans Herdian (Graduate Student Member, IEEE) received the B.Sc. degree from the Bandung Institute of Technology, Bandung, Indonesia, in 2016, and the M.S. degree from the Tokyo Institute of Technology, Tokyo, Japan, in 2018, where he is currently pursuing the Ph.D. degree.

His research interests include on-chip passive components characterization and performance enhancement on the CMOS process for mm-Wave applications.

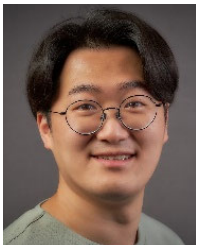
Wenqian Wang (Student Member, IEEE) was born in Xuancheng, China. He received the B.Eng. degree from the School of Microelectronics, Xidian University, Xi'an, China, and the master's degree from the Tokyo Institute of Technology, where he is currently pursuing the Ph.D. degree.

His research interests include analog and mixed-signal circuits and frequency synthesizers.

Xi Fu (Member, IEEE) received the B.E. degree (Hons.) from the Dalian University of Technology, Liaoning, China, in 2017, and the M.E. and Ph.D. degrees from the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology (Tokyo Tech), Tokyo, Japan, in 2019 and 2022, respectively.

He is currently a Post-Doctoral Researcher at the Tokyo Institute of Technology. His research interests are CMOS radio frequency (RF)/millimeter-wave/terahertz/analog transceivers, phased-array transceivers, mixed-signal systems, 5G/6G mobile systems, device modeling, and satellite communication systems.

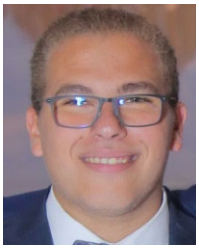
Dr. Fu was a recipient of the Japanese Government [the Ministry of Education, Culture, Sports, Science, and Technology of Japan (MEXT)] Scholarship, the IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award in 2023, the RFIC Symposium Best Paper Award in 2019, the IEEE International Solid-State Circuits Conference (ISSCC) Student-Research Preview Poster Award in 2022, and the IEEE SSCS Student Travel Grant Award in 2022. He serves as a reviewer for IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (TMTT), IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (TVLSI), IEEE SOLID-STATE CIRCUITS LETTERS (SSC-L), and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS and TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS (TCSI and TCSII).



Dongwon You (Student Member, IEEE) received the B.S. degree in electrical and computer engineering from Ajou University, Suwon, South Korea, in 2017, and the M.S. and Ph.D. degrees in electrical and electronic engineering from the Tokyo Institute of Technology (Tokyo Tech), Tokyo, Japan, in 2019 and 2023, respectively.

He is currently a Post-Doctoral Researcher at the Tokyo Institute of Technology. His research interests include CMOS RF/millimeter-wave/analog transceiver systems, MIMO, mixed-signal, wireless communication, phased-array systems, and satellite communication.

Dr. You was a recipient of the IEEE SSCS Student Travel Grant Award in 2022, the Best Student Paper Award (First Place) at the 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), and first place in the IEEE Microwave Theory and Techniques Society MTT-Sat Challenge in 2023. He also serves as a reviewer for IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, and *IEEE Microwave Magazine*.



Abanob Shehata (Graduate Student Member, IEEE) was born in Milan, Italy, in 1994. He received the B.Sc. degree in electronics engineering and the M.Sc. degree (cum laude) in electronics engineering from the Politecnico di Milano, Milan, in 2017 and 2020, respectively, and the M.E. degree from the Tokyo Institute of Technology, Tokyo, Japan, 2022, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering.

His research interests include mixer and power amplifier design for mm-wave and 300-GHz CMOS transceivers for beyond 5G applications.

Sunghwan Park received the B.E. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2023, where he is currently pursuing the M.E. degree in electrical and electronic engineering.

His research interests include CMOS RF/ sub-THz/analog transceiver systems, phased array, MIMO, device modeling, wireless communication, and 6G.

Mr. Park was a recipient of the Japanese and Korean Government Scholarship.

Yun Wang (Member, IEEE) received the B.S. and M.S. degrees from the University of Electronic Science and Technology of China, Chengdu, China, in 2011 and 2014, respectively, and the Ph.D. degree in physical electronics from the Tokyo Institute of Technology, Tokyo, Japan, in 2019.

He was an Intern with the Pohang University of Science and Technology, Pohang, South Korea, in 2013, and Device Technology Laboratories, NTT Corporation, Atsugi, Japan, in 2016. From 2019 to 2021, he was a Researcher with the Tokyo Institute of Technology. He is currently a Research Associate Professor at Fudan University, Shanghai, China. His research interests include CMOS radio frequency (RF)/millimeter-wave wireless systems, 5G phased-array mobile systems, and satellite communication.

Dr. Wang was a recipient of the IEICE Best Paper Award in 2018, the Best Student Paper Award (First Place) at the 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), and the Seiichi Tejima Research Award in 2021.

Jian Pang (Member, IEEE) received the bachelor's and master's degrees from Southeast University, Nanjing, China, in 2012 and 2014, respectively, and the Ph.D. degree from the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, in 2019.

From 2019 to 2020, he was a Post-Doctoral Researcher at the Tokyo Institute of Technology. From 2020 to 2022, he was a Special-Appointed Assistant Professor with the Tokyo Institute of Technology, where he is currently a Special-Appointed Associated Professor focusing on 5G millimeter-wave systems. His research interests include high-data-rate low-cost millimeter-wave transceivers, power-efficient power amplifiers for 5G mobile systems, multiple-in–multiple-out (MIMO), and mixed-signal calibration systems.

Dr. Pang was a recipient of the IEEE SSCS Student Travel Grant Award in 2016, the IEEE SSCS Pre-Doctoral Achievement Award from 2018 to 2019, the Seiichi Tejima Oversea Student Research Award in 2020, and the IEEE MTT-S Japan Young Engineer Award in 2021.

Hiroyuki Sakai (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Osaka University, Osaka, Japan, in 1984 and 1986, respectively, and the Ph.D. degree from the University of Fukui, Fukui, Japan, in 2020.

In 1986, he joined the Semiconductor Research Center, Matsushita Electric Industrial Company Ltd., Osaka, and engaged in research and development of high-speed GaAs digital ICs, GaAs RF ICs for very compact cellular phones. In 1993, he started to research and develop millimeter-wave devices and their ICs, which resulted in the invention of a new millimeter-wave IC concept named millimeter-wave flip-chip IC (MFIC). From 1998 to 2000, he visited Stanford University, Stanford, CA, USA, as a Visiting Scholar, and expanded his research subjects to new Si-based RF devices and their integration technologies. From 2012 to 2017, he continued his research on mm-wave ICs based on GaAs, GaN, Si-BiCMOS, and CMOS LSI technologies at some laboratories of Panasonic Corporation. In 2020, he joined the Tokyo Institute of Technology, Tokyo, Japan, as a Creative Manager of Open Innovation Platform, where he is currently a Specially Appointed Professor of Electrical and Electronic Engineering.

Prof. Sakai served as a Secretary for the IEEE Electron Devices Society Kansai Chapter from 2002 to 2003. He was a member of the Technical Program Committee of IEEE International Solid-State Circuit Conference (ISSCC) from 2002 to 2008.

Atsushi Shirane (Member, IEEE) received the B.E. degree in electrical and electronic engineering and the M.E. and Ph.D. degrees in electronics and applied physics from the Tokyo Institute of Technology, Tokyo, Japan, in 2010, 2012, and 2015, respectively.

From 2015 to 2017, he was with Toshiba Corporation, Kawasaki, Japan, where he developed an 802.11ax Wireless LAN RF transceiver. From 2017 to 2018, he was with Nidec Corporation, Kawasaki, where he researched intelligent motors with wireless communication. He is currently an Associate Professor at the Laboratory for Future Interdisciplinary Research of Science and Technology, Institute of Innovative Research, Tokyo Institute of Technology. His research interests include RF CMOS transceivers for the IoT, 5G, satellite communication, and wireless power transfer.

Dr. Shirane has been a member of the Technical Program Committee of IEEE International Solid-State Circuits Conference Student Research Preview since 2019. He is a member of the IEEE Solid-State Circuits Society and the Institute of Electronics, Information and Communication Engineers (IEICE).

Kenichi Okada (Fellow, IEEE) received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively.

From 2000 to 2003, he was a Research Fellow of the Japan Society for the Promotion of Science at Kyoto University. In 2003, he joined the Tokyo Institute of Technology, Tokyo, Japan, as an Assistant Professor, where he is currently a Professor of electrical and electronic engineering. He has authored or coauthored more than 500 journals and conference papers. His research interests include millimeter-wave and terahertz CMOS wireless transceivers for 20/28/39/60/77/79/100/300 GHz for 5G, WiGig, satellite and future wireless systems, digital PLL, synthesizable PLL, atomic clock, and ultra-low-power wireless transceivers for Bluetooth low energy, and sub-GHz applications.

Prof. Okada is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), the Information Processing Society of Japan (IPSJ), and the Japan Society of Applied Physics (JSAP). He was a recipient or co-recipient of the Ericsson Young Scientist Award in 2004, the Asian Solid-State Circuits Conference (A-SSCC) Outstanding Design Award in 2006 and 2011, the ASP-DAC Special Feature Award in 2011, the Best Design Award in 2014 and 2015, the MEXT Young Scientists' Prize in 2011, the JSPS Prize in 2014, the Suematsu Yasuharu Award in 2015, the MEXT Prizes for Science and Technology in 2017, the RFIT Best Paper Award in 2017, the IEICE Best Paper Award in 2018, the Radio Frequency Integrated Circuits Symposium (RFIC) Symposium Best Student Paper Award in 2019, the IEICE Achievement Award in 2019, the DOCOMO Mobile Science Award in 2019, the IEEE/ACM ASP-DAC Prolific Author Award in 2020, the Kenjiro Takayanagi Achievement Award in 2020, the KDDI Foundation Award in 2020, the IEEE CICC Best Paper Award in 2020, the IEEE International Solid-State Circuits Conference (ISSCC) Author-Recognition Award in 2023, and more than 50 other international and domestic awards. He is/was a member of the Technical Program Committee of IEEE ISSCC, VLSI Circuits Symposium, European Solid-State Circuits Conference (ESSCIRC), RFIC, and A-SSCC. He is/was a Guest Editor and an Associate Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), an Associate Editor of IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (T-MTT), and a Distinguished Lecturer of the IEEE Solid-State Circuits Society (SSCS).