An Area-Efficient Smart Temperature Sensor Based on a Fully Current Processing Error-Feedback Noise-Shaping SAR ADC in 180-nm CMOS

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***Abstract*— This article presents a bipolar junction transistor (BJT)-based smart temperature sensor employing a noise-shaping successive-approximation-register (SAR) analog-to-digital converter (ADC). This approach, never explored before within a temperature sensing system, was chosen to exploit the low energy/conversion benefit peculiar to SAR-based solutions while overcoming their quantization-dominated resolution with an error-feedback technique. In addition, the system features a complete current-mode architecture enabling op-amp less signal processing and resulting in a highly compact design. Developed and fabricated in a standard 180-nm CMOS process, the sensor exhibits an active area of 0.057 mm^2 and draws a 34-μA total current from a 1.8-V supply. Experimental results in the −50 °C to 110 °C sensing range demonstrate a 92-mK resolution in a conversion time of 80 μs.**

***Index Terms*— CMOS, current mode, noise-shaping successive approximation register (SAR), smart temperature sensor.**

I. Introduction

ON-CHIP temperature data are needed in many applications in the current technology market, ranging from microprocessors [1], [2], [3] to microsensors [4], [5], [6], [7], power management circuits [8], and biomedical devices [9], [10], [11]. Being able to measure and digitize the local temperature of integrated circuits (ICs) has become of paramount importance in the last decade according to the world's trend toward an increased use of smart and connected systems, commonly requiring temperature-adaptive performance [12]. Within this scenario, this article presents a smart temperature sensor designed for the thermal compensation needed in MEMS accelerometers and gyroscopes used in state-of-the-art motion sensing systems; indeed, a first-order thermal drift suppression is a primary requirement for these devices to achieve competitive performance [13], [14], [15], [16], [17], [18].

This application leads to a couple of fundamental requirements for the temperature compensation IC. First, since the considered motion sensing systems are typically included in portable and therefore battery-powered devices, the temperature-to-digital conversion process should be carried out spending an ultra-low amount of energy to ensure enough battery life; considering that state-of-the-art accelerometers and gyroscopes generate digital samples requiring an energy in the order of at least a few hundreds of nanojoules as derivable from [19] and [20], the target conversion energy limit in this work has been set to 10 nJ taking into account the temperature sensor being an auxiliary system. Second, in today's global market, cost effectiveness is what determines the success or failure of an electronic product; this drives the temperature sensor design toward the minimization of its occupied silicon area and limits its calibration to be performed at a single temperature to reduce the usage of infrastructures (oil baths and ovens) and the settling time required for the calibration procedure itself. The two addressed quantities (conversion energy and cost) are in a direct trade-off condition with the sensor's resolution and accuracy, respectively. The higher the conversion energy (that is, the higher the power consumption and/or the conversion time), the finer the achievable resolution is; on the other hand, the higher the sensor's active area and/or the number of adopted trimming points, the better the obtainable accuracy is. Within this trade space, in the proposed design, higher priority has been devoted to conversion energy and cost since resolution and inaccuracy are at some point bottlenecked by the uncertainty of the outputs of the inertial sensors to be compensated; accordingly, a resolution of at least 100 mK and a maximum relative inaccuracy of 2% have been considered as targets.

In this direction, the preferred choice for the temperature sensing core is that of a bipolar junction transistor (BJT)-based one; even if resistor-based sensors commonly offer a superior energy efficiency [21], [22], [23], they generally exhibit a larger inaccuracy after a one-point trim. In addition, although in [24] the introduction of a smart correction technique requiring few logic gates enables an effective curvature suppression, resistor-based solutions typically give rise to temperature characteristics exhibiting a larger non-linearity, undesirable feature given the first-order compensation purpose of the considered sensor. When it comes to the temperature-to-digital conversion process, instead, successive-approximation-register (SAR) architectures are the most promising solution in order to achieve the targeted conversion energy, thanks to the efficiency of their conversion algorithm; however, this kind

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of approach commonly offers too coarse resolution values for the considered application (in the order of hundreds of millikelvin). In [25], an 8-bit SAR-based sensor achieves a 580-mK resolution burning 1.6 nJ, while in [26], an asynchronous SAR analog-to-digital converter (ADC) generates temperature-dependent samples with a 590-mK resolution requiring 98 pJ per conversion; in both examples, the temperature resolution is limited by the ADC's quantization noise. This limit was overcome in [27], where the random variability of a SAR's output codes caused by thermal noise was exploited to perform a resolution refinement to 158 mK according to an oversampling technique at the cost of 2.5 nJ per conversion; in addition, a fully current-mode processing architecture was exploited to achieve a relatively compact design (0.08 mm^2).

In this article, we propose a current-mode noise-shaping SAR (NS-SAR)-based smart temperature sensor. The attractiveness of this kind of converters strongly emerged in the last decade [28], [29], [30], [31] as they combine the advantages of conventional SAR solutions with the ones of $\Sigma\Delta$ architectures and were never exploited before within a temperature sensing system. The sensor, whose block diagram is reported in Fig. 1 and discussed in Section II, implements a resolution refining process based on an error-feedback approach which effectively shapes the temperature quantization noise of a 4-bit SAR converter. This technique inherently enables a significant area efficiency compared with multi-bit $\Sigma\Delta$ solutions since it relies on the decisions of a single comparator to generate temperature-dependent digital words. Moreover, in keeping with [27], the system has been completely designed in the current domain, a feature that enables op-amp less signal processing and gives rise to an active area of just 0.057 mm^2. Considering that a standard 180-nm CMOS process was employed for its fabrication, this degree of compactness, together with [32], marks the silicon area state-of-the-art level for BJT-based sensors in such a mature technology node. Finally, as far as the authors are aware, the employed ADC is the first NS-SAR designed with a fully current-mode processing approach.

II. Temperature Sensor Architecture

The block diagram of the proposed temperature sensor is shown in Fig. 1; as introduced before, it can be noted that, except for the SAR logic, every block processes signals in the current domain. The choice of designing this system with a fully current-mode approach has been dictated by two main reasons. First, in this way, it is possible to get rid of any operational amplifier (required in a voltage-mode alternative) reducing both the current consumption and the silicon area occupation. In the second place, the addition, subtraction, and scaling of signals in the current domain are extremely simple compared with their voltage-mode counterparts; these operations are essential to set the proper temperature conversion range, to quantize the input signal and to perform the error feedback.

The BJT core is composed of proportional and complementary-to-absolute-temperature (PTAT and CTAT) current sources; it generates the signal containing the temperature information to be converted (I_{PTAT}) and a couple of reference signals

$$I_{REF} = I_{PTAT1} + I_{CTAT1} \tag{1}$$

$$I^{\star}_{REF} = I_{PTAT2} + I_{CTAT2}. \tag{2}$$

By means of three interface circuits, one n-type current mirror and two current buffers, these signals are delivered to the current-mode NS-SAR, which includes a binary p-type 4-bit current steering digital-to-analog converter (DAC), a current comparator, a SAR logic, and a noise shaper circuit. $I^{\star\star}_{REF}$, a replica of $I^{\star}_{REF}$, is provided as reference to the DAC which scales it sequentially according to the successive approximation algorithm executed by the SAR logic block; the resulting DAC current is thus given by

$$I_{DAC} = \alpha_{DAC} \cdot I^{\star\star}_{REF} \tag{3}$$

where α_{DAC} is the scaling factor the DAC implements clock cycle by clock cycle. I_{REF}, instead, is used to upshift I_{DAC} in order to determine the proper temperature conversion range leading to

$$I_{SAR} = I_{REF} + I_{DAC}. \tag{4}$$

Each 4-bit conversion is carried out in four clock cycles, in which the subsequent decisions of the current comparator about the polarity of the ADC input signals (I_X and I_{SAR}) are processed by the SAR logic; then, in a dedicated clock period, as shown in the conceptual timing diagram of Fig. 1 (bottom), a noise shaper generates a residue current (I_{RES}) that is fed back to the ADC input and added to I_{PTAT} to form

$$I_X = I_{PTAT} + I_{RES}. \tag{5}$$

The 4-bit codestream obtained by a cyclic operation of the described conversion process is finally delivered to a decimation filter which, for testing flexibility reasons, has been kept off-chip. Depending on the selected oversampling ratio (OSR), it generates more refined digital codes with a $1/(OSR \cdot T_s)$ rate, where T_s is equal to five clock periods.

III. Current-Mode Noise-Shaping Concept

The current-mode error-feedback mechanism, designed to implement a first-order quantization noise shaping, is described in detail in Fig. 2. Considering $I_{RES} = 0$ as initial condition, during the RES_1 phase, at the end of the first conversion cycle, both I_X and final I_{SAR} current value are stored by means of two current samplers, while a current subtractor computes their difference; the obtained residue current is then held by a current holder for the entire following conversion cycle until the next I_{RES} current is ready to be added to I_{PTAT}. Taking the nth conversion cycle into account

$$I_{RES}(n) = I_X(n-1) - I_{SAR}(n-1) \tag{6}$$

thanks to the combined memory function of the current samplers and the current holder. Moreover, $I_{SAR}(n)$, which is nothing but a quantized version of $I_X(n)$, can be written as follows:

$$I_{SAR}(n) = I_X(n) + \epsilon_q(n) \tag{7}$$

$$\overset{\mathcal{Z}}{\Longrightarrow}$$

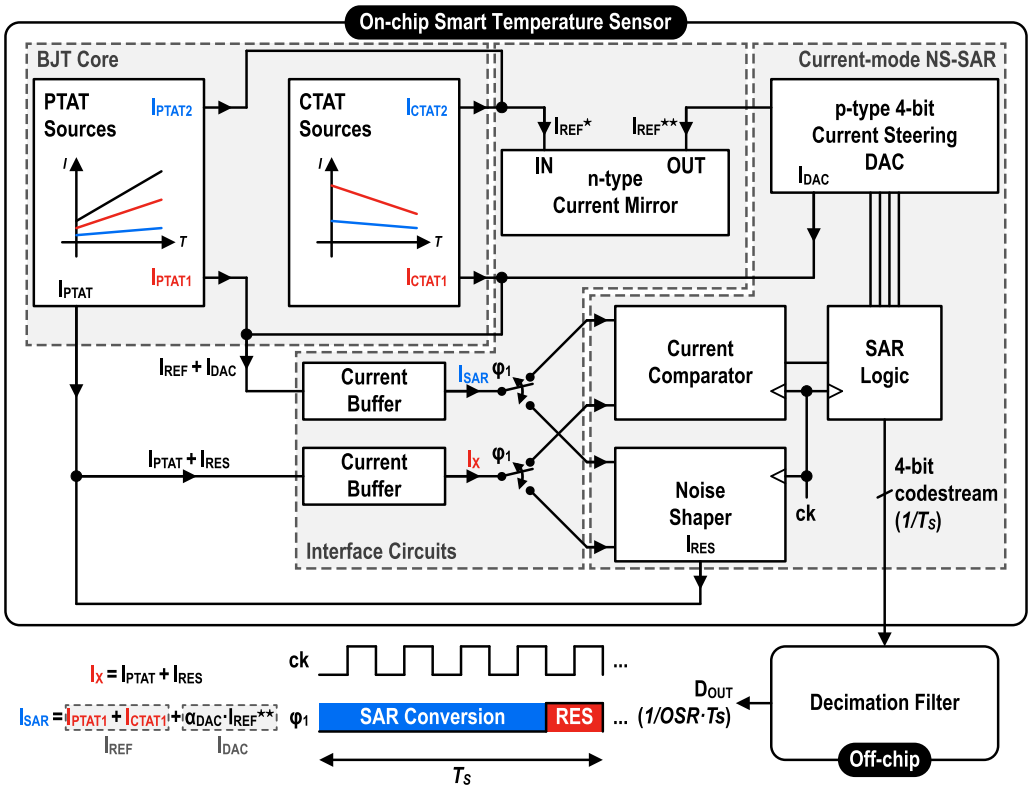

Fig. 1. Block diagram of the proposed noise-shaping SAR-based smart temperature sensor.

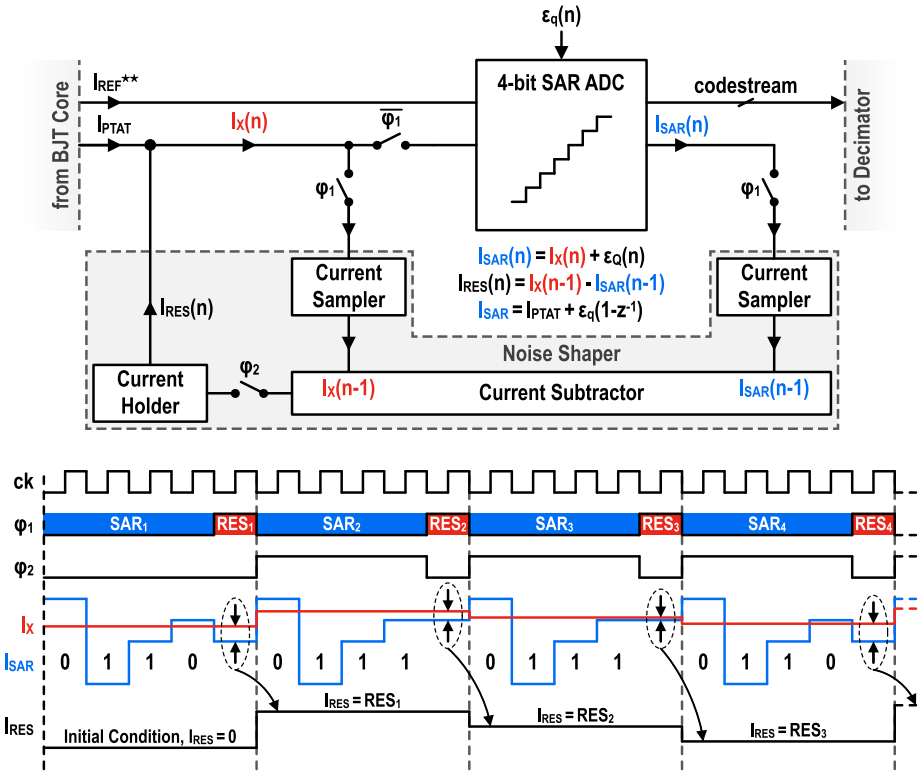

Fig. 2. Conceptual representation of the current-mode error-feedback scheme (top) and detail of the first conversion cycles (bottom).

$$I_{\mathrm{SAR}}(z) = I_X(z) + \epsilon_q(z) \tag{8}$$

where ϵ_Q is the quantization error, and a $\mathcal{Z}$-transformed version is also shown, needed for the following of this section. In addition, it can be deduced from Fig. 2 that

$$I_X(n) = I_{\mathrm{PTAT}} + I_{\mathrm{RES}}(n) \tag{9}$$

where I_{PTAT} is treated as a constant because a fixed temperature is being considered. Combining (6) with (9), a new expression

for $I_X(n)$ is derived

$$I_X(n) = I_{\text{PTAT}} + I_X(n-1) - I_{\text{SAR}}(n-1) \tag{10}$$

$$\Downarrow \mathcal{Z}$$

$$I_X(z) = I_{\text{PTAT}} + I_X(z) \cdot z^{-1} - I_{\text{SAR}}(z) \cdot z^{-1} \tag{11}$$

where its $\mathcal{Z}$-transform is reported since the next steps will be carried on in this domain. Isolating $I_X(z)$ in (11)

$$I_X(z) = \frac{I_{\text{PTAT}} - I_{\text{SAR}}(z) \cdot z^{-1}}{1 - z^{-1}}. \tag{12}$$

Incorporating (12) in (8)

$$I_{\text{SAR}}(z) = \frac{I_{\text{PTAT}} - I_{\text{SAR}}(z) \cdot z^{-1}}{1 - z^{-1}} + \epsilon_q(z). \tag{13}$$

Manipulating this equation and performing the straightforward cancellation, the final expression for $I_{\text{SAR}}(z)$ is achieved

$$\begin{aligned} I_{\text{SAR}}(z) &= \cancel{I_{\text{SAR}}(z) \cdot z^{-1}} \\ &= I_{\text{PTAT}} \cancel{- I_{\text{SAR}}(z) \cdot z^{-1}} + \epsilon_q(z) \cdot (1 - z^{-1}) \\ I_{\text{SAR}}(z) &= I_{\text{PTAT}} + \epsilon_q(z) \cdot \underbrace{(1 - z^{-1})}_{\text{NTF}}. \end{aligned} \tag{14}$$

Since a one-to-one correspondence between the values of I_{SAR} at the end of each conversion cycle and the 4-bit output codes exists ($I_{\text{SAR}} \leftrightarrow D_{\text{OUT}}$), it follows that a first-order noise shaping is achieved as proven by the noise transfer function (NTF) highlighted in (14).

The bottom part of Fig. 2 provides a more intuitive view of the time evolution of the current-mode error-feedback mechanism. The I_{RES} determination process is depicted; it can be observed that the resolution refinement happens thanks to a deterministic tracking of the temperature-dependent signal (I_{PTAT}) by a continuous evaluation and feedback of the distance between the ADC's analog input (I_X) and its quantized version (I_{SAR}). An important aspect about the proposed system is that I_{RES} is an unipolar current; in particular, it is always positive. Indeed, if during a certain conversion cycle, the I_X current is lower than the I_{SAR} current reached by the SAR algorithm after four clock cycles leading to an LSB equal to 0, in the correspondent RES phase, the DAC is updated according to this decision pushing I_{SAR} below I_X and giving rise to a positive current difference (this is, for instance, what happens in the first and the fourth reported conversion cycles); if, vice versa, the last decision is 1 (as in the second and third reported cycles), the I_X current is greater than I_{SAR} even before the RES phase starts, thus leading to an always-positive I_{RES}. Having a residue current that does not change polarity along the temperature-to-digital conversion process considerably simplifies the noise shaper circuit implementation, as will be addressed in Section IV. The described procedure, in the time domain and for a given temperature, results in a determined code pattern involving adjacent 4-bit codes that, processed by the decimation filter, provides higher resolution digital samples. The encoding of the needed temperature information in 4-bit code sequences, will be supported by simulation and experimental results reported in the following of this article.

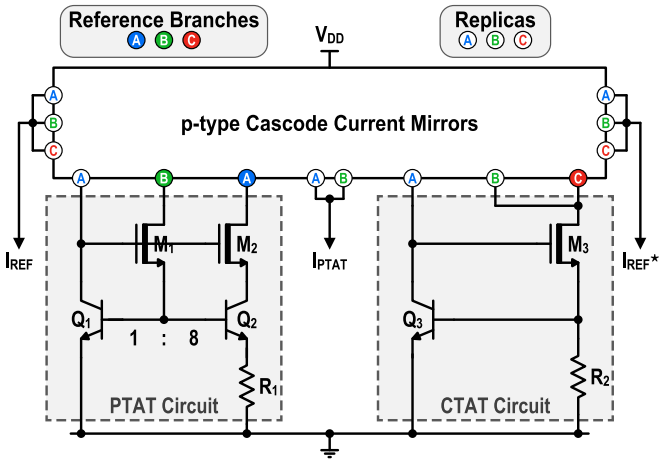

Fig. 3. Schematic of the employed BJT core circuit.

IV. Circuit Implementation

This section is devoted to the transistor-level description of the most relevant circuits implementing the proposed temperature sensor, operated at a 4-MHz clock frequency.

A. BJT Core

The schematic of the employed BJT core circuit is depicted in Fig. 3. It is composed of a PTAT part and of a CTAT one, both exploiting lateral NPN transistors; they generate three elementary current contributions which are collected and properly replicated by a set of p-type cascode current mirrors, represented on top. These contributions, which are all buffered by means of native transistors M_1, M_2, and M_3, are the collector current of Q_2 (A), the sum of the base currents of Q_1 and Q_2 (B) and the current flowing through R_2 (C), equal to V_{BE}/R_2. Within the output current delivery, contribution B is always paired with contribution A with an additional $1/2$ scaling factor to implement a recovery of the base current, needed due to the poor β factor of the available devices. According to the scheme of replicas shown in Fig. 3, the BJT core circuit provides three output currents to the rest of the temperature sensor. I_{PTAT}, which is related to the emitter current of Q_2, contains the temperature information to be processed by the ADC described next; I_{REF} and $I^{\star}_{\text{REF}}$, instead, additionally include the CTAT contribution to be used as references for the temperature-to-digital conversion.

B. Current Processing 4-bit SAR ADC

Fig. 4 shows the schematic of the current processing 4-bit SAR ADC employed for the temperature-to-digital conversion; it includes the current comparator, the SAR logic, and the binary 4-bit current-steering DAC (CS-DAC) introduced in Section II. Its operation is organized according to the φ_A and φ_B signals which, during the SAR conversion, run at the same frequency of the ck signal present in Figs. 1 and 2 (4 MHz). Having the falling and rising edges disoverlapped, φ_A and φ_B, respectively, give rise to three different phases as shown in the top-left part of Fig. 4. When φ_A is high and φ_B is low (❶), the comparator's input currents ($I_{\text{PTAT}} + I_{\text{RES}}$ and $I_{\text{REF}} + I_{\text{DAC}}$)

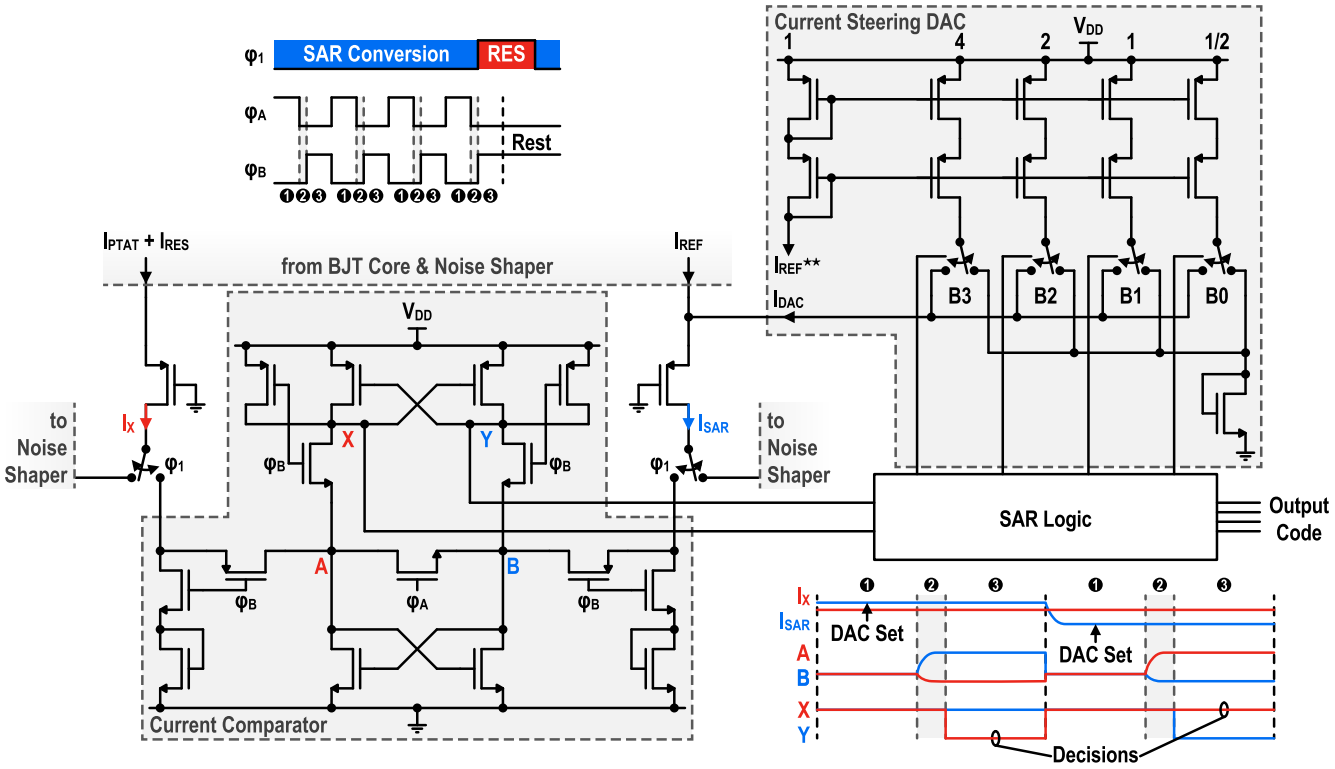

Fig. 4. Circuit diagram of the current processing 4-bit SAR ADC employed for the temperature-to-digital conversion.

get collected and buffered by means of a common-gate stage on both sides (these buffers correspond to the ones present in the interface circuits section in Fig. 1). I_X and I_{SAR} are inherently delivered to an n-type latched pair which, at this stage, is in a forced equilibrium condition since the horizontal switch driven by φ_A is on; this condition is exploited to allow the logic circuit to set the DAC to the code determined by a standard SAR algorithm. By the end of this phase, the I_{DAC} current settles so that, when φ_A gets low (❷), the comparator is enabled to take a proper decision. This occurs since the equilibrium constraint is released and nodes A and B are free to unbalance. If $I_X > I_{\mathrm{SAR}}$, the voltage at node A rises, while the voltage at node B falls; vice versa, if $I_{\mathrm{SAR}} > I_X$. When φ_B turns high (❸), I_X and I_{SAR} are steered toward two diode-connected transistors which absorb them in order not to impact the decision transfer from the bottom latch to the top one ($A \rightarrow X$ and $B \rightarrow Y$) which provides a squaring at the X and Y nodes, whose unbalancement is processed by the SAR logic to determine the next DAC status. It is important to notice the alignment of the φ_A and φ_B signals ruling this set + decision process with the φ_1 signal triggering the noise shaper operation (described below); indeed, after the fourth decision has been taken, instead of steering the comparator's input currents toward the absorption diode-connected transistors, they are directly transferred to the noise shaper circuit while the comparator is left to rest. This provides a half-clock cycle lead to the residue current generation process ensuring its feedback delivery happening before the following conversion cycle starts. It can be noticed from Fig. 4 that the reference current of the CS-DAC (I^{**}_{REF}) has been sized equal to the one controlled by $B1$ instead of the one controlled by $B0$. This

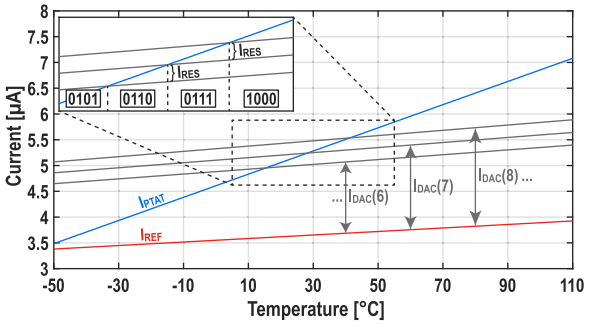

Fig. 5. Current-level scenario of the proposed architecture.

design choice has been made for two reasons. First, within the noise versus power consumption trade space of the DAC, this approach provides a 3-dB reduction of the output noise power at the cost of an additional consumption of just 1-LSB current (+6.25%). Furthermore, considering the area versus matching trade-off, this solution enables an improvement by a factor $\sqrt{2}$ of the matching performance of the DAC for the same area of the unit current source. Finally, a conventional switching scheme has been adopted since the implementation of code-dependent randomization techniques to suppress the deterministic gradient error of the DAC would have had a negligible impact on the system performance [33], [34], [35].

To summarize the current levels at stake, Fig. 5 reports the main signals of interest as a function of the temperature in the range of −50 °C to 110 °C. The I_{PTAT} signal grows linearly from about 3.5 μA to little more than 7 μA while the I_{REF} current, static component of I_{SAR}, exhibits a slight positive slope around 3.65 μA according to [36]. Three instances

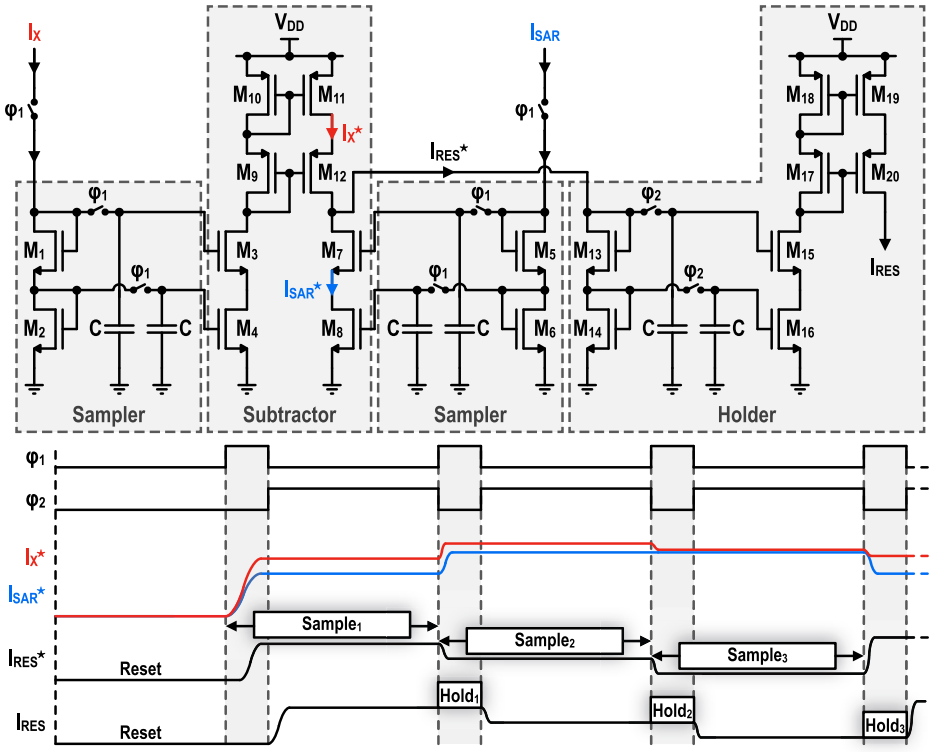

Fig. 6. Schematic (top) and timing (bottom) diagrams of the noise shaper circuit.

of the CS-DAC output current are also shown by way of example. The digital output codes are determined depending on the intercepts of the I_{PTAT} line with the sum of I_{DAC} with I_{REF}, which scans the PTAT current range for increasing temperatures. From the included enlargement, it can be noticed that, for a given code, the adopted conversion process gives rise to an always-positive residue current.

C. Current-Mode Noise Shaper

Fig. 6 reports the schematic and timing diagrams of the noise shaper circuit; after reset, it is first operated at the end of the initial SAR conversion phase. While φ_1 is high, the current samplers collect I_X and I_{SAR} into two cascode mirroring structures in which every transistor is equipped with a gate voltage sampling capacitor (C), sized to keep this information for a full conversion cycle (32 fF). In addition, to avoid the sampled gate voltage being affected by the charge injection of the switches turning off, every sampling switch in this scheme has been equipped with a half-sized dummy element driven by a complementary non-overlapped signal [37]. The input currents are thus replicated at the subtractor input that, exploiting a p-type current mirror, generates their difference as output

$$I^{\star}_{\mathrm{RES}} = I^{\star}_{X} - I^{\star}_{\mathrm{SAR}}. \tag{15}$$

Once this process has been completed, φ_1 turns low while φ_2 turns high; the obtained residue current gets passed to the holder and, with an additional mirroring step, it generates I_{RES}, which is the desired error-feedback current. A key point of the noise-shaper circuit is its timing; the current-mode error-feedback implementation is possible thanks to the synchronous current storing feature of the samplers and the holder. During the nth SAR conversion (low φ_1), the samplers are disconnected from the input signals and maintain information about the $(n-1)$th input values. Their difference is delivered to the holder that, in turn, provides it as feedback for the temperature sensor; the holder role, instead, is essential when φ_2 is low: it holds the residue corresponding to the just finished nth conversion, $I_{\mathrm{RES}}(n)$, while the generation of the one needed for the $(n+1)$th conversion, $I_{\mathrm{RES}}(n+1)$,

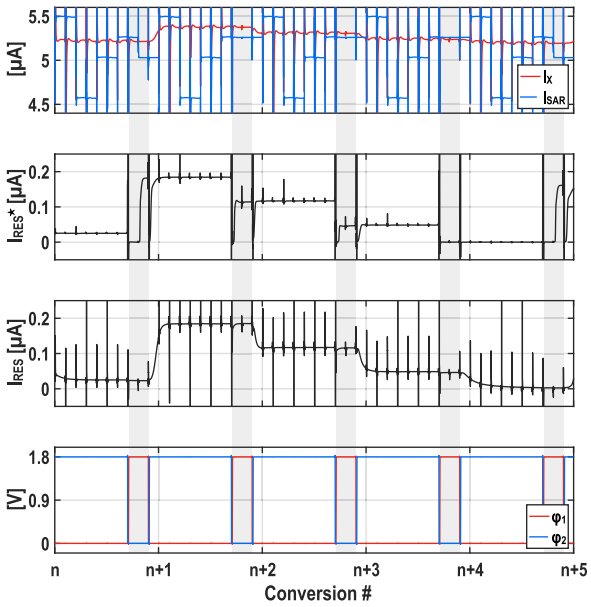

Fig. 7. Waveforms of the main signals of the noise shaper circuit during five conversion cycles (simulation results).

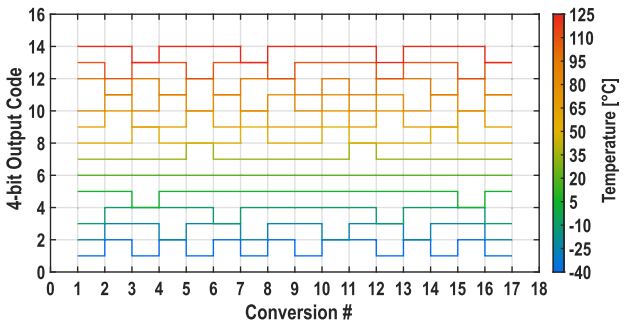

Fig. 8. NS-SAR output code patterns as a function of temperature (post-layout simulation results).

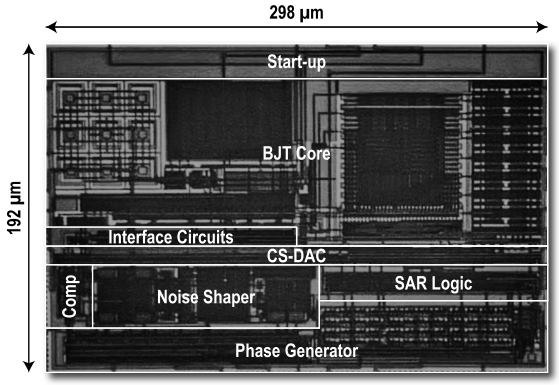

Fig. 9. Chip micrograph of the fabricated sensor.

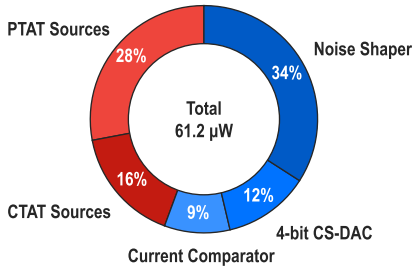

Fig. 10. Power consumption breakdown of the proposed temperature sensor.

is carried out; this is necessary considering that $I_{\mathrm{RES}}(n+1)$ should be determined on the basis of $I_{\mathrm{RES}}(n)$ and, therefore, it is fundamental that this step occurs without $I_{\mathrm{RES}}(n)$ being affected by the evaluation process of $I_{\mathrm{RES}}(n+1)$. It can be observed that, according to this implementation, the residue current has to be unipolar: this is the case of this system since, as addressed earlier, the employed ADC approximates the analog input current always by the defect. Fig. 7 reports some simulation results involving the main signals of the noise shaper circuit during five conversion cycles. It can be noticed that, according to the described procedure, the I_{RES} current value is updated half a clock cycle before a new conversion cycle begins so that, by the time of the first comparator's decision occurring one entire clock period later, the I_X signal has completely settled.

V. Temperature Effect on Output Codes

In order to provide an overall photograph of the proposed smart temperature sensor and to support the operating principle described so far, Fig. 8 reports some system-level post-layout simulation results, in which the NS-SAR ADC response for 16 consecutive conversions is shown as a function of the temperature in the range of −40 °C to 125 °C with steps of 15 °C. It can be noted that the temperature information is contained in well-defined code patterns exhibiting an increasing average as temperature rises. This behavior is a consequence of the deterministic nature of the adopted temperature-to-digital conversion process which gives rise to a cyclic time evolution of the sensor's output codestream. By decimating it, this periodicity gives rise to an improved filtering efficiency with respect to a randomly evolving codestream [27] since a first-order quantization noise shaping is present. This feature, which gives rise to a more efficient resolution refinement, is at some point limited by the impact of the system's electronic noise (thermal + flicker) on the ADC output as discussed in Section VI.

VI. Measurement Results

The proposed temperature sensor was fabricated in a standard 180-nm CMOS process and supplied at 1.8 V. Fig. 9 shows a micrograph of the die's active area with its breakdown; the complete design turns out to be a rectangle of dimensions 298 × 192 μm, corresponding to an area of less than 0.06 mm^2. 25 samples from one batch enclosed in DIL28 ceramic packages were characterized in an ACS DY200C climate chamber in the range of −50 °C to 110 °C with steps of 10 °C; the measurements were carried out with the aid of a LabVIEW-automated testing routine and considering settling times of at least 30 min between successive temperature steps.

A. Power Consumption

The consumption measurements on the fabricated samples demonstrated a 34-μA mean current flow from the 1.8-V supply, corresponding to a 61.2-μW total power consumption. Fig. 10 shows its breakdown among the main blocks of the sensor; it can be noted that the analog and the digital parts of the system are almost evenly power-hungry. The SAR Logic contribution has been omitted since its consumption is of about 0.5 μW (<1%). The significant power consumed by the noise shaper is related to its current mirror design; referring to Fig. 6, the main reason is that no attenuation has been introduced within the mirrors of the subtractor circuit in order to achieve a sufficiently high level of $I^{\star}_{\mathrm{RES}}$ to properly bias the M_{13}–M_{14} reference branch. Taking the proposed temperature-to-digital conversion process into account and considering the system being operated at a 4-MHz clock frequency, a single 4-bit sample gets generated in 1.25 μs and consequently requires a 75.6-pJ energy.

B. Error-Feedback Current

A key feature of the proposed sensor is the use of a residue current as an error-feedback signal; accordingly, some dedicated experimental results were collected to further support the adopted technique. Fig. 11 shows the measured I_{RES}

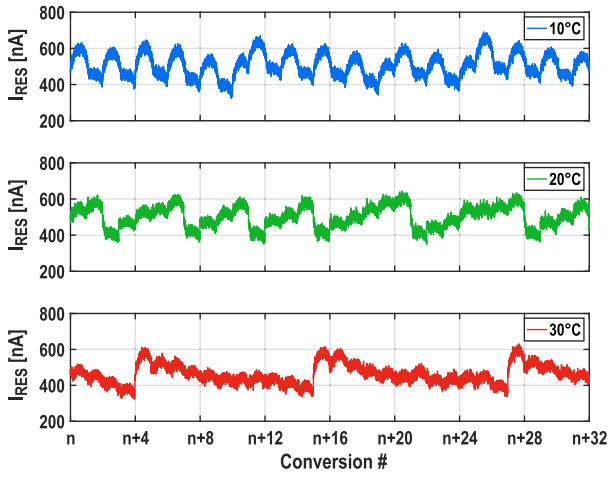

Fig. 11. Measured I_{RES} current over 32 conversion cycles at three different temperatures.

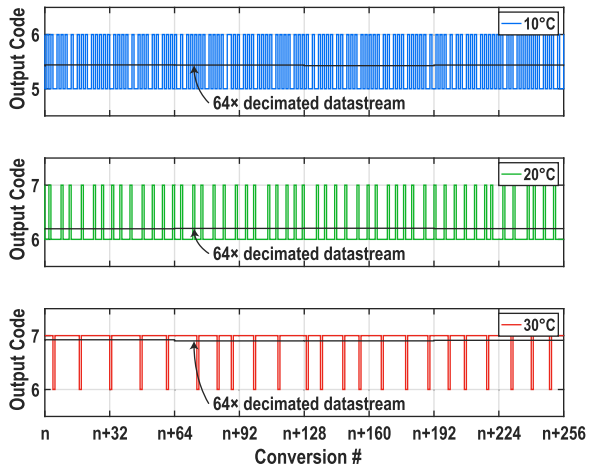

Fig. 12. Measured output codes at the previously considered temperatures with 64× decimated datastream superimposed.

current over 32 conversion cycles at three different controlled temperatures as an example (10 °C, 20 °C, and 30 °C); in these three cases, that will be recalled in Section VI-C, the sensor exhibits an emblematic behavior useful to demonstrate its operating principle. Regular and well-defined cycles can be observed in all of the considered examples; at 10 °C, I_{RES} jumps up and down at almost all conversions, at 20 °C, it periodically exhibits a rising stairy behavior, while at 30 °C, the stairy response is cyclically monotonically decreasing and at a lower frequency. The periodicity of this phenomenon depends on the distance of the PTAT signal from the closest quantization level determined by the DAC; a higher periodicity corresponds to bigger distances with a maximum frequency, equal to $1/(2 \cdot T_s)$, observed halfway between two subsequent quantization levels; in addition, a cyclically rising behavior indicates the input signal being in the lower half of the quantization step while a cyclically falling one, vice versa, means that the input signal lies in the higher half.

C. Temperature Resolution

In order to evaluate the resolution performance of the proposed sensor, 2^{20} 4-bit samples were acquired by a data

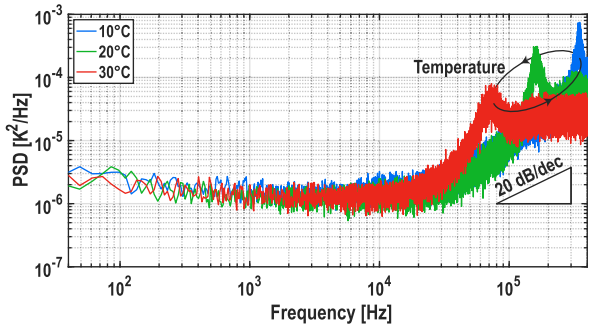

Fig. 13. Measured output noise PSD (Hanning window, 65 536 samples, 16× averaging) at the previously considered temperatures.

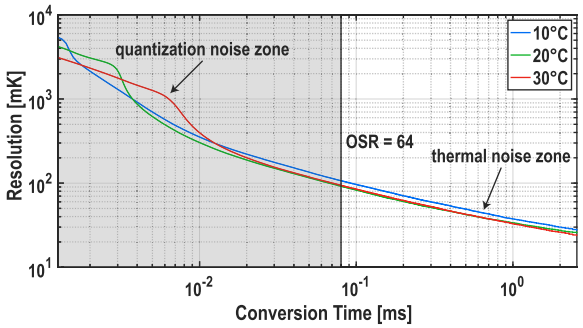

Fig. 14. Temperature resolution as a function of the conversion time at the previously considered temperatures; the shadowed part of the figure marks the effect of the selected 64× decimation.

acquisition system (DAQ) while keeping a fixed temperature. Fig. 12 reports a small subset (256 conversions) of the so collected data at the three temperatures considered earlier; the datastream obtained after an off-chip 64× decimation, exhibiting the expected reduced variability, is shown superimposed (a six-pole Chebyshev Type-I low-pass filter has been employed as decimator). It is interesting to compare the time evolution of the reported 4-bit code sequences with the residue current behavior discussed in Section VI-B. Indeed, the codestream measured at 10 °C, exhibits a relatively high bouncing frequency between code 5 and code 6; as stated earlier, this is a consequence of the position of the I_{PTAT} signal approximately in the middle of that quantization step as confirmed by the average level of the decimated datastream. Also, the measurements at 20 °C and 30 °C are consistent with the previous discussion.

The spectra corresponding to the variations of these codestreams are shown in Fig. 13. It can be noted that the right part of the reported noise power spectral density (PSD) functions exhibits a first-order noise shaping while the floor in the left part is completely determined by thermal noise, whose top contributor in the proposed sensor is the BJT core circuit. The peaking visible in the shaped part of the spectra is a consequence of the periodicity of the considered codestreams due to the limit cycles, typical of first-order noise-shaping modulators with constant input signals. Indeed, the lower periodicity of the 30 °C case observed both in Figs. 11 and 12, gives rise to a peak at lower frequency with respect to the one observed for the 10 °C case, in which the code variations occur much faster. The 20 °C case, as expected, lies in the middle. Fig. 14 reports the sensor's temperature resolution as

a function of the conversion time which, in turn, is a function of the OSR selection. On the left, the quantization noise zone can be identified. Here, the reported curves exhibit a steeper slope with respect to what happens in the thermal noise zone present on the right as the effect of the progressive low-pass filtering of the shaped quantization noise. With a positioning far removed from the peaking zone, an OSR of 64 has been selected to ensure a complete filtering of the quantization noise component while offering a 92-mK room temperature resolution, compliant with the targeted application. Combining this value with the 75.6-pJ energy-derived earlier for a single 4-bit sample, an energy efficiency of 41 pJ·K^2 is achieved [38].

To further motivate the proposed 4-bit NS-SAR approach, it is useful to compare it, by way of example, with an 8-bit oversampling SAR solution with no error feedback and with the same electronic noise level. Considering that a 469-mK noise-limited resolution (before oversampling) due to the BJT core is observed, it is clear that to achieve the target resolution for the considered application, some form of oversampling is definitely necessary. As demonstrated by the reported experimental results, the proposed architecture is able to achieve the desired resolution performance with an OSR of 64 and requires $4 + 1$ clock periods for each SAR conversion; this results in a total conversion time of 5×64 clock periods. To achieve such a resolution with the same amount of electronic noise, the 8-bit oversampling SAR alternative would need an OSR of at least 100 with the additional drawback of requiring eight clock periods per SAR conversion; this corresponds to a total conversion time of 8×100 clock periods which is 2.5 times longer with respect to the proposed approach. Moreover, the DAC area required to achieve a 4-bit matching is significantly lower if compared to the 8-bit case [27]. This emblematic comparison contains the root motivations that lead us to opt for the presented architecture.

D. Temperature Inaccuracy

The temperature characteristics of the 25 measured samples were studied to evaluate the accuracy performance of the proposed sensor. The collected thermal responses alongside their raw error spread are reported in Fig. 15, in which the average output code is considered; a simple (and low-cost) offset compensation performed at room temperature leads to the scenario reported in Fig. 16, where the peak-to-peak relative inaccuracy is equal to 1.39%, while the $\pm 3\sigma$ one is equal to 1.96%. The considerable spread of the untrimmed case and the residual error of the one-point offset-compensated one are mainly due to the mismatch effects of the several current mirrors employed within the sensor's design. This condition could have been improved by introducing chopping or dynamic element matching (DEM) techniques which are commonly used in this field [39], [40], [41], [42]; however, no effort was spent in this direction since the achieved accuracy performance, although modest with respect to other the state-of-the-art BJT-based solutions, is compliant with the application taken into account. As stated in the Introduction, the accuracy of this temperature sensor is at some point bottlenecked by the uncertainty of the outputs of the inertial sensors to be compensated; for this reason, a 2% accuracy in a

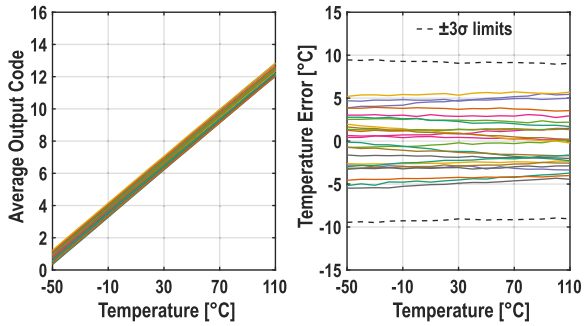

Fig. 15. Measured untrimmed temperature characteristics with correspondent temperature errors (25 samples).

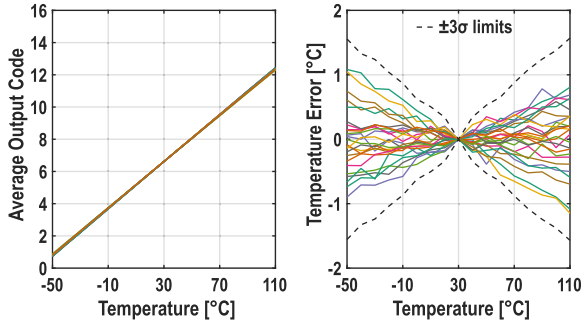

Fig. 16. Measured one-point offset-compensated temperature characteristics with correspondent temperature errors (25 samples).

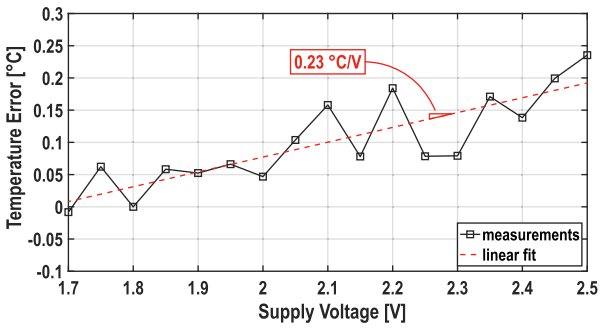

Fig. 17. Measured room temperature supply sensitivity.

160 °C temperature range is considered sufficient. The several current mirrors (especially the BJT core ones) are the major contributors to the temperature uncertainty of the proposed system, but pushing the temperature accuracy below 2% is fruitless for the targeted application.

E. Supply Sensitivity

The supply sensitivity of the proposed sensor was also measured. Fig. 17 reports the experimental results collected at room temperature with the supply voltage ranging from 1.7 to 2.5 V with steps of 0.05 V. The measured data trend features a slight increase of the temperature error for increasing supply voltages, as highlighted by the superimposed linear fit. Considering the slope of this straight line, the supply sensitivity turns out to be 0.23 °C/V, taking the extremes of the temperature error into account, instead, it amounts to 0.3 °C/V.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH RECENT BJT-BASED TEMPERATURE SENSORS

	[39] TCAS-II 2019	[3] TCAS-I 2020	[40] JSSC 2020	[41] JSSC 2022	[42] JSSC 2022	[25] ISSCC 2018	[26] TCAS-II 2020	[27] ESSCIRC 2022	**This work 2023**
ADC Type	ΣΔ1	ΣΔ1	ΣΔ2	ΣΔ2	TFC	SAR	SAR	OS-SAR	**NS-SAR**
Technology [nm]	55	65	160	180	110	22	180	180	**180**
Area [mm^2]	0.015	0.003	0.146	0.42	0.025	0.004	0.121	0.08	**0.057**
Temperature Range [°C]	-40 to 125	-10 to 110	-40 to 180	-50 to 180	-40 to 140	-30 to 120	-10 to 100	-20 to 80	**-50 to 110**
Supply Voltage [V]	1.0	1.3	1.8	1.5	1.5	1.0	1.0	1.8	**1.8**
Measured Samples	12	25	24	25	18	38	15	20	**25**
Relative Inaccuracy [%]	2.06[a]	2.25[b]	0.18[a]	0.39[a]	1.11[a]	1.43[a]	4.27[b]	1.39[b]	**1.96[a] / 1.39[b]**
Trimming Points	0	2	1	1	2	1	1	2	**1**
Power [μW]	37	111.8	9.8	3.8	3.1	50	0.0005	39.6	**61.2**
Conversion Time [ms]	32.8	4.1	20	8.3	0.8	0.032	200	0.064	**0.08**
Conversion Energy [nJ]	1214	460	195	32.5	2.5	1.6	0.098	2.5	**4.9**
Resolution [mK]	20	65	23	18	144	580	590	158	**92**
Resolution FoM [pJ·K^2]	486	1944	103	10	51	538	34	63	**41**

[a]$\pm 3\sigma$ inaccuracy. [b]Worst case inaccuracy.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH RECENT RESISTOR-BASED AND MOSFET-BASED TEMPERATURE SENSORS

	[43] CICC 2019	[44] TCAS-II 2021	[45] TCAS-II 2021	[46] JSSC 2019	[47] SSC-L 2020	[48] TCAS-I 2021	**This work 2023**
Sensing Device	Resistor	Resistor	Resistor	MOSFET	MOSFET	MOSFET	**BJT**
ADC Type	TDC	FLL	SAR	FDC	FDC	FDC	**NS-SAR**
Technology [nm]	180	65	180	180	65	130	**180**
Area [mm^2]	0.51	0.47	0.59	0.074	0.32	0.07	**0.057**
Temperature Range [°C]	-40 to 85	-5 to 95	-30 to 100	-20 to 80	-30 to 70	0 to 80	**-50 to 110**
Supply Voltage [V]	1.5	0.9	1.8	0.8	0.8	0.95	**1.8**
Measured Samples	10	14	13	9	9	9	**25**
Relative Inaccuracy [%]	0.88[a]	3.4[a]	1.14[a]	2.1[b]	1.7[b]	1.05[a]	**1.96[a] / 1.39[b]**
Trimming Points	2	2	2	2	2	2	**1**
Power [μW]	15.6	0.31	600	0.011	0.0064	0.196	**61.2**
Conversion Time [ms]	1	10	0.012	839	766	59	**0.08**
Conversion Energy [nJ]	15.6	3.1	7.2	8.9	4.9	11.56	**4.9**
Resolution [mK]	2	9.8	20	145	75	100	**92**
Resolution FoM [pJ·K^2]	0.06	0.3	2.9	187	2.75	115.6	**41**

[a]$\pm 3\sigma$ inaccuracy. [b]Worst case inaccuracy.

VII. COMPARISON TO PREVIOUS WORK

A performance summary of the proposed sensor and a comparison with recent BJT-based works is reported in Table I. It can be noted that the employed NS-SAR ADC allows the achievement of a conversion energy below 10 nJ while reaching a sub-100-mK resolution, as required by the considered application. This, resulting in a 41-pJ $\cdot$ K^2 resolution FoM, corresponds to an intermediate position between the works reported in the first four columns of Table I (high resolution) and the ones reported in the right half (low conversion energy). An attractive feature of this design is the 0.057-mm^2 occupied silicon area; excluding the sensors designed in more advanced fabrication processes, the proposed one offers the highest level of compactness. This statement is still true considering all the BJT-based works collected in [49] designed adopting technologies with a similar feature size (130-, 160-, and 180-nm). In addition, considering that this work employs a single-temperature trimming, it achieves the targeted cost effectiveness. Since resistors and MOSFETs are also widely used for temperature sensing, Table II reports a further comparison; three works per type burning a similar energy per conversion are compared with the proposed one. Even if some of them achieve a superior resolution FoM number, it can be seen that, besides offering smaller operating temperature ranges, the reported works require a two-point trimming and occupy a larger silicon area.

VIII. CONCLUSION

A smart temperature sensor for the thermal drift compensation in MEMS accelerometers and gyroscopes has been presented. The proposed system, designed and fabricated in a standard 180-nm CMOS process, features a fully current processing architecture and, for the first time, employs an error-feedback NS-SAR ADC for the temperature-to-digital conversion process; this approach combines the low energy/conversion advantage of SAR solutions with a first-order quantization noise shaping, leading to a 92-mK resolution at the cost of 4.9 nJ. The achieved $\pm 3\sigma$ inaccuracy

is quite moderate (1.96% in the −50 °C to 110 °C sensing range) but sufficient for the targeted application. Taking the adopted single-temperature offset compensation and the active area of just 0.057 mm^2 into account, the sensor offers a great cost-effectiveness, a desirable feature, especially given its auxiliary role.

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