A Temperature- and Aging-Compensated *RC* Oscillator With ±1030-ppm Inaccuracy From −40 °C to 85 °C After Accelerated Aging for 500 h at 125 °C

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***Abstract*— This article presents a temperature- and aging-compensated *RC* oscillator (TACO) in which the long-term drift of the main oscillator is compensated by periodically locking its frequency to that of the less-aged reference oscillator. To improve the long-term stability of the TACO, it employs techniques, such as the use of higher activation energy (E_a) resistors, switched dual *RC* branches to mitigate stress from dc-current-induced electromigration (EM), and duty cycling to slow down the aging rate of the reference oscillator. Using the proposed techniques, a prototype 100-MHz *RC* oscillator fabricated in a 65-nm CMOS process achieves an inaccuracy of ±1030 ppm from −40 °C to 85 °C after 500 h of accelerated aging at 125 °C, with 5.1-ps$_{rms}$ period jitter and a power efficiency of 1.4 μW/MHz.**

***Index Terms*— AC current stress, activation energy, aging compensation, delta–sigma modulator (DSM), duty cycling, pulse density modulation, *RC* oscillator, temperature compensation.**

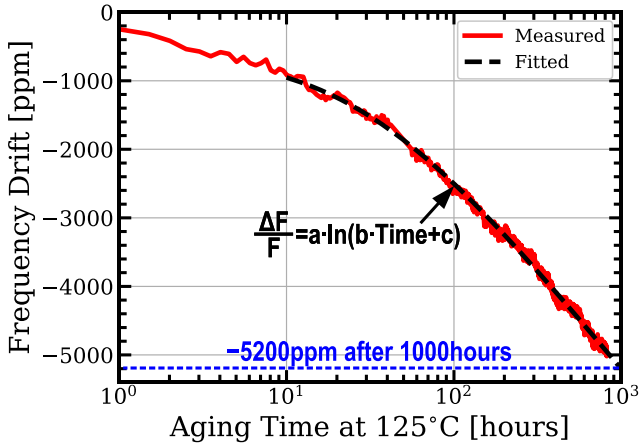

Fig. 1. *RC* oscillator aging with a p-poly resistor.

I. Introduction

INTEGRATED *RC* oscillators are becoming increasingly popular as clock sources in various applications, replacing bulky crystal or MEMS oscillators due to their smaller physical footprint, lower power consumption, and lack of expensive off-chip components [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24]. These oscillators achieve excellent short-term frequency stability through novel methods that compensate for the frequency inaccuracy caused by the temperature coefficient (TC) of resistors used in the reference *RC* networks [11], [12], [16], [17], [19], [20], [22]. Over the past decade, numerous papers have been published to improve the temperature stability of *RC* oscillators, resulting in a significant improvement in their frequency accuracy, which is now comparable to crystal oscillators [22]. Despite their exceptional performance, the lack of information on the aging behavior of *RC* oscillators and their inability to guarantee long-term performance limit their commercial deployment.

Resistor aging is the primary contributor to long-term frequency drift in *RC* oscillators, and p-poly resistors, commonly used as reference resistors in *RC* oscillators for their high sheet resistance, small area, and relatively low-temperature coefficient of resistance (TCR), are particularly prone to aging [25], [26]. Accelerated aging tests on standalone p-poly resistors have shown that their resistivity can change by over 0.5% after 1000 h at 150 °C [27]. To evaluate the effect of resistor aging on the oscillator's frequency, a temperature-compensated frequency-locked loop (FLL)-based *RC* oscillator prototype using a p-poly resistor was designed, and its long-term stability was measured by baking it at 125 °C. The results, plotted in Fig. 1, show that resistor aging significantly affects the oscillator's frequency, causing more than 5000-ppm drift after 1000 h [23]. In addition, a 5000-ppm frequency drift of *RC* oscillators using a p-poly resistor was observed from an aging experiment at 150 °C for one week [24]. To address this issue, this article presents circuit techniques to enhance the long-term stability of *RC* oscillators and compensate for frequency drift caused by aging

Manuscript received 14 May 2023; revised 19 August 2023; accepted 16 September 2023. Date of publication 11 October 2023; date of current version 28 November 2023. This article was approved by Associate Editor Drew Hall. This work was supported by Semiconductor Research Corporation (SRC) under Grant GRC Task 2810.036. *(Corresponding author: Kyu-Sang Park.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2023.3320709.

Digital Object Identifier 10.1109/JSSC.2023.3320709

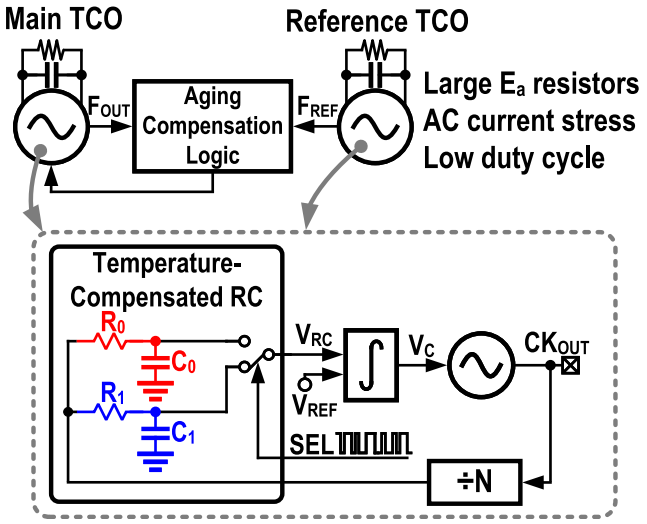


Fig. 2. Proposed aging compensation scheme and FLL-based TCO architecture.

without the need for external stable sources. A 100-MHz FLL-based *RC* oscillator prototype is fabricated in a 65-nm CMOS process, and it achieves an inaccuracy of ±1030 ppm from −40 °C to 85 °C after 500 h of accelerated aging at 125 °C, with 5.1-ps_{rms} period jitter and a power efficiency of 1.4 μW/MHz.

The rest of this article is organized as follows. Section II presents the proposed architecture. Circuit implementation details of key building blocks are described in Section III. Experimental results from the test chips are shown in Section IV. Key contributions of this article are summarized in Section V.

II. Proposed Architecture

A simplified block diagram of the proposed temperature- and aging-compensated *RC* oscillator (TACO) is shown in Fig. 2. The TACO consists of a main temperature-compensated oscillator (TCO), a reference TCO, and an aging compensation logic. The TCO operates continuously, while its long-term frequency drift due to aging is addressed by periodically synchronizing it with the less-aged reference oscillator. The main as well as the reference TCO both adopt an identical FLL-based architecture, which leverages two reference resistors (R_0 and R_1), as depicted in Fig. 2. The reference oscillator, however, is heavily duty cycled to prevent it from aging.

A. Techniques for Long-Term Stability Improvement

The TACO system uses various techniques to enhance its long-term stability. One such technique involves using reference resistors with higher activation energy (E_a) to increase their lifetime. Various resistors are available in standard CMOS technology, including poly, diffusion, and metal resistors, each governed by distinct aging mechanisms. The primary factor responsible for the shift in poly resistance is the depassivation of hydrogen at grain boundaries, coupled with hydrogen migration within an electric field [26], [27], [28], [29], [30], [31]. On the other hand, the alteration in metal resistance predominantly stems from electromigration (EM), a phenomenon that propels the migration of metal atoms and consequently leads to the formation of voids within the resistor's structure [31], [32], [33]. Despite the divergence in their aging mechanisms, these resistors' anticipated time to failure (TTF) can be empirically modeled as follows:

$$\mathrm{TTF} = A \cdot J^{-n} \cdot \exp\left(\frac{E_a}{kT}\right), \quad J > 0 \tag{1}$$

$$\mathrm{TTF} = A \cdot \exp(-nJ) \cdot \exp\left(\frac{E_a}{kT}\right) \tag{2}$$

where A is an empirically determined constant, J is current density (A/cm^2), n is the empirically determined current density factor, E_a is the activation energy (eV), k is Boltzmann's constant, and T is the absolute junction temperature of the resistor during the aging stress. The TTF estimation can be achieved through Black's approach, as demonstrated by (1) [29], [31], [32], [33], or by employing an alternate model, as depicted in (2) [26], [29], [31] to accommodate low current density (J) scenarios. E_a represents a vital aging-associated parameter obtained by fitting aging experimental data with (1) or (2). Its value is influenced by the fabrication technique employed and the predominant aging mechanism of resistors. These equations illustrate that a resistor's TTF experiences exponential growth as E_a becomes larger. The p-poly resistors have a low E_a of 0.477 eV and suffer from higher degradation caused by aging stress [26], [27]. Compared with p-poly resistors, n-poly resistors have a higher E_a of 0.68 eV and longer TTF, making them more suitable for the better long-term stability of the oscillators [26]. Metal interconnect or back-end-of-line (BEOL)-type resistors also have higher E_a and exhibit smaller resistivity shifts under electrical and temperature stress than poly resistors [31], [34]. For instance, the copper interconnects and VIA chains are characterized by E_a values spanning from 0.82 to 0.93 eV [34].

Another technique is to design the reference resistors to have the current direction alternate periodically to reduce the stress caused by electromigration induced by the dc current. The TTF of poly resistors increases monotonically with the frequency of ac current stress [35]. Electron wind induces the oscillation of dopant atoms by subjecting poly resistors to ac current stress. However, this oscillation does not result in the net movement of the dopant until it is trapped at a defect. The higher the frequency of the stress, the shorter the distance the dopant will travel, which reduces the probability of the dopant encountering a defect in the polysilicon, resulting in an improved TTF of the resistor [35]. Metal-type resistors also show better TTF with ac current stress than dc stress [33]. The circuit implementation for alternating current through reference resistors is described in detail in Section II-B.

The third technique involves using duty cycling to slow down the aging rate of the reference oscillator used to calibrate the main oscillator. The aging rate of poly and metal resistors in a standard CMOS process depends on the duty cycle. Lower duty cycles lead to slower aging rates of the resistors [30], [33]. By reducing the on-time of the reference oscillator, the amount of time that a current flows through the active devices and interconnects decreases, which also can slow down the

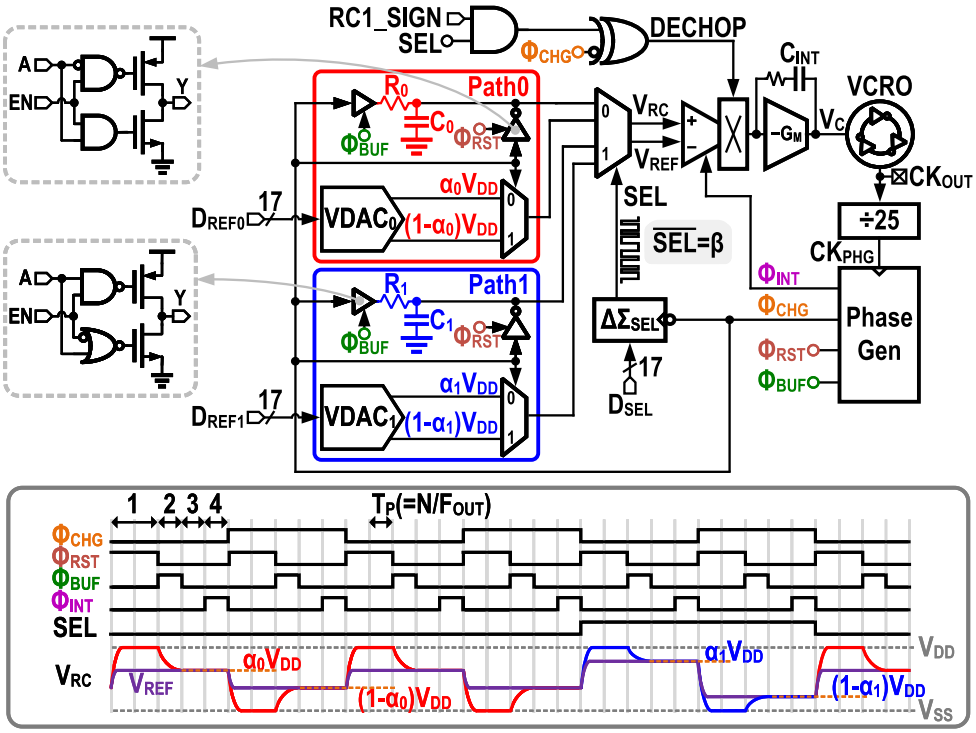


Fig. 3. Detailed TCO architecture.

rate of specific aging mechanisms, such as hot carrier injection (HCI) and EM.

B. Detailed TCO Architecture

The TCO comprises two RC branches (R_0C_0 and R_1C_1), a $G_M - C$ integrator, a voltage-controlled ring oscillator (VCRO), a divider, differential voltage $\Delta\Sigma$ digital-to-analog converters (VDACs), a phase generator, and a $\Delta\Sigma$ modulator (DSM), as shown in Fig. 3. The VCRO clock is divided by $N(=25)$ and fed to the phase generator, which generates clocks, Φ_{CHG}, Φ_{RST}, Φ_{BUF}, and Φ_{INT}. These clock phases are used to control the switching sequence in the RC branch, such that the difference between the track-and-held voltage V_{RC} generated from the RC branch and V_{REF} provided by VDAC represents the error between the desired frequency and VCRO (F_{OUT}) frequency. The error voltage, $V_{\mathrm{ERR}}(=V_{RC} - V_{\mathrm{REF}})$, is integrated by the integrator and used to drive the VCRO toward the frequency lock. To perform temperature compensation, the DSM generates mux select signal SEL, which enables either Path_0 consisting of R_0C_0 branch and VDAC_0 when SEL $= 0$ or Path_1 consisting of R_1C_1 branch and VDAC_1 when SEL $= 1$, as described later. The TCO operates in four phases, as illustrated in the timing waveforms in Fig. 3. The first phase commences with SEL $= 0$ and $\Phi_{\mathrm{CHG}} = 0$, during which the inverter of Path_0 resets C_0 to V_{DD} when $\Phi_{\mathrm{RST}} = 1$ (reset phase). In the second phase, when $\Phi_{\mathrm{BUF}} = 1$, the buffer of Path_0 is activated and discharges C_0 via R_0 for T_P duration to $V_{RC0,\mathrm{DCHG}} = \exp(-T_P/R_0C_0)V_{\mathrm{DD}}$, where $T_P = N/F_{\mathrm{OUT}}$. The value of $V_{RC}(=V_{RC0,\mathrm{DCHG}})$ exceeds $V_{\mathrm{REF}}(=\alpha_0 V_{\mathrm{DD}})$ if F_{OUT} is greater than the target output frequency, and vice versa. The third phase occurs when Φ_{RST}, Φ_{BUF}, and Φ_{INT} are all zero, providing sufficient time for the redistribution of the charge stored in the parasitic capacitor of the resistor and for V_{RC} to stabilize. In the final phase, $\Phi_{\mathrm{INT}} = 1$, and the integrator is enabled (integration phase); V_{ERR} $(= V_{RC0,\mathrm{DCHG}} - \alpha_0 V_{\mathrm{DD}})$ is integrated for T_P duration, generating the control voltage V_C of the VCRO. In the subsequent cycle with $\Phi_{\mathrm{CHG}} = 1$, C_0 is reset to V_{SS} and charged for a duration of T_P, resulting in $V_{RC0,\mathrm{CHG}} = (1 - \exp(-T_P/R_0C_0))V_{\mathrm{DD}}$, and then, V_{ERR} $(= V_{RC0,\mathrm{CHG}} - (1 - \alpha_0)V_{\mathrm{DD}})$ is integrated for T_P duration. At Φ_{CHG}, the R_0C_0 branch is chopped, and the first-stage output of the integrator is dechopped via the DECHOP signal. By reversing the current flow direction in resistor R_0 during periodic discharge and charge operations, the EM-induced stress is significantly minimized, and long-term stability is enhanced compared with unidirectional current flow. Furthermore, the discharge and charge operation occurs with an inherent duty cycle of 20% only when $\Phi_{\mathrm{BUF}} = 1$, which can decrease the aging rate of the resistor.

Assuming that SEL $= 0$ and Path_0 is selected, the output frequency, F_{OUT0}, of the TCO circuit is given by

$$F_{\mathrm{OUT0}} = \frac{N}{R_0C_0 \ln(1/\alpha_0)}. \tag{3}$$

In the steady state with SEL $= 0$, $V_{RC0,\mathrm{DCHG}}$ and $V_{RC0,\mathrm{CHG}}$ are equal to $\alpha_0 V_{\mathrm{DD}}$ and $(1-\alpha_0)V_{\mathrm{DD}}$, respectively, due to feedback loop operation. Neglecting the TC and aging of C_0 and α_0, the output frequency TC is determined by the TC and aging properties of R_0 alone. To compensate for the TC of R_0, Path_1, consisting of an R_1C_1 branch and a VDAC_1, is added. In the steady state with SEL $= 1$ and Path_1 selected, the TCO output frequency, F_{OUT1}, can be expressed as follows:

$$F_{\mathrm{OUT1}} = \frac{N}{R_1C_1 \ln(1/\alpha_1)} \tag{4}$$

where the R_1C_1 branch is designed to have the same time constant but exhibit a different TC from that of R_0C_0 branch.

The first-order temperature compensation is achieved by modulating the SEL signal with the first-order DSM. If R_0C_0 and R_1C_1 have opposite-sign TCs, the averaged V_{ERR} is forced to zero in the steady state due to the high loop gain of the FLL and can be expressed as follows:

$$\overline{V_{\mathrm{ERR}}} = (1-\beta)V_{\mathrm{ERR0}} + \beta V_{\mathrm{ERR1}} = 0 \tag{5}$$

where V_{ERR0} and V_{ERR1} represent the error between the TCO output frequency and F_{OUT0} and F_{OUT1}, respectively, and β is the average of the pulse-density-modulated SEL sequence. This equation can be rewritten as follows:

$$(1-\beta)(F_{\mathrm{OUT}} - F_{\mathrm{OUT0}}) + \beta(F_{\mathrm{OUT}} - F_{\mathrm{OUT1}}) \cong 0 \tag{6}$$

$$F_{\mathrm{OUT}} \cong (1-\beta)F_{\mathrm{OUT0}} + \beta F_{\mathrm{OUT1}} \tag{7}$$

assuming that R_0C_0 and R_1C_1 have similar time constants. There exists an optimum β (β_{OPT}) at which F_{OUT} is insensitive to temperature changes to the first order.

However, if both R_0C_0 and R_1C_1 have positive TCs, the temperature dependency of F_{OUT} cannot be compensated for by varying the average SEL sequence. To overcome this issue, the $RC1$_SIGN is added to the DECHOP signal logic, and by setting $RC1$_SIGN to one, the sign of integrator G_M is reversed when SEL $=1$, producing a negative sign in the second term of the averaged V_{ERR} equation [see (5)], given by

$$\overline{V_{\mathrm{ERR}}} = (1-\beta)V_{\mathrm{ERR0}} - \beta V_{\mathrm{ERR1}} = 0. \tag{8}$$

This equation can also be expressed as follows:

$$(1-\beta)(F_{\mathrm{OUT}} - F_{\mathrm{OUT0}}) - \beta(F_{\mathrm{OUT}} - F_{\mathrm{OUT1}}) \cong 0 \tag{9}$$

$$F_{\mathrm{OUT}} \cong \frac{(1-\beta)F_{\mathrm{OUT0}} - \beta F_{\mathrm{OUT1}}}{1-2\beta} \tag{10}$$

assuming that $R_0C_0 \cong R_1C_1$. Inverting the sign of integrator G_M when SEL $=1$ facilitates the implementation of first-order TC compensation through the utilization of distinct positive TC R_0C_0 and R_1C_1 branches. This action, however, introduces instantaneous positive feedback into the FLL loop, ultimately reducing its effective loop gain during the steady state. In Section IV, both simulation and measurement results revealed that for optimal first-order TC compensation, an optimal value of β (denoted as β_{OPT}) is approximately 0.02. This outcome is attributed to the substantial TC ratio between R_1C_1 and R_0C_0.

C. Trimming Procedure

Fig. 4 illustrates the two-point trimming process, which first calibrates both α_0 and α_1 of TCO to the target frequency F_{TAR} at 85 °C and then switches to −40 °C to calibrate β for the first-order TC compensation. The detailed steps of this process are as follows. Initially, Path_0 is chosen by setting the SEL signal to zero. Then, a binary search is conducted for α_0 of VDAC_0 to attain the target frequency F_{TAR} with $F_{\mathrm{OUT}} = F_{\mathrm{OUT0}} = F_{\mathrm{TAR}}$ at a temperature of 85 °C. Subsequently, Path_1 is selected by setting the SEL signal to one, and a similar search is performed for α_1 of VDAC_1 to achieve $F_{\mathrm{OUT}} = F_{\mathrm{OUT1}} = F_{\mathrm{TAR}}$. The process is completed by setting the temperature to −40 °C. If R_0C_0 and R_1C_1 have opposite sign TCs, then $RC1$_SIGN is set to zero, otherwise to one. A binary search is then conducted for β that causes $F_{\mathrm{OUT}} = F_{\mathrm{TAR}}$. These steps provide alpha and beta value estimates, which are then fine-tuned to obtain near-optimal values. The process of fine-tuning encompassed manually sweeping across the estimated alpha and beta values. The optimal alpha and beta values were subsequently obtained via linear interpolation. Finally, α_0, α_1, and β are truncated to 17-bit digital words D_{REF0}, D_{REF1}, and D_{SEL} in Fig. 3, respectively. This trimming process is performed for both the main and reference TCOs.

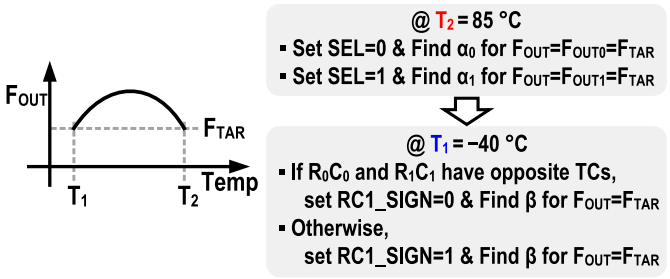


Fig. 4. Two-point trimming logic.

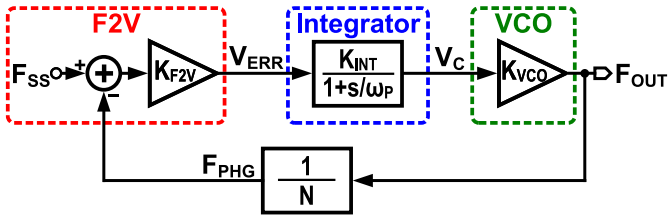


Fig. 5. Linearized FLL model.

D. FLL Design

The TCO's discrete-time operation can be represented as a linearized FLL, illustrated in Fig. 5, comprising a frequency-to-voltage (F2V) converter, an integrator, and a voltage-controlled oscillator (VCO). This model is utilized to determine loop parameters and ensure stable closed-loop operation of the TCO. The two RC branches, modulated by signal SEL with an average density of β_{OPT}, act as a temperature-compensated RC branch that serves as F2V with the divided VCO clock $F_{\mathrm{PHG}}(=F_{\mathrm{OUT}}/N = 1/T_P)$ as input and the error voltage $V_{\mathrm{ERR}}(=V_{RC} - V_{\mathrm{REF}})$ as output during integration phase ($\Phi_{\mathrm{INT}} = 1$). F_{PHG} is equal to F_{SS} in the steady state. Since $R_0C_0 \cong R_1C_1$ and $\beta_{\mathrm{OPT}} \sim 0.02$, the temperature-compensated RC branch's time constant is approximately equal to R_0C_0. When $\Phi_{\mathrm{CHG}} = 0$, V_{ERR} of F2V can be expressed as follows:

$$V_{\mathrm{ERR}} = V_{RC0,\mathrm{DCHG}} - V_{\mathrm{REF}} \tag{11}$$

$$= V_{\mathrm{DD}}e^{-1/(R_0C_0F_{\mathrm{PHG}})} - V_{\mathrm{REF}}. \tag{12}$$

The gain of F2V, K_{F2V}, can be derived as follows:

$$K_{\mathrm{F2V}} = \frac{dV_{\mathrm{ERR}}}{dF_{\mathrm{PHG}}} = \frac{V_{\mathrm{DD}}}{R_0C_0F_{\mathrm{PHG}}^2}e^{-1/(R_0C_0F_{\mathrm{PHG}})} \tag{13}$$

$$= \frac{V_{\mathrm{DD}}N^2}{R_0C_0F_{\mathrm{OUT}}^2}e^{-N/(R_0C_0F_{\mathrm{OUT}})}. \tag{14}$$

When $\Phi_{\mathrm{CHG}} = 1$, the V_{ERR} and K_{F2V} of F2V can be written as follows:

$$V_{\mathrm{ERR}} = V_{RC0,\mathrm{CHG}} - V_{\mathrm{REF}} \tag{15}$$

$$= V_{\mathrm{DD}}\left(1 - e^{-1/(R_0 C_0 F_{\mathrm{PHG}})}\right) - V_{\mathrm{REF}} \tag{16}$$

$$K_{\mathrm{F2V}} = -\frac{V_{\mathrm{DD}} N^2}{R_0 C_0 F_{\mathrm{OUT}}^2} e^{-N/(R_0 C_0 F_{\mathrm{OUT}})} \tag{17}$$

where K_{F2V} has the same magnitude of (14) but a negative sign.

The Miller effect, caused by C_{INT} and the second-stage voltage gain (refer to Fig. 3), results in the integrator having a dominant pole at its first-stage output. This can be represented as a simple one-pole system, as shown in Fig. 5, with K_{INT} and ω_P denoting the voltage gain and the dominant pole of the integrator, respectively. As the integrator operates exclusively during the integration phase, and its first-stage output is dechopped by the DECHOP signal (see Fig. 3), the effective transconductance of its first-stage $G_{M1,\mathrm{EFF}}$ is equivalent to $0.2G_{M1}$ when $\Phi_{\mathrm{CHG}} = 0$ and $-0.2G_{M1}$ when $\Phi_{\mathrm{CHG}} = 1$, where G_{M1} is the transconductance of the first stage. The K_{INT} and ω_P are given as follows:

$$K_{\mathrm{INT}} = G_{M1,\mathrm{EFF}} R_{O1} A_2 \tag{18}$$

$$\omega_P \approx \frac{1}{(A_2 + 1) R_{O1} C_{\mathrm{INT}}} \tag{19}$$

where R_{O1} is the output impedance of the integrator's first stage and A_2 is the voltage gain of its second stage.

From Fig. 5, the loop gain, LG(s), is given by

$$\mathrm{LG}(s) = K_{\mathrm{F2V}} \frac{G_{M1,\mathrm{EFF}} R_{O1} A_2}{1 + s(A_2 + 1) R_{O1} C_{\mathrm{INT}}} \frac{K_{\mathrm{VCO}}}{N} \tag{20}$$

where K_{VCO} is the voltage-to-frequency gain of the VCO. Due to the chopping/dechopping operation, K_{F2V} and $G_{M1,\mathrm{EFF}}$ have the same sign, irrespective of Φ_{CHG}, resulting in the loop maintaining negative feedback. The closed-loop bandwidth of the loop can be approximated by its unity gain frequency in rad/s, denoted as ω_{UGF}, which is equal to

$$\omega_{\mathrm{UGF}} \approx \frac{G_{M1,\mathrm{EFF}} K_{\mathrm{F2V}} K_{\mathrm{VCO}}}{C_{\mathrm{INT}} N}. \tag{21}$$

To achieve FLL stability and minimize ΔΣ quantization error, the unity gain frequency is set to approximately 1 kHz.

III. Circuit Implementation

The schematic of the R_1C_1 branch is illustrated in Fig. 6. It comprises a controllable resistor R_1, a capacitor C_1, a buffer for discharging/charging C_1, and an inverter for resetting C_1. To cope with process variation of the resistor R_1, eight buffers are connected to eight taps of the segmented resistor R_1, and one of the buffers is chosen by 8-bit select signal SEL_$R1$. This programmability allows tuning of R_1C_1 to have comparable time constant to that of R_0C_0.

The reference voltage (V_{REF}) in Fig. 3 is produced through differential ΔΣ DACs illustrated in Fig. 7. The 17-bit digital input ($D_{\mathrm{REF0/1}}$) is first truncated to 1 bit via a second-order DSM that operates at a switching frequency of $F_{\mathrm{OUT}}/10$ (=10 MHz). Using a buffer and an inverter, it is then

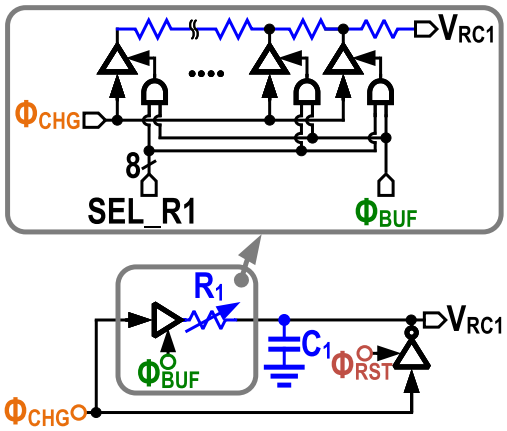


Fig. 6. Schematic of the R_1C_1 branch.

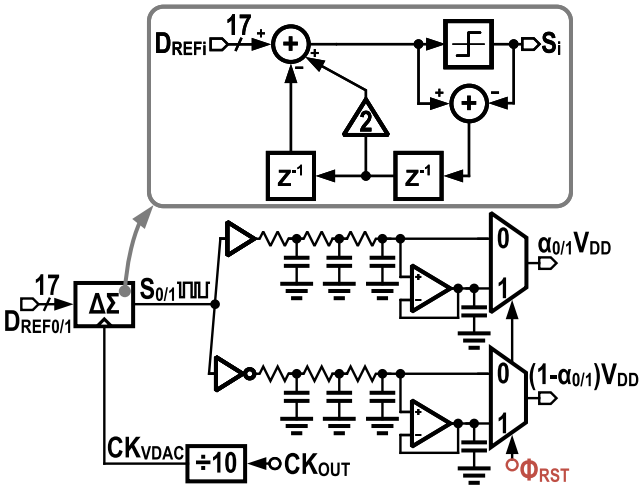


Fig. 7. Schematic of the VDAC.

transformed into a pulse-density-modulated sequence $S_{0/1}$. This process provides superior reference voltage accuracy (better than 8 ppm) and output frequency tuning resolution (22.5 ppm). To avoid potential aging effects, the supply and ground voltage levels (V_{DD} and V_{SS}) are used for the 1-bit sequence conversion. The DSM employs the error feedback architecture shown in Fig. 7 and generates the second-order shaped quantization error, which is suppressed by third-order RC low-pass filters (LPFs) with 16-kHz 3-dB cutoff frequency. The differential VDAC outputs can be expressed as $\alpha_{0/1}V_{\mathrm{DD}}$ and $(1 - \alpha_{0/1})V_{\mathrm{DD}}$, where $\alpha_{0/1}$ denotes the average of sequence $S_{0/1}$. To prevent charge sharing between the parasitic capacitor located at the input of the integrator and the capacitors within LPF, the output of the unity gain buffer is connected to V_{REF} in Fig. 3 when Φ_{RST} equals 1. This is done to charge the input capacitor of the integrator initially. Conversely, when Φ_{RST} equals 0, the unbuffered LPF output is connected to avoid inaccuracies stemming from the buffer's offset.

The integrator utilizes a two-stage $G_M - C$ topology, as shown in Fig. 8. The RC branches are chopped at 0.4-MHz Φ_{CHG}, and the first-stage output of the integrator is dechopped by the DECHOP signal to remove offset and flicker noise, thus improving the temperature stability and Allan deviation of the TCO. The transconductance of the first stage is 2 μS, and

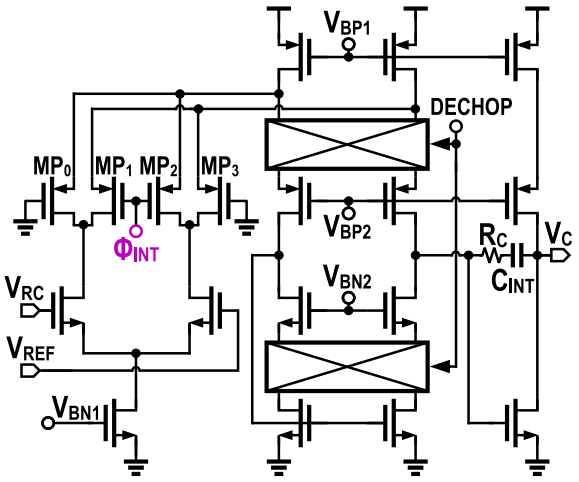


Fig. 8. Schematic of the $G_M - C$ integrator.

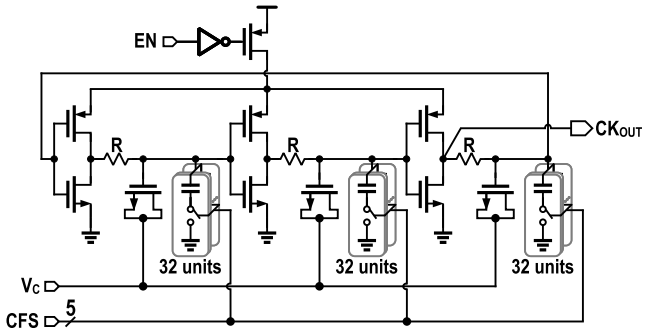


Fig. 9. Schematic of the VCRO.

the PMOS switches (MP_0, MP_1, MP_2, and MP_3) steer the tail current equally to the folding node when $\Phi_{INT} = 0$, preventing integration of the input signal. Integration is enabled by turning off MP_1 and MP_2 when $\Phi_{INT} = 1$. The mismatch between MP_{0-3} introduces an additional input-referred integrator offset, which the chopping/dechopping operation removes. The second stage of the integrator enhances the gain and establishes a large integrator time constant by using a capacitor $C_{INT} = 8.8$ pF. The Miller effect results in a dominant pole at the output of the first stage, stabilizing the loop and limiting the loop bandwidth to ~1 kHz, which is necessary to suppress the shaped quantization error of DSMs. To remove the right-half-plane (RHP) zero caused by the Miller effect, a resistor R_C is used. The high gain of the integrator allows the dc loop gain to be more than 126 dB, sufficient to suppress the supply and temperature sensitivity of the VCRO effectively.

Fig. 9 displays the VCO schematic, which consists of three delay elements implemented with an inverter, a poly resistor, and controllable capacitors, along with a power-gating PMOS switch. The resistor and capacitors' sensitivity primarily determines the delay element's temperature sensitivity. The VCO's nominal frequency is coarsely tuned to 100 MHz using 5-bit binary-weighted metal-oxide-metal (MOM) capacitor arrays and finely tuned using MOS varactors. When the reference TCO is unused, the power-gating PMOS switch is turned off to reduce leakage current.

The schematic of the on-chip aging compensation logic is depicted in Fig. 10. A feedback loop is utilized to counteract

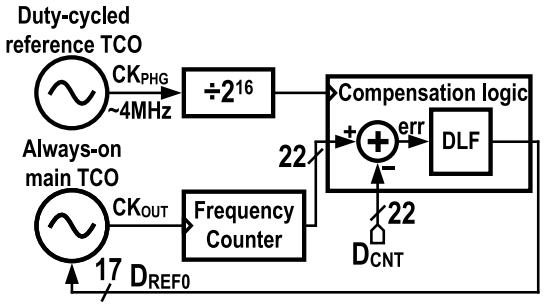


Fig. 10. On-chip aging compensation logic.

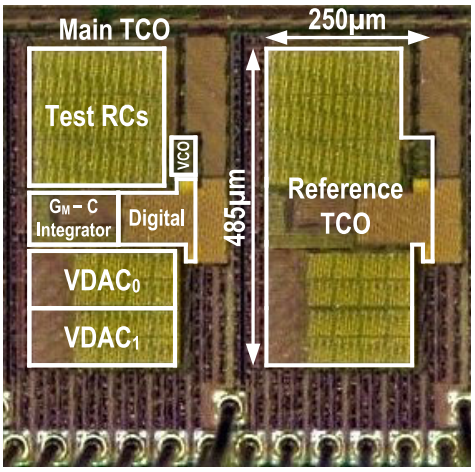


Fig. 11. Die micrograph.

the frequency drift caused by aging in the main oscillator, which locks the main TCO's frequency to a less-aged reference TCO. The frequency error is measured by counting the number of main oscillator cycles within 2^{16} periods of the reference clock CK_{PHG}. This clock is obtained by dividing the reference TCO output clock by 25. Then, the ideal count represented by the 22-bit D_{CNT} is subtracted from the counter output. The resulting error is accumulated by the digital loop filter (DLF) and is used to adjust the 17-bit digital word D_{REF0}, which tunes the main oscillator's frequency.

IV. Measurement Results

The TACO prototype was fabricated in a 65-nm CMOS process and packaged in a plastic quad flat no-lead (QFN) package. Fig. 11 shows the prototype's die micrograph, and its active area is 0.22 mm^2. To fully characterize the impact of resistor aging on frequency drift, RC branches with different resistors (a p-poly resistor, an n-poly resistor, an n-diffusion resistor, a silicided p-poly resistor, a metal interconnect resistor, a VIA resistor, and so on) were implemented in the prototype with the option of choosing any one or two RC branches out of them. Each RC branch comprises a 50-kΩ resistor and a 7.2-pF capacitor implemented with an MOM capacitor situated beneath an MIM capacitor. If we count only the two RC branches that use n-poly and VIA resistors utilized in the experiment, the total area is reduced to 0.15 mm^2. The VIA and metal resistors are implemented using a variable resistor labeled as R_1, as shown in Fig. 6. This R_1 resistor is engineered to cover a range extending from 0.5 to 2 times the

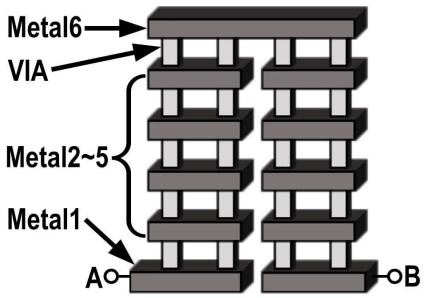


Fig. 12. Unit segment of the VIA resistor.

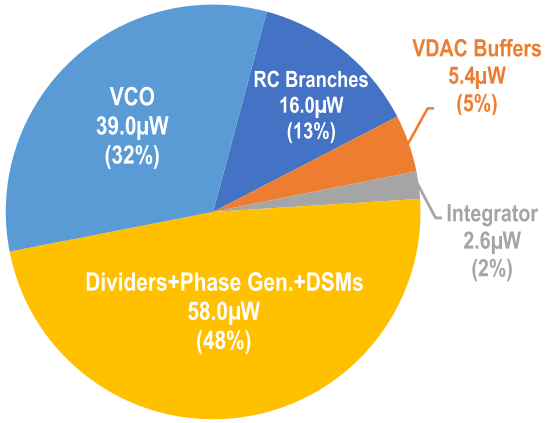


Fig. 13. Power breakdown of the single TCO.

standard 50-kΩ resistance, providing the capability to accommodate significant fluctuations in VIA and metal resistance. The VIA resistor implementation consists of 7980 individual unit segments, culminating in a total resistance of 100 kΩ, all encapsulated within an area measuring 3500 μm^2. Fig. 12 shows one such unit segment, which consists of VIA stacks and metal layers 1–6. Double VIAs connect the upper and lower routing metal layers instead of a single VIA to enhance reliability and minimize yield loss due to VIA failures. The metal resistor is constructed in a serpentine configuration, utilizing metal layers 1–6 to attain a resistance of 100 kΩ. This resistor occupies a total area of 4050 μm^2.

The prototype is powered by three external power supplies with the voltage levels of 1.15, 1, and 1 V for the analog, digital, and VCO blocks, respectively. The TCO's total power consumption is 121 μW, and its power breakdown is illustrated in Fig. 13. Digital blocks, such as dividers, phase generators, and DSMs, consume 58.0 μW (48%) from the 1-V supply. The VCO accounts for 39 μW (32%), while the *RC* branches, VDAC unity-gain buffers, and the integrator use 20% of the TCO power from the 1.15-V supply. The average power consumption of the TACO (including main and reference TCOs) is 142 μW with 21 μW of the power coming from the leakage current of the disabled reference TCO. When the aging compensation function enables, the TACO consumes 263 μW instantaneously. However, this increase has an insignificant effect on the TACO's average power consumption because of its 0.1% duty cycle.

A. Aging Test Using Standalone Resistor

An accelerated aging test was conducted on the TCO with different resistors to evaluate its aging behavior. During the testing phase, only one resistor was active at any given time, and the observed frequency drift and comparisons are illustrated in Fig. 14 and summarized in Table I. The continuous operation of the TCO with an n-poly resistor resulted in a long-term frequency drift of within ±1033 ppm after 817 h at 125 °C, as indicated in Fig. 14(a). Conversely, the TCO with a duty cycle of 0.1% exhibited a frequency drift within ±385 ppm, highlighting the capacity of duty cycling to mitigate aging effects. Similarly, the TCOs employing various resistor types in Fig. 14 demonstrated reduced long-term frequency drift when subjected to 0.1% duty cycling compared with continuous operation. Analyzing the aging behavior of TCOs with different resistor types, TCOs equipped with p-poly resistors exhibited the most significant frequency drift of ±5200 ppm, as illustrated in Fig. 1. In contrast, duty-cycled TCOs employing alternative resistors displayed resilience in maintaining a stable frequency under aging conditions, as evidenced in Fig. 14. To investigate the impact of chopping/dechopping operation and alternating current direction through the *RC* branches on the frequency, the frequency drift of TCOs using VIA resistors without these techniques was measured for 817 h of aging at 125 °C, as illustrated in Fig. 15. The worst frequency drift was ±1630 ppm for the TCO with a duty cycle of 0.1% and within ±1230 ppm for the 100% duty-cycled TCO. These results demonstrate a significant frequency drift compared with the measurements in Fig. 14(d), indicating that the chopping operation and alternating current direction through *RC* branches can reduce the aging effect caused by long-term instability of integrator offset and dc-current-induced EM.

TABLE I
MEASURED TCO FREQUENCY DRIFT COMPARISON WITH DIFFERENT RESISTORS

Resistor Type	100% Duty-Cycled TCO Min/Max Frequency Drift Over Aging Time [ppm]	0.1% Duty-Cycled TCO Min/Max Frequency Drift Over Aging Time [ppm]
n-poly	0 / 1033	-128 / 385
n-diffusion	-505 / 216	-278 / 243
Silicided p-poly	-98 / 523	-464 / 73
VIA	-89 / 436	-232 / 184
Metal	-283 / 199	-267 / 204

B. Aging Test After Two-Point Trim

The selection of resistors for the main and reference TCOs was based on the aging behavior of the TCOs described earlier. The frequency drift observed in the standalone aging test was similar among TCOs utilizing various resistor types, as depicted in Fig. 14. Nevertheless, TCOs employing n-poly and VIA resistors displayed superior frequency accuracy both before and after aging when compared with their counterparts. This advantage can be attributed to their smaller second-order TCs. Based on their superiority, in both TCOs, n-poly and VIA resistors were selected as R_0 and R_1, respectively. The digital control words D_{REF0}, D_{REF1}, and D_{SEL} were determined for each sample by trimming the TCOs at 85 °C and −40 °C for $F_{\mathrm{OUT}} = F_{\mathrm{TAR}} = 100$ MHz. The β_{OPT} value was calculated to be ∼0.02, as the ratio of R_1C_1 TC (1000 ppm/°C) to R_0C_0 product (20 ppm/°C) was found to be large. The accelerated aging test was performed on the two-point trimmed TCOs for 500 h at 125 °C, and the results from 14 samples are shown in

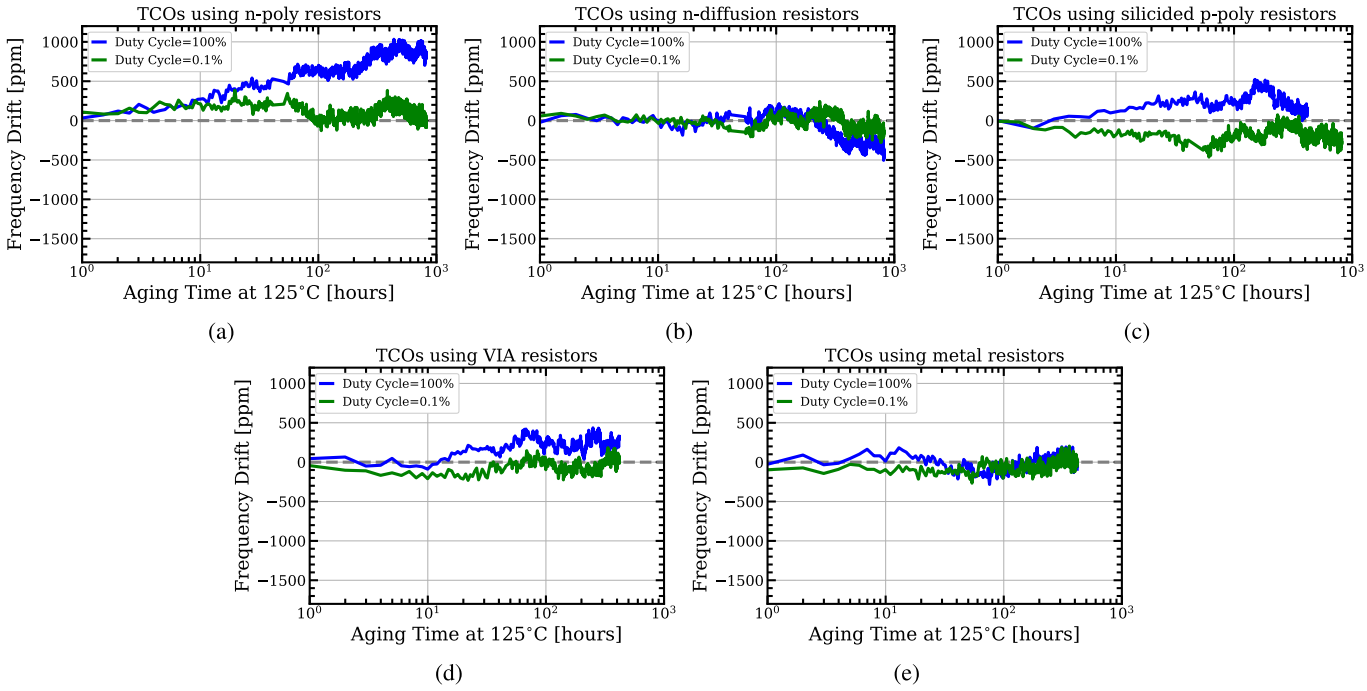


Fig. 14. Measured frequency drift of TCOs when always-on and with 0.1% duty cycle using (a) n-poly resistors, (b) n-diffusion resistors, (c) silicided p-poly resistors, (d) VIA resistors, and (e) metal resistors.

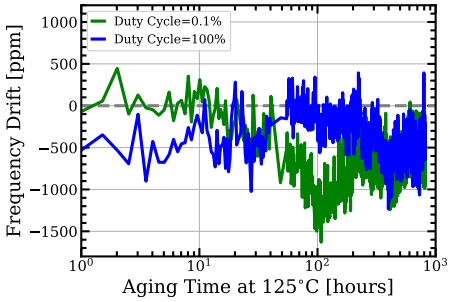


Fig. 15. Measured frequency drift of TCOs using VIA resistors without chopping and without alternating current direction in RC branches.

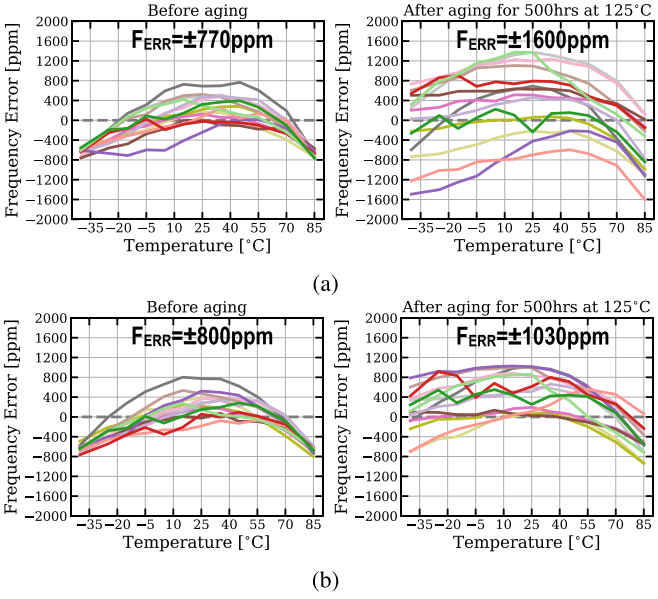


Fig. 16. Measured frequency inaccuracy of main TCOs using n-poly and VIA resistors before and after aging (a) without the aging compensation and (b) with the compensation.

Fig. 16. The inaccuracy at trim temperature points before aging in Fig. 16 is not zero, which we believe is limited by ±0.2 °C short-term temperature variation of our temperature chamber (TestEquity Model 107) during trimming. The frequency accuracy of the main TCOs before aging was ±770 ppm, but it degraded to ±1600 ppm after aging, indicating an 830-ppm degradation due to aging [Fig. 16(a)]. However, with the proposed aging compensation, which involves locking the frequency of the always-on main TCO to that of a 0.1% duty-cycled reference TCO at 1-h intervals, the frequency accuracy of the main TCOs was ±800 ppm before aging. It degraded to ±1030 ppm after aging, indicating degradation of only 230 ppm due to aging [Fig. 16(b)]. The equivalent lifetime of the prototype can be estimated using the Arrhenius empirical prediction model as follows:

$$t_{\text{life}} = \text{AF} \cdot t_{\text{stress}} \tag{22}$$

$$\text{AF} = \exp\left(\frac{E_a}{k}\left(\frac{1}{T_u} - \frac{1}{T_s}\right)\right) \tag{23}$$

where t_{life} is the equivalent lifetime, t_{stress} is the time the prototype was tested at the accelerated stress temperature T_s, AF is the acceleration factor, E_a is the activation energy, k is Boltzmann's constant, and T_u is the temperature at normal use. With the assumption that the aging mechanism in the prototype is dominated by an n-poly resistor with an E_a of 0.68 eV [26], along with a normal use temperature (T_u) of 50 °C, conducting 500 h of accelerated aging at 125 °C is equivalent to 5.7 years of the prototype's lifetime. Fig. 17 depicts the outcomes of an aging test carried out on seven

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ON-CHIP *RC* OSCILLATORS

	This Work		An [24] ISSCC23	Ji [36] ISSCC22	Gurleyuk [22] JSSC22	Park [20] JSSC22	Khashaba [19] JSSC21	Jiang [16] ISSCC21	Choi [17] JSSC21
Process	65nm		180nm	180nm	180nm	65nm	65nm	180nm	65nm
Frequency [Hz]	100M		10M	2.3M	16M	100M	32M	16M	28M
Power [μW]	142		85	7.6	220	101	34	158	142
Power Efficiency [μW/MHz]	1.4		8.5	3.3	13.8	1.0	1.1	10	5
P-poly Resistor Used	No	Yes	Yes						
Aging Compensation	Yes		No						
Frequency Inaccuracy w/o Aging [ppm]	±770	±870	±2800	±1550**	±90	±140	±530	±400	±200
Frequency Inaccuracy w/ Aging [ppm] Uncompensated/ Compensated	±1600/ ±1030	±6210/ ±1070	±7800/ -	-					
Trim Points	2		1+Batch	2	2+Batch	3	2	1+Batch	2+Batch
Temp. Range [°]	−40 to 85		−45 to 125	−40 to 125	−45 to 85	−40 to 95	−40 to 85	−45 to 85	−40 to 85
Supply Sensitivity [%/V]	0.14		0.9	0.51	0.12	0.0083*	0.008*	0.2	0.29
Supply Range [V]	1.1 to 1.3		1.5 to 1.8	1.3 to 2.0	1.6 to 2.0	1.1 to 2.5	1.1 to 2.3	1.6 to 2.0	0.85 to 1.05
# of Samples	14	7	112	11	20	20	6	18	16
Period Jitter [ps_{rms}]	5.1		41.4	-	39.9	13.3	24	10.2	7
ADEV@τ=1s [ppm]	8.1		2.3	9	1	1.6	2.5	0.8	2
Area [mm^2]	0.22		0.01	0.07	0.3	0.19*	0.18*	0.14	0.06

* With on-chip LDO ** Worst case

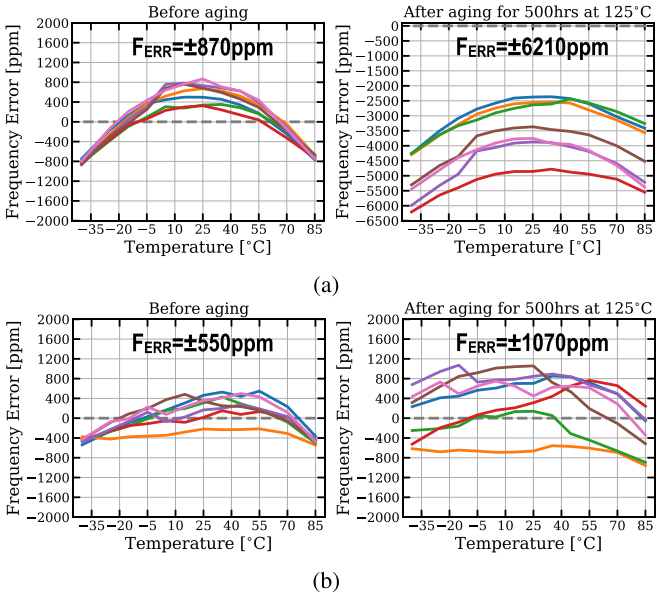


Fig. 17. Measured frequency inaccuracy of main TCOs using p-poly and VIA resistors before and after aging (a) without the aging compensation and (b) with the compensation.

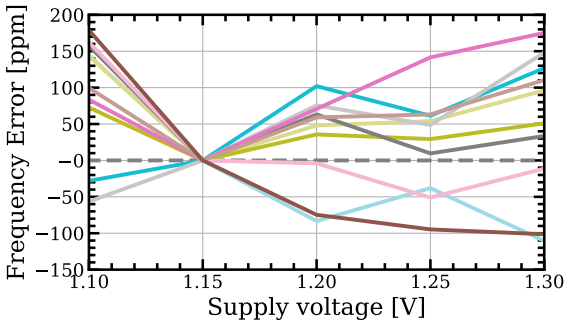


Fig. 18. Measured supply sensitivity on analog supply.

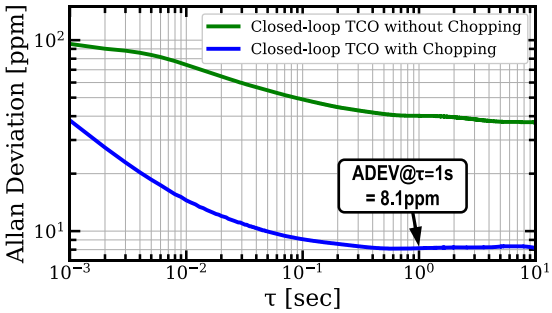
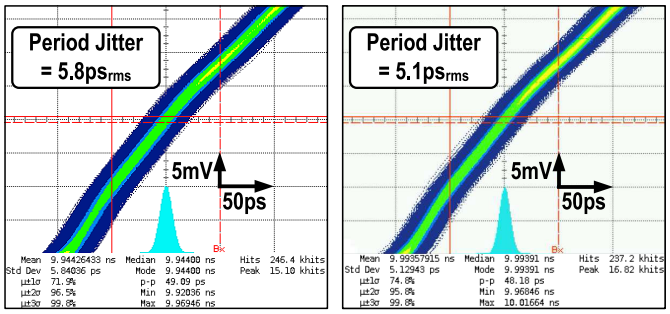


Fig. 19. Allan deviation.

samples, wherein a p-poly resistor is substituted for R_0 in the main TCOs (it is worth noting that the R_0 of the reference TCOs is represented by an n-poly resistor, while the R_1 of both the main and reference TCOs is a VIA resistor). This test provides a fair comparison with the state of the art, since most TCOs reported in the literature use p-poly resistors [16], [19], [20], [22], [36]. Before aging, the inaccuracy of uncompensated main TCOs is ±870 ppm, while after 500 h of aging, it degrades to ±6210 ppm, as shown in Fig. 17(a). The degradation in accuracy appears to be mainly due to the aging of the p-poly resistor, as indicated by the comparison with the results shown in Fig. 16(a). However, with compensation, the main TCOs have a frequency accuracy of ±550 ppm before aging, which degrades to ±1070 ppm after the aging test. The compensation reduces the degradation to only 520 ppm [see Fig. 17(b)].

C. Supply Sensitivity and Output Clock Performance

Fig. 18 shows that the supply sensitivity of ten samples on the analog supply, measured using n-poly and VIA resistors, was 1440 ppm/V over the supply range of 1.1–1.3 V. The Allan deviation for a 1-s stride without chopping was found to be 40 ppm, but it was reduced to 8.1 ppm with chopping, as depicted in Fig. 19. The measured output period jitter of the open-loop ring oscillator was 5.8 ps_{rms} [see Fig. 20(a)], while the closed-loop TCO shows a lower period jitter of



(a) (b)

Fig. 20. Period jitter of (a) open-loop ring oscillator and (b) closed-loop TCO.

5.1 ps_{rms} [see Fig. 20(b)], because dominant open-loop VCO phase noise is suppressed by the FLL loop.

The performance of the TACO is summarized in Table II, where it is also compared with state-of-the-art *RC* oscillators. The proposed TACO exhibits a good power efficiency of 1.4 μW/MHz, and its frequency inaccuracy is comparable to that of state-of-the-art oscillators, even in the presence of aging.

V. Conclusion

The presented *RC* oscillator is a temperature- and aging-compensated design that mitigates the long-term drift of the main oscillator by periodically locking its frequency to that of a less-aged reference oscillator. To improve the long-term stability of the oscillator, several techniques are employed. The first technique involves using higher activation energy resistors, because they exhibit smaller resistivity shifts under temperature stress. The second technique involves switching dual *RC* branches to mitigate the stress from dc-current-induced electromigration. Finally, the duty-cycling method is employed to slow down the reference oscillator's aging rate. Because of these techniques, the proposed TACO achieves a frequency inaccuracy of $\pm$1030 ppm from -40 °C to 85 °C, even after 500 h of accelerated aging at 125 °C. The oscillator exhibits a period jitter of 5.1 ps_{rms} and a power efficiency of 1.4 μW/MHz. The proposed TACO is suitable for use in low-power micro-controller applications that require good frequency accuracy even when aging effects are present.

Acknowledgment

The authors thank Stefano Pietri, John Pigott, and Domenico Liberti of NXP Semiconductors, USA, and Danielle Griffith of Texas Instruments, Dallas, TX, USA, for useful discussion and critical feedback.

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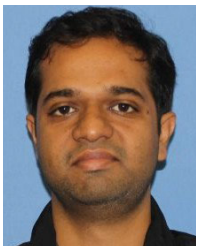

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