Guest Editorial Introduction to the Special Section on the 2023 IEEE International Solid-State Circuits Conference (ISSCC)

THIS Special Section of IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) highlights outstanding papers presented at the 2023 IEEE International Solid-State Circuits Conference (ISSCC), which was held from February 19 to 23, 2023, in San Francisco, USA, under the conference theme "Building on 70 years of Innovation in Solid-State Circuit Design." ISSCC is the foremost global forum for the presentation of advances in solid-state circuits and systems-on-a-chip and offers a unique opportunity for engineers working at the cutting edge of integrated circuit (IC) design and application. The conference includes several technical programs ranging from analog to mixed-mode, digital, RF, and power management circuits and systems with applications in a wide variety of fields. This JSSC Special Section highlights selected papers from ISSCC particularly on topics related to the Imagers, MEMS, Medical, and Displays (IMMD), and Technology Directions (TD) technical programs.

In 2023, ISSCC had a $\sim$ 30% acceptance rate on all received papers, and more than 2000 people attended the conference in person. This Special Section of JSSC features nine selected papers from ISSCC 2023, out of which four papers are selected from the IMMD technical program and five papers are selected from the TD technical program. These papers provide comprehensive materials extending their conference proceedings and were carefully selected from highly qualified accepted papers. The acceptance of these papers to JSSC was based on a thorough peer review process. The accepted papers cover a wide range of topics as described below.

The first two articles introduce novel ideas for hybrid image/vision sensing and X-ray detection. The article by Guo et al. [A1] from OmniVision Technologies, Santa Clara, CA, USA, introduces a hybrid 4096 $\times$ 3680 CMOS image sensor with an embedded 1032 $\times$ 928 event-based vision sensor. The hybrid sensor mitigates challenges in synchronization and parallax error compared to a two-sensor solution. The vision sensor pixel achieves sub-1-Hz noise rates and 3% contrast non-uniformity at a linear nominal contrast threshold of 15%. The sensor achieves an event rate of up to 4.6 GEvents/s. This article shows on-chip integration of image and event signal processors. The other paper by Park et al. [A2] from Yonsei University, Seoul, South Korea, describes a 400 $\times$ 200 single-photon avalanche diode X-ray detector that supports seamless global shutter operation. For use under low or high X-ray dose conditions, it operates in a fully digital manner (avoiding the noise penalty of the readout) or in extrapolation mode (achieving high dynamic range with low power), respectively. Furthermore, seamless global shutter operation is realized, achieving a 100% temporal aperture for the X-ray photon. The implemented X-ray detector with a pixel pitch of 49.5 μm in a 65-nm CMOS process achieves a 117.7-dB dynamic range while consuming 127.2 mW.

In the area of biomedical circuits, three articles are included. The article by Eom et al. [A3] from Korea University, Seoul, presents a 505-channel pixel-sharing sub-retinal prosthesis chip for restoring visual acuity. It employs a modular active/return electrode scheme to mitigate current scattering (by up to 95.4%) and a time-based photodiode sensing to increase the dynamic range (to 35.8 dB). Per-pixel dynamic voltage scaling improves stimulation efficiency (by up to 64%). The chip has also been verified in ex vivo experiments with retinal samples of mice. The article by Chen et al. [A4] from imec, Leuven, Belgium, introduces intelligent on-chip neural-signal processing to reduce the data-transmission power and enable real-time closed-loop applications with minimum latency. An online spike-sorting chip is presented to process 384 channels of neural signals with techniques such as employing a central spike detection algorithm (mitigating the impact of redundant spikes on accuracy), a peak first and second derivative extrema method (accomplishing robust feature extraction), and a geometry-aware algorithm (providing a tradeoff between accuracy and complexity). The fabricated chip in a 22-nm FDSOI CMOS process achieves 1.78 μW/channel, 33.9 μs latency, and 97.7% accuracy without pre-training. The article by Aghlmand et al. [A5] from Caltech, Pasadena, CA, USA, presents a CMOS fluorescence sensor chip employing on-chip bandpass optical filters and sensitive photodetection circuitry, allowing compact biosensors for dynamic monitoring of living cells. The sensor can measure the growth of living *E. coli* bacterial cells and can detect fluorescence responses from genetically engineered bacterial cells.

The next article by Lin et al. [A6] from the University of Macau, Macau, China, presents an ultra-low-power mixed-signal voice activity detector for edge devices. It employs a short-time convolutional neural network (ST-CNN) and a recurrent neural network (RNN)-based classifier. Implemented in 65-nm CMOS, the chip exhibits a 94% and 91% overall hit rate on the Google Speech Command Dataset and the Texas Instruments/Massachusetts Institute of Technology (TIMIT)

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Dataset, respectively, while dissipating 47 nW of power. In the area of integrated photonics, the article by Ives et al. [A7] from Caltech, Pasadena, CA, USA, presents an approach for implementing photonic waveguides in bulk CMOS processes. Using metals and glass to pattern in the back-end-of-the-line layers, and then etching away the metal layers, the authors demonstrate suspended waveguides capable of operating up to visible range. The article presents multimode waveguides with measured losses of 4.1 dB/cm at 1550 nm and integrated photodetectors that can work cooperatively with the implemented waveguides.

Finally, in the area of quantum computing, there are two articles. The article by Yoo et al. [A8] from Google Quantum AI, Santa Barbara, CA, USA, presents a cryogenic quantum control IC that has the ability to control all the necessary degrees of freedom of a 2-qubit subcircuit of a superconducting quantum processor. The IC integrates a pair of 4–8-GHz RF pulse generators for *XY* control, and baseband current generators for qubit and coupler frequency control. The IC achieves single qubit *XY* and *Z* average gate error rates of 0.17%–0.36% and 0.14%–0.17%, respectively, while dissipating 4 mW/qubit. The final article by Guo et al. [A9] from Tsinghua University, Beijing, China, presents a polar-modulation approach to qubit state controller ICs. It employs a switched-capacitor digital power amplifier for amplitude modulation and an injection-locking local oscillator with a constant-slope digital-to-time-converter for open-loop phase modulation. Dissipating 13.7 mW/qubit, the chip achieves a spurious-free dynamic range of 40 dB for a 1 GS/s *XY*-path driver and 48 dB for a 1 GS/s *Z*-path driver at 3.5 K, and shows control of the transmon superconducting cubit at 10 mK.

We convey our sincere gratitude to all the authors and diligent reviewers for their dedicated efforts and time in ensuring the production of high-quality manuscripts within a challenging timeline. We would also like to express our appreciation to the members of the IMMD and TD technical program committees of the 2023 ISSCC, whose contributions played a crucial role in the success of the conference. In addition, we wish to extend our deepest appreciation to Dennis Sylvester, the Editor-in-Chief of JSSC, for his valuable guidance. We also express our sincere thanks to Danielle Marinese and the dedicated JSSC administration for their indispensable assistance in publishing this Special Section.

MEHDI KIANI, *Guest Editor*
School of Electrical Engineering and Computer Science
The Pennsylvania State University
University Park, PA 16802 USA

KAUSHIK SENGUPTA, *Guest Editor*
Department of Electrical and Computer Engineering
Princeton University
Princeton, NJ 08544 USA

APPENDIX: RELATED ARTICLES

[A1] M. Guo et al., "A three-wafer-stacked hybrid 15-MPixel CIS + 1-MPixel EVS with 4.6-GEvent/s readout, in-pixel TDC, and on-chip ISP and ESP function," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 2955–2964, Nov. 2023.

[A2] B. Park, H.-S. Choi, J. Jeong, T. Kim, M.-J. Lee, and Y. Chae, "A 113.3-dB dynamic range 600 frames/s SPAD X-ray detector with seamless global shutter and time-encoded extrapolation counter," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 2965–2975, Nov. 2023.

[A3] K. Eom et al., "A low-stimulus-scattering pixel-sharing sub-retinal prosthesis SoC with time-based photodiode sensing and per-pixel dynamic voltage scaling," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 2976–2989, Nov. 2023.

[A4] Y. Chen et al., "An online-spike-sorting IC using unsupervised geometry-aware OSort clustering for efficient embedded neural-signal processing," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 2990–3002, Nov. 2023.

[A5] F. Aghlmand, C. Hu, S. Sharma, K. Pochana, R. M. Murray, and A. Emami, "A 65nm CMOS fluorescence sensor for dynamic monitoring of living cells," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 3003–3019, Nov. 2023.

[A6] J. Lin, K.-F. Un, W.-H. Yu, R. P. Martins, and P.-I. Mak, "A 47-nW voice activity detector (VAD) featuring a short-time CNN feature extractor and an RNN-based classifier with a non-volatile CAP-ROM," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 3020–3029, Nov. 2023.

[A7] C. Ives, D. Sarkar, and A. Hajimiri, "Subtractive photonics in bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 3030–3043, Nov. 2023.

[A8] J. Yoo et al., "Design and characterization of a < 4 mW/qubit 28-nm cryo-CMOS integrated circuit for full control of a superconducting quantum processor unit cell," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 3044–3059, Nov. 2023.

[A9] Y. Guo et al., "A polar-modulation-based cryogenic transmon qubit state controller in 28 nm bulk CMOS for superconducting quantum computing," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 3060–3073, Nov. 2023.

Mehdi Kiani (Senior Member, IEEE) received the B.S. degree from Shiraz University, Shiraz, Iran, in 2005, the M.S. degree from the Sharif University of Technology, Tehran, Iran, in 2008, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2012 and 2013, respectively.

He joined the faculty of the School of Electrical Engineering and Computer Science, The Pennsylvania State University, State College, PA, USA, in August 2014. His research interests are in the multidisciplinary areas of analog, mixed-signal, and power-management integrated circuits, wireless implantable medical devices, neural interfaces, and ultrasound-based medical systems.

Dr. Kiani was a recipient of the 2020 NSF CAREER Award. Currently, he is an Associate Editor of IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS (TBioCAS) and IEEE TRANSACTIONS ON BIOMEDICAL ENGINEERING (TBME). He serves as a Technical Program Committee (TPC) Member of the IEEE International Solid-State Circuits Conference (ISSCC). He has also served as the TPC Member for the IEEE Custom Integrated Circuits Conference (CICC) and the IEEE Sensors Conference.

Kaushik Sengupta (Senior Member, IEEE) received the B.Tech. and M.Tech. degrees in electronics and electrical communication engineering from IIT Kharagpur, Kharagpur, India, in 2007, and the M.S. and Ph.D. degrees in electrical engineering from Caltech, Pasadena, CA, USA, in 2008 and 2012, respectively.

In 2013, he joined the Department of Electrical and Computer Engineering, Princeton University, Princeton, NJ, USA, as a Faculty Member, where he is currently a Professor. He directs the IMRL Laboratory focused on RF-to-THz-to-optical chip-scale systems for wireless and biosensing.

Dr. Sengupta was a recipient of the 2015 Microwave Prize from the IEEE Microwave Theory and Techniques Society, the ONR Young Investigator Award, the Bell Labs Prize in 2017, the DARPA Young Faculty Award in 2018, the Inaugural Young Alumni Achievement Award from IIT Kharagpur in 2018, the E. Lawrence Keys, Jr. Emerson Electric Co. Junior Faculty Award from the Princeton School of Engineering and Applied Science in 2018, and the Excellence in Teaching Award in 2018 nominated by the Undergraduate and Graduate Student Council in the Princeton School of Engineering and Applied Science, the Charles Wilts Prize in 2013 from the Department of Electrical Engineering, Caltech, for the best Ph.D. thesis, the Caltech Institute Fellowship, and the Prime Minister Gold Medal Award from IIT Kharagpur in 2007. He was also a recipient of the Outstanding Young Engineer Award from IEEE MICROWAVE THEORY AND TECHNIQUES in 2021 and the New Frontier Award from IEEE Solid-State Circuits Society in 2022. He has served as the Chair for Emerging Technologies for the IEEE Custom Integrated Circuits Conference (CICC). He currently serves for the Technical Program Committee of the International State Circuits Conference (ISSCC). He has served as a Distinguished Lecturer for the IEEE Solid-State Circuits Society from 2019 to 2020. He is also serving as a Distinguished Lecturer for the IEEE Microwave Theory and Techniques from 2021 to 2023 and a Co-Chair of the IEEE Solid-State Circuits Directions Committee.