Design and Characterization of a <4-mW/Qubit 28-nm Cryo-CMOS Integrated Circuit for Full Control of a Superconducting Quantum Processor Unit Cell

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***Abstract*— A universal fault-tolerant quantum computer will require large-scale control systems that can realize all the waveforms required to implement a gateset that is universal for quantum computing. Optimization of such a system, which must be precise and extensible, is an open research challenge. Here, we present a cryogenic quantum control integrated circuit (IC) that is able to control all the necessary degrees of freedom of a two-qubit subcircuit of a superconducting quantum processor. Specifically, the IC contains a pair of 4–8-GHz RF pulse generators for *XY* control, three baseband current generators for qubit and coupler frequency control, and a digital controller that includes a sequencer for gate sequence playback. After motivating the architecture, we describe the circuit-level implementation details and present experimental results. Using standard benchmarking techniques, we show that the cryogenic CMOS (cryo-CMOS) IC is able to execute the components of a gateset that is universal for quantum computing while achieving single-qubit *XY* and *Z* average gate error rates of 0.17%–0.36% and 0.14%–0.17%, respectively, as well as two-qubit average cross-entropy benchmarking (XEB) cycle error rates of 1.2%. These error rates, which were achieved while dissipating just 4 mW/qubit, are comparable to the measured error rates obtained using baseline room-temperature electronics.**

***Index Terms*— Cryogenic CMOS (cryo-CMOS), cryogenic electronics, quantum computing, quantum control.**

I. Introduction

THE field of quantum computing has experienced rapid growth over the past decade, with focus shifting from small-scale studies of the requisite quantum mechanical building blocks to the implementation of a large-scale fault-tolerant quantum computer. Examples of recent advances in the field include the demonstration of beyond-classical computations [1], [2], [3], [4] and reaching the break-even point in system performance where scaling quantum error correction (QEC) codes begin to improve rather than degrade error rates [5]. However, today's most advanced quantum computers still have about four orders of magnitude fewer qubits than is believed to be required for a useful fault-tolerant quantum computer. Scaling quantum computing systems to this level requires significant research and development across the entire system stack.

Of the many areas requiring attention, here, we focus on control of the quantum processor. For today's $\mathcal{O}(100)$ qubit superconducting quantum computers, the necessary control waveforms are generated using custom-built rack-mounted electronic control systems that leverage high-speed digital-to-analog converters (DACs) driven from field-programmable gate array (FPGA)-based interfaces [6], [7]; this approach has been logical due to the fact that system development to date has focused primarily on basic demonstrations and, as such, the optimization of electronics has not been critical. However, realization of the $\mathcal{O}(10^6)$ qubit systems currently believed necessary for fault-tolerant quantum computing will require reducing the size, power, and cost of these electronic interfaces.

Using cryogenic CMOS (cryo-CMOS) integrated circuits (ICs) for quantum control is one promising approach to implement large-scale quantum controllers. Cryogenic cooling is already required for the quantum processor, and cooling the electronics to around 4 K has the advantage that it becomes possible to connect between the quantum processor and the electronics via low-dispersion and nearly lossless superconducting interconnects while at the same time maintaining a high degree of thermal isolation [8]. While the improved transmission channel promises the opportunity to remove the need for waveform predistortion (currently in wide use [9], [10]), the available power budget at cryogenic temperatures is limited and it is thus important to determine whether the necessary

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performance can be achieved while keeping the power consumption manageable.

Use of cryo-CMOS ICs for quantum control was first proposed well over a decade ago [11]. However, progress in the field has sped up considerably over the past six years. At ISSCC in 2017, Charbon et al. [12] proposed an architecture for quantum control and measurement and demonstrated the basic cryo-CMOS building blocks. We then presented our first-generation cryo-CMOS quantum control IC at ISSCC in 2019, demonstrating coherent microwave control of a superconducting qubit [13]. This was followed by system demonstrations of cryo-CMOS chips performing microwave control of spin [14] and superconducting qubits [15] at ISSCC 2020 and 2022, respectively. These ICs were later benchmarked with qubits, with average single-qubit gate error rates of 0.31% [16] and 0.078% [17] reported. Numerous component-level cryo-CMOS demonstrations have also been reported, e.g., [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. However, to the best of our knowledge, a single chip capable of performing all of the control operations needed to implement universal quantum computation on a frequency tunable superconducting quantum processor has not been previously reported.

Here, we report the design and characterization of a prototype low-power cryo-CMOS quantum control IC [29], which contains all of the control features required to implement universal quantum computing on a Sycamore [1] quantum processor. Using standard benchmarking techniques, we show that its system performance is comparable to the state-of-the-art room-temperature electronics currently used for quantum control. The outline of the remainder of this article is organized as follows.

II) Design considerations related to control in the Sycamore architecture are discussed. Requirements for universal quantum computing and the gate metrics required to implement QEC codes are described. Key performance specifications are presented.

III) Details of the cryo-CMOS control IC are presented. Schematics of each key block are described and design considerations are discussed.

IV) Experimental results are presented. Each of the control functions is benchmarked and shown to be competitive with baseline room-temperature electronics. Selected calibration routines are presented.

V) The work is summarized and the high-level results are interpreted. Future directions are discussed.

While outside of the scope of this article, we refer readers interested in an introduction to the field of superconducting quantum computing to the following review articles [30], [31], [32].

II. Quantum Controller Specifications

Here, we consider control of a two-qubit patch of a Sycamore quantum processor [1], which is the smallest representative subcircuit that is sufficient to demonstrate the basic functionality required for universal control of larger-scale quantum processors. In the Sycamore architecture [Fig. 1(a)], transmon qubits (red "+" symbols) are interconnected on a 2-D grid via tunable couplers (black squares). The qubits are realized as flux-tunable transmon qubits [33], which are nonlinear LC resonators, with superconducting quantum interference devices (SQUIDs) playing the role of flux-tunable nonlinear inductors. As shown in Fig. 1(b), each transmon requires two control signals: a microwave (XY) signal for resonant excitation of the qubit and a baseband (Z) current for tuning of the qubit's frequency via the SQUID flux bias. An additional readout port is used to measure the qubit state via microwave reflectometry.

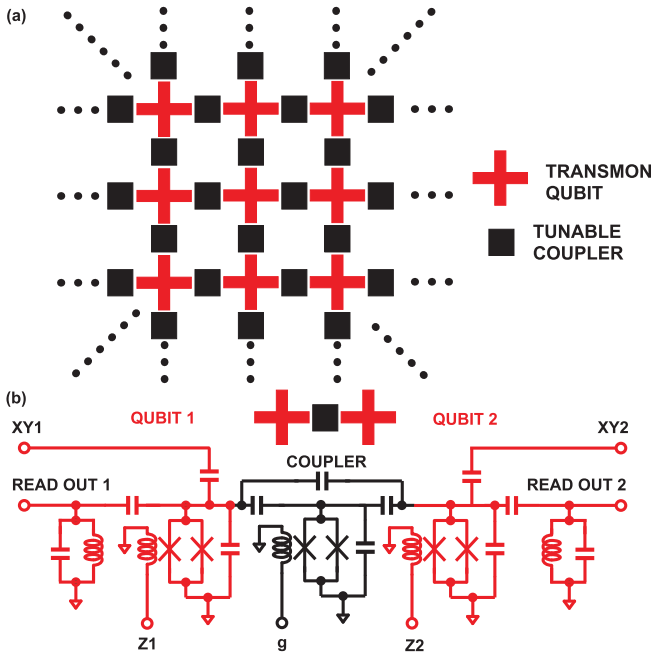


Fig. 1. Sycamore quantum processor architecture. (a) High-level architecture showing arrangements of qubits and couplers on a 2-D grid. (b) Representative schematic of a two-qubit patch of the Sycamore processor, highlighting internal control and measurement ports. In the actual chip, XY and Z signals are multiplexed to a single port.

The couplers are realized using additional transmon circuits that are embedded in capacitive coupling networks connecting the qubits. The coupler transmon is operated OFF-resonance and serves the purpose of a flux-tunable impedance. By tuning the coupler transmon to the right frequency, coupling between the qubits can be completely nulled. By moving away from this bias, a continuous range of deterministic couplings between the qubits can be realized, forming a basis for two-qubit gates. As shown in Fig. 1(b), each coupler has a single bias current (g), which is used to control the coupler transmon frequency. Control of a two-qubit patch of the Sycamore processor requires two XY, two Z, and one g control channels.

A. High-Level Considerations

Prior to describing the detailed electrical requirements for the quantum control IC, we first review the high-level considerations from which these specifications are derived.

1) Gate Library: A gateset that is universal for quantum computation is a necessary component of a universal quantum computer. Fig. 2 shows the gate sequence and associated waveforms of an algorithm that creates a maximally entangled

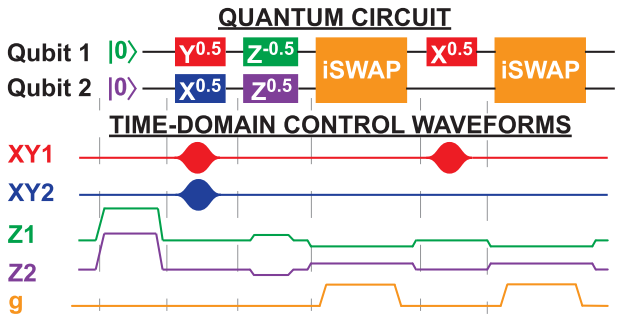


Fig. 2. Example control waveforms required to run an algorithm that generates a two-qubit maximally entangled Bell state. First, the qubits are reset via the Z control by bringing their frequencies into resonance with their readout resonators. Next, each qubit is put in a superposition of $|0\rangle$ and $|1\rangle$ via a resonant microwave pulse applied to the qubit's XY drive line, with the phase of the superposition determined by the phase of the microwave carrier signal. The phase of each of the qubits' states is then shifted in magnitude by $\pi/2$ by detuning the qubit frequency by Δf for a duration Δt such that a phase $|\phi| = 2\pi\Delta f\Delta t = \pi/2$ accumulates, with the sign depending on if the qubit is tuned up or down in the frequency. Next, a two-qubit iSWAP gate is applied by bringing the qubits on resonance using their Z controls before enabling the coupling between the qubits using the g control. This entangling gate has the effect of swapping single excitation modes between the qubits (i.e., $|01\rangle \Longleftrightarrow |10\rangle$) while imparting a 90° phase shift on the swapped state. Finally, one more XY gate is applied to the first qubit before one more iSWAP gate is run to generate the Bell state $(|00\rangle + |11\rangle)/\sqrt{2}$.

Bell pair state on the two-qubit processor patch. The set of operations in this example is illustrative of how the processor must be controlled to realize a gateset that is universal for quantum computing. Specifically, the controller should be able to reset the qubits, perform a finite set of single qubit operations (there is flexibility in the exact set), and perform at least one two-qubit entangling gate [34], [35], [36]. For the architecture of Fig. 1, this can all be accomplished with XY, Z,[1] and g control waveforms, similar to those shown in Fig. 2. Further specifications for these signals are given as follows.

2) Controller Contribution to Gate Error Rates: A fault-tolerant quantum computer must run QEC protocols, which in turn requires carrying-out single- and two-qubit gate operations with error rates kept below a threshold, which is about 1% for the surface code [38]. The number of physical qubits required to implement a logical (encoded) qubit depends on the ratio of this threshold error rate to the achieved physical error rates. To limit the required number of physical qubits, it is highly desirable that physical error rates be at least 10× smaller than this error threshold. The error rates in turn are an aggregate of many different error mechanisms, including those intrinsic to the qubit and those imparted by the control and readout systems. For the qubits in our Sycamore quantum processor, internal mechanisms limit gate error rates to the order of 0.1%; it is critical that our quantum controller not further degrades the gate infidelity. As such, we specify that the control error rates due to each of the error mechanisms are limited to 0.001% so that the aggregate contribution of the controller is well below 0.1%.

3) Physical Temperature: If a connection between the quantum processor and cryo-CMOS IC is to be made using superconducting cables, the cryo-CMOS chip must be thermalized below the critical temperature of the superconducting material. This generally means that the chip must be cooled to below 10 K. In this work, we choose to thermalize the cryo-CMOS IC to 3 K, which is easily accessible in our systems.

4) Power Consumption: Today's quantum computers employ closed-cycle pulse-tube cryocoolers, which can remove about 2 W of dissipation at 4 K [39]. Employing such a device to cool the electronics associated with an $\mathcal{O}(10^6)$ qubit quantum computer would limit the allowable dissipation to $\mathcal{O}(2\ \mu$W/qubit), which is orders of magnitude below what has been shown to be practical using cryo-CMOS electronics. Instead, helium liquification systems similar to those used by the high-energy physics community can be employed [40]. With such an approach, it is possible to remove a kilowatt or more at 4 K, so it becomes possible to budget $\mathcal{O}(1$ mW/qubit). For this exploratory work, we budget 5 mW/qubit.

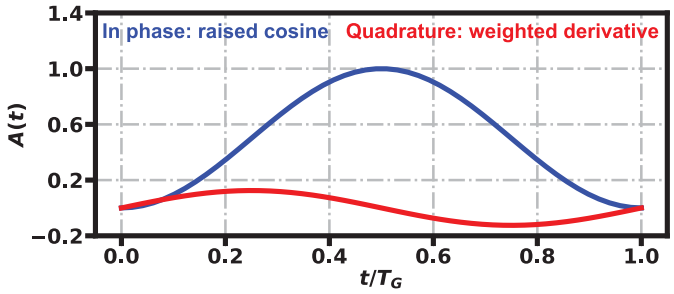


Fig. 3. Baseband envelopes of a raised cosine pulse and weighted derivative pulse used to implement a DRAG correction.

B. Controller Electrical Requirements

We now continue with a summary of the block-level specifications for the proposed quantum control IC. Derivations of these specifications are beyond the scope of this article. We refer the interested reader to [41] for relevant methods.

1) XY Control: The qubits are driven resonantly between their $|0\rangle$ and $|1\rangle$ states using XY control. Detailed microwave pulse specifications for XY control of transmon qubits were previously provided and justified [42], so we only review them briefly here. The baseband envelope we employ is a DRAG [43] compensated raised cosine envelope (Fig. 3). In this approach, a symmetric envelope and its weighted derivative are used as the real and imaginary components of the baseband envelope. By proper selection of the weighting factor, one can either introduce a notch—useful to suppress energy at the f_{12} transition for XY pulses of length below 15 ns [44]—or suppress errors due to the ac-Stark shift (pulses <15 ns require an additional dynamic detuning to compensate this effect). In this work, we employ raised cosine envelopes and leverage DRAG modulation to suppress the ac-Stark shift. The remainder of the specifications for the XY controller is listed in Table I (see [42] for a justification of the signal specifications). Here, we choose a pulse duration of 22 ns and specify that the controller is able to generate at least six different pulse waveforms, as this is required for benchmarking and is also sufficient for the realization of an XY gateset that is universal for quantum computing.

[1] Z gates can also be done virtually by updating the phase of XY gates [37].

TABLE I
XY AND *g*/*Z* CONTROLLER SPECIFICATIONS

***XY* Specifications**		***g*/*Z* Specifications**	
RF. Frequency	4–8 GHz	Waveform type	Baseband current
Modulation	DRAG		
Envelope error	$< 0.25\%$	Current	0–500 μA
RF phase error	$< 0.22°$	Resolution	$\geq$14-bit
Pulse duration	22 ns	Rise time	$\geq$1 ns
Peak power*	> -40 dBm	Settling time (0.5%)#	$\leq$ 5 ns
ON/OFF ratio†	$\geq$57 dB	Settling time (0.01%)##	$\leq$ 500 ns
Noise floor*	< 25 K	Noise floor	$\leq$ 1 LSB
# *XY* waveforms	≥ 6	# Current levels	≥ 5
DC power	$\leq$ 2 mW	DC power	$\leq$ 1 mW

*Assumes 30 dB of attenuation between the IC output and the quantum processor XY port. †Corresponds to a 0.1% initialization error after a 500 ns reset settling period. #Required dead time between Z and XY gates to achieve $\leq$ 100 kHz frequency error. ##Required wait time after reset pulse $0.99 \times f_{\max}$ to achieve $\leq$ 100 kHz frequency error for $f_{\text{IDLE}} = 0.99 f_{\max}$ and $f_{\text{reset}} = 0.65 f_{\max}$.

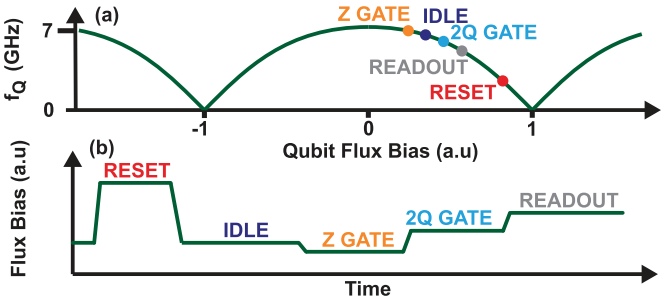


Fig. 4. Z control. (a) Flux tuning curve showing example points required during an algorithm. (b) Example flux bias waveform during operation.

2) Z Control: For a transmon with a symmetric SQUID, the qubit frequency f_Q depends on the Z current, i_Z, as

$$f_Q(i_Z) = f_{\max}\sqrt{\left|\cos\left(\pi \frac{M i_Z + \Phi_{\text{EXT}}}{\Phi_0}\right)\right|} \tag{1}$$

where $f_{\max}$ is the qubit frequency at the "flux insensitive" (zero bias) point, M is the mutual inductance between the Z control line and the SQUID, $\Phi_0 = h/2q = 2.07$ mV·ps is the flux quantum, and Φ_{EXT} is an external flux that is trapped in the SQUID during the normal–superconducting transition.[2] For full frequency coverage from dc to $f_{\max}$, it is required that $i_{Z,\max} \geq \Phi_0/2M$. Taking typical parameters of M in the 2–4-pH range, $i_{Z,\max}$ from 250 to 500-μA range is needed.

While a continuous range of frequencies can be reached using Z control, this is not a requirement. Instead, universal quantum computation requires adjusting the qubits' frequencies to locations to idle (where single-qubit XY gates are done), perform two-qubit gates, perform state readout, and reset each qubit. A helpful additional operation involves slightly detuning the qubits from their idling frequencies to enable physical Z gates such as the $T = Z^{0.25}$ gate, which is used in universal gateset constructions. As such, the controller must tune the qubit to at least five frequencies (see Fig. 4).

The static frequency accuracy during idling must be sufficient to avoid affecting the average error rate of XY gates, which is related to qubit frequency errors by [41]

$$\epsilon_{XY,\Delta f_Q} = \frac{1}{3}(1 - \cos(\theta))\frac{\Delta f^2}{f_{\text{RABI}}^2} \tag{2}$$

where θ is the XY gate rotation angle, Δf is the qubit (or microwave carrier) frequency error, and f_{RABI} is the Rabi oscillation frequency associated with the gate.[3] For a π-pulse duration of 22 ns, the frequency must be set to be within about $\pm$100 kHz to keep $\epsilon_{XY,\Delta f_Q} \leq 10^{-5}$. Achieving sufficient resolution to meet this specification while operating as far as 10% below $f_{\max}$ requires 14 bits of resolution. Similarly, to prevent white noise on the Z line from contributing to XY gate error while operating at this large offset from $f_{\max}$, the RMS current noise, including dc-to-f_{RABI}, should be $\leq$1 LSB.[4]

The impact of Z current noise on the qubit coherence time T_2 should also be considered. Assuming a white spectrum, the pure dephasing limit of T_2 due to Z current noise is [45]

$$T_{\phi,i_Z} = \frac{2}{S_{i_Z}\left(\partial f_Q/\partial i_Z\right)^2}, \tag{3}$$

where S_{i_Z} is the current noise spectral density. Limiting the error contribution of dephasing to 10^{-5} for $M = 4$ pH, 22-ns gate duration, $f_{\max} = 7$ GHz, and an offset frequency of $0.9 \times f_{\max}$ requires keeping the noise temperature on the Z drive line below 13 K (short-circuit current noise of about 3.8 pA/$\sqrt{\text{Hz}}$).

The dynamic Z performance must also be specified. The Z-pulse rise time should be greater than 1 ns to avoid the excitation of diabatic transitions. In addition, settling must be rapid to minimize gate errors; a conservative specification is that the qubit frequency must reach within 100 kHz of its idle value within 500 ns of a reset pulse and within 5 ns of a gate pulse. Meeting these specifications requires i_Z settle to be within 0.5% and 0.01% on timescales of 5 and 500 ns, respectively.

Finally, we consider the interface between the Z controller and the quantum processor. In a typical configuration using a room-temperature control system, about 20 dB of attenuation is incorporated on the Z line at a physical temperature of 3 K. This attenuation serves two purposes. First, it dampens standing waves that would otherwise be present due to the inductive load presented by the Z port. Second, it serves to reduce the noise floor, minimizing degradation to T_2. However, when considering a cryogenic controller, to minimize power consumption, the Z controller should drive the qubit directly (i.e., with no series attenuation). This means that the output impedance of the Z driver should present a broad 50-Ω match and its noise floor should be low enough to not limit T_2. Z control specifications are summarized in Table I.

3) g Control: The coupler bias current specifications are similar to those of the Z current bias. However, as the primary purpose of this controller is to deterministically enable and disable coupling, only two distinct bias points are needed.

[2] Φ_{EXT} can be minimized by controlling the stray flux during cooldown.

[3] For a gate with duration T_{gate}, $f_{\text{RABI}} = \theta T_{\text{gate}}/360°$.

[4] The specifications are significantly relaxed for operation closer to $f_{\max}$.

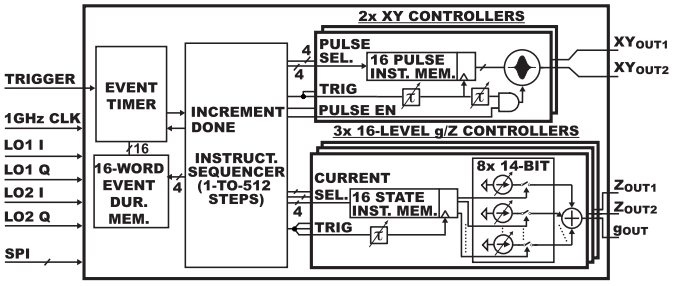


Fig. 5. Top-level chip block diagram.

During idling, when the coupling is set to the OFF state, the device is insensitive to small changes in the coupler bias current. However, when the coupler is biased to the ON state, small changes in the coupler bias current lead to appreciable changes in the coupling rate between the qubits [46], [47]. Since the fidelity of the two-qubit gates orchestrated by the coupler can be limited by coupling rate errors, it is necessary that we maintain sufficiently high precision and low noise on this control line to enable high-fidelity gates. For our system, where typical values of $\partial g/\partial I_{\mathrm{CPL}}$ at a bias corresponding to an iSWAP gate are in the range of 0.5 MHz/μA, it can be shown that the noise and accuracy requirements imposed on the g line are less stringent than those of the Z control line. Therefore, we maintain the Z specifications here.

III. Circuit Design

A block diagram of the quantum controller IC appears in Fig. 5. The system contains three main functional blocks. First, there are a pair of microwave pulse generators, which are configured to generate XY control signals. Second, there are three dynamic current sources, each of which can dynamically switch between up to nine different high-precision currents. These circuits are used to provide Z and g controls. Finally, there is a controller which interfaces to each of the five control channels and is used to orchestrate playback of sequences with up to 512 steps. The chip runs off a 1-V core supply, a 1.8-V input/output (IO) supply (for digital pads), and a 1-GHz digital clock.

Before discussing block-level implementation details, let us briefly discuss some unique challenges related to the design for operation at 3 K. Typical foundry process design kits (PDK) tend to be optimized for operation at temperatures above -40 °C, and this is the case for the 28-nm technology platform targeted for use here. As such, we were not able to run simulations at the nominal operating temperature. To ensure functionality, we took several measures. For instance, we determined the temperature that the I–V curves predicted by the PDK best approximated the expected behavior (an increase in subthreshold slope of about 5× and threshold increase of about 100 mV [42]) and performed simulations of critical blocks at this temperature to ensure that the circuits dc biased properly (for this PDK, we found that this corresponded to a temperature of about -170 C). In addition, as we did not have digital timing libraries for cryogenic temperatures, all digital blocks were implemented manually, using standard cell libraries along with careful simulations. Finally, where possible, we chose circuit architectures that are

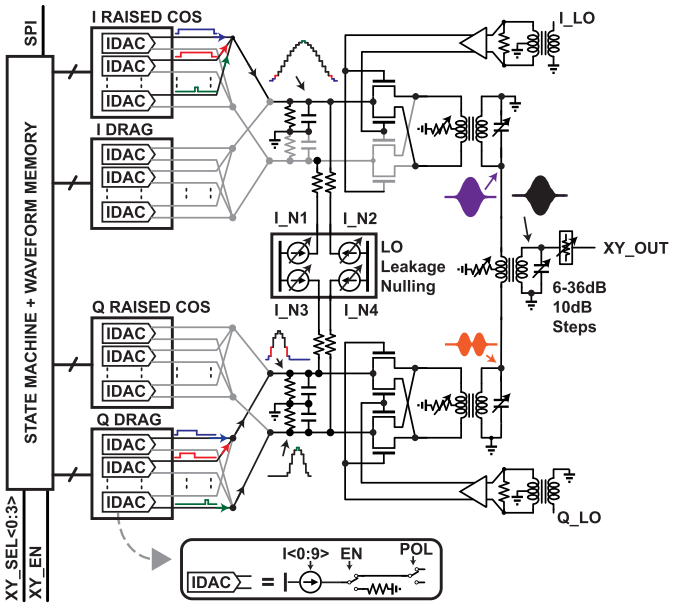


Fig. 6. XY controller block diagram, showing DRAG waveform generation.

only weakly sensitive to mismatch (expected to degrade cryogenically) and added extensive reconfigurability and dc voltage monitoring capabilities to enable post-fabrication performance optimization.

A. XY Controller

A block diagram of the XY controller circuit appears in Fig. 6. Similar to [13], a complex baseband envelope is generated using an array of current-mode sub-DACs. This signal is upconverted to the desired RF frequency using an IQ modulator driven by a room-temperature local oscillator (LO) signal.[5] To enable the DRAG protocol, the circuit can generate baseband envelopes with both even and odd symmetry.

To understand the XY controller operation, consider Fig. 6, which includes example waveforms for the case where the I and Q channels are configured to generate pulses with symmetric raised cosine and derivative of raised cosine envelopes, respectively (for the DRAG protocol). At the core of the circuit is an array of sub-DACs, each of which has 10 bits of resolution and contains a switch to enable the DAC output as well as a polarity switch to route its output current to one of two outputs. Generation of a symmetric raised cosine pulse is accomplished using a bank of 11 sub-DACs. The controller first sets the value of each of these sub-DACs to one of 16 pre-programmed values and sets their polarities to a common value. The sub-DACs are then sequentially enabled to create a symmetric pulse of current, which is filtered and upconverted. This approach guarantees a smooth pulse due to the inherent monotonicity of the rising and falling edges, overcoming challenges related to MOSFET mismatch degradation at cryogenic temperatures [48], [49]. The mixer center tap is grounded through a balance resistor, providing a ground return for the single-ended current pulse. This balance resistor is incorporated to implement a transformer-based 180° hybrid [50], which provides isolation between

[5]Since f_Q can be tuned, a large control system could operate with a finite number of qubit frequencies, minimizing LO generation overhead.

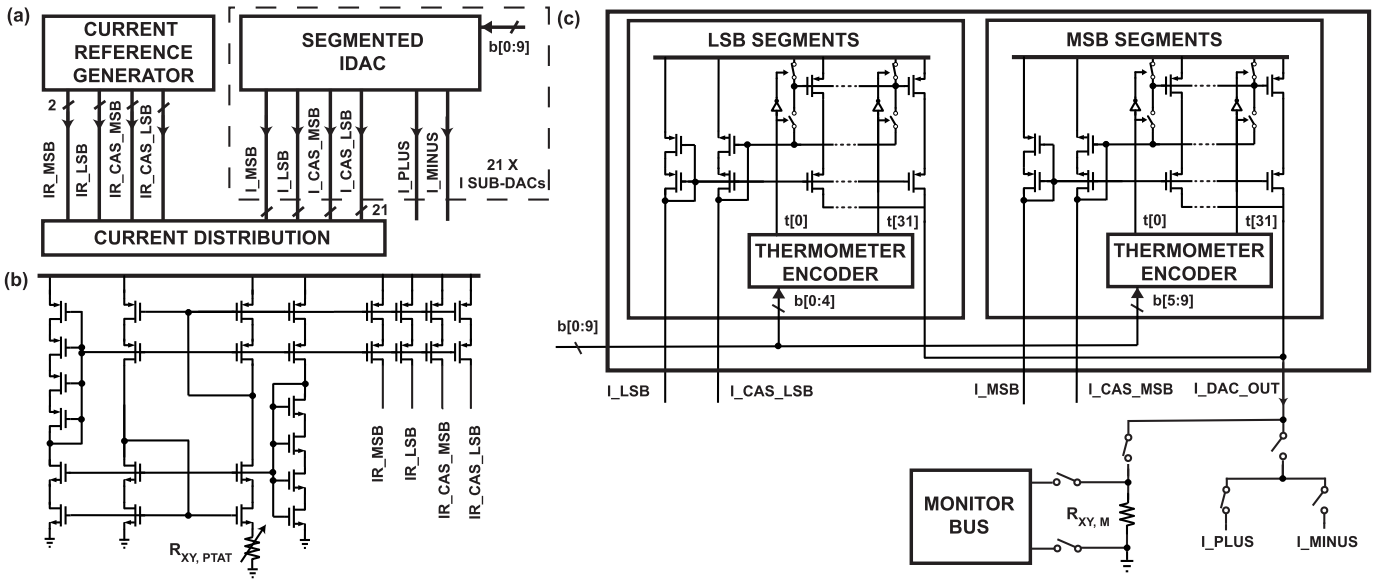


Fig. 7. *XY* baseband DAC. (a) Simplified block diagram explaining biasing of *XY* DACs. The current reference generator provides two sets of four currents, which are used to reference current distribution networks feeding the *I* and *Q* sub-DACs, respectively. Connections from the current distribution block to the *Q* sub-DACs were omitted. (b) PTAT reference generator for *XY* sub-DACs. Start-up circuitry omitted. (c) Segmented DAC architecture. The signal routing circuit is also shown.

its ports. This helps to avoid distortion due to coupling between the transformer ports from the transparency of the passive mixers. Referring now to the *Q* channel, the DRAG envelope is generated using an array of ten sub-DACs. The sub-DAC values are set to one of 16 pre-programmed values and the polarity of the first five sub-DACs is set opposite to the remaining five. The sub-DACs are then sequentially enabled to generate two current pulses, which flow in opposite directions through the circuit, resulting in an envelope with odd symmetry. This pulse is combined with the raised-cosine-modulated pulse using a third 180° combiner and the output signal passes through a step attenuator at the chip output. The control circuitry orchestrating the activation and deactivation of each of the sub-DACs is clocked from the system clock and is similar to that reported in [42], with additional controls to enable the DRAG pulse. When the chip is clocked at the nominal rate of 1 GHz, the *XY* pulse duration is 22 ns.

Fig. 7 shows the *XY* sub-DAC details. As shown in Fig. 7(a), a common reference current generator sources two sets of four currents, which are each mirrored 21 ways to provide each sub-DAC with the four currents required for its operation. Each of the mirrors in the current distribution network has 5 bits of binary control. This flexibility was added to overcome uncertainty associated with the cryogenic behavior of the transistors, which was expected to be exacerbated due to the low current levels (used to minimize dc power).

The reference currents are generated using a CMOS proportional to absolute temperature (PTAT) circuit [Fig. 7(b)]. Obtaining the amplitude stability needed to reach the desired fidelity requires ensuring the reference current is insensitive to time-dependent supply variations, which are expected in this application due to wiring resistances from room temperature down to the cryo-CMOS IC. To minimize supply voltage sensitivity, transistors in this circuit are cascoded and use maximum length devices (2 μm). In addition, $R_{XY,\mathrm{PTAT}}$ has 8 bits of control to ensure that an appropriate current can be obtained at cryogenic temperatures. Unsalicided polysilicon resistors were used in this circuit and elsewhere in the design.

The 10-bit sub-DAC schematic is shown in Fig. 7(c). It is segmented into five MSBs and five LSBs, with thermometer encoding employed in both segments. The sub-DAC uses a wide-swing-cascode current-mirror architecture. The output of each sub-DAC flows through two single-pole double-throw (SPDT) switches. The first switch enables the output or sends the current to an on-chip 50-Ω resistor. The potential on each side of this resistor can be measured via an on-chip analog monitor bus, enabling off-line calibration of the individual sub-DACs.[6] The second switch serves as a polarity switch, enabling the routing of the current to a positive or negative output port.

The mixer and LO drive chain used in this work are identical to that reported in [42]. However, as discussed above, a network of transformer-based 180° combiners was used to combine the various RF signals, preventing crosstalk.

LO leakage cancellation was also incorporated to improve the achievable ON-to-OFF ratio. This was implemented by injecting a static current into each of the four mixer input ports via a 2-kΩ resistor. These currents are generated via 14-bit current-mode DACs (identical to those described in the following) and are used to leak a controllable amount of LO signal to each mixer output; by selecting the correct combination of these currents, it is possible to control both the amplitude and phase of the leaked LO signal, as required to cancel feedthrough.

B. g/Z Controller

A block diagram of the *g* and *Z* controller circuit is shown in Fig. 8. It contains an array of eight single-ended 14-bit

[6]We note that, in the experimental work described in Section IV, the monitor bus was used for observation rather than calibration.

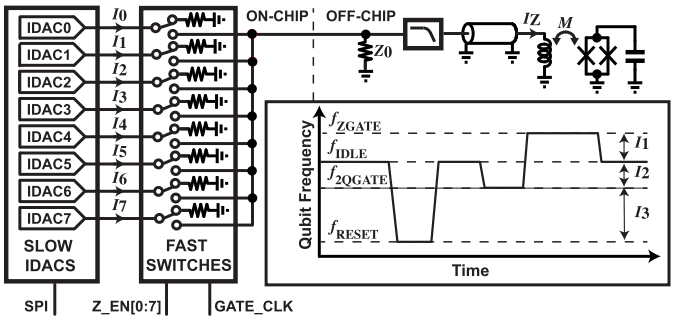


Fig. 8. Block diagram of g/Z controller with example Z control waveform.

current-mode sub-DACs whose outputs are routed by fast SPDT switches to the chip output or to ground via on-chip 50-Ω resistors. The sub-DAC values are loaded via SPI, with the settings determined during quantum processor calibration and fixed during operation. On the other hand, the switches are toggled dynamically by the controller. Therefore, during the execution of an algorithm, this configuration is capable of switching between up to nine independent current values, including a zero-bias state. As mentioned in Section II, this is adequate for the envisioned Z and g control use cases, where the qubits and coupler must be commanded to a finite set of frequencies. This approach, in which static currents are routed to the output through a fast switch, is advantageous for two primary reasons. First, the integral nonlinearity/differential nonlinearity (INL/DNL) specifications for the sub-DACs are relaxed, as sub-DAC current values are static during operation and not updated after processor calibration is complete. Thus, as long as the DACs have sufficient degrees of freedom to reach the required current values, the INL/DNL of each of the sub-DACs is of second-order importance. Second, it allows for the timing resolution of a 1-GHz clock while avoiding the power consumption associated with a high-speed DAC. Rather, the power consumption is limited by the largest current that must be supplied to the quantum processor, which, in the case of the Sycamore architecture, is required for the reset gate. As in the case of the XY controller, the voltage on each side of the on-chip 50-Ω resistors can be read-out through the analog monitor bus, allowing for off-line calibration of the sub-DAC currents.

The output signal is terminated off-chip, filtered via an absorptive 250-MHz Gaussian low-pass filter, and routed to the relevant g or Z port of the quantum processor. The absorptive filter provides a wideband output match, as required for direct drive of the g and Z ports, and limits the pulse rise time to ≈2 ns, as required to avoid exciting diabatic transitions. The schematics of the g/Z sub-DACs are shown in Fig. 9. As shown in Fig. 9(a), each of the g/Z sub-DACs has its own reference current generator, which generates three reference currents that are mirrored to bias the segmented sub-DAC core.

The g/Z sub-DAC reference current generators [Fig. 9(b)] are based on a PTAT circuit, similar to those in the XY circuit. Here, regulated cascodes have been used to minimize supply sensitivity and resistor $R_{Z,\mathrm{PTAT}}$ has 6 bits of reconfigurability. Since each of the sub-DACs has their own programmable reference generator, the range of each sub-DAC is independently controllable. This flexibility was added to address uncertainty related to the lack of cryogenic transistor models. A simplified schematic of the 14-bit sub-DAC core circuit is shown in Fig. 9(c). It is a segmented current-mirror DAC, where the five LSBs are binary encoded and the other two banks are thermometer encoded. In the actual circuit, the transistors have been replaced with regulated cascodes and additional trimming circuitry allows alignment between the segments.

It was possible to estimate the dynamic and static performance of g/Z controller using the foundry PDK with appropriate assumptions related to changes with cryogenic cooling. However, due to the lack of adequate noise models, it was not feasible to predict the noise performance. As such, we neglected this during the design process with plans to evaluate the performance experimentally.

C. Digital Controller

The chip also features a digital controller that allows triggering of algorithms via a single trigger pulse. At the core of the controller is an instruction timer and an instruction sequencer, the latter of which is distributed across the chip, with blocks local to each of the five signal generators.

A block diagram of the instruction timing circuitry is shown in Fig. 10(a). This circuit accepts a trigger and outputs a 9-bit instruction pointer, `INSTR<0:8>`, and a gate clock signal, used to trigger events. The circuit contains three main subsystems. First, a triggering circuit arms the system on the rising edge of an externally applied trigger signal, enabling the digital system clock to reach internal control blocks. Second, a gate-clock generation circuit produces a sequence of single-clock-cycle pulses that are used to trigger events. The dead time between these pulses is set by a 4-bit control signal, which is updated dynamically by the controller and selects between 16 different durations (each of 16-bit resolution and preloaded via SPI). This circuit can operate with inter-pulse dead times from 2 ns to 65.535 ms, given the 1-GHz system clock. Third, an instruction counter generates an instruction pointer that increments with each gate-clock pulse and provides a termination signal that is used to reset the circuit when the instruction count reaches a preset value (loaded via SPI).

The instruction timing circuit of Fig. 10(a) interfaces with instruction sequencers that are local to the XY, Z, and g waveform generators. Each waveform generator has a 16-element waveform memory [Fig. 10(b)], which is preloaded during chip initialization. Nominal waveform values are determined during the quantum processor calibration process. As described in Section II, this waveform memory depth is sufficient for storage of a gateset that is universal for quantum computing. Instruction sequencers are provided to orchestrate events in the XY, Z, and g controllers and to set the duration between gate clock cycles. During each gate-clock cycle, the circuit executes a 26-bit instruction `[XY1<0:3>; XY1EN; XY2<0:3>; XY2EN; Z1<0:3>; Z2<0:3>; g<0:3>; DUR<0:3>]`, where the 4-bit words are used to select which of the waveform table entries to play back and `XY1EN` and `XY2EN` are used to enable the respective XY pulse output. Local circuitry, programmable via the SPI, allows for independently delaying the start of the XY, Z, and g events by up to 15 clock cycles. An example instruction sequence

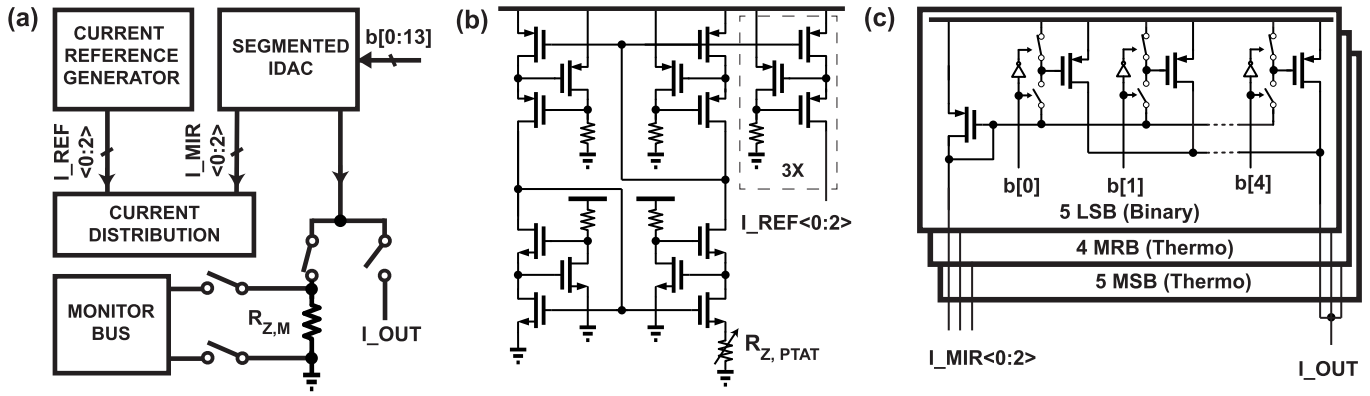


Fig. 9. Simplified 14-bit Z sub-DAC schematic. (a) Block diagram. (b) PTAT reference current for each of the eight sub-DACs. (c) Segmented sub-DAC core.

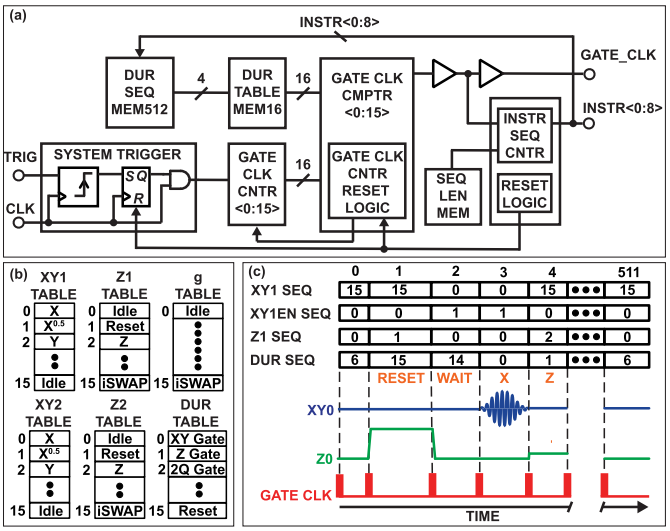


Fig. 10. Digital controller. (a) Block diagram of instruction timing circuitry. (b) Arrangement of 16-element waveform memories. (c) Example sequence for single-qubit control and corresponding waveforms.

focusing on single-qubit control using Channel 1 is shown along with the corresponding waveforms in Fig. 10(c). In a more scaled system, the instructions would be generated from a microcontroller rather than the sequencer used here.

IV. Results

The quantum control IC was fabricated in a 28-nm bulk-CMOS process, and a die micrograph is shown in Fig. 11(a). The chip measures 1.8 × 3.9 mm and was packaged in a connectorized housing for cryogenic testing. As shown in Fig. 11(a) and (b), the IC was mounted within a cutout in a printed circuit board (PCB) to minimize bondwire lengths and keep signal–signal coupling and parasitic inductances low.

The module was mounted on the 3 K stage of a dilution refrigerator [Fig. 11(d)] and connected to a two-qubit sub-circuit of a 54-qubit Sycamore quantum processor. The qubits employed in the experiments—referred to as qubits 1 and 2—had measured $f_{\max}$ values of 7.12 and 6.99 GHz, respectively. Both qubits had anharmonicity parameters of about −200 MHz, with coherence times T_1 in the range of 7–9 μs for f_{01} within 300 MHz of $f_{\max}$ (this is lower than typical for our processors and bounds the reported errors).

A simplified test setup block diagram is shown in Fig. 12. The LO and clock signals required by the cryo-CMOS IC were generated at room temperature using commercial synthesizers. The quadrature and differential phases of these signals required by the IC were generated at 3 K using quadrature hybrids and a balun, mounted to the backside of the module. The chip's SPI port was interfaced to a room-temperature microprocessor and the trigger signal was driven via a room-temperature arbitrary waveform generator (AWG). The chip's five output signals were each connected to the relevant ports of the quantum processor with a SOI-CMOS SPDT switch (Analog Devices ADRF5021) included in the signal path to allow selection between the relevant cryo-CMOS output and a corresponding signal that was generated using baseline room-temperature electronics [7]. This both allowed for the acquisition of baseline measurements using room-temperature electronics and also enabled hybrid measurements, where a subset of the signals were generated by the cryo-CMOS IC and the remaining signals were generated using the baseline room-temperature electronics. These hybrid measurements enabled the use of existing metrology procedures for isolated characterization of each of the control functions.

Several additional components were integrated into the XY, Z, and g control paths to condition and route the signals. Each of the cryo-CMOS IC's XY outputs drove a 20-dB coupler and 20-dB attenuator at 3 K. An additional 20 dB of attenuation was included at 10 mK prior to connection to the quantum processor's XYZ port via the RF port of a bias tee, which was used to diplex the XY and Z control signals. The output of each coupler was amplified using a cryogenic low-noise amplifier with ≈40 dB gain. While necessary to observe the XY waveforms on an oscilloscope, this amplifier does not have sufficient linearity to prevent imparting some distortion on the RF pulses. The g and Z lines were low-pass filtered at 3 K before further filtering by an IR-blocking filter at 10 mK. The g signal was directly interfaced to the associated quantum processor port, whereas the Z signals connected to the XYZ ports of the quantum processor via the dc ports of bias tees. Finally, 20 dB of attenuation was incorporated in series with each of the baseline signal paths at 3 K to reduce the noise floor on these lines. All measurements were orchestrated using our standard quantum-computer software

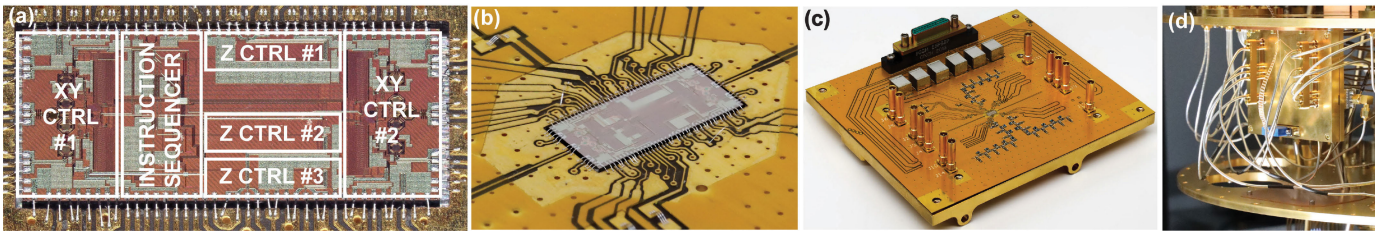


Fig. 11. (a) Die micrograph. The chip measures 1.8 × 3.9 mm. (b) Packaged IC. The chip was mounted within a cut-out of a PCB to minimize the wirebond length. (c) PCB with chip mounted on the cryogenic module. (d) Cryogenic module mounted onto the 3 K stage of a dilution refrigerator.

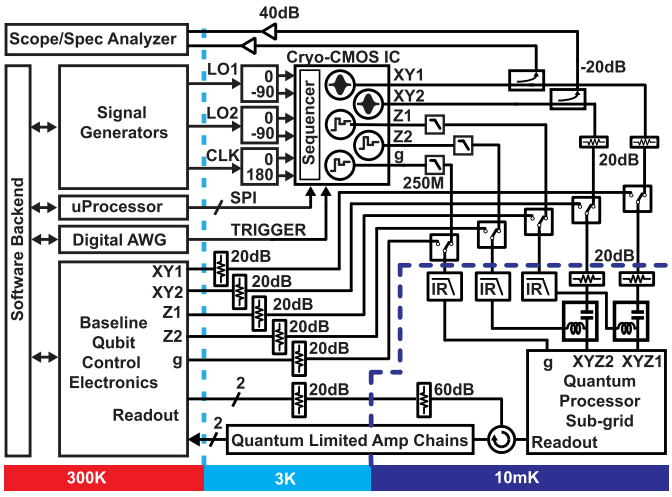


Fig. 12. Block diagram of the test setup used for quantum control experiments.

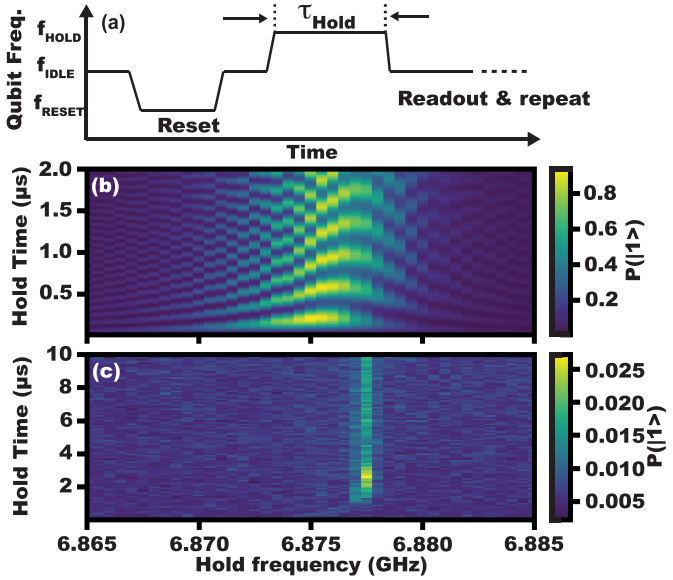


Fig. 13. LO nulling: (a) protocol, (b) spectrogram prior to nulling, and (c) spectrogram after nulling.

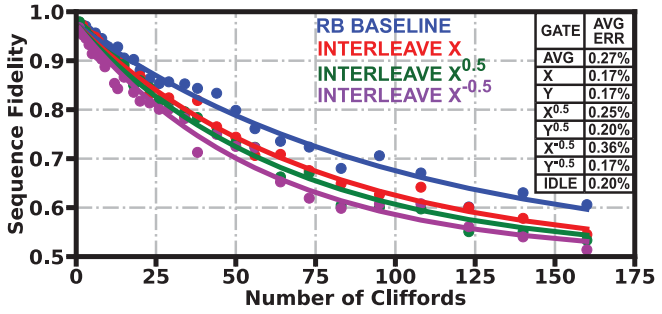


Fig. 14. *XY* randomized benchmarking (RB) results. The RB result for the baseline electronics is 0.2% (not shown).

backend. The physical temperature of the stage to which the cryo-CMOS IC was thermalized was less than 3 K for all reported measurements. Additional baseline electronics (not shown) were used to control and measure the qubits surrounding the two-qubit patch connected to the quantum control IC. Readout was accomplished using our standard hardware.

A. XY Control

With the cryo-CMOS IC installed within the dilution refrigerator and cooled to 3 K, we first characterized the performance of the cryo-CMOS *XY* controllers. For these experiments, the g and Z ports of the quantum processor were controlled by the baseline room-temperature electronics, and the g and Z port tuning curves had been previously calibrated.

1) LO Leakage Nulling: We began by performing LO leakage nulling using the protocol shown in Fig. 13(a). First, the qubit is reset by tuning it into resonance with its readout resonator. It is then brought to f_{IDLE}, which is off-resonant with the LO signal frequency, f_{LO}. Next, the qubit is tuned to f_{HOLD} for a duration τ_{HOLD}. During this time, if f_{HOLD} is sufficiently close to f_{LO}, any LO leakage will drive oscillations between the $|0\rangle$ and $|1\rangle$ states. Finally, the qubit is tuned back to f_{IDLE} and its state is read out. The experiment was carried out as a function of both f_{HOLD} and τ_{HOLD}, with statistics collected at each point to estimate the $|1\rangle$ state population.

Initial results obtained for qubit 1 prior to enabling the LO leakage nulling are shown in Fig. 13(b). A chevron pattern centered around $f_{\mathrm{LO}} = 6.875$ GHz was observed, confirming the presence of strong enough LO leakage to drive the qubit coherently. Given the observed Rabi oscillation period of about 300 ns, LO leakage was found to be strong enough to severely impact both initialization fidelity and gate error rates.[7]

We next used an optimization routine to find nominal values of the LO nulling currents by minimizing the $|1\rangle$ state

[7]The dominant source of LO leakage is believed to be between the center conductors of RF connectors on the PCB. This could be improved by a PCB redesign.

population for τ_{hold} ranging from 100 ns to 10 μs. Example results obtained after running this optimization for qubit 1 are shown in Fig. 13(c). In this case, the drive due to LO leakage was sufficiently weak that it resulted in a negligible incoherent population of <2.5% on a timescale of the qubit coherence time. This level of parasitic drive is sufficiently low to permit high-fidelity initialization and gates.

2) XY Gate Benchmarking: We next characterized the average gate error rates achievable by the XY controller using randomized benchmarking (RB) [51]. For this, we first determined waveform parameters for X, Y, $X^{0.5}$, $X^{-0.5}$, $Y^{0.5}$, and $Y^{-0.5}$ gates, using standard gate calibration techniques [52]. This set of gates allows compilation of the full set of single-qubit Clifford gates, as required for RB. In combination with a set of Z gates, it also allows the construction of a single-qubit gateset that is universal for quantum computing.

The decay curve we obtained through RB is plotted in Fig. 14 (RB baseline curve). From these data, we obtained an average gate error rate of 0.27% per XY gate. This compares well with the average error rate of about 0.2%, obtained using the room-temperature baseline electronics.

We next performed interleaved RB (IRB) [53] to quantify the performance of the individual XY gates. Example decay curves appear along with extracted average error rates for each of the gates in Fig. 14. Remarkably, all but two of the gates achieved error rates at least as low as the idle gate, indicating that, with improved gate calibration, we could likely improve the error rate performance of the $X^{0.5}$ and $X^{-0.5}$ gates.

B. Z Control

Next, we characterized the performance of the cryo-CMOS Z control channels while generating the XY and g signals using the baseline room-temperature electronics. Since, to the best of our knowledge, this is the first reported use of a cryo-CMOS IC to control the Z ports of a quantum processor—and we do so without attenuation on the 3 K stage of the signal path—we include details related to static performance and gate tune-up before describing gate benchmarking.

1) Z Tuning Curve: We first found the relationship between the ZDAC settings and the qubit frequencies via the spectroscopic approach shown in Fig. 15 [52]. Here, we biased the qubit with the Z controller and made two sets of measurements. First, we simply read out the qubit state many times and found the average IQ coordinates for the $|0\rangle$ state. Next, we repeated the experiment but first excited the qubit with a weak XY pulse centered at f_{test} before making a measurement. Finally, we calculated the IQ plane displacement caused by the XY drive, which is proportional to the $|1\rangle$ state population. We repeated this experiment sweeping f_{test} and stepping through many ZDAC settings.

Example spectroscopy data are shown in Fig. 15(d). The qubit frequency at a given bias can be estimated from the spectroscopy curve peaks. The experiment was repeated for a wide range of Z DAC currents and used to extract a tuning curve, as shown for qubit 2 in Fig. 15(e). Good agreement between the nominal and observed shape of the tuning curve was observed, indicating that the Z sub-DACs have excellent linearity.

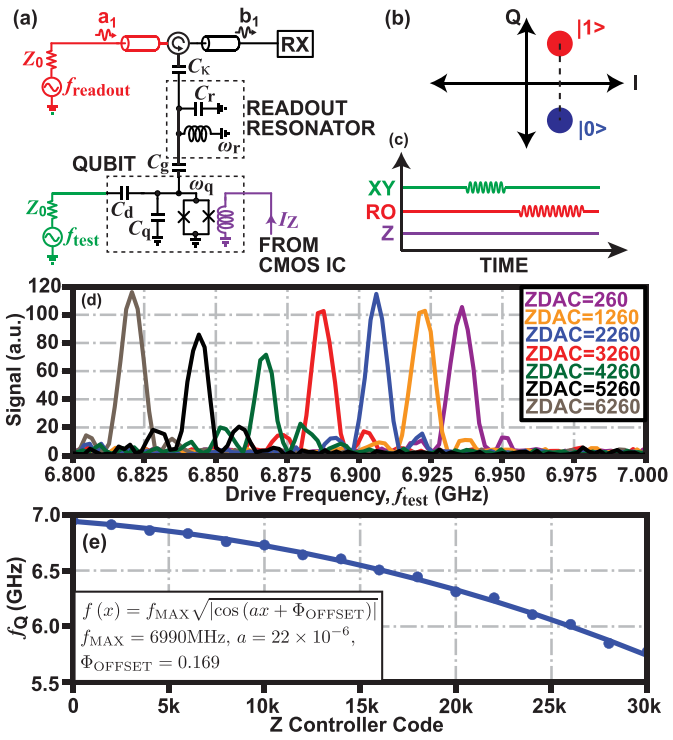


Fig. 15. Spectroscopy experiment. (a) Experimental setup. The readout and XY ports are under room-temperature control, whereas the Z port is under cryo-CMOS control. (b) Readout constellation for the $|0\rangle$ and $|1\rangle$ states. When averaged, superposition states will map along the dashed line. (c) Experimental protocol. (d) Example data for different ZDAC settings. (e) Measured and fit qubit frequency as a function of ZDAC setting. One LSB corresponds to a current of about 7 nA.

2) Reset Gate: We next tuned up an active reset gate, which sets the qubit to its $|0\rangle$ state orders of magnitude faster than the native T_1-based passive reset. In the Sycamore architecture, this gate is carried out by bringing the qubit into resonance with its (low-Q) readout resonator so that an excitation stored in the qubit can be dissipated into this lossy component. The protocol employed to tune-up this gate is described in Fig. 16. The qubit is first excited to the $|1\rangle$ state using an XY π-pulse, and then, a current pulse of varying amplitude and duration is applied to the qubit Z port, causing the qubit frequency to drop for the duration of the pulse. Finally, the qubit's state is read out. At each point, $|1\rangle$ population is estimated statistically. The goal of this tune-up is to find the appropriate Z current to minimize the time required to reset the qubit to the $|0\rangle$ state.

Data taken for qubit 1 are shown in Fig. 16. The nominal Z controller reset code was found to be about 42 000 (requiring three sub-DACs) and readout-limited initialization errors were achieved for reset pulses as short as 300 ns. Compared to $\approx 10 \times T_1 \approx 90$ μs that is typically used for passive reset, this active reset is orders of magnitude faster.

3) Z Gate Tuneup: We next tuned up physical Z, $Z^{0.5} = S$, and $Z^{0.25} = T$ gates, corresponding to 180°, 90°, and 45° rotations of the qubit state about the Z-axis of the Bloch sphere, respectively. We note that, when combined with the XY gates benchmarked above, these gates form the basis for a single-qubit gateset that is universal for quantum computing.

We used the Ramsey protocol shown in Fig. 17(a) to calibrate these gates. Here, the qubit is first reset to its $|0\rangle$ state,

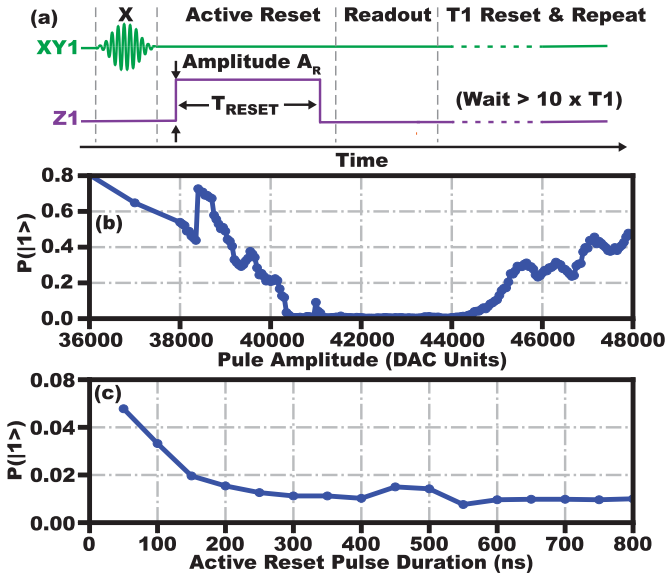


Fig. 16. Active reset calibration. (a) Protocol used for determining reset pulse amplitude. (b) Calibration results for 800-ns pulse versus ZDAC code. (c) Calibration results for ZDAC code of 42 000 versus pulse duration. One LSB corresponds to a current of about 7 nA.

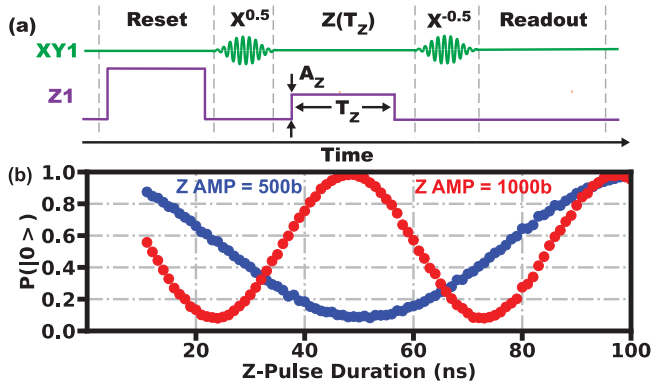


Fig. 17. Ramsey experiment. (a) Protocol. (b) Example data.

and then, an $X^{0.5}$ pulse is applied, rotating the qubit state 90° about the X-axis to the equator of the Bloch sphere. A Z pulse of varying duration is then applied, causing a frequency detuning and corresponding rotation about the Z-axis. Finally, an $X^{-0.5}$ pulse is applied, rotating the qubit state $-90°$ about the X-axis, and a state measurement is performed. For a given Z pulse amplitude, the experiment was repeated for different Z pulse durations and statistics were acquired at each point.

Example results are shown in Fig. 17(b). As expected, we observed clean Ramsey oscillation curves, with the period inversely proportional to the programmed ZDAC current. By varying the pulse amplitude, we were able to determine appropriate ZDAC parameters to achieve Ramsey oscillation frequencies of 20, 10, and 5 MHz, as required to implement the desired 25-ns Z, S, and T gates.

4) Z Gate Benchmarking: We performed IRB to quantify the performance of the Z gates. The baseline decay curve appears alongside the curve for interleaved Z gates in Fig. 18. As also shown in Fig. 18, the controller achieved error rates below 0.2% for all three gates, which is consistent with the achieved XY gate error rates and likely coherence limited.

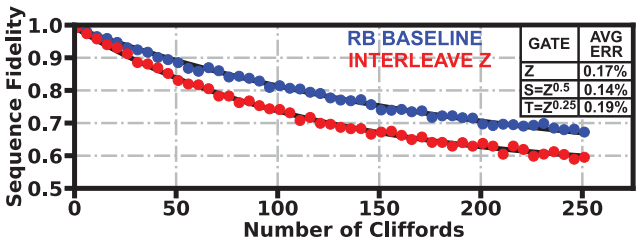


Fig. 18. Z IRB results.

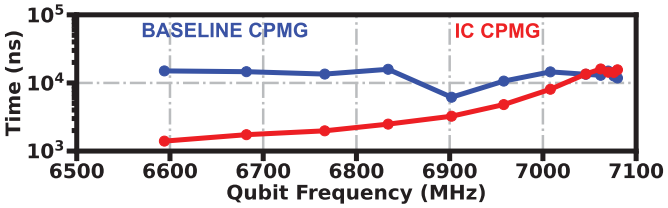


Fig. 19. $T2^{\star}_{\mathrm{CPMG}}$ versus qubit frequency for the IC and baseline electronics.

5) Dephasing: Finally, we measured the dephasing performance to quantify the impact of noise on the Z control lines on qubit coherence. The measured dephasing rate while employing standard Carr–Purcell–Meiboom–Gill (CPMG) refocusing [54], [55], $T_{2,\mathrm{CPMG}}$, appears for the baseline and cryo-CMOS controllers in Fig. 19. We were able to achieve similar qubit dephasing performance at modest frequency offsets from qubit $f_{\max}$, but at larger offsets, we saw lower dephasing performance from the cryo-CMOS IC. This indicates that the cryo-CMOS Z control channels do not meet the noise specification set forth in Section II-B. We explain the inferior performance under cryo-CMOS control and its bias dependence both by excess noise injected by the reference and mirroring circuitry and by the channel noise current dependence on drain current [56], [57], [58], which leads to an increase in the current noise spectral density as the qubit is tuned to lower frequencies. This increase in current noise is exacerbated by the enhancement to the qubit tuning sensitivity that occurs at higher frequency offsets [see (1)]. While we believe that the excess Z noise can be overcome through adjustments to the circuit architecture, we note that for frequency offsets as high as 100 MHz from $f_{\max}$, we found through RB that the noise from the cryo-CMOS Z controller had no observable impact on gate performance. Nonetheless, we believe that cryo-CMOS Z controllers with significantly reduced broadband noise can be realized.

C. Two-Qubit Gates

We next evaluated the performance of the IC in doing two-qubit gates. Here, we controlled the quantum processor's XY and g ports with the baseline room-temperature electronics and cryo-CMOS IC, respectively. Sets of experiments were performed both with the Z ports controlled by the baseline room-temperature electronics and by the cryo-CMOS IC. We focused on characterizing iSWAP-like gates, which are a subset of the Sycamore architecture's native fsim gate class [47].

TABLE II

PERFORMANCE OF BASELINE ELECTRONICS AND STATE-OF-THE-ART QUANTUM CONTROL ICS CHARACTERIZED WITH A QUANTUM PROCESSOR

Reference/Hardware	[13]	[16]	[17]	This: Baseline	This: Cryo-CMOS IC
Qubit type	Transmon	Spin	Transmon	Transmon	Transmon
Tech Node	28-nm Bulk	22-nm FinFET	14-nm FinFET	N/A	28-nm Bulk
Die Area	1.6 mm^2	4 mm^2 *	3.2 mm^2	N/A	7 mm^2
Operating Temperature	3 K	3 K	3 K	Room Temperature	3 K
Architecture					
Channels	1 XY	16 XY (FDM/TDM)**	2 XY	N/A	2 XY, 2 Z, 1 g
XY Control	Direct Conversion	Single Sideband	Single Sideband	Single Sideband	Direct Conversion
Z Control	N/A	Virtual	Virtual	Physical and Virtual	Physical
2Q Control	N/A	RF	RF	Baseband	Baseband
Instruction set	4-bit	8 per NCO	37 × 32-bit	N/A	26-bit
Program Execution	External control	2048-step sequencer	Microprocessor	FPGA	512-step sequencer
Performance					
XY Frequency Range	4–8 GHz	2–20 GHz	4.5–5.5 GHz	2.5–7.2 GHz	4–8 GHz
XY Average Gate Error	Not Reported	0.31%	0.78%	0.2%	0.17–0.36%
Z Average Gate Error	N/A	N/A	N/A	N/A	0.14–0.19%
2-Qubit Average XEB Cycle Error	N/A	Not Reported	Not Reported	1.1±0.2%	1.2±0.3%
Power/Qubit Under Active Control	< 2 mW	192 mW	23 mW	> 5 W	< 4 mW

*Die area for part of chip used during measurements. **FDM allows drive of 2 qubits simultaneously. 16 NCOs for FDM.

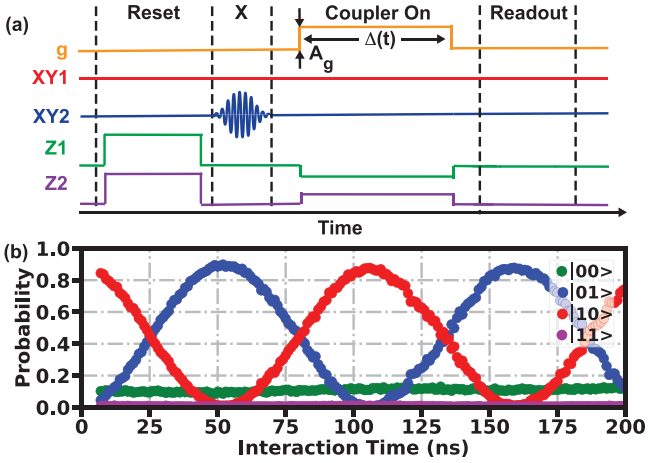


Fig. 20. (a) Control waveforms used during swap experiment. (b) Swapping between $|01\rangle$ and $|10\rangle$ using settings for a 27 ns$\sqrt{\text{iSWAP}}$-like gate.

1) Gate Calibration: During the normal operation, the qubits idle at different frequencies and coupling between the qubits is disabled. During an iSWAP-like gate, the qubits are first brought on resonance by the Z controls, and then, the g control is used to momentarily enable coupling between the qubits before the qubits are tuned back to their idling values. Doing such a gate requires first determining appropriate values for the g and Z biases, both during idling and the two-qubit gate. We used the protocol described in Fig. 20(a) to iteratively determine parameters for iSWAP-like and $\sqrt{\text{iSWAP}}$-like gates. Here, we start with the qubits in the $|0\rangle$ state while idling off resonance and the g line biased to $I_g = I_{\text{OFF}}$, so the qubit–qubit coupling is disabled. We then excite one of the qubits to the $|1\rangle$ state and tune the qubits into resonance. Next, we apply a pulse of length Δt and amplitude A_g to the coupler bias, enabling coupling and causing the excitation to oscillate back and forth between the qubits at a rate proportional to A_g. Finally, we bring the qubits back off resonance and measure the state. The experiment is run as a function of Δt and statistics are acquired at each point.

With the Z lines under control of the baseline room-temperature electronics, we first determined the g controller setting to disable coupling by running the experiment with $A_g = 0$ and sweeping the g current. The nominal I_{OFF} setting was determined by finding the point that minimized oscillations between the $|10\rangle$ and $|01\rangle$ states. Next, we determined appropriate values for A_g to realize iSWAP-like and $\sqrt{\text{iSWAP}}$-like gates by adjusting this amplitude to get the desired swap rates. Finally, once parameters for the coupler setting were determined, we changed the Z control lines to the cryo-CMOS controller and optimized the frequency detuning values for each of the Z lines to maximize swap visibility.

Experimental results for the tuned-up parameters corresponding to a $\sqrt{\text{iSWAP}}$-like gate with $\Delta t = 27$ ns are shown in Fig. 20(b). As expected, swapping between $|10\rangle$ and $|01\rangle$ was observed, with a period of about 108 ns. The observed $|00\rangle$ population is related to $|1\rangle$ state readout errors.

2) Cross-Entropy (XEB) Benchmarking: We evaluated the error rates of a $\sqrt{\text{iSWAP}}$-like gate with the cryo-CMOS IC providing g control and also with it providing both g and Z (gZ) control. Our iSWAP-like gates carry extra single-qubit phases as well as a (undesired) controlled phase ϕ [47], the latter of which can be zeroed through careful tune-up [59]. As such, we used two-qubit cross-entropy benchmarking (XEB) benchmarking [1] to estimate fidelity, which allows us to take up unwanted phases (ϕ here) without impacting the fidelity, and is thus useful for benchmarking the controller and comparing to existing controllers without deep-diving into gate tune-up to minimize ϕ. Example benchmarking results are shown in Fig. 21 along with the refitted gate parameters and error rates for both cases, as well as an iSWAP-like gate carried out using the baseline room-temperature electronics. The cryo-CMOS IC achieved an XEB cycle[8] infidelity of 1.0% ± 0.2% and 1.2% ± 0.3% when providing g and gZ control, respectively. This shows excellent agreement with the XEB cycle error

[8]An XEB cycle includes two single-qubit gates and one two-qubit gate.

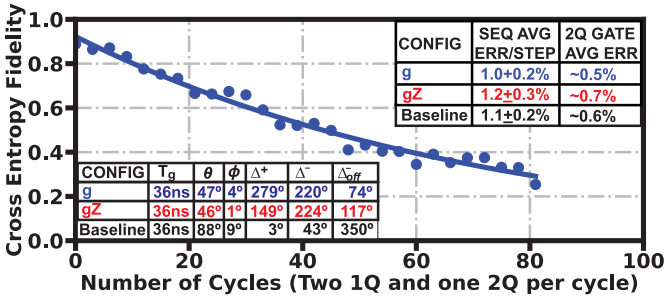


Fig. 21. XEB results. T_g: gate duration; θ: swap angle; ϕ: controlled phase; and Δ^+, $\Delta^=$, and Δ^-_{OFF}: single-qubit phases (see [47]).

of $1.1\% \pm 0.2\%$ for the iSWAP-like gate using the baseline room-temperature electronics. These values, which include separately measured single-qubit average error rates of 0.26%, correspond to two-qubit error rates of 0.5% and 0.7% for g and gZ control, respectively.

D. Power Consumption and Comparison to the State-of-the-Art

The dc power consumption of the IC was measured for a high activity factor and found to be 7.4 mW ($g + Z_1 + Z_2 = 1.3$ mW, $XY_1 + XY_2 = 3.8$ mW, and digital $= 2.3$ mW). The cryo-CMOS IC's performance is compared to the state-of-the-art cryo-CMOS control ICs that have been characterized with quantum processors in Table II. The IC provides competitive XY, Z, and two-qubit gate performance and, of the other reported quantum control ICs, it is the only one that has been benchmarked for all of the elements of a gateset that is universal for quantum computing.

V. Conclusion

The results presented here show that it is feasible to achieve excellent single- and two-qubit gate performance using a control architecture that is specifically tailored towards control of a superconducting quantum processor and, hence, is much more energy-efficient than the AWG-based control systems that are widely in use across the field. The level of power consumption demonstrated here—approximately 2.4 mW per XY channel and 0.9 mW per flux bias—correspond to a power consumption of about 5 mW/qubit for control of a large-scale processor of the Sycamore architecture, which has a higher density of flux control lines compared to the two-qubit patch that was addressed by the cryo-CMOS IC. Assuming that 1 kW of cooling capacity could be devoted to cooling of the quantum controller, this would permit integration of a $\mathcal{O}(200000)$ qubit quantum controller. However, our proof-of-concept demonstration is far from a deployable solution, and significant research and development is still required to make such a large-scale quantum controller a reality.

For example, the results shown here relied upon our baseline room-temperature electronics, which are tightly integrated with a software backend that permits using mature calibration and metrology techniques. To transition from the proof-of-concept work presented here to ICs that can be deployed at scale, similar routines must be developed and may even need to be integrated so that processor bring-up can run autonomously. Additionally, at a scale beyond a few tens of qubits, arrays of ICs will be required and these chips must operate coherently while maintaining low dc power; implementation of such a distributed quantum controller will likely require developing dense packaging and, if the controller is cryogenically cooled, this packaging must be robust to wide temperature swings. Finally, while the performance presented here was promising, the achievable error rates must be improved (e.g., by reducing Z noise) before the hybrid cryo-CMOS/quantum system can be used to implement QEC protocols and the power consumption of the cryo-CMOS quantum controller should be reduced. These topics, among others, are the focus of our ongoing research.

References

[1] F. Arute et al., "Quantum supremacy using a programmable superconducting processor," *Nature*, vol. 574, no. 7779, pp. 505–510, 2019.
[2] Y. Wu et al., "Strong quantum computational advantage using a superconducting quantum processor," *Phys. Rev. Lett.*, vol. 127, no. 18, Oct. 2021, Art. no. 180501.
[3] H.-S. Zhong et al., "Quantum computational advantage using photons," *Science*, vol. 370, no. 6523, pp. 1460–1463, 2020.
[4] A. Deshpande et al., "Quantum computational advantage via high-dimensional Gaussian boson sampling," *Sci. Adv.*, vol. 8, no. 1, Jan. 2022, Art. no. eabi7894.
[5] R. Acharya et al., "Suppressing quantum errors by scaling a surface code logical qubit," *Nature*, vol. 614, no. 7949, pp. 676–681, Feb. 2023.
[6] G. Zettles, S. Willenborg, B. R. Johnson, A. Wack, and B. Allison, "Design considerations for superconducting quantum systems," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 1–3.
[7] J. Bardin, "Beyond-classical computing using superconducting quantum processors," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 422–424.
[8] D. B. Tuckerman et al., "Flexible superconducting Nb transmission lines on thin film polyimide for quantum computing applications," *Superconductor Sci. Technol.*, vol. 29, no. 8, Aug. 2016, Art. no. 084007.
[9] S. Gustavsson et al., "Improving quantum gate fidelities by using a qubit to measure microwave pulse distortions," *Phys. Rev. Lett.*, vol. 110, no. 4, Jan. 2013, Art. no. 040502.
[10] M. A. Rol et al., "Time-domain characterization and correction of on-chip distortion of control pulses in a quantum processor," *Appl. Phys. Lett.*, vol. 116, no. 5, Feb. 2020, Art. no. 054001.
[11] S. R. Ekanayake, T. Lehmann, A. S. Dzurak, and R. G. Clark, "Quantum bit controller and observer circuits in SOS-CMOS technology for gigahertz low-temperature operation," in *Proc. 7th IEEE Conf. Nanotechnol. (IEEE NANO)*, Aug. 2007, pp. 1283–1287.
[12] E. Charbon et al., "Cryo-CMOS circuits and systems for scalable quantum computing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 264–265.
[13] J. C. Bardin et al., "A 28 nm bulk-CMOS 4-to-8 GHz İ2 mW cryogenic pulse modulator for scalable quantum computing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 456–458.
[14] B. Patra et al., "A scalable cryo-CMOS 2-to-20 GHz digitally intensive controller for 4× 32 frequency multiplexed spin qubits/transmons in 22 nm FinFET technology for quantum computers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 304–306.
[15] D. J. Frank et al., "A cryo-CMOS low-power semi-autonomous qubit state controller in 14 nm FinFET technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 360–362.
[16] X. Xue et al., "CMOS-based cryogenic control of silicon quantum circuits," *Nature*, vol. 593, no. 7858, pp. 205–210, May 2021.
[17] S. Chakraborty et al., "A cryo-CMOS low-power semi-autonomous transmon qubit state controller in 14-nm FinFET technology," *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3258–3273, Nov. 2022.

[18] J. Gong, Y. Chen, F. Sebastiano, E. Charbon, and M. Babaie, "A 200dB FoM 4-to-5 GHz cryogenic oscillator with an automatic common-mode resonance calibration for quantum computing applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 308–310.

[19] S. J. Pauka et al., "A cryogenic CMOS chip for generating control signals for multiple qubits," *Nature Electron.*, vol. 4, no. 1, pp. 64–70, Jan. 2021.

[20] J.-S. Park et al., "A fully integrated cryo-CMOS SoC for qubit control in quantum computers capable of state manipulation, readout and high-speed gate pulsing of spin qubits in Intel 22 nm FFL FinFET technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 208–210.

[21] R. Acharya et al., "Overcoming I/O bottleneck in superconducting quantum computing: Multiplexed qubit control with ultra-low-power, base-temperature cryo-CMOS multiplexer," 2022, *arXiv:2209.13060*.

[22] Y. Peng, A. Ruffino, J. Benserhir, and E. Charbon, "A cryogenic SiGe BiCMOS hybrid class B/C mode-switching VCO achieving 201dBc/Hz figure-of-merit and 4.2 GHz frequency tuning range," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 364–366.

[23] K. Kang et al., "A cryo-CMOS controller IC with fully integrated frequency generators for superconducting qubits," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 362–364.

[24] G. Zhang, H. Lin, and C. Wang, "A calibration-free 12.8–16.5 GHz cryogenic CMOS VCO with 202 dBc/Hz FoM for classic-quantum interface," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 512–514.

[25] Y. Guo et al., "A polar-modulation-based cryogenic qubit state controller in 28 nm bulk CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 508–510.

[26] K. Kang, D. Minn, J. Lee, H.-J. Song, M. Lee, and J.-Y. Sim, "A cryogenic controller IC for superconducting qubits with DRAG pulse generation by direct synthesis without using memory," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 33–35.

[27] L. Enthoven, J. van Staveren, J. Gong, M. Babaie, and F. Sebastiano, "A 3 V 15b 157 μW cryo-CMOS DAC for multiplexed spin-qubit biasing," in *Proc. IEEE Symp. VLSI Technol. Circuits, VLSI Technol. Circuits*, Jun. 2022, pp. 228–229.

[28] K. Kang et al., "A 5.5 mW/channel 2-to-7 GHz frequency synthesizable qubit-controlling cryogenic pulse modulator for scalable quantum computers," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.

[29] J. Yoo et al., "A 28-nm bulk-CMOS IC for full control of a superconducting quantum processor unit-cell," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 506–508.

[30] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver, "A quantum engineer's guide to superconducting qubits," *Appl. Phys. Rev.*, vol. 6, no. 2, Jun. 2019, Art. no. 021318.

[31] J. C. Bardin, D. Sank, O. Naaman, and E. Jeffrey, "Quantum computing: An introduction for microwave engineers," *IEEE Microw. Mag.*, vol. 21, no. 8, pp. 24–44, Aug. 2020.

[32] J. C. Bardin, D. H. Slichter, and D. J. Reilly, "Microwaves in quantum computing," *IEEE J. Microw.*, vol. 1, no. 1, pp. 403–427, Jan. 2021.

[33] J. Koch et al., "Charge-insensitive qubit design derived from the Cooper pair box," *Phys. Rev. A, Gen. Phys.*, vol. 76, no. 4, Oct. 2007, Art. no. 042319.

[34] D. P. DiVincenzo, "Two-bit gates are universal for quantum computation," *Phys. Rev. A, Gen. Phys.*, vol. 51, no. 2, pp. 1015–1022, Feb. 1995.

[35] A. Barenco et al., "Elementary gates for quantum computation," *Phys. Rev. A, Gen. Phys.*, vol. 52, no. 5, pp. 3457–3467, Nov. 1995.

[36] D. P. DiVincenzo, "The physical implementation of quantum computation," *Fortschritte der Physik, Prog. Phys.*, vol. 48, nos. 9–11, pp. 771–783, Sep. 2000.

[37] D. C. McKay, C. J. Wood, S. Sheldon, J. M. Chow, and J. M. Gambetta, "Efficient *Z* gates for quantum computing," *Phys. Rev. A, Gen. Phys.*, vol. 96, no. 2, Aug. 2017, Art. no. 022330.

[38] A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland, "Surface codes: Towards practical large-scale quantum computation," *Phys. Rev. A, Gen. Phys.*, vol. 86, no. 3, Sep. 2012, Art. no. 032324.

[39] Cryomech. (2022). *PT420-RM Cryocooler Capacity Curve*. Accessed: May 10, 2023. [Online]. Available: https://cryomechprod.wpenginepowered.com/wp-content/uploads/2021/10/PT425-CPA1114-Capacity-Curve.pdf

[40] Linde. *L-Series: The New Standard for Helium Liquefiers and Refrigerators*. Accessed: May 10, 2023. [Online]. Available: https://www.linde-kryotechnik.ch/wp-content/uploads/2016/10/l-series_eng_en.pdf

[41] J. P. G. van Dijk et al., "Impact of classical control electronics on qubit fidelity," *Phys. Rev. Appl.*, vol. 12, no. 4, Oct. 2019, Art. no. 044054.

[42] J. C. Bardin et al., "Design and characterization of a 28-nm bulk-CMOS cryogenic quantum controller dissipating less than 2 mW at 3 K," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3043–3060, Nov. 2019.

[43] F. Motzoi, J. M. Gambetta, P. Rebentrost, and F. K. Wilhelm, "Simple pulses for elimination of leakage in weakly nonlinear qubits," *Phys. Rev. Lett.*, vol. 103, no. 11, Sep. 2009, Art. no. 110501.

[44] J. M. Chow et al., "Optimized driving of superconducting artificial atoms for improved single-qubit gates," *Phys. Rev. A, Gen. Phys.*, vol. 82, no. 4, Oct. 2010, Art. no. 040305.

[45] P. J. J. O'Malley, "Superconducting qubits: Dephasing and quantum chemistry," Dept. Phys., Univ. California, Santa Barbara, CA, USA, Tech. Rep., 2016.

[46] F. Yan et al., "Tunable coupling scheme for implementing high-fidelity two-qubit gates," *Phys. Rev. Appl.*, vol. 10, no. 5, Nov. 2018, Art. no. 054062.

[47] B. Foxen et al., "Demonstrating a continuous set of two-qubit gates for near-term quantum algorithms," *Phys. Rev. Lett.*, vol. 125, no. 12, Sep. 2020, Art. no. 120504.

[48] P. A. 'T Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and modeling of mismatch in cryo-CMOS," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 263–273, 2020.

[49] P. A. T Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Subthreshold mismatch in nanometer CMOS at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 797–806, 2020.

[50] E. Sartori, "Hybrid transformers," *IEEE Trans. Parts, Mater. Packag.*, vol. PMP-4, no. 3, pp. 59–66, Sep. 1968.

[51] E. Knill et al., "Randomized benchmarking of quantum gates," *Phys. Rev. A, Gen. Phys.*, vol. 77, no. 1, Jan. 2008, Art. no. 012307.

[52] Z. Chen, "Metrology of quantum control and measurement in superconducting qubits," Ph.D. dissertation, Dept. Phys., Univ. California, Santa Barbara, CA, USA, 2018.

[53] E. Magesan et al., "Efficient measurement of quantum gate error by interleaved randomized benchmarking," *Phys. Rev. Lett.*, vol. 109, no. 8, Aug. 2012, Art. no. 080505.

[54] H. Y. Carr and E. M. Purcell, "Effects of diffusion on free precession in nuclear magnetic resonance experiments," *Phys. Rev.*, vol. 94, no. 3, pp. 630–638, May 1954.

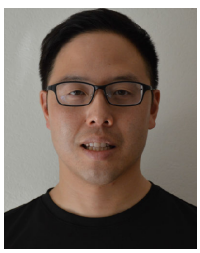
[55] S. Meiboom and D. Gill, "Modified spin-echo method for measuring nuclear relaxation times," *Rev. Sci. Instrum.*, vol. 29, no. 8, pp. 688–691, Aug. 1958.

[56] R. Navid, C. Jungemann, T. H. Lee, and R. W. Dutton, "High-frequency noise in nanoscale metal oxide semiconductor field effect transistors," *J. Appl. Phys.*, vol. 101, no. 12, Jun. 2007, Art. no. 124501.

[57] X. Chen, C.-H. Chen, and R. Lee, "Fast evaluation of the high-frequency channel noise in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1502–1509, Apr. 2018.

[58] S. Das and J. C. Bardin, "Characterization of shot noise suppression in nanometer MOSFETs," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 892–895.

[59] R. Barends et al., "Diabatic gates for frequency-tunable superconducting qubits," *Phys. Rev. Lett.*, vol. 123, no. 21, Nov. 2019, Art. no. 210501.



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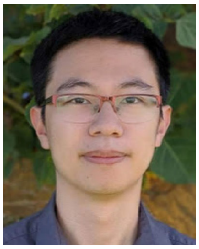

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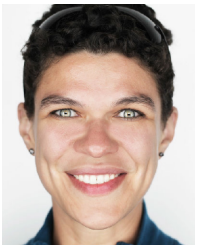

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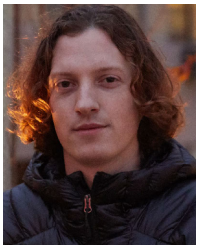

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