A 37–43.5-GHz Phase and Amplitude Detection Circuit With 0.049° and 0.036-dB Accuracy for 5G Phased-Array Calibration Using Transformer-Based Injection-Enhanced ILFD

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***Abstract*— This article introduces a high-accuracy phase and amplitude detection circuit for 5G phased-array calibration. By utilizing a 39 GHz–150 kHz down-conversion scheme, the phase and amplitude information are detected separately with a phase-to-digital converter (PDC) and an analog-to-digital converter (ADC). In addition, to reduce the number of reference signals, a divide-by-4 injection-locked frequency divider (ILFD) using a transformer-based injection-enhancing technique is implemented for wideband reference signal generation. This ILFD realizes a wide locking range of 16.3–23.4 GHz (35.8%) with 5.05-mW power consumption. The detection circuit achieves less than 0.049° and 0.036-dB detection rms errors at 39 GHz. The wideband high-accuracy detection is also achieved from 37 to 43.5 GHz. The total power consumption is 50 mW with a 1-V VDD. The total core area is 1.43 mm^2 in a 65-nm CMOS process.**

***Index Terms*— 5G, calibration, detection circuit, divide-by-4 injection-locked frequency divider (ILFD), phased array.**

I. Introduction

RECENTLY, the data rate of wireless communication has been increasing exponentially. In 5G, a more than 10-Gb/s data rate is one of the targets to achieve massive channel communication for the increasing future applications, such as the internet of things (IoT), factory automation, and self-driving. Thus, wideband communication using a frequency of frequency range 2 (FR2) is necessary. The FR2 band realizes high-data-rate communication due to the large wideband frequency resource. However, these frequencies also have huge free-space path loss, which makes long-distance communications difficult. The beamforming technique with a phased-array transceiver is generally used to solve this issue. A phased-array transceiver consists of multiple TRX elements and antenna arrays. The TRX element is composed of a variable-gain amplifier (VGA), a phase shifter, a power amplifier (PA), and a low-noise amplifier (LNA). Such phased-array transceivers can compensate for the path loss at millimeter-wave frequencies, thanks to the large equivalent isotropic radiation power (EIRP) [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12].

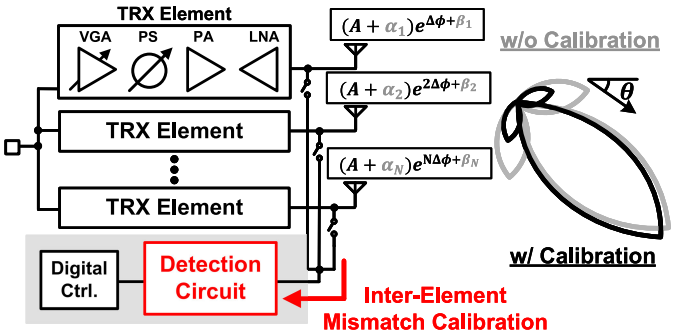

Fig. 1. 5G phased-array beamforming in actual conditions with phase and amplitude mismatches between each element.

In phased-array transceivers, the high-resolution phase and amplitude control with low errors is required for creating flexible beampatterns and preventing null degradation for multiinput and multioutput (MIMO) communications. However, the on-chip implementation of the transceiver is sensitive to the mismatch caused by process, voltage, and temperature (PVT) variations. Fig. 1 shows the phased-array beampattern with phase and amplitude mismatches between each TRX element. Ideally, the beam angle θ is determined by the phase difference $\Delta\phi$ between each element output. On the other hand, in an actual condition, each output signal has amplitude mismatch α and phase mismatch β, shown in Fig. 1. These mismatches cause sidelobe growth, beam pointing errors, and null degradation.

To calibrate these errors, a high-accuracy phase and amplitude detection circuit should be implemented [12], [13], [14],

Manuscript received 20 January 2023; revised 23 March 2023; accepted 21 April 2023. Date of publication 18 May 2023; date of current version 26 September 2023. This article was approved by Associate Editor Minoru Fujishima. This work was supported in part by the Ministry of Internal Affairs and Communications in Japan under Grant JPJ000254, in part by the Japan Society for the Promotion of Science (JSPS), in part by the Tokyo Tech Advanced Researchers (STAR), and in part by the VLSI Design and Education Center (VDEC) in collaboration with Cadence Design Systems, Inc., Mentor Graphics, Inc., and Keysight Technologies Japan, Ltd. *(Corresponding author: Yudai Yamazaki.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2023.3272829.

Digital Object Identifier 10.1109/JSSC.2023.3272829

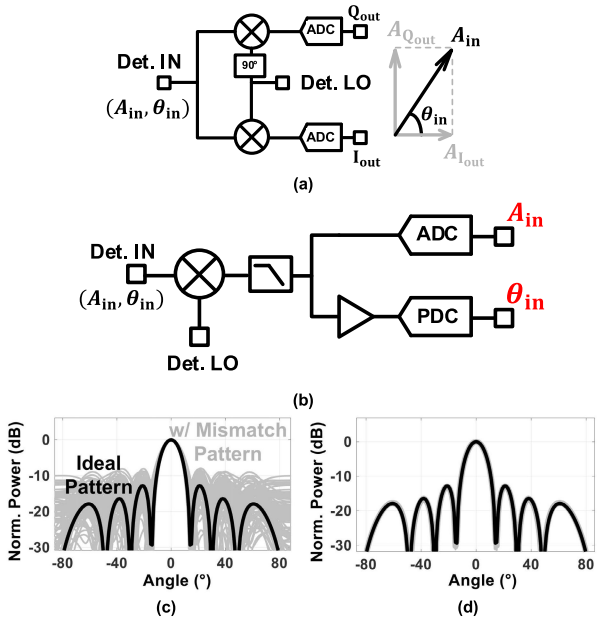

Fig. 2. Phase and amplitude detection circuit (a) with I/Q modulated detection technique and (b) with PDC/ADC detection technique, and beampattern simulation (c) with I/Q modulated detection accuracy and (d) with PDC/ADC detection accuracy.

[15], [16], [17], [18], [19], [20]. In recent research, there are two detection types of circuits for phased-array calibration. One is the I/Q modulation technique, shown in Fig. 2(a) [13], [14], [15], [18]. This detection technique realizes phase and amplitude detection with low power and small area consumption. However, this technique has large detection errors due to the large I/Q mismatch in the circuit. The other one is the phase-to-digital converter (PDC)/analog-to-digital converter (ADC) detection technique shown in Fig. 2(b) [12], [17], [21]. This technique achieves less than 0.1° and 0.1-dB detection accuracy with the independent phase and amplitude detection. Fig. 2(c)–(d) shows the simulated beampattern with I/Q modulated detection and PDC/ADC detection using MATLAB. The simulation is performed at 39 GHz with eight array elements and an array spacing of $\lambda/2$. The simulation applies phase and amplitude Gaussian errors on the output of each element corresponding to the detection accuracy. The pattern with I/Q detection is plotted based on the accuracy of [14]. From these simulation results, the PDC/ADC detection technique achieves high-accuracy phased-array calibration, compared to the I/Q modulated technique. As a result, [12] realizes a high-accuracy beampattern in the 39-GHz phased-array transceiver using PDC/ADC detection. However, the detection circuit needs 35 and 4 GHz off-chip signals for the calibration. Moreover, the calibration can only operate within a limited frequency band due to the narrowband characteristics of the detection circuit.

This article presents a high-accuracy phase and amplitude detection circuit with PDC/ADC detection technique for the calibration of phased-array beamforming [22]. This detection circuit is designed to extend [12] and enable the high-accuracy and wide-range detection around 39 GHz. A 37–43.5-GHz detecting operation is achieved by utilizing a divide-by-4 Ring injection-locked frequency divider (ILFD)

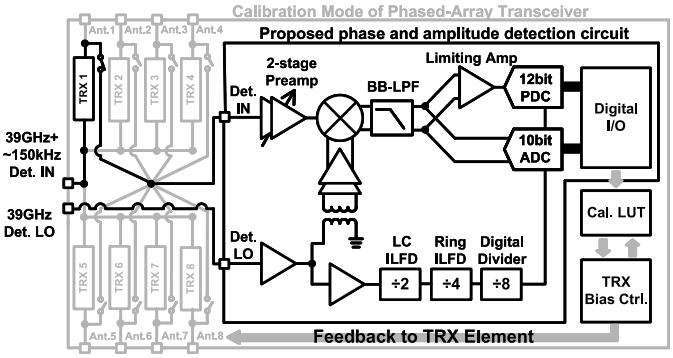

Fig. 3. Detailed architecture of the proposed phase and amplitude detection circuit for a phased-array calibration system.

using a transformer-based injection-enhancing technique [23]. In addition, a more detailed explanation of the PDC/ADC detection technique is provided in this article. The high-accuracy phased-array calibration using the proposed detection circuit is discussed in Section II. The detailed circuit implementations including the proposed ILFD are demonstrated in Section III, followed by the measurement results presented in Section IV. Finally, this work is concluded in Section V.

II. System Consideration

Fig. 3 shows the detail of the proposed phase and amplitude detection circuit for phased-array calibration. In this figure, the mismatch calibration of the transceiver 1 element is presented. In calibration mode, a 39 GHz + 150 kHz signal is input to TRX1, and the output signal is sent to the detection circuit through the calibration path. Then, the phase and amplitude of the TRX1 output signal could be relatively detected by the proposed detection circuit. Finally, the mismatch calibration of TRX1 could be performed by tuning the VGA and phase shifter, based on the detected digital values. Similarly, the other elements could also be calibrated in the calibration mode. The required size of the Cal. LUT varies depending on the number of elements and the resolution of the beam steering for phased-array transceivers. For example, in [24], an eight-element phased-array transceiver capable of beamforming with 8-bit patterns is realized. The LUT in this transceiver consists of 256-bank SRAM for storing beam ID, and conversion tables for 256-level amplitude setting and 256-level phase setting. In Fig. 3, Cal. LUT and TRX Bias Ctrl. are shared with the phased-array control part. In the calibration mode, the Cal. LUT is updated by comparing the detected values with the original phase and amplitude values at each beam pattern. Fig. 3 explains the case where the detection circuit is implemented in a conventional phased-array transceiver. On the other hand, this detection circuit can also be implemented in a dual-polarized phased-array transceiver. In that case, Det. IN and Det. local oscillator (LO) signals can be easily input using the H and V paths without additional signal paths for calibration.

In the proposed detection circuit, a 39 GHz – 150 kHz down-conversion scheme is utilized. The 39 GHz + 150 kHz signal is downconverted to a detection signal around 150 kHz by mixing with a 39-GHz LO signal. The 150-kHz detection signal is then sent to the ADC and

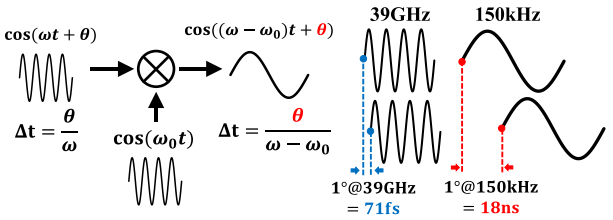

Fig. 4. High-accuracy phase detection with 39 GHz–150 kHz down-conversion scheme.

limiting amplifier (LA)-PDC chain. With a low-frequency detection signal, high-accuracy detections with 12-bit PDC and 10-bit ADC are achieved easily. Furthermore, to remove the requirement of an additional reference signal for the PDC/ADC, an on-chip clock signal generation scheme is also presented. A clock signal with around 600 MHz is generated from the 39-GHz LO signal with the divider-chain circuit, which divides the LO by 64. This clock signal is directly input to the PDC and is input to the ADC after the frequency is reduced to about 20 MHz internally.

As shown in Fig. 4, the 39 GHz–50 kHz down-conversion scheme is applied for high-resolution phase and amplitude detection with low errors. The generation of the low-frequency detection signal from 39 GHz + 150 kHz ($=\omega_{\mathrm{RF}}$) to around 150 kHz ($=\omega_{\mathrm{RF}}-\omega_{\mathrm{LO}}$) is represented as follows:

$$\begin{aligned}\mathrm{BB} &= \alpha \times A_{\mathrm{Det}} \cos\left(\omega_{\mathrm{RF}} t + \theta_{\mathrm{Det}}\right) \times A_{\mathrm{LO}} \cos(\omega_{\mathrm{LO}} t) \\ &\approx \frac{\alpha A_{\mathrm{LO}}}{2} \times A_{\mathrm{Det}} \cos((\omega_{\mathrm{RF}} - \omega_{\mathrm{LO}})t + \theta_{\mathrm{Det}}) \qquad (1)\end{aligned}$$

where BB is the down-converted 150-kHz detection signal and α is the conversion gain of the mixer with an LO voltage A_{LO}. The values of phase and amplitude in the detection signal are θ_{Det} and A_{Det}, respectively. The part of $\omega_{\mathrm{RF}} + \omega_{\mathrm{LO}}$ frequency is ignored because a low-pass filter (LPF) in the next stage will filter it out. This equation shows that the phase and amplitude information of the RF output signal can still be maintained with θ_{Det} and A_{Det}, after this down-conversion. In amplitude detection, the 150 kHz can easily be detected by using an ADC with high accuracy. In phase detection, the phase information of the 150-kHz signal also becomes much easier for detection than the 39-GHz counterpart. At 39 GHz, a phase shift of 1° corresponds to a very short time of 71 fs. Therefore, it is very difficult to detect the phase of a 39-GHz signal with high resolution. On the other hand, 1° of the 150-kHz signal corresponds to 18 ns, which is much easier for detection. Therefore, high-accuracy phase detection can be realized with low errors by down-converting the 39-GHz signal down to 150 kHz.

III. Building Block Design Consideration and Measurement

A. High-Accuracy Detection Circuit Architecture

Fig. 5(a) shows the detail of the 39 GHz–150 kHz down-conversion block. This block consists of a 39-GHz two-stage preamplifier, a 39 GHz–150 kHz single-balanced mixer, and an LPF. The 39-GHz two-stage preamp amplifies the detection signal with low input power. To achieve high-linearity detection at large input power, a 1-bit attenuator is added in the preamp. The amplified detection signal is input to a single-balanced mixer for 39 GHz–150 kHz down-conversion.

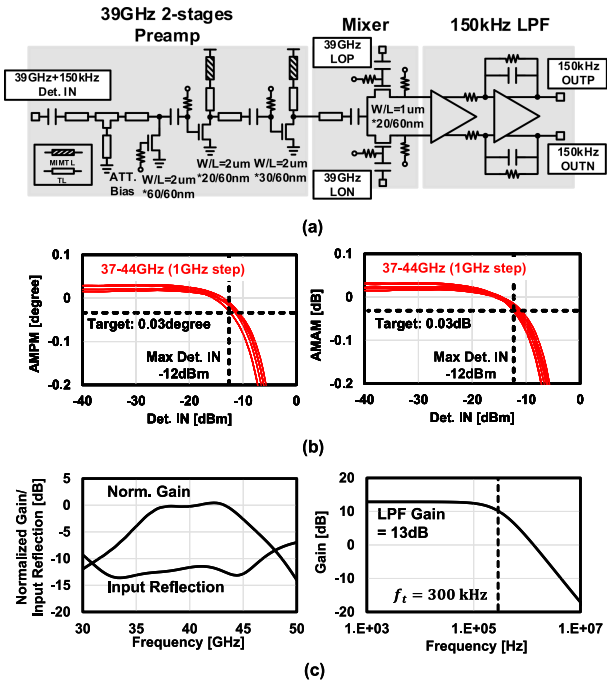

Fig. 5. (a) Schematic of the 39 GHz–150 kHz down-conversion circuit chain with (b) simulated AMPM and AMAM characteristics from 37 to 44 GHz and (c) more detailed characteristics.

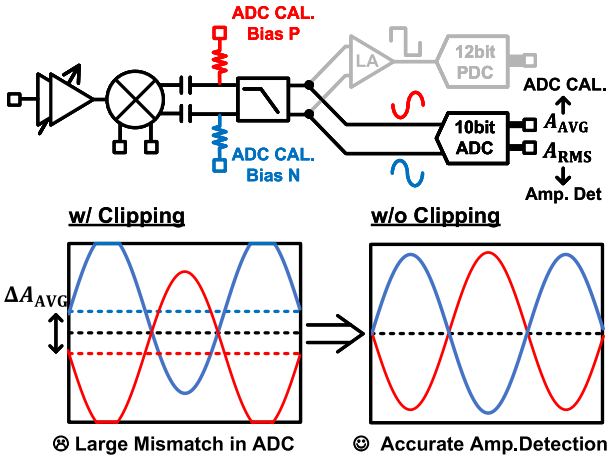

Fig. 6. Clipping calibration for accurate amplitude detection in the proposed circuit.

And then, the 150-kHz signal is input to the LPF to remove the unwanted mixing components. This down-conversion block is designed to suppress the degradation of the phase and gain linearity for wide dynamic-range demonstration. The simulated amplitude-modulation phase-modulation (AMPM) and amplitude-modulation amplitude-modulation (AMAM) characteristic is less than 0.03° and 0.03 dB in 37–43.5 GHz, as presented in Fig. 5(b). The maximum input power is −12 dBm for high-accuracy detection. Fig. 5(c) expresses the detailed characteristics of the simulated down-conversion block. The flat gain and low input reflection are realized from 37 to 43.5 GHz by the matching circuit using transmission lines in the 39-GHz preamp. The LPF has a 300-kHz cutoff frequency and a gain of 13 dB.

In Fig. 6, the amplitude detection with 10-bit successive approximation register (SAR) ADC is presented. The amplitude information of the detection signal is output with its

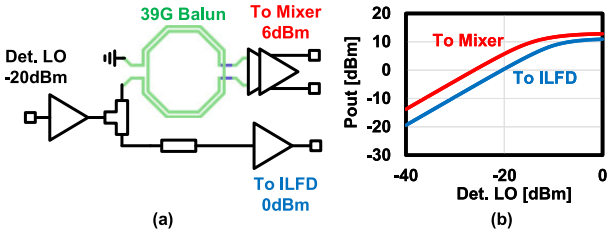

Fig. 7. (a) Block diagram of the LO circuit and (b) simulated LO power distribution at 39 GHz.

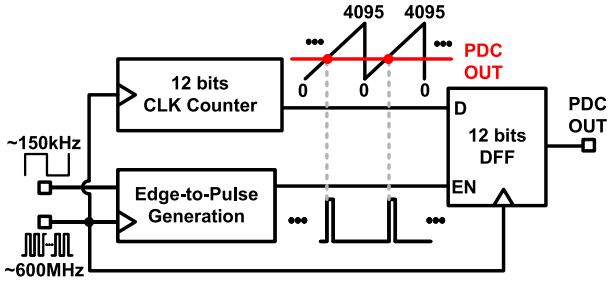

Fig. 8. Block diagram of the 12-bit PDC.

rms value. Furthermore, the average amplitude value is also detected in the ADC to compensate for the unbalance of the differential input. With a large input power, the dc offset causes clipping. Thus, the clipping calibration is performed before the amplitude rms detection. This clipping calibration ensures accurate amplitude detection for a wide dynamic range.

Fig. 7(a) shows the block diagram of the 39-GHz LO distribution. The LO signal is used for both mixing operation and reference signal generation. A multistage buffer is used in the LO circuit. The impedance matching is realized by transmission lines at each stage. In addition, a 39-GHz balun is applied to generate the differential LO signal for a single-balanced mixer. The simulated output power for the LO distribution for the mixer and the ILFD are shown in Fig. 7(b).

Fig. 8 presents the block diagram of the PDC. The PDC consists of a 12-bit counter, an edge detector for the 150-kHz detection signal, and a 12-bit D flip flop (DFF) for the output of the digital phase value. The detailed relationship between the input RF frequency f_{RF}, the LO frequency f_{LO} for down-conversion, and the detection frequency f_{Det} can be represented with the following equations:

$$f_{\mathrm{LO}} = \left(2^{12} \times 2 \times 4 \times 8\right) \times f_{\mathrm{Det}} \tag{2}$$

$$f_{\mathrm{RF}} = \left(2^{12} \times 2 \times 4 \times 8 + 1\right) \times f_{\mathrm{Det}} \tag{3}$$

where f_{Det} is finally selected at around 150 kHz considering the desired detection accuracy. For example, when $f_{\mathrm{Det}} =$ 149 kHz, values of f_{LO} and f_{RF} are determined to be 39.059456 and 39.059605 GHz, respectively. The PDC is designed to operate with a clock frequency of 2^{12} times f_{Det}, which is around 600 MHz. In the PDC, the input phase of the detection signal is converted to the counter output, which is a value from 0 to 4095. Thanks to the PDC, the phase value could be relatively detected. The PDC can realize phase detection with 0.088° resolution corresponding to the 12-bit accuracy.

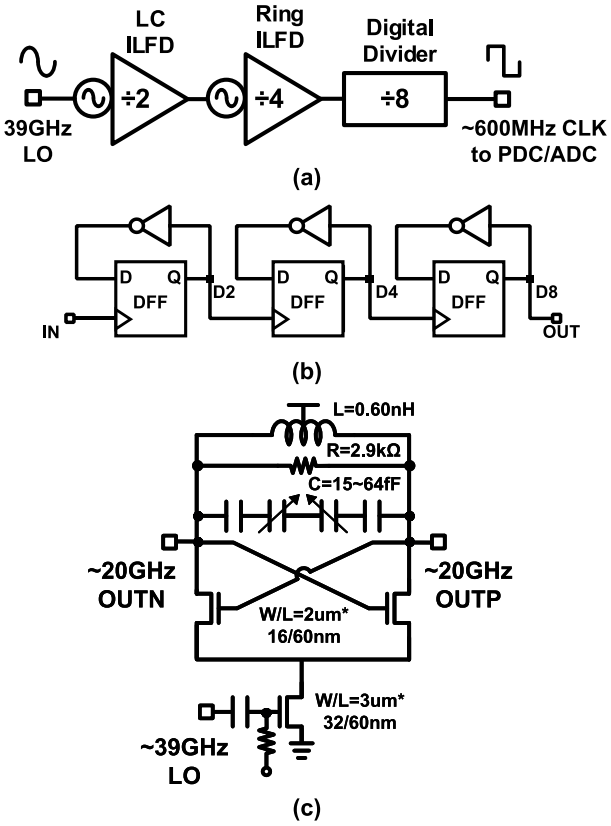

Fig. 9. (a) Block diagram of 600-MHz reference signal generation from a 39-GHz LO signal and (b) divide-by-8 digital divider and (c) divide-by-2 39 GHz LC ILFD.

In addition, to generate the clock signal, a frequency-divider-chain circuit is utilized, as shown in Fig. 9(a). The divider chain consists of a divide-by-8 digital frequency divider, a divide-by-2 LC ILFD, and a divide-by-4 Ring ILFD. Fig. 9(b) presents the digital divider, which consists of a three-stage cascade DFF with an inverter loop. An approximate 600-MHz clock signal is generated from the 5-GHz input. Usually, the digital divider can only be used at a few GHz frequency divisions. However, at a much higher frequency such as 39 GHz, the ILFDs are usually applied. To divide the 39-GHz LO signal, a divide-by-2 LC ILFD is first utilized for low-phase-noise characteristics, as shown in Fig. 9(c). In [17], a Ring ILFD using a dual-step injection technique is used for reference signal generation. However, the conventional ILFD cannot cover a large enough locking range due to the degradation of the injection signal at high frequency. As a result, the operating frequencies of the detection circuit become a narrow band. Next, a divide-by-4 Ring ILFD using a transformer-based injection-enhancing technique is introduced in Section III-B.

B. Transformer-Based Injection-Enhanced ILFD

A Ring ILFD can achieve high-division-ratio operation with the harmonic-signal mixing technique [25], [26], [27]. However, the locking range is limited because undesired harmonic signals will interfere with the oscillator's injection locking. In recent research, ILFDs using a dual-step injection approach

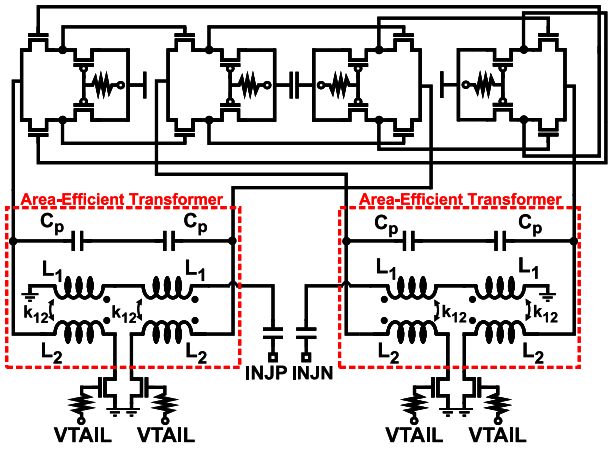

Fig. 10. Divide-by-4 ILFD using the transformer-based injection-enhancing technique.

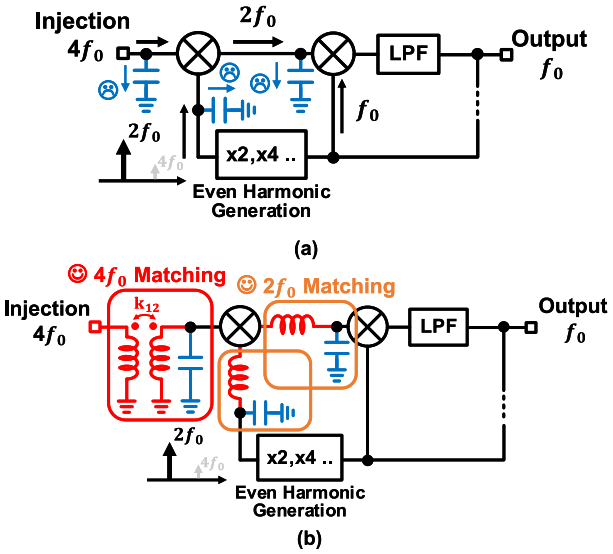

Fig. 11. Block diagram of the dual-step injection Ring ILFD (a) with a conventional approach and (b) with the proposed transformer for injection enhancing.

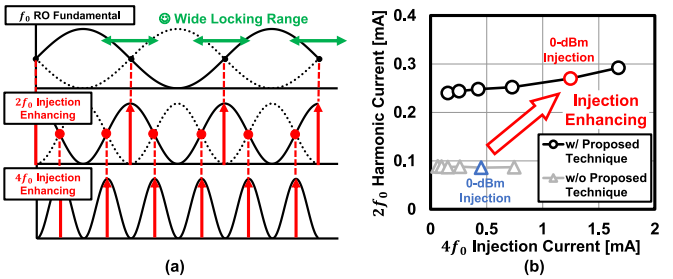

Fig. 12. (a) Divide-by-4 operation using the dual-step injection approach and (b) values of $4f_0$ and $2f_0$ currents with and without the proposed injection-enhancing technique.

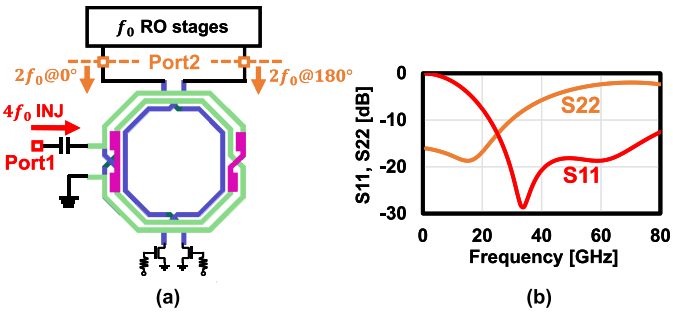

Fig. 13. (a) Operation of four-times and two-times signal input and (b) S11 and S22 simulation results with the proposed area-efficient transformer.

are presented for removing undesired harmonic signals in divide-by-4 operation [28], [29], [30]. However, the operation at higher frequencies is limited due to the degradation of the injection signal by the large parasitic capacitance of transistors.

In this work, a divide-by-4 dual-step-injection ILFD using a transformer-based injection-enhancing technique is implemented. Fig. 10 shows the schematic of the proposed divide-by-4 ILFD. It consists of a 4-stage differential ring oscillator and two area-efficient transformers for injection enhancement. The differential input signal, whose frequency is about four times the oscillation frequency ($4f_0$), is injected from INJP and INJN. The signals are sent to each stage of the ring oscillator through transformers. Then, the oscillation frequency is synchronized to the divide-by-4 injection frequency. Fig. 11(a)–(b) shows the block diagram of the dual-step injection ILFD with the conventional approach and with the proposed approach. As shown in Fig. 11(a), which refers to [29], the $4f_0$ injection signal is first mixed with the harmonic signal of two times frequency ($2f_0$) generated from each common node of differential inverters. And then, the generated $2f_0$ signal is mixed with the fundamental oscillation frequency. This dual-step injection ILFD could eliminate the unwanted harmonic signal that disturbs the injection locking operation. However, the locking range at higher frequencies is limited due to the degradation of both $4f_0$ and $2f_0$ injection signals by the large parasitic capacitance of transistors. On the other hand, Fig. 11(b) presents the proposed ILFD that applies the area-efficient transformer for impedance matching with parasitic capacitance to enhance both $4f_0$ and $2f_0$ injection signals. These injection signals are therefore increased, and the locking range could be extended. Fig. 12(a) demonstrates the transient waveform of the divide-by-4 operation with the dual-step injection technique and the proposed injection-enhancing technique. The locking range of the Ring ILFD is expanded by enhancing the dual-step injection approach with the proposed technique. Fig. 12(b) demonstrates an increase in the $4f_0$ and $2f_0$ current to the inverter stages with the injection-enhancing technique. These simulation results are obtained with an injection power range from -20 to 5 dBm and an injection frequency of 20 GHz. Thanks to the proposed technique, both the $4f_0$ and $2f_0$ currents are increased at the same injection power.

Fig. 13(a) shows the $4f_0$ and $2f_0$ signal input operation to the area-efficient transformer. In general, inductors are used for high-frequency impedance matching with parasitic capacitance. However, these inductors consume a large area for matching. In the proposed ILFD, a highly area-efficient injection enhancing technique is realized using two area-efficient multilayer transformers. In the ring oscillator, the second harmonic signals are generated at a common node of each inverter stage. At each transformer, the $4f_0$ injection signal and the differential $2f_0$ harmonic signal are inserted. The

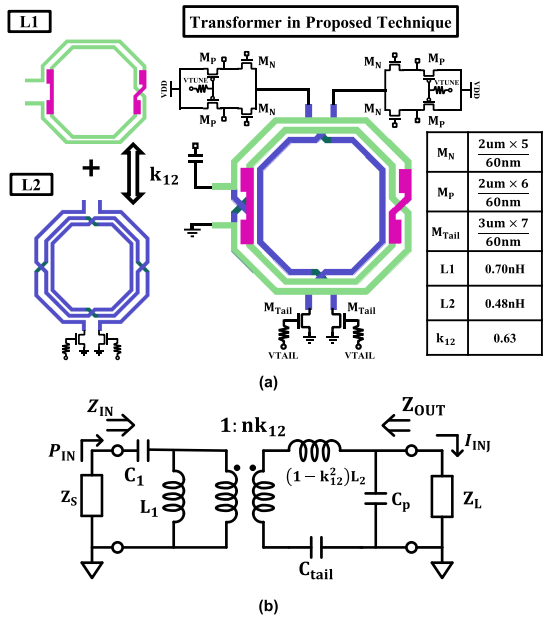

Fig. 14. (a) Layout and (b) equivalent circuit of the area-efficient transformer in the proposed technique.

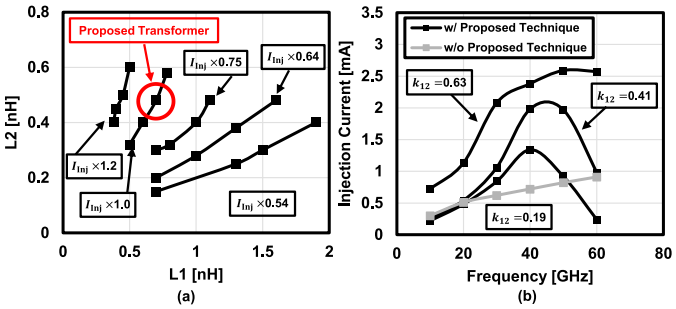

Fig. 15. (a) Simulated injection current for optimization of L1 and L2 and (b) from 10 to 60 GHz frequency range with varying k_{12} values.

$2f_0$ harmonic signals with 0° and 180°, 90° and 270° are combined, respectively. Fig. 13(b) presents the simulation results of the impedance matching at port1 and port2 in Fig. 13(a). The $4f_0$ injection signal is sent to port1 and the $2f_0$ harmonic signal is sent to port2. According to the S-parameter simulation, port1 achieves wideband $4f_0$ frequency matching, which is from 20 to 80 GHz and port2 achieves $2f_0$ frequency matching from 0 to 30 GHz. As a result, wideband injection signal enhancement is realized for both $4f_0$ and $2f_0$ signals simultaneously for each transformer.

Fig. 14(a) shows the detailed layout of the area-efficient transformer at each layer. The transformer consists of L1 for four-times injection signal input and L2 for second harmonic signal input. The coupling coefficient between L1 and L2 is shown by k_{12}. In Fig. 14(b), the equivalent circuit from the injection node to the common node of the differential stage is presented. The input capacitance C1 for removing dc, the parasitic capacitance of tail transistor Ctail, and the parasitic capacitance Cp at the common node of the differential inverter are shown. Z_S and Z_L are the input impedance and the common-node impedance, respectively. P_{IN} is the injection power to the proposed ILFD. I_{INJ} is the injection current to

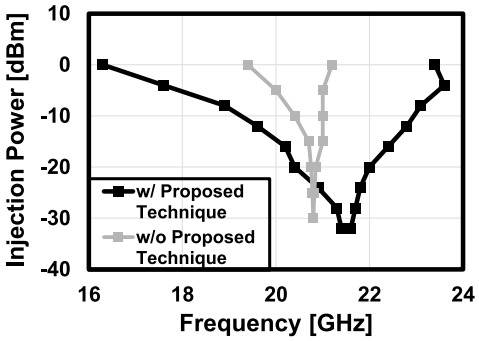

Fig. 16. Measurement results of the locking range around 20 GHz with and without the proposed technique.

the differential stage in the ring oscillator. The locking range of ILFDs depends on the magnitude of injection current into the oscillator [31]. Thus, in this ILFD, the injection current is enhanced at the same value of P_{IN}. When $Z_{IN} = Z_S^*$ and $Z_{OUT} = Z_L^*$ are achieved with the impedance matching, the relationship between the injection current I_{INJ} into each inverter stage and the injection power P_{IN} from the outside can be simply expressed by the following equation:

$$I_{INJ} \propto k_{12}\sqrt{\frac{L_2}{L_1}} \times \sqrt{P_{IN}}. \tag{4}$$

According to this equation, the injection current can be improved by maximizing k_{12}, L_2, and minimizing L_1 at the same injection power P_{IN}. The simulated injection current against different L_1 and L_2 is demonstrated in Fig. 15(a). To optimize L_1 and L_2 regardless of k_{12}, the lumped transformer is used for simulation. They are swept from 0.38 to 1.9 nH and from 0.15 to 0.60 nH, respectively. Equation (4) shows that it is possible to inject the largest current by lowering L_1 and increasing L_2. However, in the actual layout, k12 decreases dramatically as the L1 value decreases. Increasing L2, the area consumption of the transformer becomes large. Thus, L_1 and L_2 are optimized to 0.70 and 0.48 nH, respectively. Fig. 15(b) shows the simulated injection current to differential inverter stages with and without the proposed technique. The ILFD without the technique reuses the design of the conventional dual-step-injection ILFD [29]. Injection power is kept constant at 0 dBm. In this figure, the current values are plotted in a divide-by-4 operation (i.e., 10–60 GHz injection frequency). The value of k_{12} is swept from 0.19 to 0.63 by electro magnetic (EM) simulation. At $k_{12} = 0.63$, the injection current is increased by more than three times at a higher frequency range compared with the conventional method.

The measured locking range around 20 GHz with fixed bias condition is shown in Fig. 16. At 0-dBm injection power, the proposed ILFD achieves a locking range of 16.3–23.4 GHz, which is an absolute locking range of more than three times larger than the conventional technique. The power consumption is 5.05 mW at 1-V VDD. Fig. 17(a) demonstrates the total operating range with different bias settings of the ring oscillator. A 1.8–67-GHz operating range can be achieved at a 0-dBm injection power. The locking range at each center

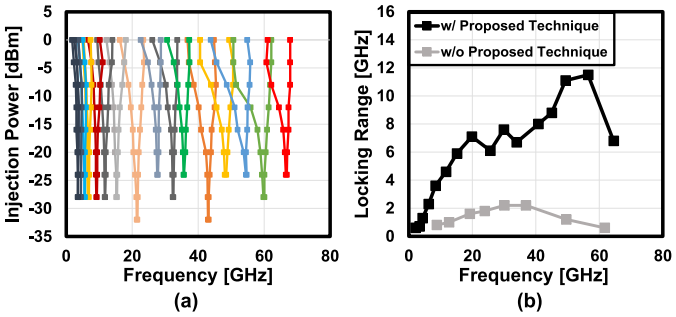

Fig. 17. (a) Measured operating range with variable bias settings and (b) measured locking range at each center frequency with and without the proposed technique.

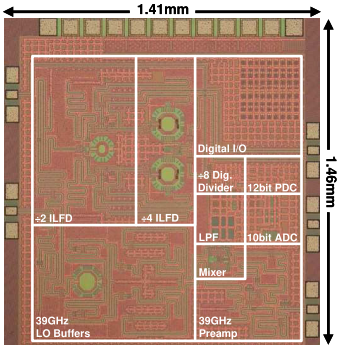

Fig. 18. Die photograph of the proposed phase and amplitude detection circuit.

frequency is summarized in Fig. 17(b). Locking ranges of 26.1–33.7 GHz (25.4%), 36.8–44.8 GHz (19.6%), and 61.1–67 GHz (10.5%) are also achieved with each fixed bias setting. These measurement results of the stand-alone ILFD are provided by a signal generator (Keysight E8257D), which is connected to an external RF balun to generate differential signals. The output signal is observed by a spectrum analyzer (Keysight E4448A) in this work. Compared with the conventional ILFD, this result is greatly improved with the transformer injection. Note that the measured locking range was limited to less than 67 GHz due to the operating frequency range of the used signal generator. Thus, this ILFD could work at an even higher frequency.

IV. Detection Measurement

Fig. 18 shows the die micrograph of the proposed detection circuit. This work is fabricated in a 65-nm CMOS process, which minimizes the manufacturing cost. The total area including pads is 1.41 × 1.46 mm^2. The core area is 1.43 mm^2, and the power consumption is 50 mW at 1-V VDD. To perform the detection over a larger frequency range, the divide-by-4 Ring ILFD using a transformer-based injection-enhancing technique is implemented. The PDC and ADC readouts are sent to the external side by the serial peripheral interface (SPI) block. Fig. 19 presents the measurement setup for the phase detection with PDC. The Det. IN and the Det. LO signals are generated from the external signal generators in this measurement. The input phase of Det. IN is changed by an external phase shifter. In addition, an external mixer and an oscilloscope are used to check the input phase value. Fig. 20 shows the waveform of the

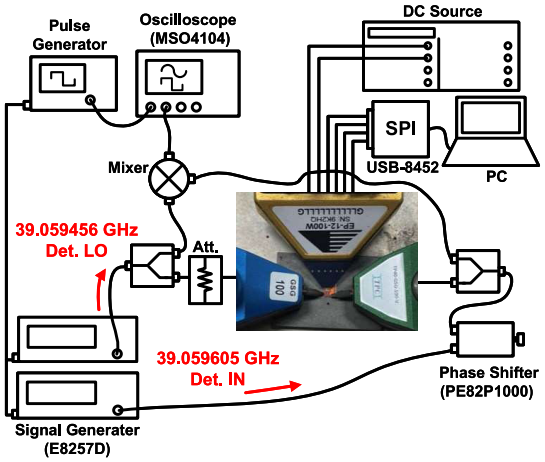

Fig. 19. Measurement setup of the proposed detection circuit for around 39-GHz signal detection.

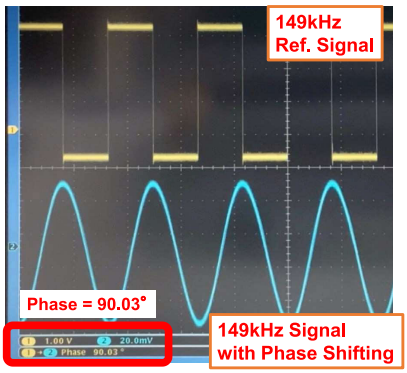

Fig. 20. Checking 90° phase shifting with an oscilloscope.

external mixer output. The input phase of the RF signal is read by comparing the external mixer output and a reference signal at 149 kHz. The input phase value is set to 90° in this figure. In this condition, the PDC readout is 90.08°. In amplitude detection, the input power of the RF signal is swept by the signal generator, and the detected values from ADC are sent to the external side-by-side SPI.

Fig. 21(a)–(b) shows the measurement results of the phase and amplitude detection accuracy at 39 GHz. The phase detection is performed from 0° to 360°, and the amplitude is from −26 to −12 dBm. The measured detection results realize high-accuracy phase and amplitude detection with the PDC/ADC detection technique. The detailed detection accuracy at each input value is presented in Fig. 21(c)–(d). The measured phase and amplitude detection errors at 39 GHz are less than 0.067° and 0.060 dB, respectively, and the rms detection errors are 0.049° and 0.036 dB, respectively. In addition, wide-range high-accuracy detection within 37–43.5 GHz is achieved, as shown in Fig. 22(a)–(b). The rms phase detection error is less than 0.060°, and the rms amplitude detection error is less than 0.051 dB. Fig. 23 shows the amplitude detection results at the different bias settings of the attenuator in the 39 GHz preamp. This result was measured in the Det. IN range of −42 to 6 dBm with the step of 0.5 dB at the frequency of 39 GHz. The dynamic range for high-accuracy

TABLE I
PERFORMANCE COMPARISON OF THE DETECTION CIRCUIT FOR PHASED-ARRAY CALIBRATION

	This work	[17]	[12]	[14]	[13]	[16]	[20]	[18]
Process	65nm CMOS	65nm CMOS	65nm CMOS	0.13μm BiCMOS	0.18μm SiGe	55nm CMOS	90nm CMOS	0.12um SiGe BiCMOS
Frequency	37-43.5GHz	28GHz	39GHz	76-84GHz	2-15GHz	26-28GHz	14GHz	90-100GHz
Stand Alone/ In TRX IC	Stand Alone	Stand Alone	In TRX IC	In TRX IC	In TRX IC	In TRX IC	In TRX IC	In TRX IC
Phase Det. Scheme	PDC	PDC	PDC	I/Q	I/Q	Symmetric Mixer	Phasor Sum	I/Q
Phase Error (degree)	0.067 (MAX) 0.049 (RMS)	0.29 (MAX) 0.17 (RMS)	0.08 (RMS)	11 (MAX)	3.0 (MAX)	1.0 (MAX)	16 (MAX) 5.9 (RMS)	7.0 (MAX)
Amp. Det. Scheme	ADC	ADC	ADC	I/Q	I/Q	N/A	N/A	I/Q
Amp. Error (dB)	0.060 (MAX) 0.036 (RMS)	0.21 (MAX) 0.12 (RMS)	0.04 (MAX)	1.0 (MAX)	0.3 (MAX)	0.097 (RMS)	N/A	1.0 (MAX)
DC Power (mW)	50	59	30	N/A	275-308	N/A	110	84
Core Area (mm^2)	1.43	1.12	N/A	N/A	0.824	N/A	0.57	N/A

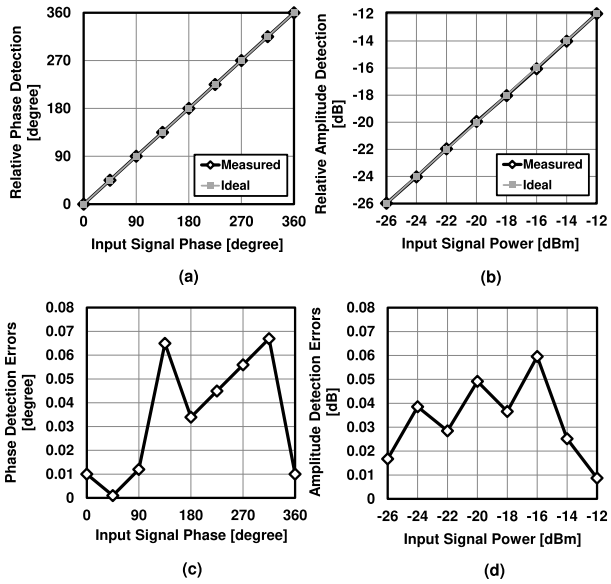

Fig. 21. Measurement results of (a) phase and (b) amplitude detection accuracy, and the detection errors of (c) phase and (d) amplitude detection at 39 GHz.

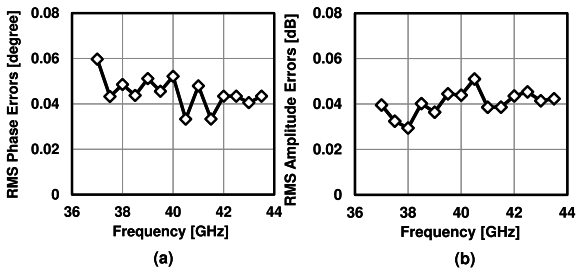

Fig. 22. Measured (a) phase and (b) amplitude rms detection errors in 37–43.5 GHz.

detection is limited by two factors. One is the nonlinearity of the 39 GHz–150 kHz down-conversion circuit chain at a large Det. IN signal. The other is the lower resolution of the ADC at a small Det. IN signal. The dynamic range is from

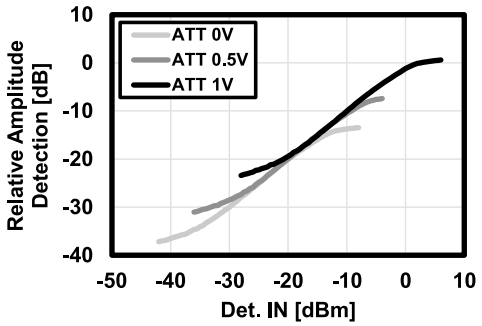

Fig. 23. Measured amplitude detection with the Det. IN step of 0.5 dB at the different bias settings of the attenuator in the 39-GHz preamp.

−31 to −19, −26 to −12, and −18 to −6 dBm at the bias settings of 0, 0.5, and 1 V, respectively.

Table I presents the comparison table of state-of-the-art detection circuits for phased-array calibration. The high-accuracy phase and amplitude detection is realized by using the PDC/ADC detection technique in this work. In addition, the proposed divide-by-4 Ring ILFD achieves wide-range high-accuracy detection in 37–43.5 GHz.

V. CONCLUSION

In this article, a 37–43.5-GHz high-accuracy phase and amplitude detection circuit for 5G phased-array calibration is introduced. In the proposed detection circuit, the PDC/ADC detection technique is applied for high-accuracy detection. To realize high-accuracy and low-cost detections, the 39 GHz–150 kHz down-conversion and the reference signal generation scheme is also applied. In addition, to realize the wideband operation of the detection circuit, the divide-by-4 Ring ILFD using a transformer-based injection-enhancing technique is implemented. The measured rms phase and amplitude detection errors are 0.049° and 0.036 dB at 39 GHz, respectively. The wideband high-accuracy detection is also performed in 37–43.5 GHz with 50-mW dc power consumption at 1-V VDD. The total core area is 1.43 mm^2 in a 65-nm CMOS process.

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